

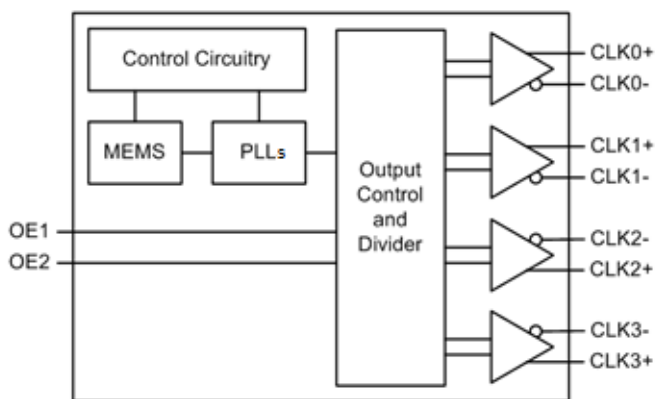


General Description

The DSC557-05 is a Crystal-less™, four output PCI express clock generator meeting Gen1, Gen2, and Gen3 specifications. The clock generator uses proven silicon MEMS technology to provide excellent jitter and stability over a wide range of supply voltages and temperatures. By eliminating the external quartz crystal, MEMS clock generators significantly enhance reliability and accelerate product development, while meeting stringent clock performance criteria for a variety of communications, storage, and networking applications.

DSC557-05 has an Output Enable / Disable feature allowing it to disable all outputs when OE1 and OE2 are low. Each output enable pin controls two banks of synchronous PCIe clocks. See the OE function diagram for more detail. The device is available in a 20 pin QFN. Additional output formats are in any combination of LVPECL, LVDS, and HCSL.

Block Diagram



* Clk0+/-, Clk1+/-, Clk2 +/- and Clk3 +/- are 100 MHz as per PCIe standards. For other frequencies, please contact the factory.

Features

- **Meets PCIe Gen1, Gen2 & Gen3 specs**
- **Available Output Formats:**
 - o HCSL, LVPECL, or LVDS
 - o Mixed Outputs: LVPECL/HCSL/LVDS
- **Wide Temperature Range**
 - o Ext. Industrial: -40° to 105° C
 - o Industrial: -40° to 85° C
 - o Ext. commercial: -20° to 70° C
- **Supply Range of 2.25 to 3.6 V**
- **Low Power Consumption**
 - o 30% lower than competing devices
- **Excellent Shock & Vibration Immunity**
 - o Qualified to MIL-STD-883
- **Available Footprints:**
 - o 20 QFN
- **Lead Free & RoHS Compliant**
- **Short Lead Time: 2 Weeks**

Applications

- **Communications/Networking**
 - o Ethernet
 - o 1G, 10GBASE-T/KR/LR/SR, and FcoE
 - o Routers and Switches
 - o Gateways, VoIP, Wireless AP's
 - o Passive Optical Networks
- **Storage**
 - o SAN, NAS, SSD, JBOD
- **Embedded Applications**
 - o Industrial, Medical, and Avionics
 - o Security Systems and Office Automation
 - o Digital Signage, POS and others
- **Consumer Electronics**
 - o Smart TV, Bluray, STB

Specifications (Unless specified otherwise: T=25° C, VDD =3.3V)

Parameter		Condition	Min.	Typ.	Max.	Unit
Supply Voltage ¹	V _{DD}		2.25		3.6	V
Supply Current	I _{DD}	EN pin low – outputs are disabled		42	46	mA
Supply Current ² (Four HCSL Outputs)	I _{DD}	EN pin high – outputs are enabled R _L =50 Ω, F _{O1} =F _{O2} =F _{O3} = F _{O4} =100 MHz		120		mA
Frequency Stability	Δf	Includes frequency variations due to initial tolerance, temp. and power supply voltage			±100 ±50	ppm
Startup Time ³	t _{SU}	T=25°C			5	ms
Input Logic Levels Input logic high Input logic low	V _{IH} V _{IL}		0.75xV _{DD} -		- 0.25xV _{DD}	V
Output Disable Time ⁴	t _{DA}				5	ns
Output Enable Time	t _{EN}				20	ns
Pull-Up Resistor ²		Pull-up on OE pin		40		kΩ

HCSL Outputs ⁶						
Parameter		Condition	Min.	Typ.	Max.	Unit
Output Logic Levels Output logic high Output logic low	V _{OH} V _{OL}	R _L =50Ω	0.725 -		- 0.1	V
Pk to Pk Output Swing		Single-Ended		750		mV
Output Transition time ⁴ Rise Time Fall Time	t _R t _F	20% to 80% R _L =50Ω, C _L = 2pF	200		400	ps
Frequency	f ₀	Single Frequency	2.3	100 ⁷	460	MHz
Output Duty Cycle	SYM	Differential	48		52	%
Period Jitter ⁵	J _{PER}	F _{O1} =F _{O2} = F _{O3} = F _{O4} =100 MHz		2.5		ps _{RMS}
Jitter, Phase (Common Clock Architecture)	T _J	PCIe Gen 1.1		22.7	86.0 ⁸	ps _{p-p}
	J _{RMS-CCHF}	PCIe Gen 2.1, 1.5MHz to Nyquist		2.20	3.1 ⁸	ps _{RMS}
	J _{RMS-CCLF}	PCIe Gen 2.1, 10 kHz to 1.5 MHz		0.08	3.0 ⁸	ps _{RMS}
	J _{RMS-CC}	PCIe Gen 3.0		0.37	1.0 ⁸	ps _{RMS}
Integrated Phase Noise (Data Clock Architecture)	J _{RMS-DCHF}	PCIe Gen 2.1, 1.5MHz to Nyquist		2.15	4.0 ⁸	ps _{RMS}
	J _{RMS-DCLF}	PCIe Gen 2.1, 10 kHz to 1.5 MHz		0.06	7.5 ⁸	ps _{RMS}
	J _{RMS-DC}	PCIe Gen 3.0		0.32	1.0 ⁸	ps _{RMS}

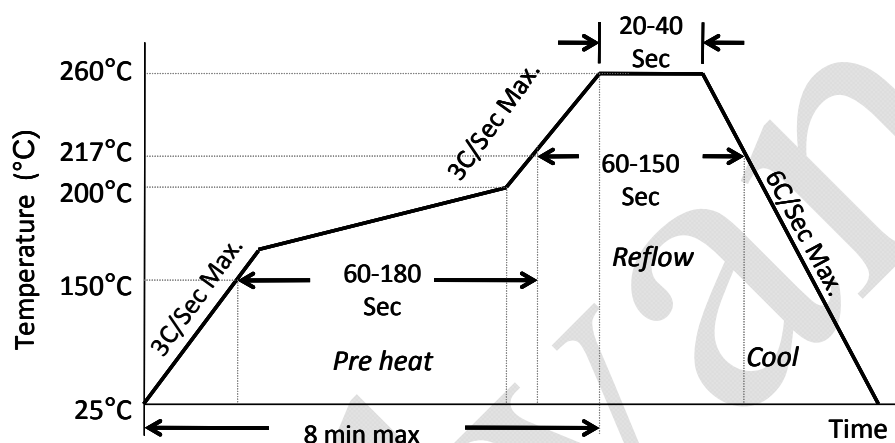
Notes:

- Each V_{DD} pin should be filtered with 0.01uf capacitor.
- Output is enabled if OE pin is floated or not connected.
- t_{SU} is time to 100PPM stable output frequency after V_{DD} is applied and outputs are enabled.
- Output Waveform and Connection Diagram define the parameters.
- Period Jitter includes crosstalk from adjacent output.
- Contact Sales@Discera.com for alternate output options (LVPECL, LVDS, LVCMOS).
- Contact Sales@Discera.com for alternative frequency options
- Jitter limits established by Gen 1.1, Gen 2.1, and Gen 3.0 PCIe standards.

Absolute Maximum Ratings

Item	Min	Max	Unit	Condition
Supply Voltage	-0.3	+4.0	V	
Input Voltage	-0.3	$V_{DD}+0.3$	V	
Junction Temp	-	+150	°C	
Storage Temp	-55	+150	°C	
Soldering Temp	-	+260	°C	40sec max.
ESD	-		V	
HBM		4000		
MM		400		
CDM		1500		

Solder Reflow Profile

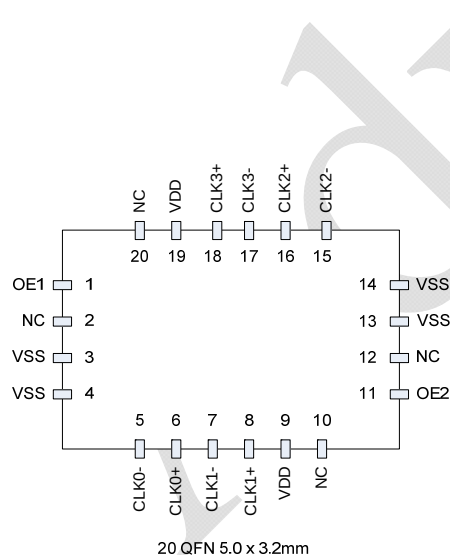


20 QFN MSL 1 @ 260°C refer to JSTD-020C	
Ramp-Up Rate (200°C to Peak Temp)	3°C/Sec Max.
Preheat Time 150°C to 200°C	60-180 Sec
Time maintained above 217°C	60-150 Sec
Peak Temperature	255-260°C
Time within 5°C of actual Peak	20-40 Sec
Ramp-Down Rate	6°C/Sec Max.
Time 25°C to Peak Temperature	8 min Max.

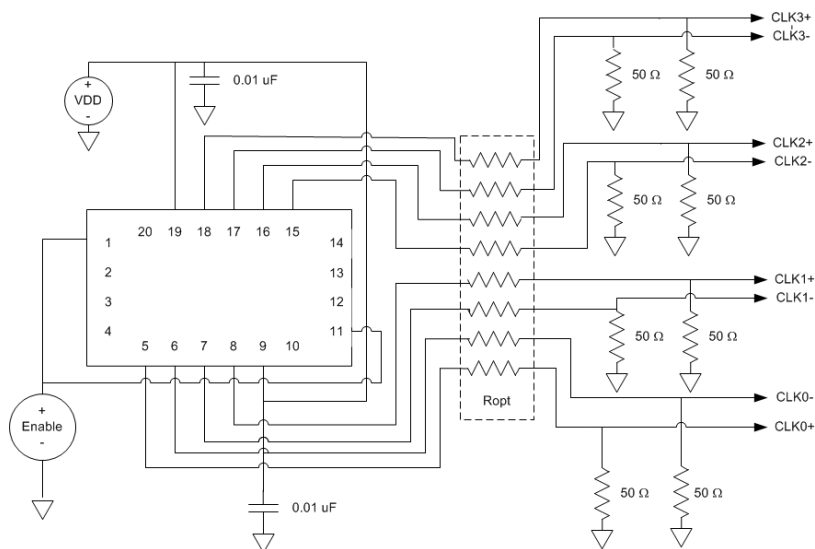
Pin Description (20 QFN)

Pin No.	Pin Name	Pin Type	Description
1	OE1	I	Output Enable; active high
2	NC	NA	Leave unconnected or grounded
3	VSS	Power	Ground
4	VSS	Power	Ground
5	CLK0-	O	Complement output of differential pair
6	CLK0+	O	True output of differential pair
7	CLK1-	O	Complement output of differential pair
8	CLK1+	O	True output of differential pair
9	VDD	Power	Power Supply
10	NC	NA	Leave unconnected or grounded
11	OE2	I	Output Enable; active high
12	NC	NA	Leave unconnected or grounded
13	VSS	Power	Ground
14	VSS	Power	Ground
15	CLK2-	O	Complement output of differential pair
16	CLK2+	O	True output of differential pair
17	CLK3-	O	Complement output of differential pair
18	CLK3+	O	True output of differential pair
19	VDD	Power	Power Supply
20	NC	NA	Leave unconnected or grounded

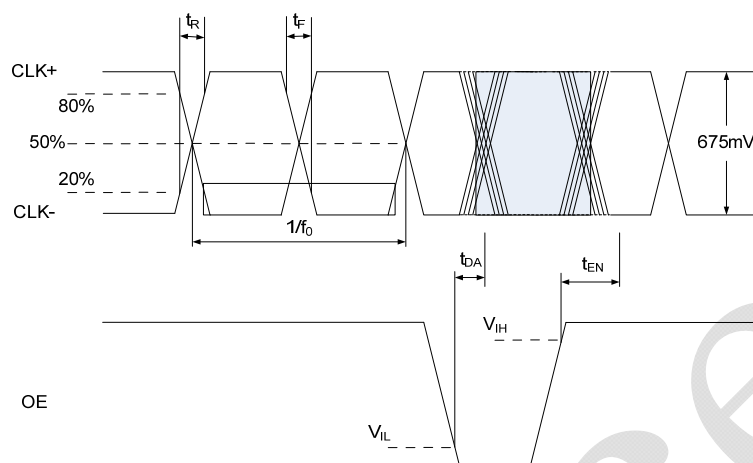
Pin Diagram (20 QFN)



Connection Diagram (20 QFN Four HCSL Outputs)



OE Function and Output Waveform: HCSL



		CLK1/CLK2 Synchronous			
OE1	OE2	CLK0	CLK1	CLK2	CLK3
0	0	Hi-Z	Hi-Z	Hi-Z	Hi-Z
0	1	Hi-Z	EN	EN	Hi-Z
1	0	EN	Hi-Z	Hi-Z	EN
1	1	EN	EN	EN	EN

CLK0/CLK3 Synchronous

Ordering Information

DSC557-05 4 4 4 4 K I 0 T

CLK 3 Output Format

- 1: LVCMOS
- 2: LVPECL
- 3: LVDS
- 4: **HCSL**

CLK 2 Output Format

- 1: LVCMOS
- 2: LVPECL
- 3: LVDS
- 4: **HCSL**

CLK 1 Output Format

- 1: LVCMOS
- 2: LVPECL
- 3: LVDS
- 4: **HCSL**

CLK 0 Output Format

- 1: LVCMOS
- 2: LVPECL
- 3: LVDS
- 4: **HCSL**

Packing

T: Tape & Reel

Stability

0: ±100ppm
1: ±50ppm

Temp Range

E: -20 to 70
I: -40 to 85
L: -40 to 105

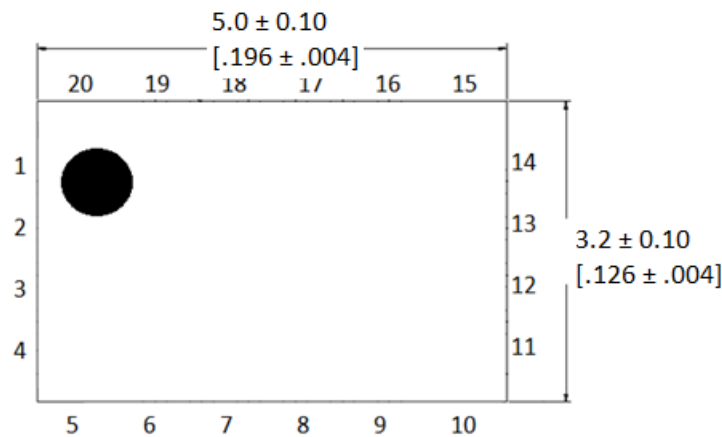
Package

K: 20 QFN

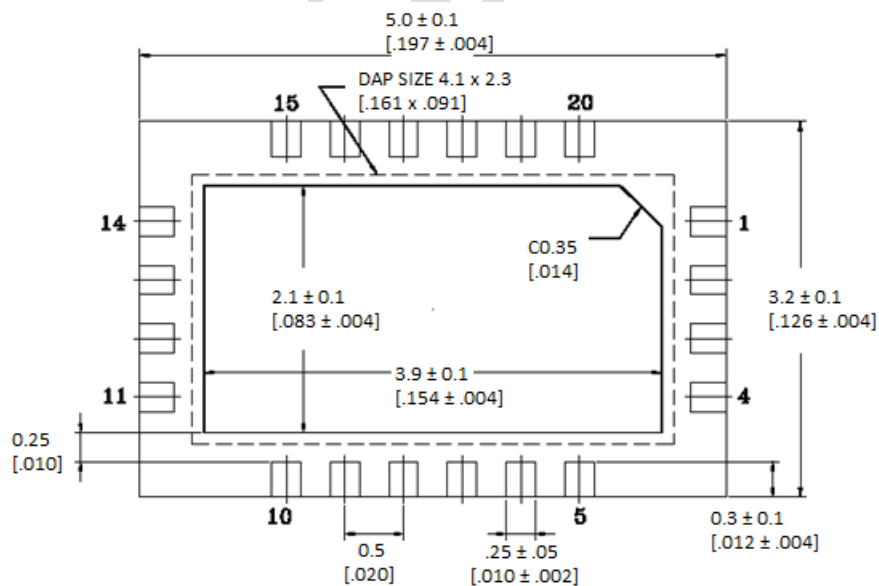
Package Dimensions

20 QFN, 5.0 x 3.2 mm

Top View units: mm[inches]



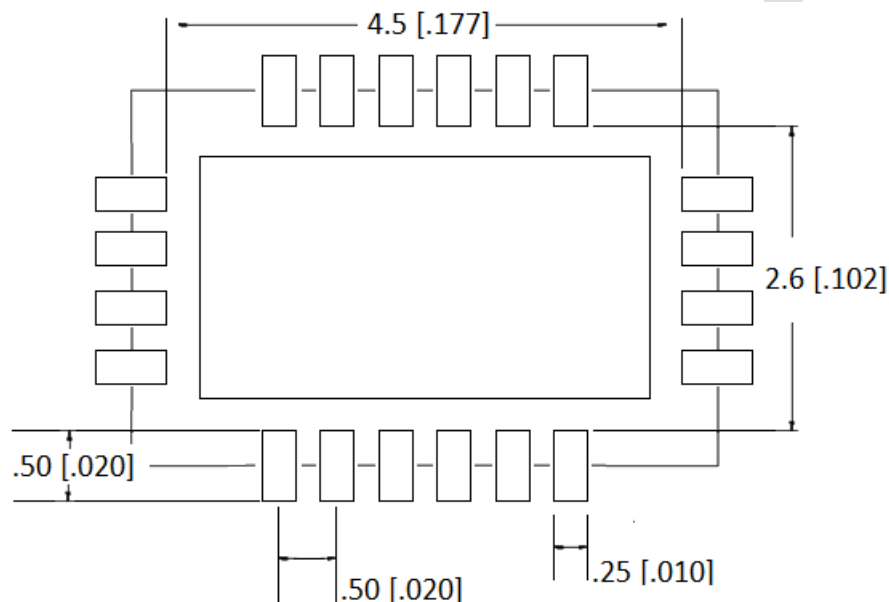
Bottom View units: mm[inches]



Side View
units: mm[inches]



Recommended Solder Pad Layout
units: mm[inches]



*Connect the center pad to VSS for best thermal performance

Disclaimer:

Discera makes no warranty of any kind, express or implied, with regard to this material, including, but not limited to, the implied warranties of merchantability and fitness for a particular purpose. Discera reserves the right to make changes without further notice to materials described herein. Discera does not assume any liability arising from the application or use of any product or circuit described herein. Discera does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Discera's product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Discera against all charges.