

DS91M124 125 MHz 1:4 M-LVDS Repeater with LVCMOS Input

Check for Samples: [DS91M124](#)

FEATURES

- DC - 125 MHz / 250 Mbps Low Jitter, Low Skew, Low Power Operation
- Independent Driver Enable Pins
- Conforms to TIA/EIA-899 M-LVDS Standard
- Controlled Transition Times Minimize Reflections
- 8 kV ESD on M-LVDS I/O Pins Protects Adjoining Components
- Flow-Through Pinout Simplifies PCB Layout
- Industrial Operating Temperature Range (–40°C to +85°C)
- Available in a Space Saving SOIC-16 Package

APPLICATIONS

- Multidrop / Multipoint Clock and Data Distribution
- High-Speed, Low Power, Short-Reach Alternative to TIA/EIA-485/422
- Clock Distribution in AdvancedTCA (ATCA) and MicroTCA (μTCA) Backplanes

DESCRIPTION

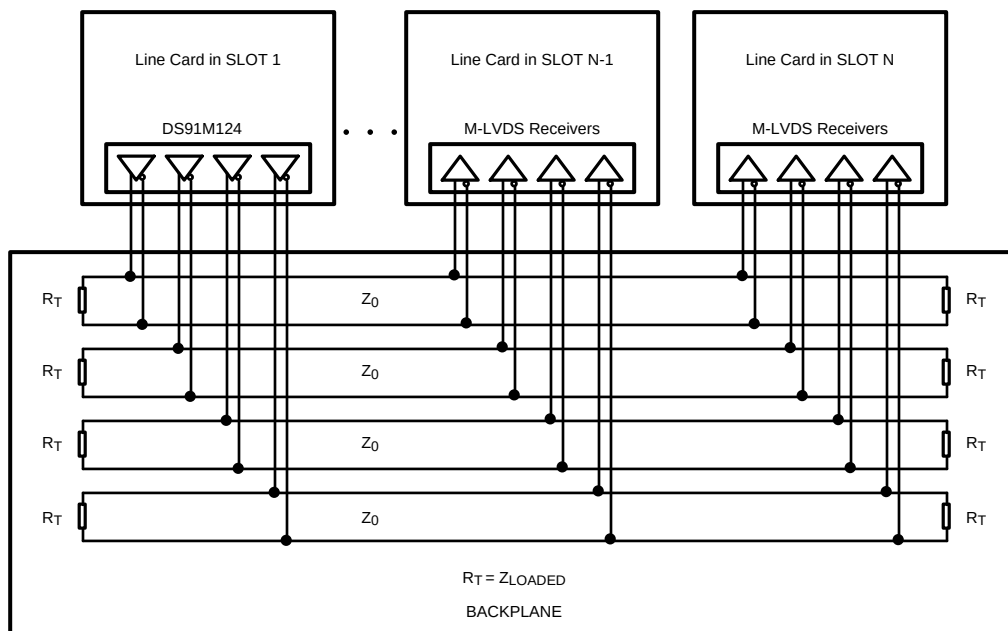
The DS91M124 is a 1:4 M-LVDS repeater for driving and distributing clock or data signals to up to four multipoint networks.

M-LVDS (Multipoint LVDS) is a new family of bus interface devices based on LVDS technology specifically designed for multipoint and multidrop cable and backplane applications. It differs from standard LVDS in providing increased drive current to handle double terminations that are required in multipoint applications. Controlled transition times minimize reflections that are common in multipoint configurations due to unterminated stubs.

A single DS91M124 channel is a 1:4 repeater that accepts LVTTTL/LVCMOS signals at the driver inputs and converts them to differential M-LVDS signal levels. It features independent driver enable pins for each driver output.

The DS91M124 has a flow-through pinout for easy PCB layout. It provides a new alternative for high speed multipoint interface applications. It is packaged in a space saving SOIC-16 package.

Typical Application



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Pin Diagram

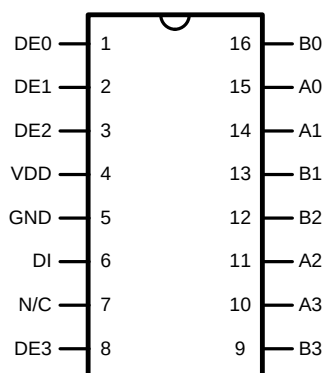
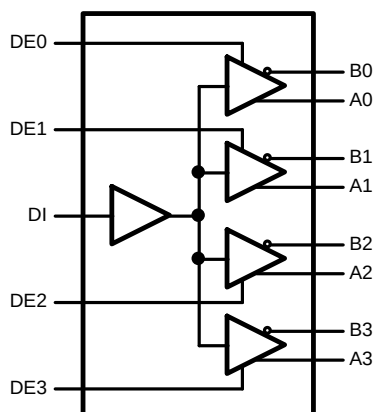


Figure 1. SOIC Package
See Package Number D0016A

Logic Diagram



Pin Descriptions

Number	Name	I/O, Type	Description
1, 2, 3, 8	DE	I, LVCMOS	Driver enable pin: When a DE pin is low, the corresponding driver output is disabled. When a DE pin is high, the corresponding driver output is enabled. There is a 300 kΩ pulldown resistor on each DE pin.
6	DI	I, LVCMOS	Driver input pin.
5	GND	Power	Ground pin.
10, 11, 14, 15	A	O, M-LVDS	Non-inverting driver output pins.
9, 12, 13, 16	B	O, M-LVDS	Inverting driver output pins.
4	V _{DD}	Power	Power supply pin, +3.3V ± 0.3V
7	N/C	N/A	NO CONNECT pin.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings ⁽¹⁾⁽²⁾

Power Supply Voltage	–0.3V to +4V
LVC MOS Input Voltage	–0.3V to ($V_{DD} + 0.3V$)
M-LVDS Output Voltage	–1.9V to +5.5V
M-LVDS Output Short Circuit Current Duration	Continuous
Junction Temperature	+140°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature Range	
Soldering (4 sec.)	+260°C
Maximum Package Power Dissipation @ +25°C	
D0016A Package	2.21W
Derate D0016A Package	19.2 mW/°C above +25°C
Package Thermal Resistance (4-Layer, 2 oz. Cu, JEDEC)	
θ_{JA}	+52°C/W
θ_{JC}	+19°C/W
ESD Susceptibility	
HBM ⁽³⁾	≥8 kV
MM ⁽⁴⁾	≥250V
CDM ⁽⁵⁾	≥1250V

- (1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
- (3) Human Body Model, applicable std. JESD22-A114C
- (4) Machine Model, applicable std. JESD22-A115-A
- (5) Field Induced Charge Device Model, applicable std. JESD22-C101-C

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage, V_{DD}	3.0	3.3	3.6	V
Voltage at Any Bus Terminal (Separate or Common-Mode)	–1.4		+3.8	V
LVTTL Input Voltage High V_{IH}	2.0		V_{DD}	V
LVTTL Input Voltage Low V_{IL}	0		0.8	V
Operating Free Air				
Temperature T_A	–40	+25	+85	°C

DC Electrical Characteristics

Over supply voltage and operating temperature ranges, unless otherwise specified. ⁽¹⁾⁽²⁾⁽³⁾⁽⁴⁾

Parameter		Test Conditions	Min	Typ	Max	Units
LVC MOS DC Specifications						
V _{IH}	High-Level Input Voltage		2.0		V _{DD}	V
V _{IL}	Low-Level Input Voltage		GND		0.8	V
I _{IH}	High-Level Input Current	V _{IH} = 3.6V	-15	±1	15	μA
I _{IL}	Low-Level Input Current	V _{IL} = 0V	-15	±1	15	μA
V _{CL}	Input Clamp Voltage	I _{IN} = -18 mA	-1.5			V
M-LVDS DC Specifications						
V _{AB}	Differential Output Voltage Magnitude	R _L = 50Ω, C _L = 5 pF Figure 2 Figure 4	480		650	mV
ΔV _{AB}	Change in Differential Output Voltage Magnitude Between Logic States		-50		50	mV
V _{OS(SS)}	Steady-State Common-Mode Output Voltage	Figure 2 Figure 3 R _L = 50Ω	0.30	1.6	2.10	V
ΔV _{OS(SS)}	Change in Steady-State Common-Mode Output Voltage Between Logic States		0		50	mV
V _{A(OC)}	Maximum Steady-State Open-Circuit Output Voltage	Figure 5	0		2.4	V
V _{B(OC)}	Maximum Steady-State Open-Circuit Output Voltage		0		2.4	V
V _{P(H)}	Voltage Overshoot, Low-to-High Level Output (5)	R _L = 50Ω, C _L = 5 pF C _D = 0.5 pF Figure 7 Figure 8			1.2V _{SS}	V
V _{P(L)}	Voltage Overshoot, High-to-Low Level Output (5)		-0.2V _{SS}			V
I _{OS}	Output Short-Circuit Current ⁽⁶⁾	Figure 6	-43		43	mA
I _A	Driver High-Impedance Output Current	V _A = 3.8V, V _B = 1.2V	0		32	μA
		V _A = 0V or 2.4V, V _B = 1.2V	-20		20	μA
		V _A = -1.4V, V _B = 1.2V	-32		0	μA
I _B	Driver High-Impedance Output Current	V _A = 3.8V, V _B = 1.2V	0		32	μA
		V _A = 0V or 2.4V, V _B = 1.2V	-20		20	μA
		V _A = -1.4V, V _B = 1.2V	-32		0	μA
I _{AB}	Driver High-Impedance Output Differential Current (I _A - I _B)	V _A = V _B , -1.4V ≤ V ≤ 3.8V	-4		4	μA
I _{A(OFF)}	Driver High-Impedance Output Power-Off Current	V _A = 3.8V, V _B = 1.2V DE _n = 0V 0V ≤ V _{DD} ≤ 1.5V	0		32	μA
		V _A = 0V or 2.4V, V _B = 1.2V DE _n = 0V 0V ≤ V _{DD} ≤ 1.5V	-20		20	μA
		V _A = -1.4V, V _B = 1.2V DE _n = 0V 0V ≤ V _{DD} ≤ 1.5V	-32		0	μA

- (1) The Electrical Characteristics tables list ensured specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not ensured.
- (2) Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except V_{OD} and ΔV_{OD}.
- (3) Typical values represent most likely parametric norms for V_{DD} = +3.3V and T_A = +25°C, and at the Recommended Operation Conditions at the time of product characterization and are not ensured.
- (4) C_L includes fixture capacitance and C_D includes probe capacitance.
- (5) Specification is ensured by characterization and is not tested in production.
- (6) Output short circuit current (I_{OS}) is specified as magnitude only, minus sign indicates direction only.

DC Electrical Characteristics (continued)

Over supply voltage and operating temperature ranges, unless otherwise specified. ⁽¹⁾⁽²⁾⁽³⁾⁽⁴⁾

Parameter	Test Conditions	Min	Typ	Max	Units
$I_{B(OFF)}$	Driver High-Impedance Output Power-Off Current $V_A = 3.8V$, $V_B = 1.2V$ $DE_n = 0V$ $0V \leq V_{DD} \leq 1.5V$	0		32	μA
	$V_A = 0V$ or $2.4V$, $V_B = 1.2V$ $DE_n = 0V$ $0V \leq V_{DD} \leq 1.5V$	-20		20	μA
	$V_A = -1.4V$, $V_B = 1.2V$ $DE_n = 0V$ $0V \leq V_{DD} \leq 1.5V$	-32		0	μA
$I_{AB(OFF)}$	Driver High-Impedance Output Power-Off Current ($I_{A(OFF)} - I_{B(OFF)}$) $V_A = V_B$, $-1.4V \leq V \leq 3.8V$ $DE_n = 0V$ $0V \leq V_{DD} \leq 1.5V$	-4		4	μA
C_A	Driver Output Capacitance		7.8		pF
C_B	Driver Output Capacitance		7.8		pF
C_{AB}	Driver Output Differential Capacitance		3		pF
$C_{A/B}$	Driver Output Capacitance Balance (C_A/C_B)		1		
I_{CCL}	Loaded Supply Current Enabled $R_L = 50\Omega$ (All Outputs) $DI = V_{DD}$ or GND $DE_n = V_{DD}$ or GND (All Outputs)		65	75	mA
I_{CCZ}	No Load Supply Current Disabled $DI = V_{DD}$ or GND, $DE_n = GND$ (All Outputs)		19	24	mA

Switching Characteristics

Over supply voltage and operating temperature ranges, unless otherwise specified. ⁽¹⁾⁽²⁾⁽³⁾

Parameter	Test Conditions	Min	Typ	Max	Units
t_{PHL}	Differential Propagation Delay High to Low	1.8	3.9	6.5	ns
t_{PLH}	Differential Propagation Delay Low to High	1.8	3.9	6.5	ns
t_{SKD1}	Differential Pulse Skew $ t_{PHL} - t_{PLH} $ ^{(4) (5)}	0	25	100	ps
t_{SKD2}	Channel-to-Channel Skew ^{(4) (6)}	0	70	250	ps
t_{SKD3}	Differential Part-to-Part Skew ^{(4) (7)} (Constant T_A and V_{DD})	0	1.5	2	ns
t_{SKD4}	Differential Part-to-Part Skew ^{(4) (8)}	0		4.7	ns
t_{TLH}	Rise Time ⁽⁴⁾	1.1	2.0	3.0	ns
t_{THL}	Fall Time ⁽⁴⁾	1.1	2.0	3.0	ns
t_{PHZ}	Disable Time High to Z		6	11	ns
t_{PLZ}	Disable Time Low to Z		6	11	ns
t_{PZH}	Enable Time Z to High		6	11	ns
t_{PZL}	Enable Time Z to Low		6	11	ns
f_{MAX}	Maximum Operating Frequency ⁽⁴⁾	125			MHz

- The Electrical Characteristics tables list ensured specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not ensured.
- Typical values represent most likely parametric norms for $V_{DD} = +3.3V$ and $T_A = +25^\circ C$, and at the Recommended Operation Conditions at the time of product characterization and are not ensured.
- C_L includes fixture capacitance and C_D includes probe capacitance.
- Specification is ensured by characterization and is not tested in production.
- t_{SKD1} , $|t_{PLHD} - t_{PHLD}|$, Pulse Skew, is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.
- t_{SKD2} , Channel-to-Channel Skew, is the difference in propagation delay (t_{PLHD} or t_{PHLD}) among all output channels.
- t_{SKD3} , Part-to-Part Skew, is defined as the difference between the minimum and maximum differential propagation delays. This specification applies to devices at the same V_{DD} and within $5^\circ C$ of each other within the operating temperature range.
- t_{SKD4} , Part-to-Part Skew, is the differential channel-to-channel skew of any event between devices. This specification applies to devices over recommended operating temperature and voltage ranges, and across process distribution. t_{SKD4} is defined as $|Max - Min|$ differential propagation delay.

Test Circuits and Waveforms

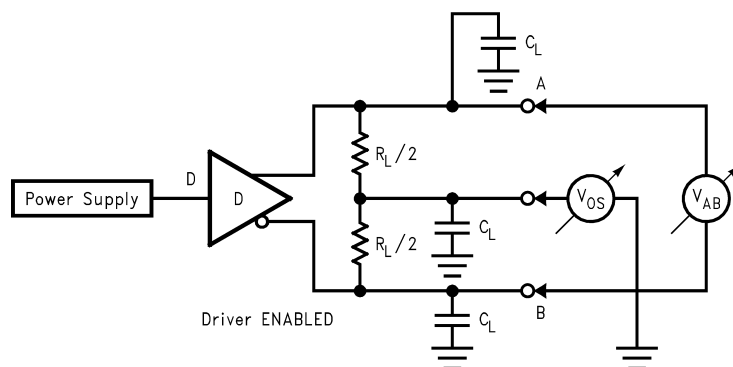


Figure 2. Differential Driver Test Circuit

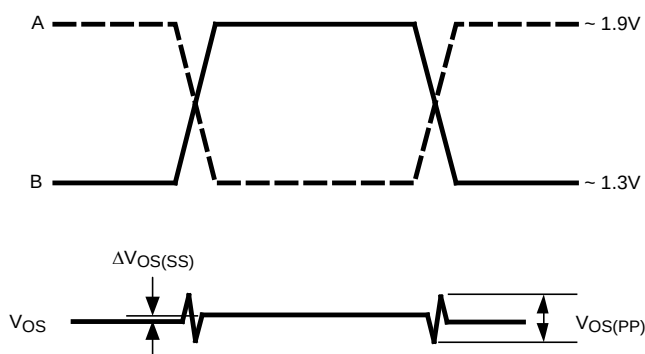


Figure 3. Differential Driver Waveforms

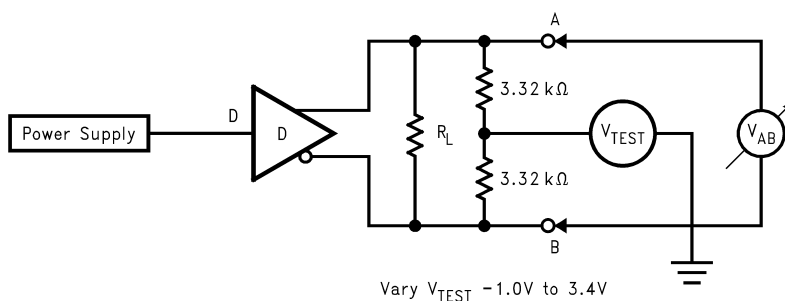


Figure 4. Differential Driver Full Load Test Circuit

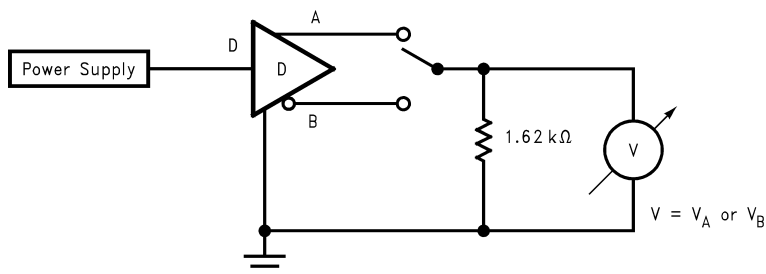


Figure 5. Differential Driver DC Open Test Circuit

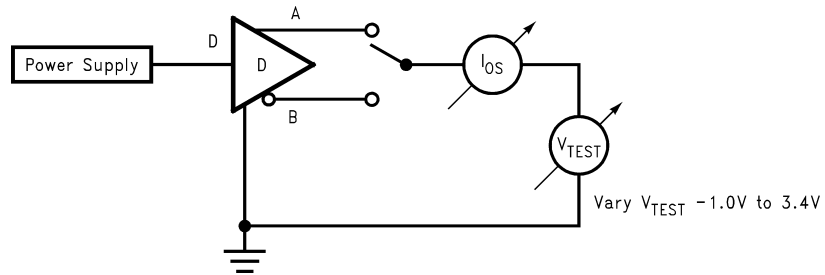


Figure 6. Differential Driver Short-Circuit Test Circuit

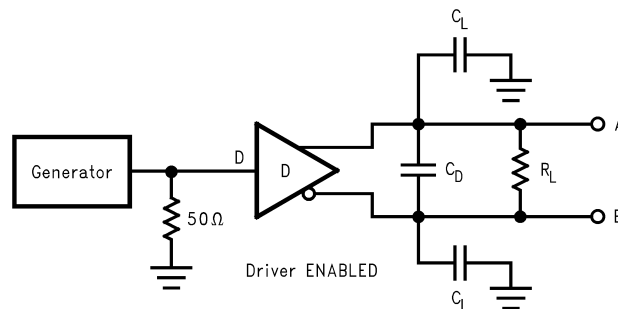


Figure 7. Driver Propagation Delay and Transition Time Test Circuit

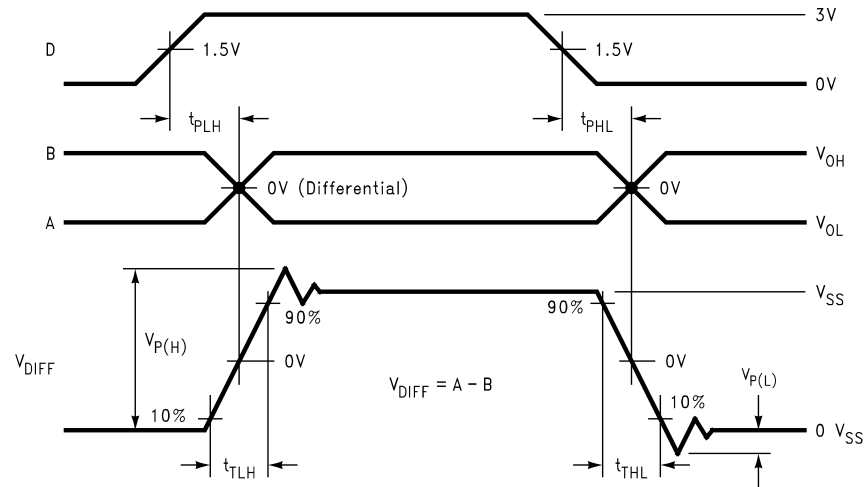


Figure 8. Driver Propagation Delays and Transition Time Waveforms

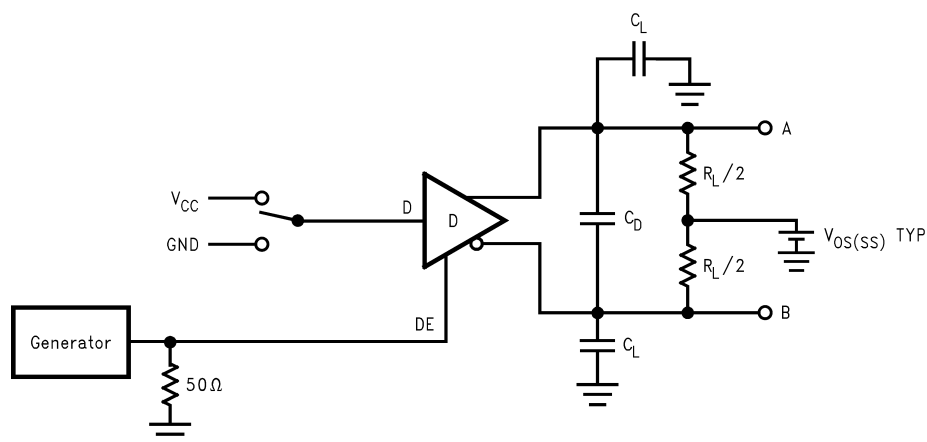


Figure 9. Driver TRI-STATE Delay Test Circuit

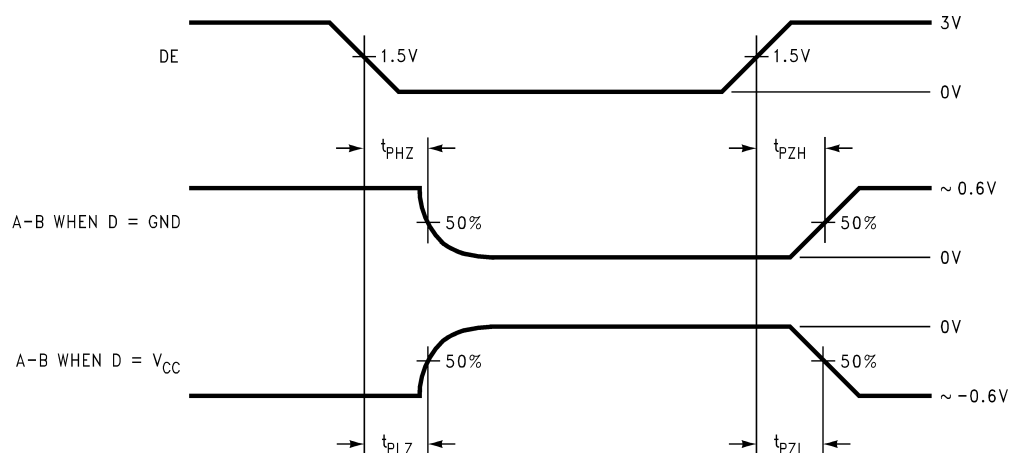


Figure 10. Driver TRI-STATE Delay Waveforms

Typical Performance Characteristics

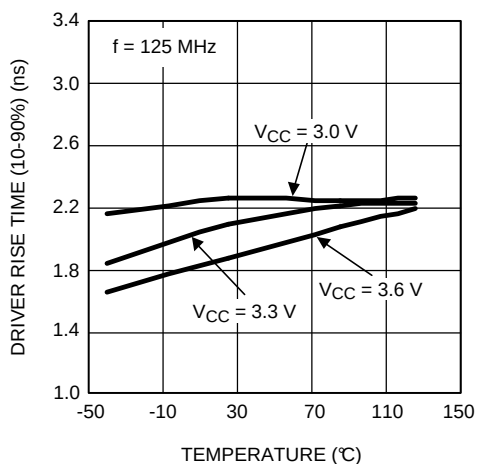


Figure 11. Driver Rise Time as a Function of Temperature

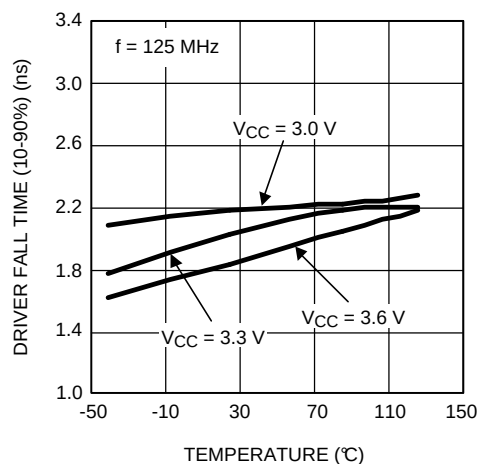


Figure 12. Driver Fall Time as a Function of Temperature

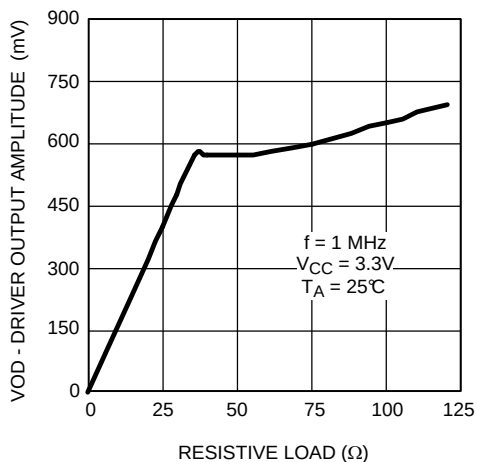


Figure 13. Driver Output Signal Amplitude as a Function of Resistive Load

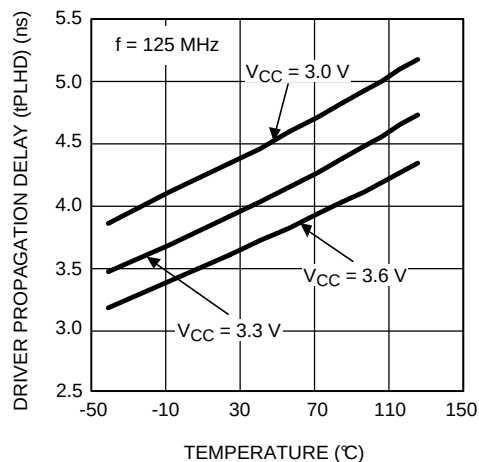


Figure 14. Driver Propagation Delay (tPLHD) as a Function of Temperature

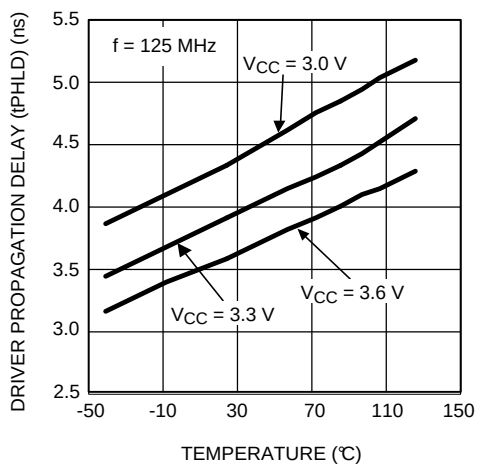


Figure 15. Driver Propagation Delay (tPHLD) as a Function of Temperature

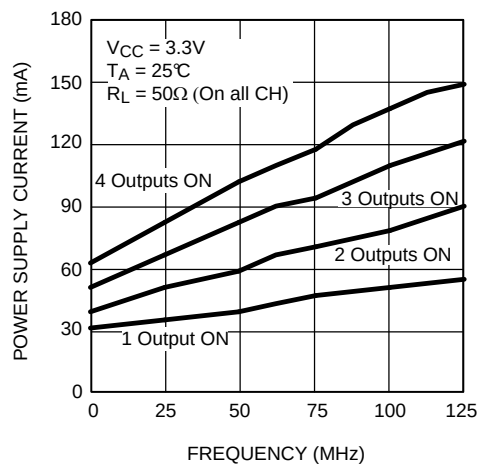


Figure 16. Driver Power Supply Current as a Function of Frequency

REVISION HISTORY

Changes from Revision D (April 2013) to Revision E	Page
• Changed layout of National Data Sheet to TI format	9

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS91M124TMA/NOPB	ACTIVE	SOIC	D	16	48	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 85	DS91M124 TMA	Samples
DS91M124TMAX/NOPB	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 85	DS91M124 TMA	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

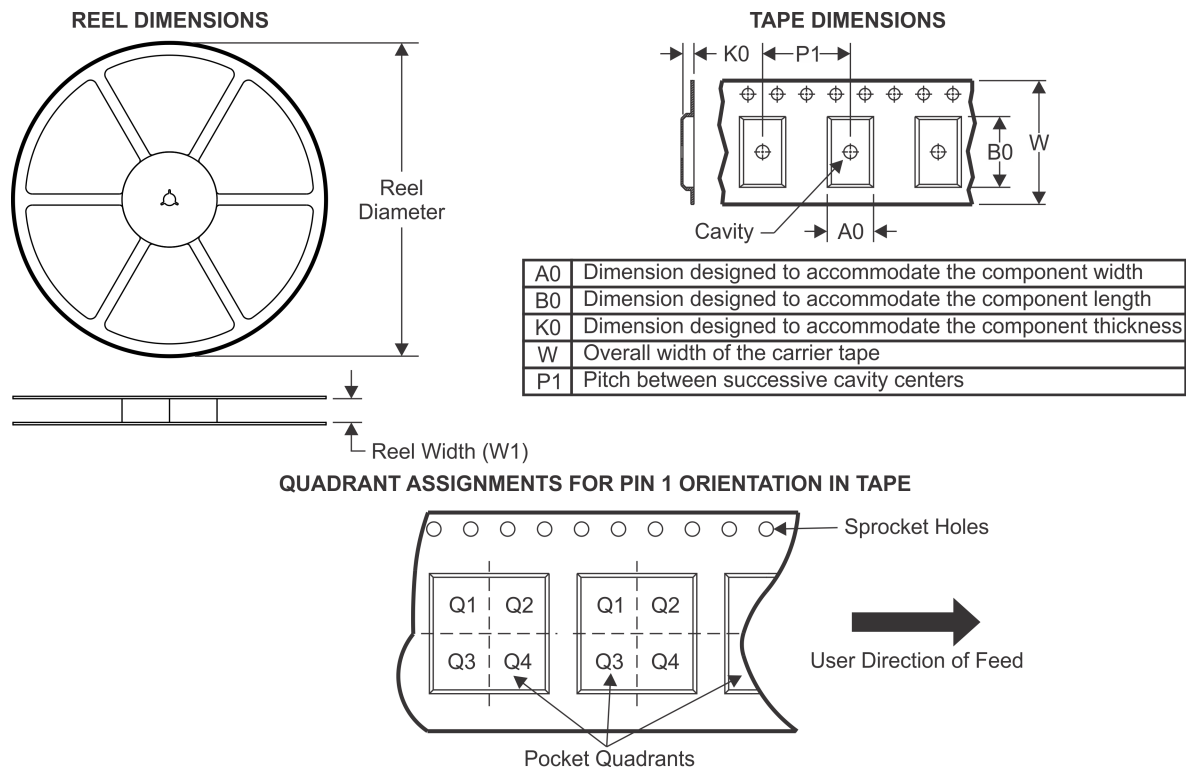
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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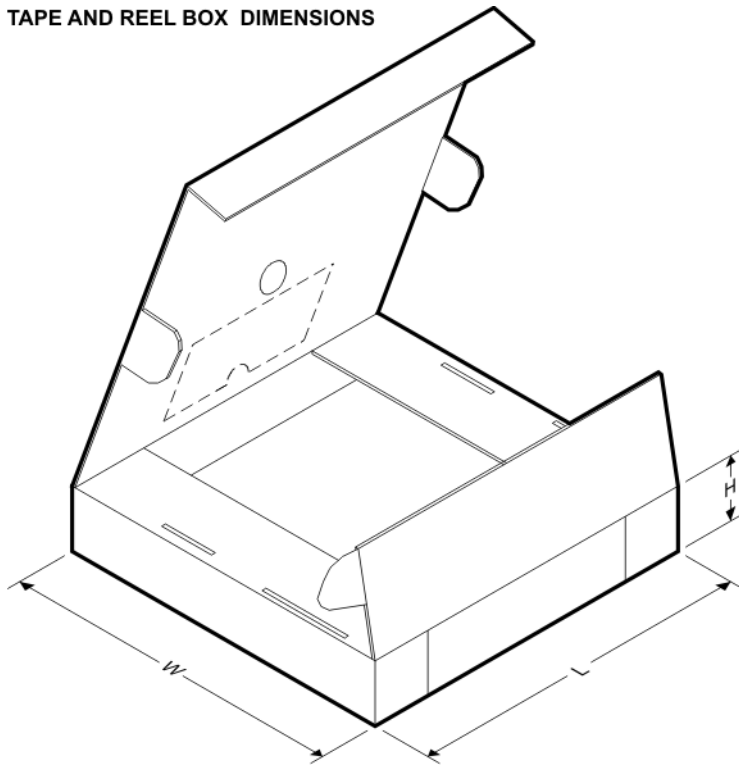
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TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS91M124TMAX/NOPB	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

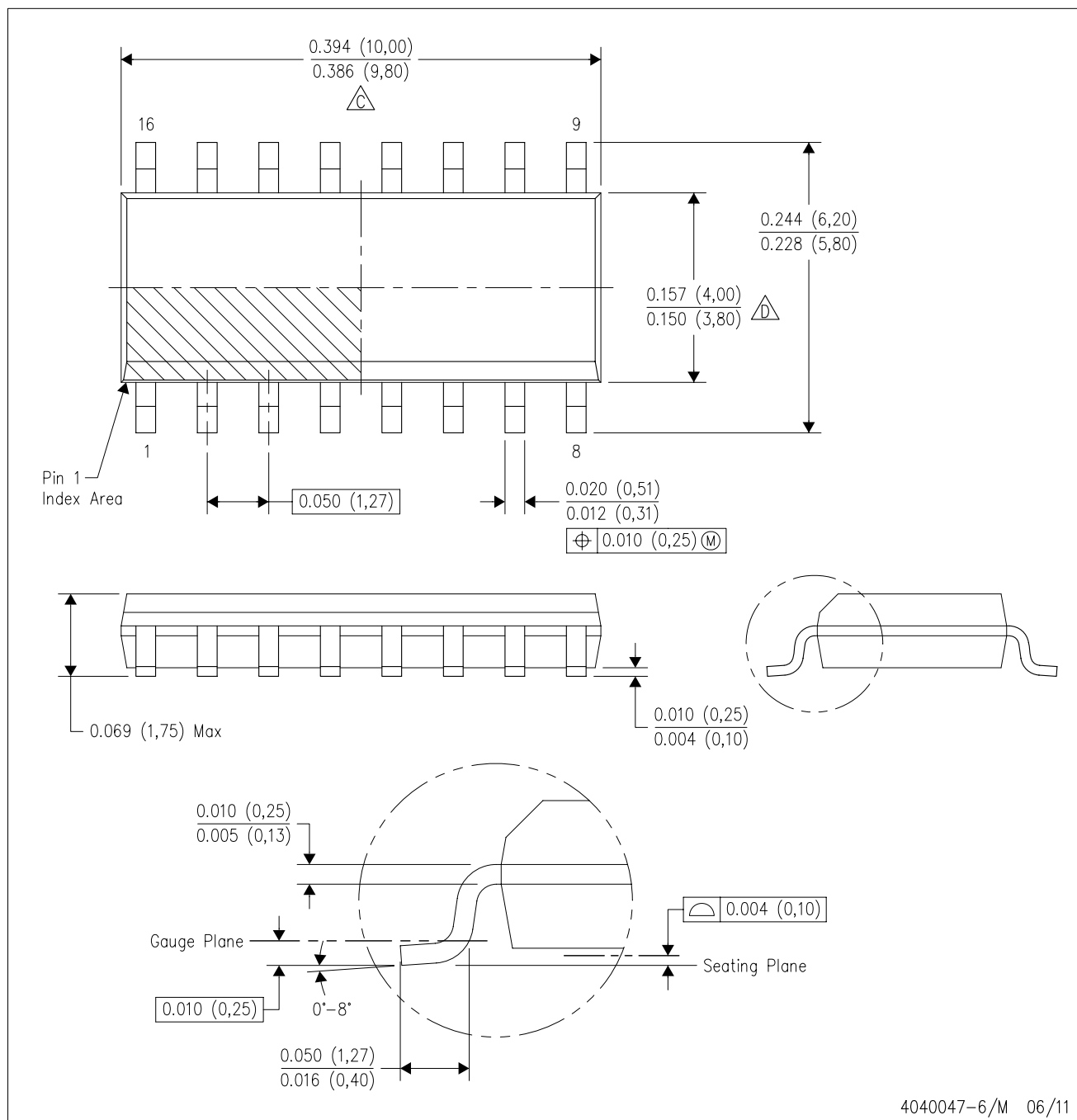


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS91M124TMAX/NOPB	SOIC	D	16	2500	367.0	367.0	35.0

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

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