DS90Ux941AS-Q1EVM User's Guide

The DS90Ux941AS-Q1EVM (Evaluation Module) converts DSI to FPD-Link III. This kit will demonstrate the functionality and operation of the DS90Ux941AS-Q1. The DS90Ux941AS-Q1 is a DSI to FPD-Link III Serializer which, in conjunction with the DS90Ux940-Q1/DS90Ux948-Q1 Deserializers, takes the data from a DSI serial stream and translates it into either single- or dual-lane FPD-Link III interface. The DS90Ux941AS-Q1 serializes a MIPI DSI input supporting video resolutions up to 2K, WUXGA and 1080p60 with 24-bit color depth.

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1 General Description

The DS90Ux941AS-Q1EVM (Evaluation Module) converts DSI to FPD-Link III. This kit will demonstrate the functionality and operation of the DS90Ux941AS-Q1. The DS90Ux941AS-Q1 is a DSI to FPD-Link III Serializer which, in conjunction with the DS90Ux940-Q1/DS90Ux948-Q1 Deserializers, takes the data from a DSI serial stream and translates it into either single- or dual-lane FPD-Link III interface. The DS90Ux941AS-Q1 serializes a MIPI DSI input supporting video resolutions up to 2K, WUXGA and 1080p60 with 24-bit color depth.

The FPD-Link III interface supports video and audio data transmission and full duplex control, including I2C communication, over the same differential link. Consolidation of video data and control over two differential pairs reduces the interconnect size and weight and simplifies system design. EMI is minimized by the use of low voltage differential signaling, data scrambling, and randomization.

The demo board is not intended for EMI testing. The demo board was designed for easy accessibility to device pins with tap points for monitoring or applying signals, additional pads for termination, and multiple connector options.

2 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified for Automotive Applications With the Following Results:
  - Device Temperature Grade 2: −40℃ to +105℃ Ambient Operating Temperature
  - Device HBM ESD Classification Level 3A
  - Device CDM ESD Classification Level C5
- Supports Pixel Clock Frequency up to 210 MHz for 2K (2880x1080), WUXGA (1920x1200), or 1080p60 (1920x1080) Resolutions with 24-Bit Color Depth
- MIPI D-PHY / Display Serial Interface (DSI) Receiver Provides a High-Bandwidth Interface to Video Processor or FPGA
  - DSI Input Port with Up to 4 Data Lanes
  - Up to 1.5 Gbps Per Lane
  - ECC and CRC Generation
  - Virtual Channel Capability
- Single and Dual FPD-Link III Outputs
  - Single Link: Up to 105-MHz Pixel Clock
  - Dual Link: Up to 210-MHz Pixel Clock

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3 System Requirements

To demonstrate, the following is required:

1. FPD-Link III compatible Deserializer
    1. DS90Ux940-Q1, DS90Ux948-Q1 up to 1080p60
2. DSI source
3. Optional I^2C controller
4. Power supply for 12 V at 1 A (required)

4 Contents of the Demo Evaluation Kit

One EVM board with the DS90Ux941A-Q1

5 Applications Diagram

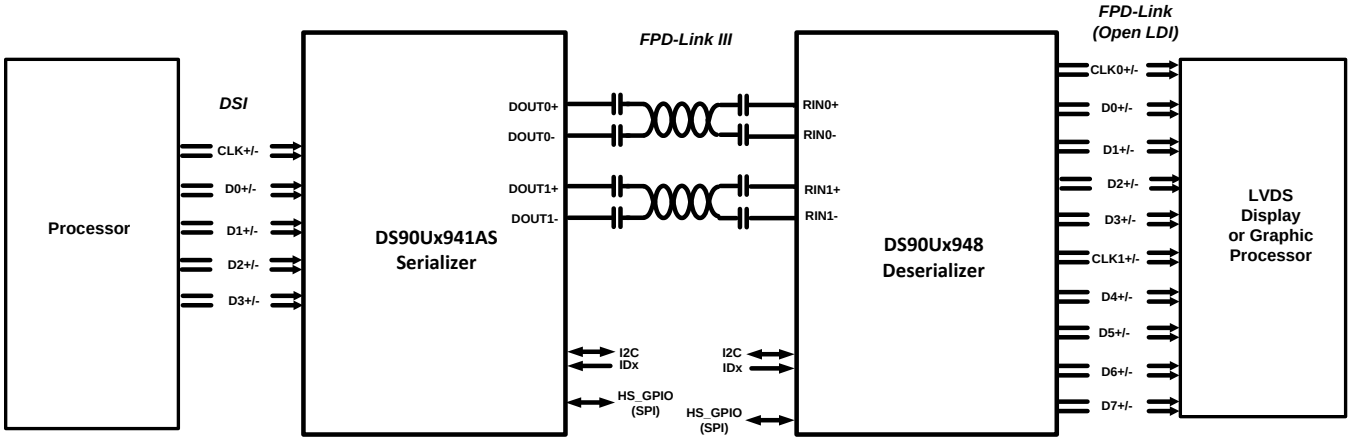


Figure 1. Applications Diagram

6 Typical Configuration

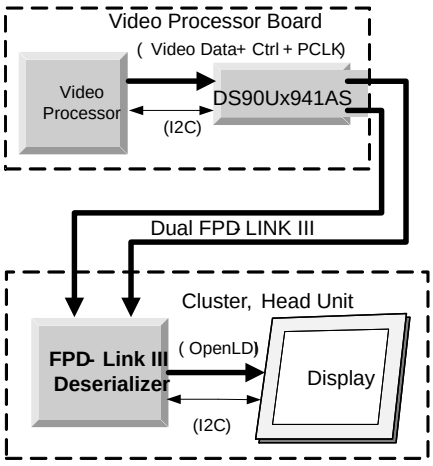


Figure 2. Typical Configuration

Figure 1 and Figure 2 show the use of the chipset in a display application.

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7 Quick Start Guide

1. Configure switches S2, S3, S5 and S6 to set device's operating modes
   - S2: MODE_SEL0 = 4 (default factory setting)
   - S3: IDx = 1 (address 0x18 - default factory setting)
   - S6: MODE_SEL1 = 1 (default factory setting)
   - S5: PDB and INTB = OFF (PDB and INTB will be pulled up to VDDIO - default factory setting)
2. Connect P1 (DOUT[1:0]+/-) to a compatible Deserializer (for example, the DS90Ux940-Q1/DS90Ux948-Q1) using STP cable (default)
3. Connect J28 to 12V.
   a. Optional power options available (see Table 3)
4. Plug in DSI source to J8
5. Connect J14 with miniUSB (5-pin_ to USB A (4-pin)) cable to PC USB port

For details of pin names and pin functions, refer to the DS90Ux941AS-Q1 data sheets.

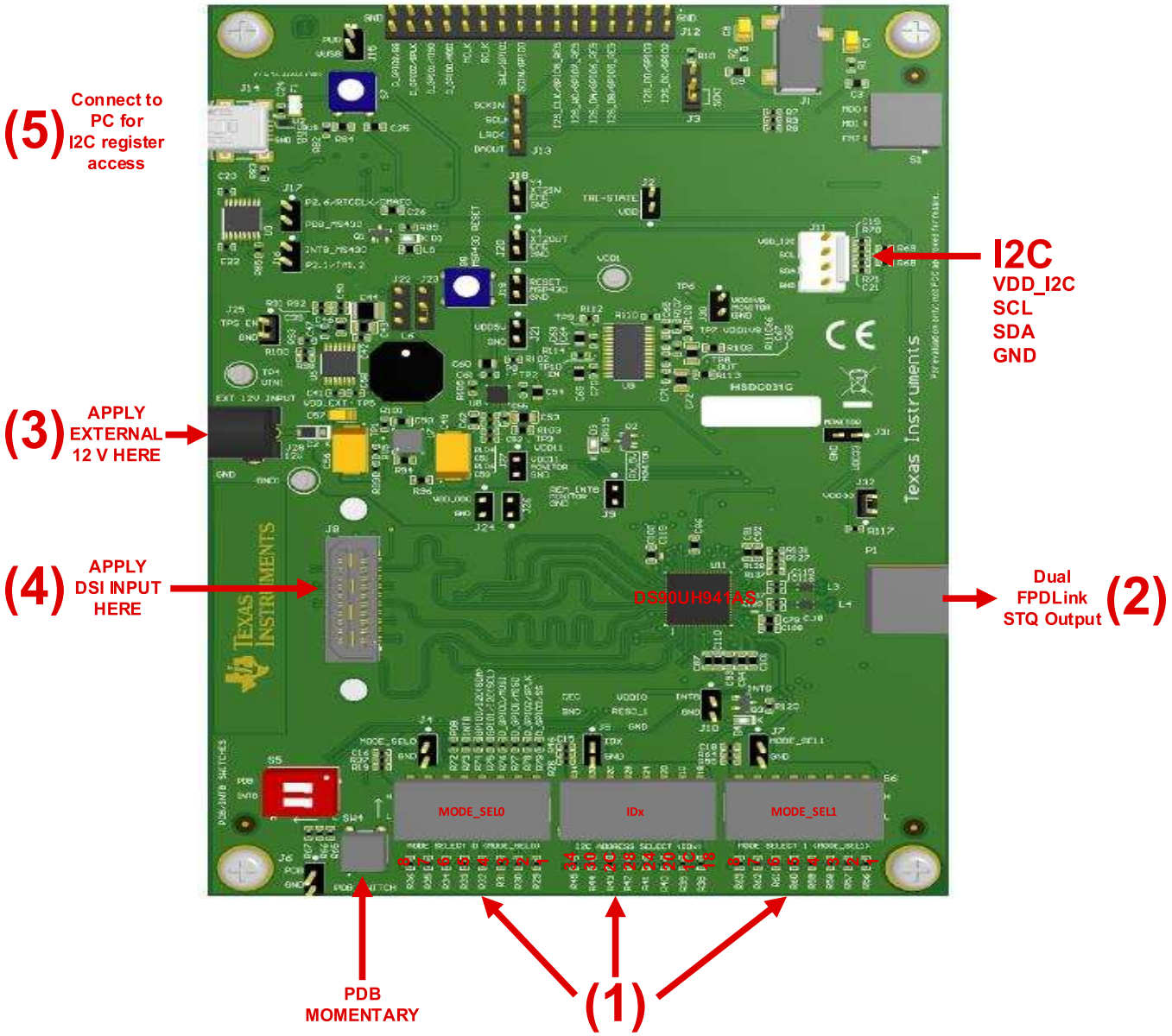


Figure 3. Interfacing to the EVM

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8 Default Jumper Settings

Ensure that the board has the default board jumper settings:

Table 1. Default Board Jumper Settings

JUMPER	JUMPER SETTINGS
J3	Connect 2 and 3
J22/J23	Connect J22 pin 2 to J23 pin 2
J24	Connect 1 and 2
J25	Connect 1 and 2
J32	Connect 1 and 2

9 Default Switch Settings

Ensure that the board has the default board switch settings:

Table 2. Default Board Switch Settings

SWITCH	SWITCH SETTINGS
S1	1-3 ON
S2	4 ON, 1-3, 5-8 OFF
S3	1 ON, 2-8 OFF
S5	1-2 OFF
S6	1 ON, 2-8 OFF

10 Demo Board Connections

Table 3. Power Supply

DESIGNATOR	SIGNAL	DESCRIPTION
J28	+12 V	12 V ±5% Main Power Single +12V power connector that supplies power to the entire board.
J27.1 (Optional)	+1.1 V	1.1 V ±5% Alternative to Main Power. **If used, remove R103.**
J30.1 (Optional)	+1.8 V	1.8 V ±5% Alternative to Main Power. **If used, remove R109.**
J31.1 (Optional)	+3.3 V	3.3 V ±5% Alternative to Main Power. **If used, remove R113.**
J23.1 (Optional)	+5 V	5 V ±5% Alternative to Main Power. **If used, remove jumper to J22.**

Table 4. FPD-Link III Output Signals P1

DESIGNATOR	PORT	SIGNAL
P1.1	FPD-Link III Port 0	DOUT0-
P1.3		DOUT0+
P1.2	FPD-Link III Port 1	DOUT1-
P1.4		DOUT1+

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Table 5. DSI Input Signals

DESIGNATOR	SIGNAL	DESCRIPTION
J8.33 J8.35	DSI0_D0_P DSI0_D0_N	DSI0 D0 input
J8.25 J8.27	DSI0_D1_P DSI0_D1_N	DSI0 D1 input
J8.17 J8.19	DSI0_CLK_P DSI0_CLK_N	DSI0 CLK input
J8.9 J8.11	DSI0_D2_P DSI0_D2_N	DSI0 D2 input
J8.1 J8.3	DSI0_D3_P DSI0_D3_N	DSI0 D3 input
J8.34 J8.36	DSI1_D0_P DSI1_D0_N	DSI1 D0 input
J8.26 J8.28	DSI1_D1_P DSI1_D1_N	DSI1 D1 input
J8.18 J8.20	DSI1_CLK_P DSI1_CLK_N	DSI1 CLK input
J8.10 J8.12	DSI1_D2_P DSI1_D2_N	DSI1 D2 input
J8.2 J8.4	DSI1_D3_P DSI1_D3_N	DSI1 D3 input

Table 6. USB2ANY Connector

DESIGNATOR	DESCRIPTION
J14	mini USB 5 pin

Table 7. I2C/CCI Interface Header

DESIGNATOR	SIGNAL
J11.1	VDDI2C
J11.2	SCL
J11.3	SDA
J1.4	GND

Table 8. GPIO/Audio Interface

DESIGNATOR	SIGNAL	DESCRIPTION
J12.2	I2S_DC/GPIO2	Slave Mode I2S Data Input / Remote or Local I/O
J12.4	I2S_DD/GPIO3	Slave Mode I2S Data Input / Remote or Local I/O
J12.8	I2S_DB/GPIO5_REG	Slave Mode I2S Data Input / Remote or Local I/O
J12.10	I2S_DA/GPIO6_REG	Slave Mode I2S Data Input / Remote or Local I/O
J12.12	I2S_WC/GPIO7_REG	Slave Mode I2S Word Clock Input / Remote or Local I/O
J12.14	I2S_CLK/GPIO8_REG	Slave Mode I2S Clock Input / Remote or Local I/O
J12.18	SDIN/GPIO0	Master I2S Data Input / Remote or Local I/O
J12.20	SWC/GPIO1	Master I2S Word Clock Input / Remote or Local I/O
J12.22	SCLK	Master I2S Clock Input
J12.24	MCLK	Master Mode I2S System Clock

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Table 9. SPI/D_GPIO Interface

DESIGNATOR	SIGNAL	DESCRIPTION
J12.26	D_GPIO0/MOSI	I/O in FPD-Link III mode / Master Out, Slave In
J12.28	D_GPIO1/MISO	I/O in FPD-Link III mode / Master In, Slave Out
J12.30	D_GPIO2/SPLK	I/O in FPD-Link III mode / Serial Clock
J12.32	D_GPIO3/SS	I/O in FPD-Link III mode / Slave Select

Configuration of the device may be done through the MODE_SEL[1:0]. These modes are latched into register location during power-up:

Table 10. MODE_SEL[1:0] Settings

MODE	SETTING	FUNCTION
Split	0	Disable
	1	Enable
DSI Lanes	00	1 DSI Lane
	01	2 DSI Lanes
	10	3 DSI Lanes
	11	4 DSI Lanes
Non-continuous Clock Mode	0	Continuous mode
	1	Non-continuous mode
COAX	0	Enable FPD-Link III for twisted pair cabling
	1	Enable FPD-Link III for coaxial cabling
Disable DSI	0	Enable DSI
	1	Disable DSI

Table 11. Configuration Select (MODE_SEL0) - SW-DIP8 - S2(1)

MODE NO.	V_{TARGET} VOLTAGE RANGE			V_{TARGET} STRAP VOLTAGE	SUGGESTED STRAP RESISTORS (1% TOL)		SPLIT	DSI LANES
	V_{MIN}	V_{TYP}	V_{MAX}	(V); $V_{(VDD18)}$ = 1.8 V	R_3 (kΩ)	R_4 (kΩ)		
0	0	0	0.126 × $V_{(VDD18)}$	0	OPEN	10.0	0	1
1	0.179 × $V_{(VDD18)}$	0.211 × $V_{(VDD18)}$	0.244 × $V_{(VDD18)}$	0.380	73.2	20.0	0	2
2	0.272 × $V_{(VDD18)}$	0.325 × $V_{(VDD18)}$	0.364 × $V_{(VDD18)}$	0.585	60.4	30.1	0	3
3	0.404 × $V_{(VDD18)}$	0.441 × $V_{(VDD18)}$	0.472 × $V_{(VDD18)}$	0.794	51.1	40.2	0	4
4	0.526 × $V_{(VDD18)}$	0.556 × $V_{(VDD18)}$	0.590 × $V_{(VDD18)}$	1.001	40.2	51.1	1	1
5	0.643 × $V_{(VDD18)}$	0.673 × $V_{(VDD18)}$	0.708 × $V_{(VDD18)}$	1.211	30.1	61.9	1	2
6	0.763 × $V_{(VDD18)}$	0.790 × $V_{(VDD18)}$	0.825 × $V_{(VDD18)}$	1.421	18.7	71.5	1	3
7	0.880 × $V_{(VDD18)}$	$V_{(VDD18)}$	$V_{(VDD18)}$	1.8	10	OPEN	1	4

(1) Only set one high

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Table 12. Configuration Select (MODE_SEL1) - SW-DIP8 - S6(1)

MODE NO.	V_{TARGET} VOLTAGE RANGE			V_{TARGET} STRAP VOLTAGE	SUGGESTED STRAP RESISTORS (1% TOL)		CLOCK	COAX	DISABLE DSI
	V_{MIN}	V_{TYP}	V_{MAX}	(V); $V_{(VDD18)}$ = 1.8 V	R_5 (kΩ)	R_6 (kΩ)			
0	0	0	0.126 × $V_{(VDD18)}$	0	OPEN	10.0	0	0	0
1	0.179 × $V_{(VDD18)}$	0.211 × $V_{(VDD18)}$	0.244 × $V_{(VDD18)}$	0.380	73.2	20.0	0	0	1
2	0.272 × $V_{(VDD18)}$	0.325 × $V_{(VDD18)}$	0.364 × $V_{(VDD18)}$	0.585	60.4	30.1	0	1	0
3	0.404 × $V_{(VDD18)}$	0.441 × $V_{(VDD18)}$	0.472 × $V_{(VDD18)}$	0.794	51.1	40.2	0	1	1
4	0.526 × $V_{(VDD18)}$	0.556 × $V_{(VDD18)}$	0.590 × $V_{(VDD18)}$	1.001	40.2	51.1	1	0	0
5	0.643 × $V_{(VDD18)}$	0.673 × $V_{(VDD18)}$	0.708 × $V_{(VDD18)}$	1.211	30.1	61.9	1	0	1
6	0.763 × $V_{(VDD18)}$	0.790 × $V_{(VDD18)}$	0.825 × $V_{(VDD18)}$	1.421	18.7	71.5	1	1	0
7	0.880 × $V_{(VDD18)}$	$V_{(VDD18)}$	$V_{(VDD18)}$	1.8	10	OPEN	1	1	1

(1) Only set one high

The strapped values can be viewed and/or modified in the following register locations:

- SPLIT : Latched into DUAL_CTL(0x5B[2:0]).
- DSI LANES : Latched into BRIDGE_CTL (0x4F[3:2]).
- CLOCK : Latched into BRIDGE_CTL (0x4F[7]).
- COAX : Latched into DUAL_CTL(0x5B[7]).
- DISABLE DSI : Latched into RESET (0x01[3]).

Table 13. IDx SW-DIP8 - S3(1)

DESIGNATOR	7-BIT ADDRESS	8-BIT ADDRESS
S3.1 (Default)	0x0C	0x18
S3.2	0x0E	0x1C
S3.3	0x10	0x20
S3.4	0x12	0x24
S3.5	0x14	0x28
S3.6	0x16	0x2C
S3.7	0x18	0x30
S3.8	0x1A	0x34

(1) Only set one high.

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11 ALP Software Setup

11.1 System Requirements

Operating System:	Windows 10 64-bit
USB:	USB2ANY
USB2ANY Firmware Version:	2.7.0.0

11.2 Download Contents

TI Analog LaunchPAD can be downloaded from: http://www.ti.com/tool/alp.

Download and extract the “snlc048.zip” file to a temporary location that can be deleted later.

Make sure J14 on the DS90Ux941AS-Q1 is connected to a PC USB port with USB cable and power is applied to the DS90Ux941AS-Q1 EVM.

The following installation instructions are for the Windows 10 64-bit Operating System.

11.3 Installation of the ALP Software

Execute the ALP Setup Wizard program called “ALPF_setup_v_x_x_x.exe” that was extracted to a temporary location on the local drive of your PC.

There are 7 steps to the installation once the setup wizard is started:

1. Select the "Next" button.
2. Select “I accept the agreement” and then select the “Next” button.
3. Select the location to install the ALP software and then select the “Next” button.
4. Select the location for the start menu shortcut and then select the “Next” button.
5. There will then be a screen that allows the creation of a desktop icon. After selecting the desired choices select the “Next” button.
6. Select the “Install” button, and the software will then be installed to the selected location.
7. Uncheck “Launch Analog LaunchPAD” and select the “Finish” button. The ALP software will start if “Launch Analog LaunchPAD” is checked, but it will not be useful until the USB driver is installed and board is attached.

Connect J14 USB jack of the DS90Ux941AS-Q1Q EVM board to a PC/laptop USB port using a Type A 

A to mini-B 

MINI USB cable. Power the DS90Ux941AS-Q1Q EVB board with a 12 VDC power supply. The “Found New Hardware Wizard” will open on the PC/laptop.

11.4 Installation of the Device Profiles

There are 2 steps to add the DS90Ux941AS-Q1 profile:

1. Download the ALP-PROFILE-UPDATE, snlc062.zip, from the TI Analog LaunchPAD page: http://www.ti.com/tool/alp.
2. Extract the files and run the executable file ALP_PROFILE_UPDATE_v02_setup_v_x_x_x.exe. The profile will be installed to the profile folder found at: C:\Program Files (x64)\Texas Instruments\Analog LaunchPAD vx.x.x\Profiles\.

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11.5 Start-Up - Software Description

Make sure all the software has been installed and the hardware is powered on and connected to the PC. Execute “Analog LaunchPAD” shortcut from the start menu. The default start menu location is under All Programs > Texas Instruments > Analog LaunchPAD vx.x.x > Analog LaunchPAD to start MainGUI.exe.



Figure 4. Launching ALP

The application should come up in the state shown in the figure below. If it does not, see Section 12, “Troubleshooting ALP Software”.

Under the Devices tab click on “DS90Ux941AS-Q1” to select the device and open up the device profile and its associated tabs.

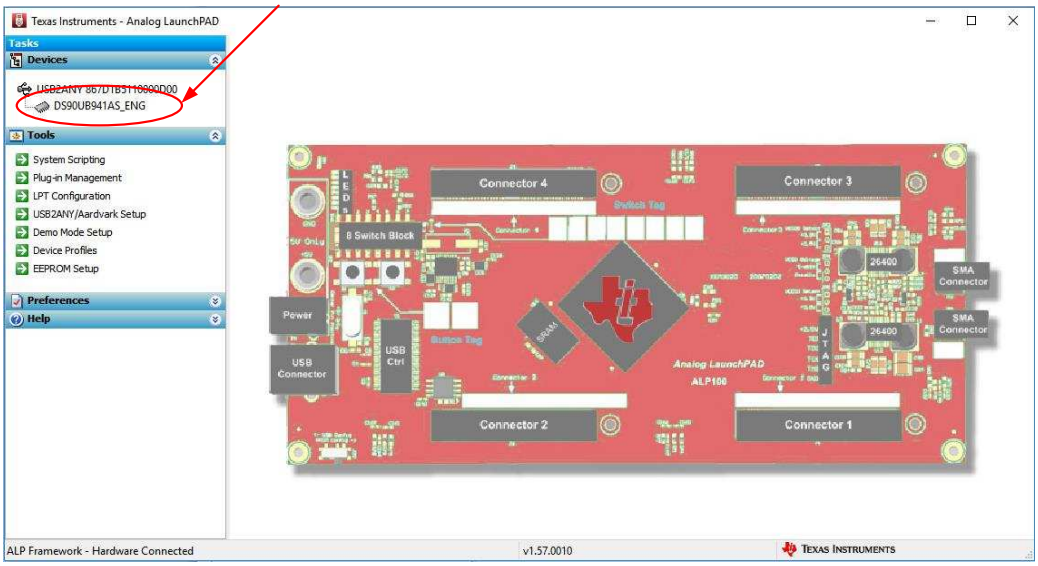


Figure 5. Initial ALP Screen

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After selecting the DS90Ux941AS-Q1, the screen shown in Figure 6 should appear.

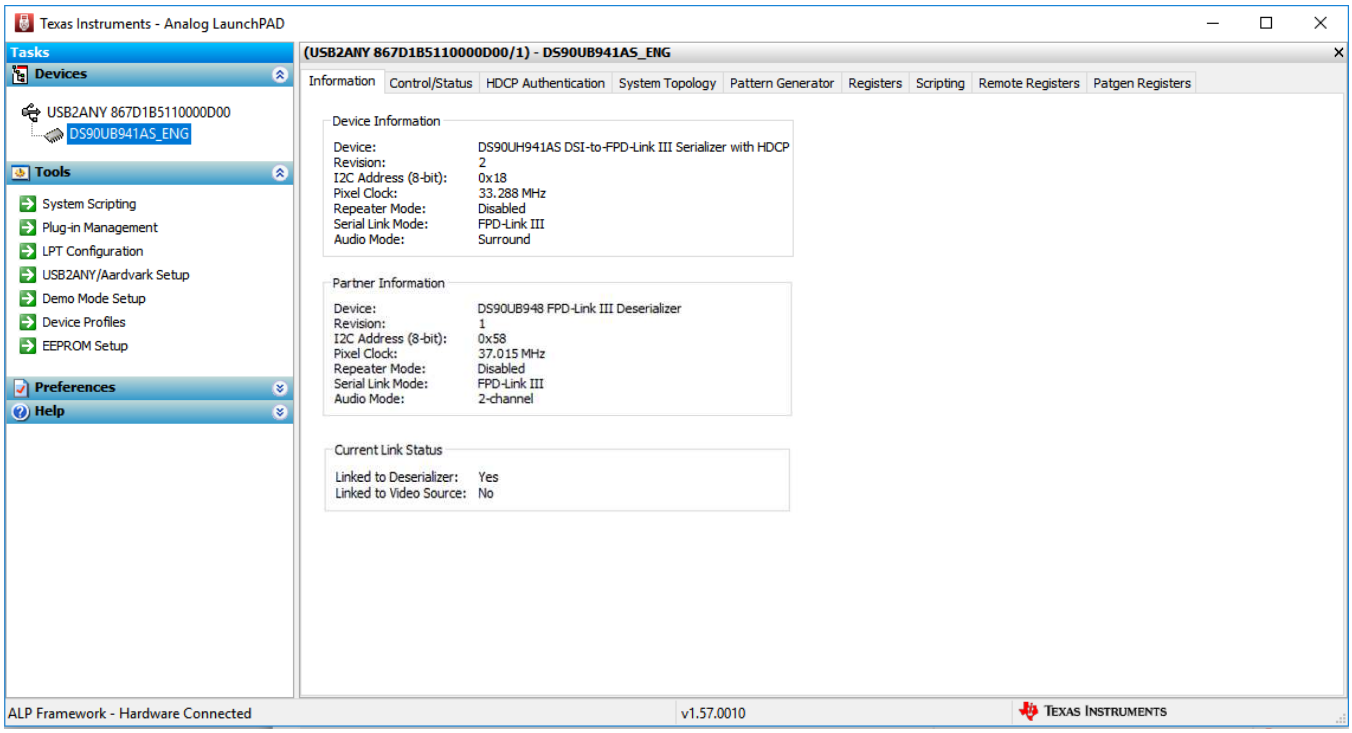


Figure 6. Follow-Up Screen

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11.6 Information Tab

The Information tab is shown in Figure 7. Note that the device revision could be different.

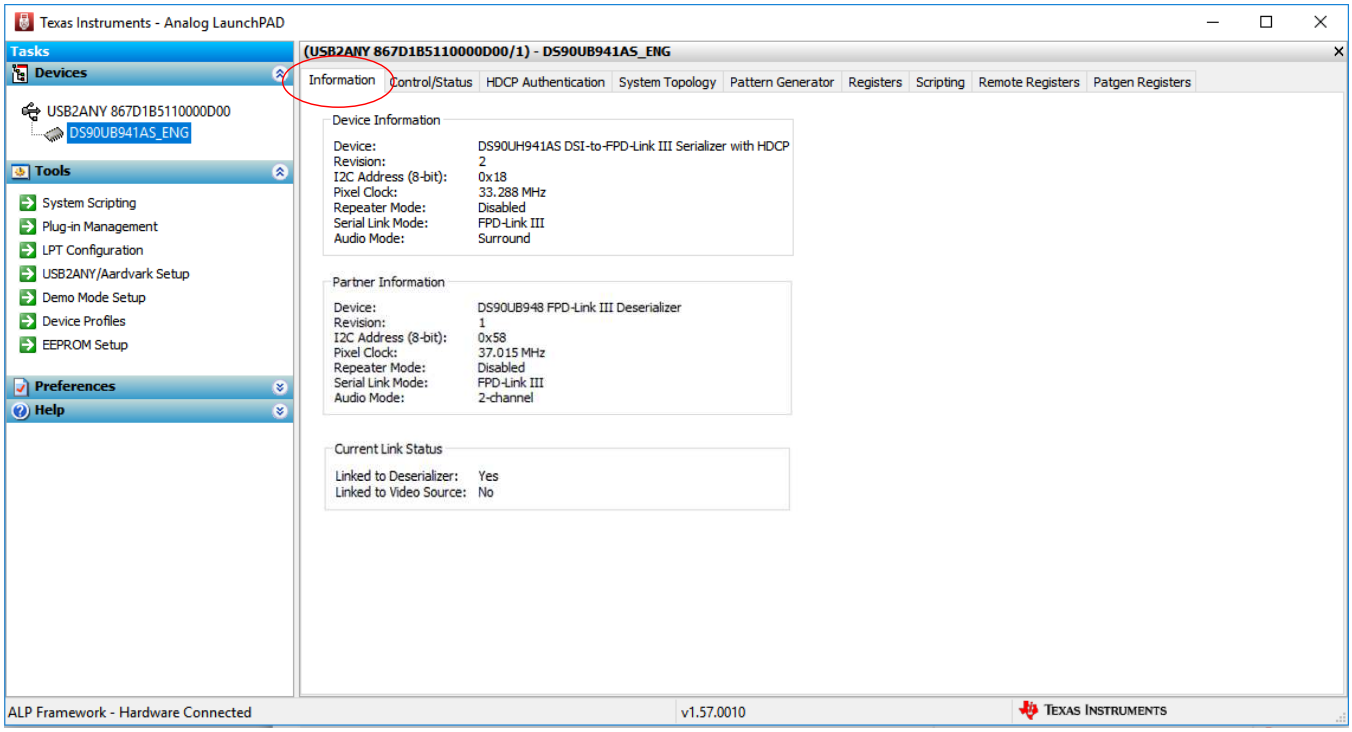


Figure 7. ALP Information Tab

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11.7 Pattern Generator Tab

The SER Pattern Generator tab is shown in Figure 8.

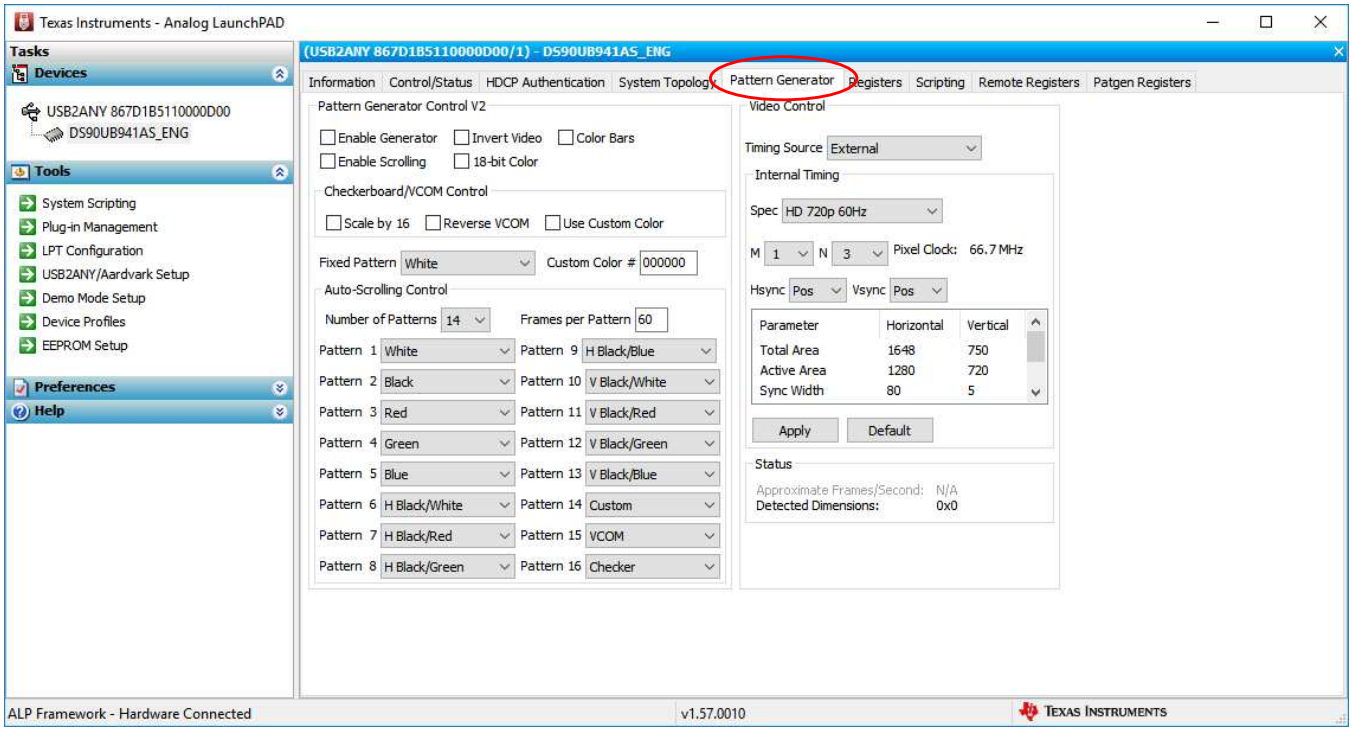


Figure 8. ALP Pattern Generator Tab

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11.8 Registers Tab

The Register tab is shown in Figure 9.

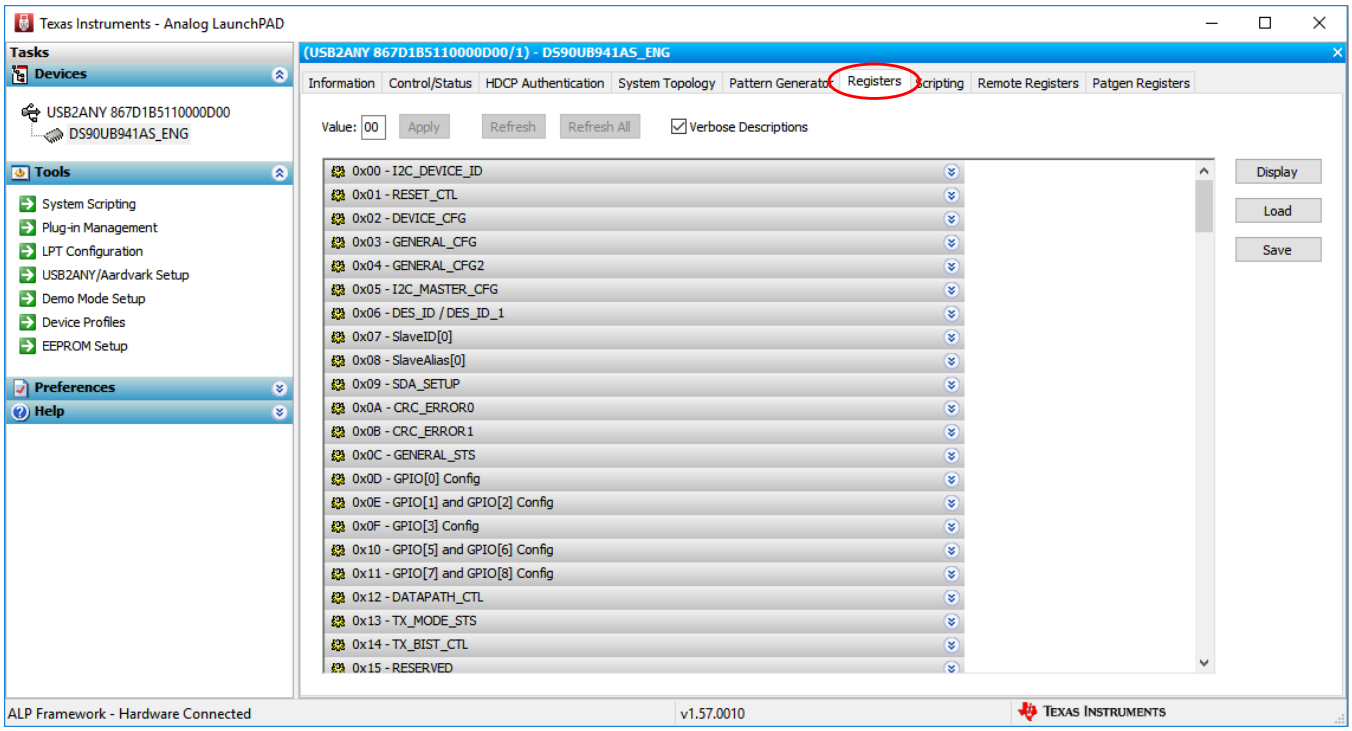


Figure 9. ALP Registers Tab

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11.9 Registers Tab - Address 0x00 Selected

Figure 10 shows the Address 0x00 selected. Note that the “Value:” box (Value: 18) will now show the hex value of that register.

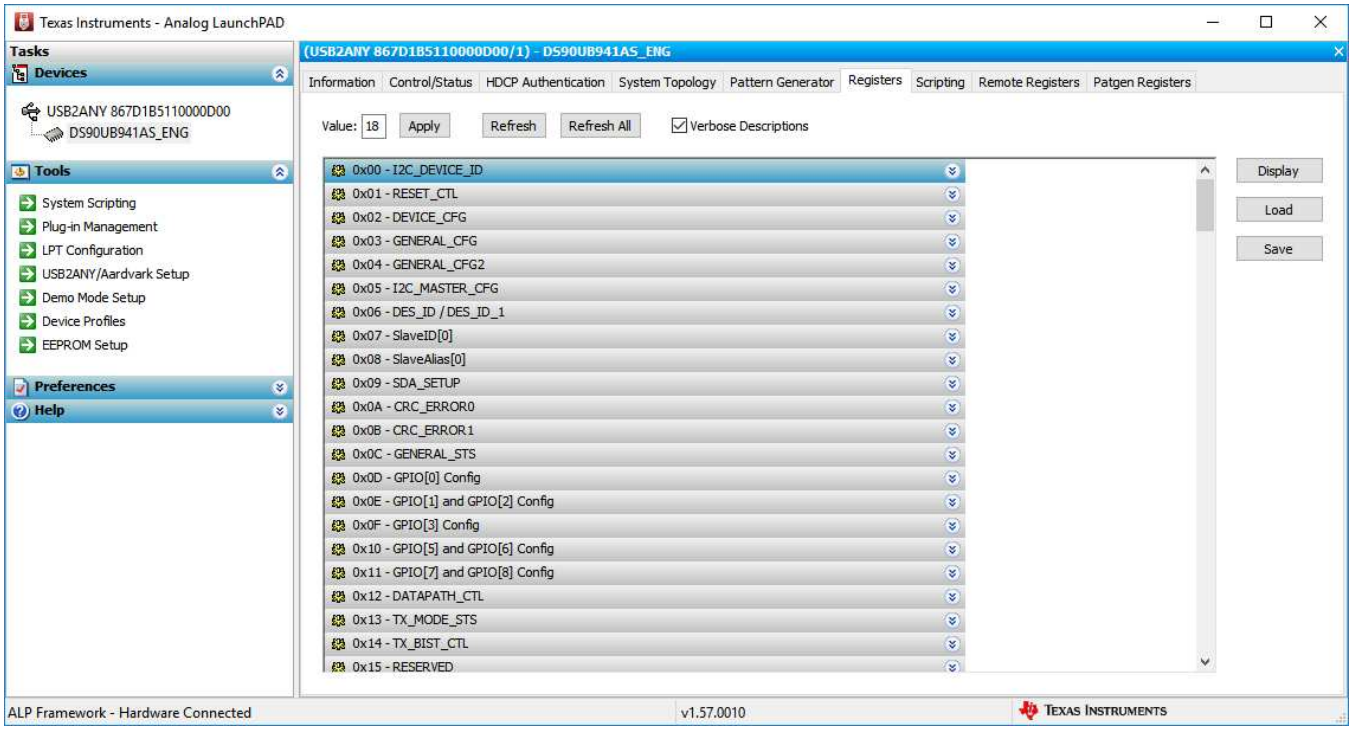


Figure 10. ALP Device ID Selected

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11.10 Registers Tab - Address 0x00 Expanded

To expand Address 0x00, double-click the Address bar



or single-click the  . The expanded Address 0x00 reveals the content for each bits. Any register address displayed can be expanded.

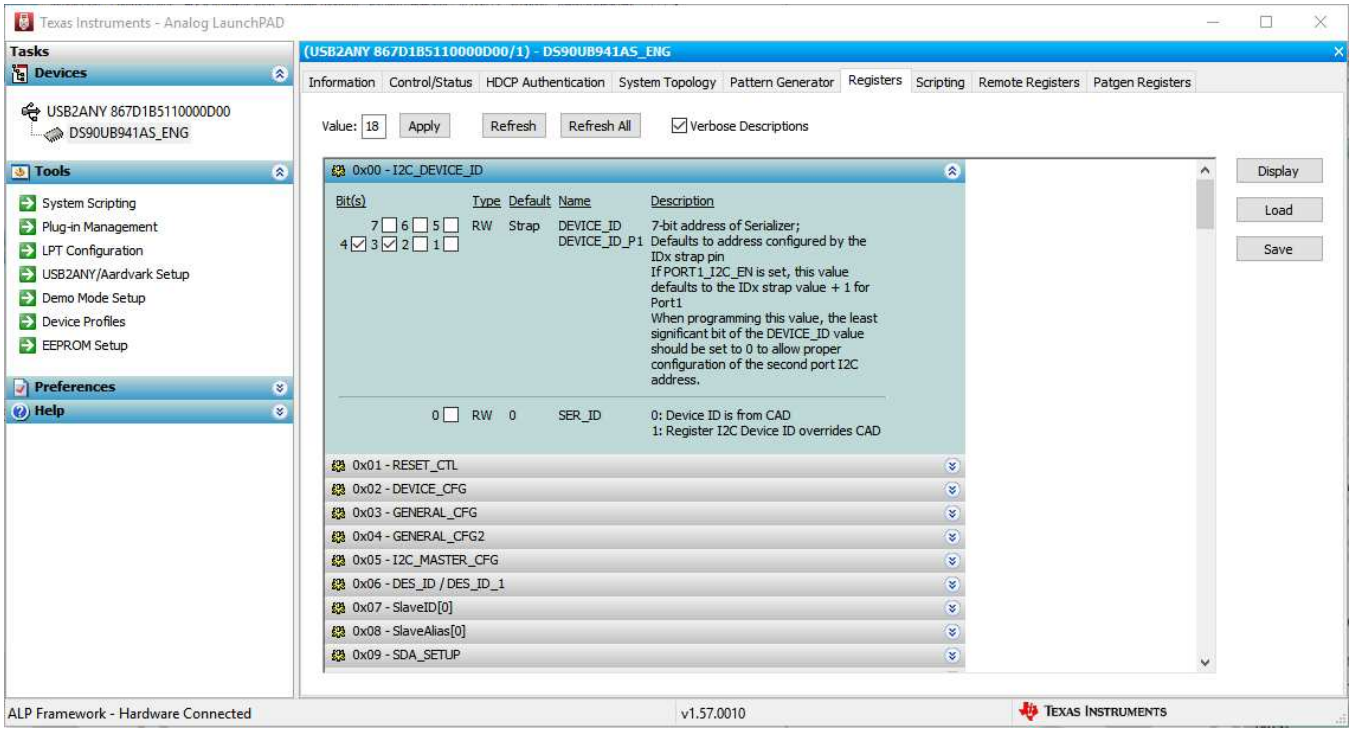
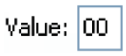
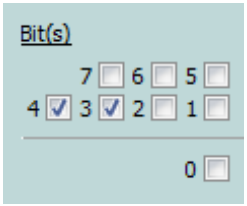


Figure 11. ALP Device ID Expanded

Users can change any RW Type register (

) by writing the hex value into the “Value:” box (

) or by clicking the checkboxes next to each register bit. A check mark indicates a "1" or R, while a blank checkbox indicates a “0” or W. Click the “Apply” button to write to the register, and “refresh” to see the new value of the selected (highlighted) register.



The box toggles on every mouse click.

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11.11 Scripting Tab

The Scripting tab is shown in Figure 12.

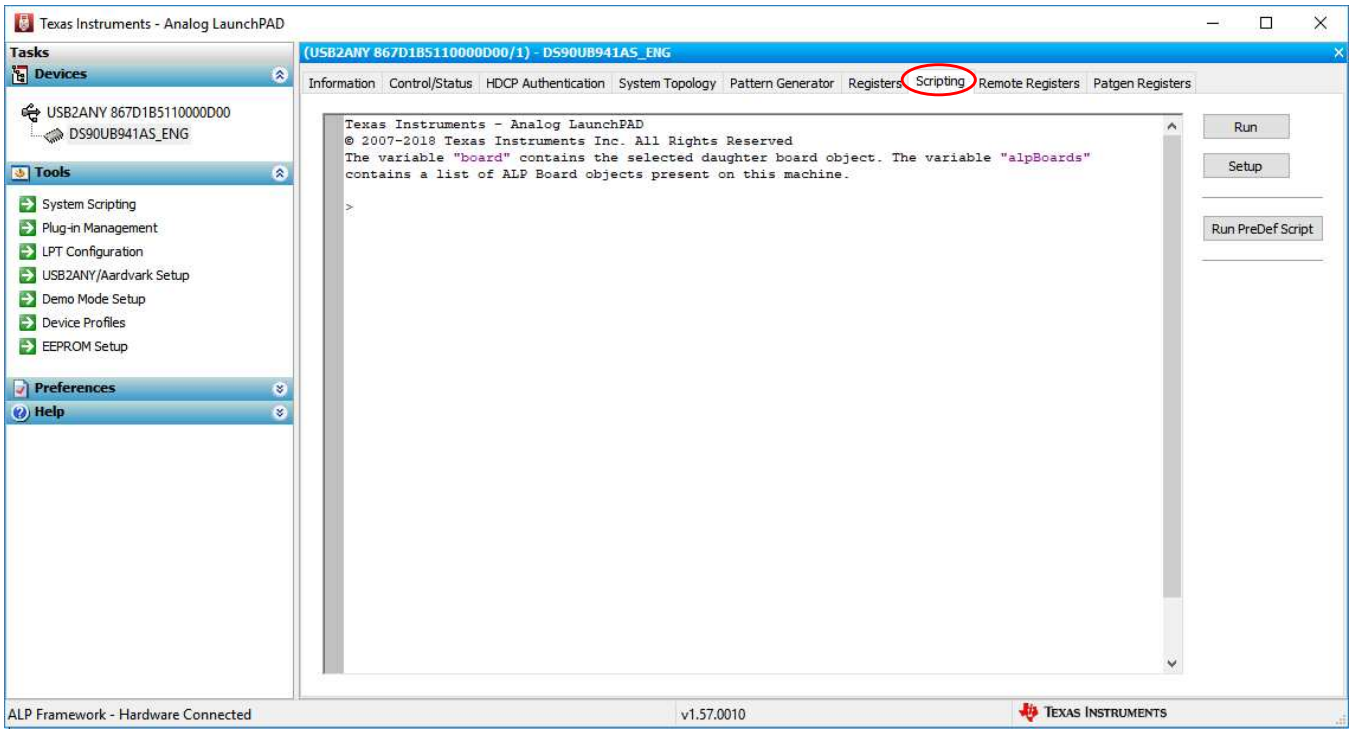


Figure 12. ALP Scripting Tab

The script window provides a full Python scripting environment to run scripts and interact with the device in an interactive or automated fashion.

WARNING

Directly interacting with devices either through register modifications or calling device support library functions can effect the performance and/or functionality of the user interface and may even crash the ALP Framework application.

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12 Troubleshooting ALP Software

12.1 ALP Loads the Incorrect Profile

If ALP opens with the incorrect profile loaded the correct profile can be loaded from the USB2ANY/Aardvark Setup found under the tools menu.

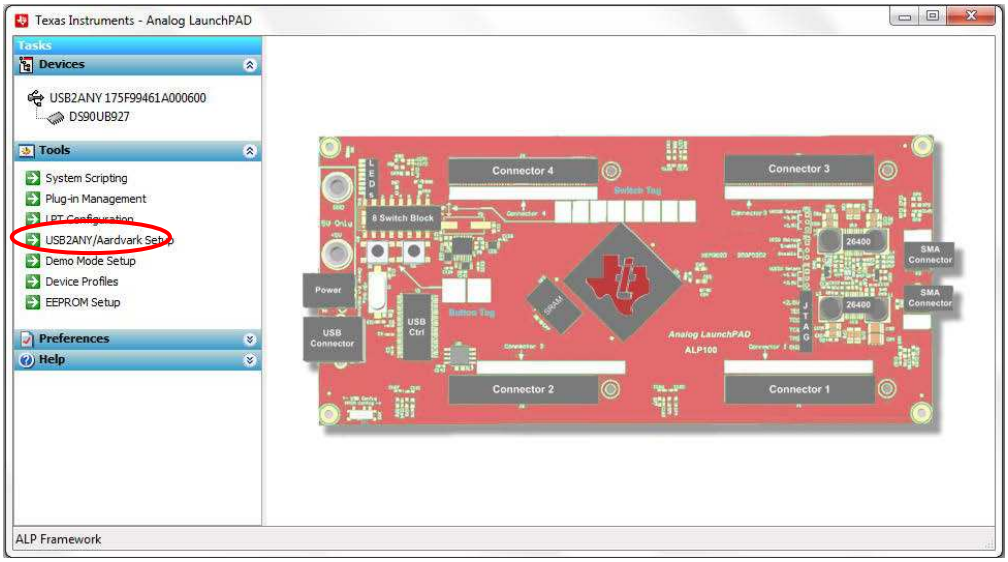


Figure 13. USB2ANY Setup

Highlight the incorrect profile in the Defined ALP Devices list and press the remove button.

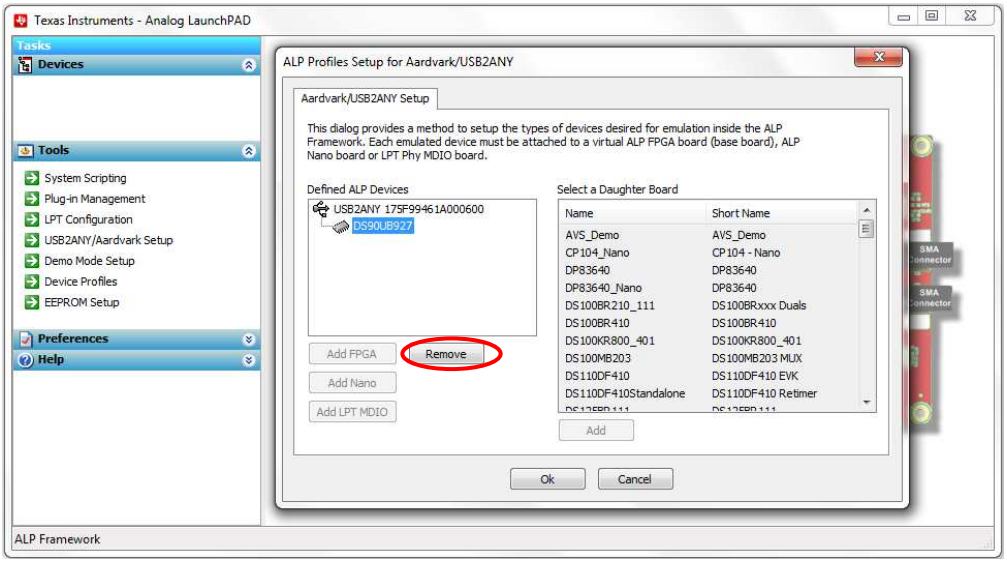


Figure 14. Remove Incorrect Profile

Find the correct profile under the Select a Daughter Board list, highlight the profile and press Add.

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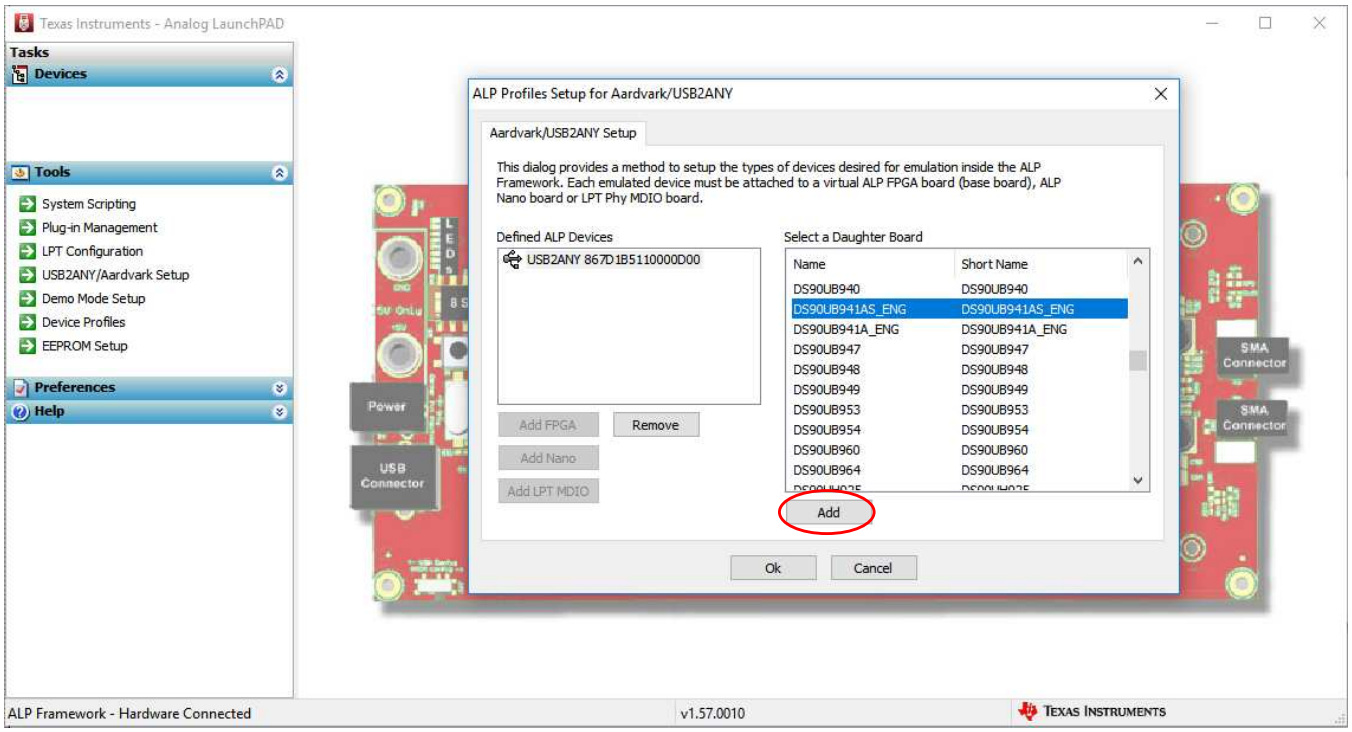


Figure 15. Add Correct Profile

Select Ok and the correct profile should now be loaded.

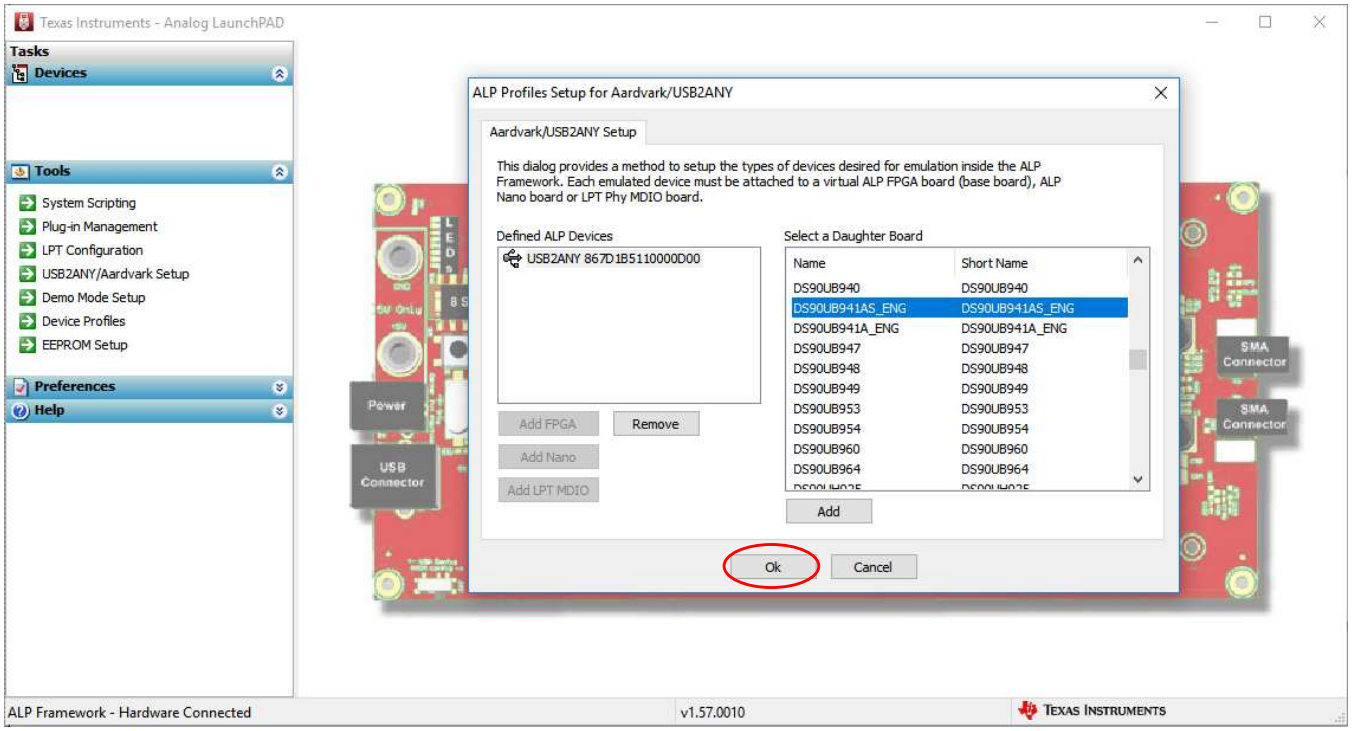


Figure 16. Finish Setup

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12.2 ALP Does Not Detect the EVM

If the window shown in Figure 17 opens after starting the ALP software, double-check the hardware setup.

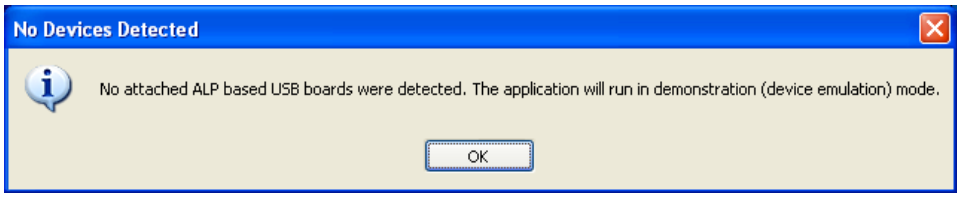


Figure 17. ALP No Devices Error

It may also be that the USB driver is not installed. Check the device manager. There should be a “HID-compliant device” under the “Human Interface Devices” as shown in Figure 18.

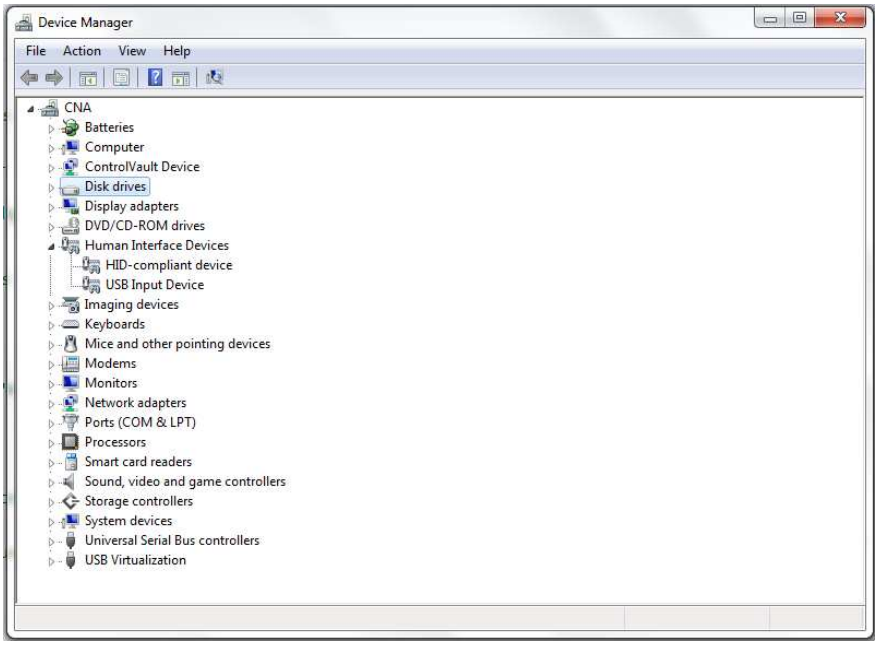


Figure 18. Windows 10, ALP USB Driver

The software should start with only “DS90Ux941AS-Q1” in the “Devices” drop-down menu. If there are more devices then the software is most likely in demo mode. When the ALP is operating in demo mode there is a “(Demo Mode)” indication in the lower left of the application status bar as shown in Figure 19.

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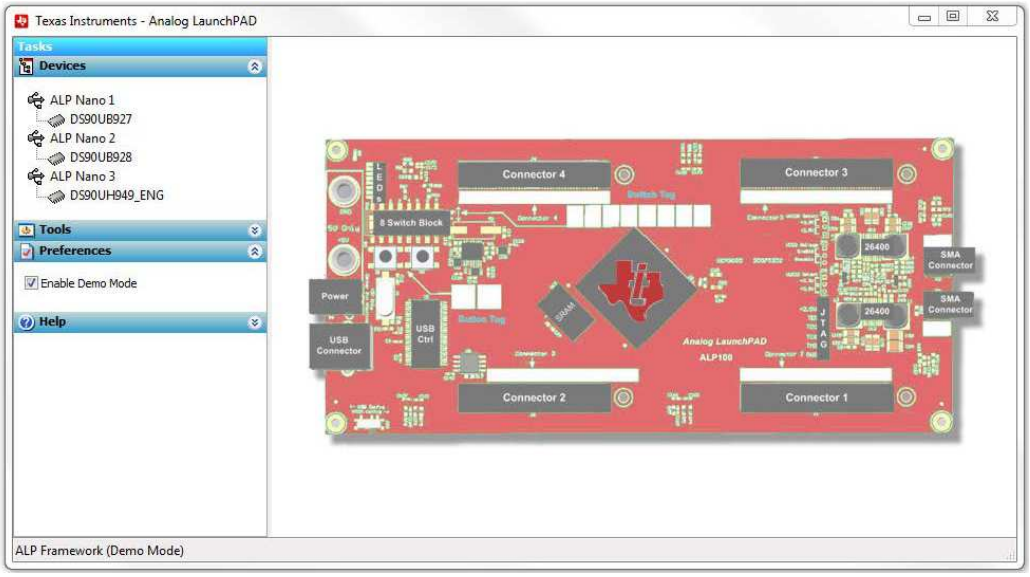


Figure 19. ALP in Demo Mode

Disable the demo mode by selecting the “Preferences” drop-down menu and un-checking “Enable Demo Mode”.

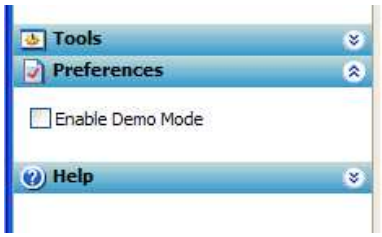


Figure 20. ALP Preferences Menu

After demo mode is disabled, the ALP software will poll the ALP hardware. The ALP software will update and have only “DS90Ux941AS-Q1” under the “Devices” drop-down menu.

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13 Typical Connection and Test Equipment

The following is a list of typical test equipment that may be used to generate signals for the Serializer inputs:

1. Digital Video Source – for generation of specific display timing such as Digital Video Processor or Graphics Controller (GPU) with OpenLDI output.
2. Any other signal generator / video source - This video generator may be used for video signal sources for DVI or DP++
3. Any other signal / video generator that provides the correct input levels as specified in the data sheet.

Figure 21 shows a typical test setup using a Graphics Controller and display.

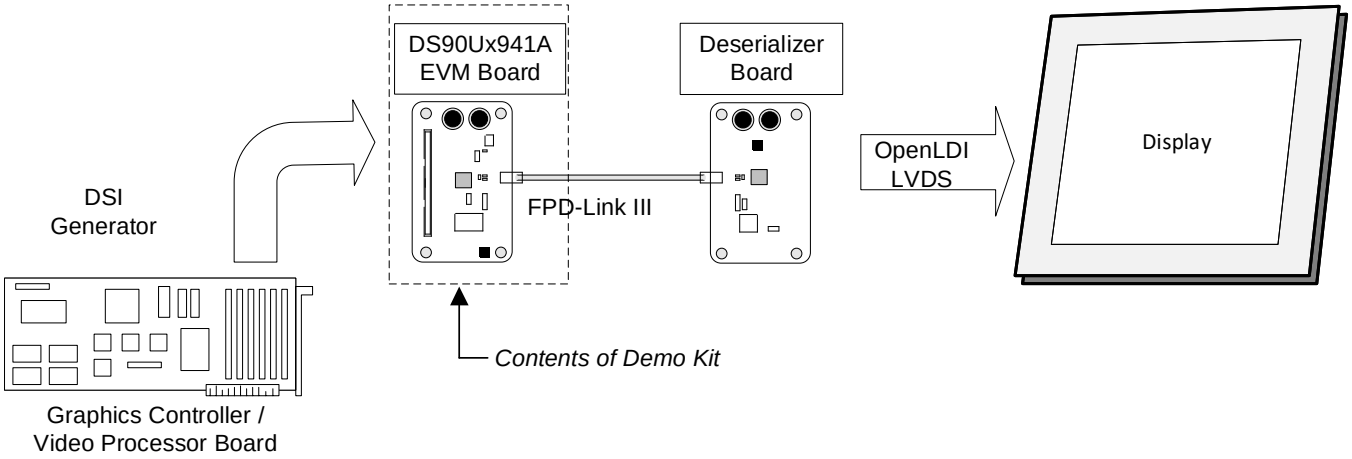


Figure 21. Typical Test Setup for Video Application

Figure 22 shows a typical test setup using a video generator and logic analyzer.

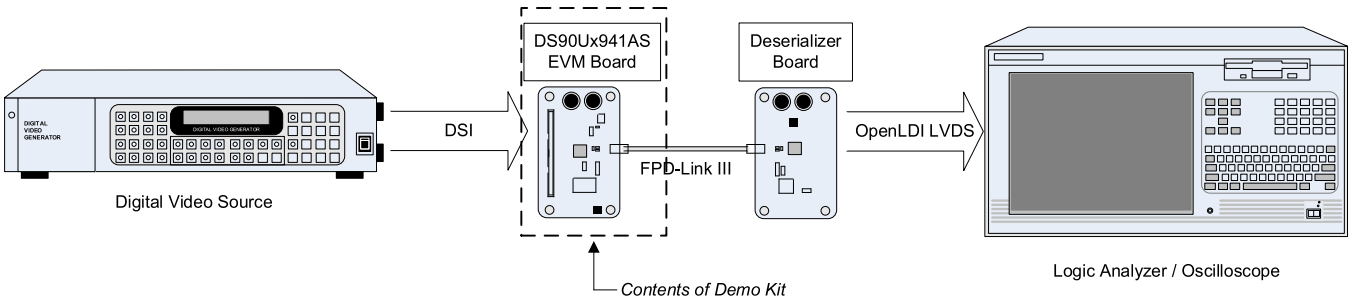


Figure 22. Typical Test Setup for Evaluation

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14 Equipment References

NOTE: The following references are supplied only as a courtesy to our valued customers. It is not intended to be an endorsement of any particular equipment or supplier.

Digital Video Pattern Generator:

Astrodesign

www.astro-americas.com

Logic Analyzer:

Keysight

www.keysight.com

Corelis CAS-1000-I2C/E I2C Bus Analyzer and Exerciser Products:

www.corelis.com/products/I2C-Analyzer.htm

Aardvark I2C/SPI Host Adapter Part Number: TP240141

www.totalphase.com/products/aardvark_i2cspi

15 Cable References

For optimal performance, TI recommends a Shielded Twisted-Pair (STP), 100-Ω differential impedance and 24 AWG (or larger diameter) cable for high-speed data applications.

Leoni Dacar 538 series cable:

www.leoni-automotive-cables.com

Rosenberger HSD connector:

www.rosenberger.de/en/Products/35_Automotive_HSD.php

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Bill of Materials

Table 14. Bill of Materials

ITEM	DESIGNATOR	DESCRIPTION	MANUFACTURER	PART NUMBER	QTY
1	!PCB1	Printed Circuit Board	Any	HSDC031	1
2	C1, C5, C6, C10, C11, C13, C17, C32, C36, C43, C53, C68, C72	CAP, CERM, 10 uF, 10 V, +/- 10%, X7R, 0805	MuRata	GRM21BR71A106KE51L	13
3	C2, C7, C12, C14, C15, C16, C18, C19, C22, C23, C24, C27, C28, C29, C35, C37, C38, C41, C42, C52, C55, C58, C61, C64, C67, C70, C71	CAP, CERM, 0.1 uF, 16 V, +/- 10%, X7R, 0402	MuRata	GRM155R71C104KA88D	27
4	C3, C9, C62	CAP, CERM, 0.01 uF, 100 V, +/- 5%, X7R, 0603	AVX	06031C103JAT2A	3
5	C4, C8	CAP, TA, 1 uF, 16 V, +/- 10%, 9.3 ohm, SMD	Vishay-Sprague	293D105X9016A2TE3	2
6	C20, C21	CAP, CERM, 4.7 pF, 25 V, +/- 5%, C0G/NP0, 0402	MuRata	GRM1555C1E4R7CA01D	2
7	C25, C26	CAP, CERM, 220 pF, 50 V, +/- 1%, C0G/NP0, 0603	AVX	06035A221FAT2A	2
8	C30, C31	CAP, CERM, 30 pF, 100 V, +/- 5%, C0G/NP0, 0603	MuRata	GRM1885C2A300JA01D	2
9	C33	CAP, CERM, 2200 pF, 50 V, +/- 10%, X7R, 0603	Kemet	C0603X222K5RACTU	1
10	C34	CAP, CERM, 0.47 uF, 16 V, +/- 10%, X7R, 0603	MuRata	GRM188R71C474KA88D	1
11	C39	CAP, CERM, 1.8 pF, 50 V, +/- 5%, C0G/NP0, 0402	MuRata	GRM1555C1H1R8CA01D	1
12	C40, C51, C66	CAP, CERM, 10 pF, 50 V, +/- 5%, C0G/NP0, 0402	MuRata	GRM1555C1H100JA01D	3
13	C44	CAP, CERM, 47 uF, 16 V, +/- 20%, X5R, 1210	MuRata	GRM32ER61C476ME15L	1
14	C45	CAP, TA, 100 uF, 16 V, +/- 20%, 0.1 ohm, SMD	Kemet	T495D107M016ATE100	1
15	C46	CAP, CERM, 1 uF, 16 V, +/- 10%, X7R, 0603	TDK	C1608X7R1C105K080AC	1
16	C47	CAP, CERM, 3300 pF, 50 V, +/- 10%, X7R, 0402	MuRata	GRM155R71H332KA01D	1
17	C48, C50	CAP, CERM, 1 uF, 16 V, +/- 10%, X5R, 0603	MuRata	GRM185R61C105KE44D	2
18	C49, C56	CAP, TA, 22 uF, 25 V, +/- 20%, 0.7 ohm, SMD	Vishay-Sprague	293D226X0025D2TE3	2
19	C54, C60, C63, C69	CAP, CERM, 4.7 µF, 25 V,+/- 10%, X7R, AEC-Q200 Grade 1, 0805	TDK	CGA4J1X7R1E475K125AC	4
20	C57	CAP, TA, 2.2 uF, 25 V, +/- 10%, 6.3 ohm, SMD	Vishay-Sprague	293D225X9025A2TE3	1
21	C59, C65	CAP, CERM, 20 pF, 50 V, +/- 5%, C0G/NP0, 0402	MuRata	GRM1555C1H200JA01D	2
22	C75, C83, C90, C97, C104, C112	CAP, CERM, 10 uF, 10 V, +/- 10%, X5R, 0805	Kemet	C0805C106K8PACTU	6
23	C76, C84, C91, C93, C98, C105, C106, C107, C108, C109, C110, C111, C113	CAP, CERM, 1 uF, 16 V, +/- 10%, X5R, 0603	Kemet	C0603C105K4PACTU	13
24	C77, C78, C79, C80, C85, C86, C87, C92, C94, C99, C100, C101, C114	CAP, CERM, 0.1 uF, 25 V, +/- 10%, X7R, 0603	AVX	06033C104KAT2A	13
25	C115, C116, C117, C118	CAP, CERM, 0.1 uF, 50 V, +/- 10%, X7R, 0402	TDK	C1005X7R1H104K050BB	4
26	C119, C120	CAP, CERM, 0.012 uF, 16 V, +/- 10%, X7R, 0402	MuRata	GRM155R71C123KA01D	2
27	D1	LED, Green, SMD	Lite-On	LTST-C190GKT	1
28	D2	Diode, Schottky, 40 V, 1 A, SOD-123	Diodes Inc.	1N5819HW-7-F	1
29	D3, D4	LED, Orange, SMD	Lite-On	LTST-C190KFKT	2

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Table 14. Bill of Materials (continued)

ITEM	DESIGNATOR	DESCRIPTION	MANUFACTURER	PART NUMBER	QTY
30	F1	Fuse, 7 A, 24VAC/VDC, SMD	Littelfuse	0429007.WRML	1
31	GND1, TP4, VDD1	Terminal, Turret, TH, Double	Keystone	1502-2	3
32	H1, H4, H6, H8	Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead	B and F Fastener Supply	NY PMS 440 0025 PH	4
33	H2, H3, H5, H7	Standoff, Hex, 0.5"L #4-40 Nylon	Keystone	1902C	4
34	J1	Audio Jack, 3.5mm, Stereo, R/A, SMT	CUI Inc.	SJ-3523-SMT	1
35	J2, J4, J5, J6, J7, J9, J10, J15, J16, J17, J18, J19, J21, J24, J25, J26, J27, J30, J31, J32	Header, 100mil, 2x1, Gold, TH	TE Connectivity	5-146261-1	20
36	J3, J22, J23, J29	Header, 100mil, 3x1, Gold, TH	Samtec	TSW-103-07-G-S	4
37	J8	Receptacle, Differential, 0.5mm, 10 pair x2, Gold, SMT	Samtec	QSH-020-01-H-D-DP-A	1
38	J11	Header (friction lock), 100mil, 4x1, Gold, TH	Molex	0022112042	1
39	J12	Header, 100mil, 16x2, Gold, TH	Samtec	TSW-116-07-G-D	1
40	J13	Header, 100mil, 4x1, Gold, TH	Samtec	TSW-104-07-G-S	1
41	J14	Connector, Receptacle, Mini-USB Type B, R/A, Top Mount SMT	TE Connectivity	1734035-2	1
42	J28	Connector, DC Jack 2.1X5.5 mm, TH	CUI Inc.	PJ-102A	1
43	L1, L2, L5	Ferrite Bead, 330 ohm @ 100 MHz, 1.5 A, 0603	MuRata	BLM18SG331TN1D	3
44	L6	Inductor, Shielded Drum Core, Ferrite, 4.7 uH, 4.2 A, 0.02 ohm, SMD	Wurth Elektronik	7440650047	1
45	L7	Ferrite Bead, 1000 ohm @ 100 MHz, 0.3 A, 0805	Taiyo Yuden	BK2125HS102-T	1
46	L8, L9, L10	Ferrite Bead, 120 ohm @ 100 MHz, 3 A, 0603	MuRata	BLM18SG121TN1D	3
47	LBL 1	Thermal Transfer Printable Labels, 1.250" W x 0.250" H - 10,000 per roll	Brady	THT-13-457-10	1
48	P1	HSD Right Angle Plug, 4-Leads, 2mm Pitch, TH	Rosenberger	D4S20F-40MA5-Z	1
49	Q1, Q2, Q3	MOSFET, N-CH, 50 V, 0.22 A, SOT-23	Fairchild Semiconductor	BSS138	3
50	R1, R2	RES, 100, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	Vishay-Dale	CRCW0402100RFKED	2
51	R3, R7, R8, R10, R67, R70, R71, R72, R73, R74, R75, R76, R77, R78, R79, R105, R112, R114, R115, R121, R122, R123, R124, R125, R126, R127, R129, R130, R131, R132, R133, R134, R135, R136, R137, R138, R139, R140	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0402	Panasonic	ERJ-2GE0R00X	38
52	R4, R5, R6, R9, R18, R27, R29, R38, R54, R56, R66, R85, R86, R95, R98, R101	RES, 10.0 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	Vishay-Dale	CRCW040210K0FKED	16
53	R12, R21, R35, R44, R48, R62	RES, 64.9 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	Vishay-Dale	CRCW040264K9FKED	6
54	R13, R22, R34, R43, R49, R61	RES, 40.2 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	Vishay-Dale	CRCW040240K2FKED	6
55	R14, R23, R33, R42, R50, R60	RES, 41.2 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	Vishay-Dale	CRCW040241K2FKED	6
56	R15, R24, R32, R41, R51, R59	RES, 30.9 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	Vishay-Dale	CRCW040230K9FKED	6
57	R16, R25, R31, R40, R52	RES, 16.2 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	Vishay-Dale	CRCW040216K2FKED	5
58	R17, R26, R30, R39, R53, R57	RES, 10.7 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	Vishay-Dale	CRCW040210K7FKED	6
59	R65	RES, 1.00 k, 1%, 0.1 W, 0402	Panasonic	ERJ-2RKF1001X	1
60	R68, R69, R116, R117, R118, R128	RES, 4.7 k, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	Vishay-Dale	CRCW04024K70JNED	6
61	R80, R81	RES, 33, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	Vishay-Dale	CRCW040233R0JNED	2
62	R82, R87, R88	RES, 1.5 k, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	Vishay-Dale	CRCW04021K50JNED	3

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Table 14. Bill of Materials (continued)

ITEM	DESIGNATOR	DESCRIPTION	MANUFACTURER	PART NUMBER	QTY
63	R83, R90	RES, 33 k, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	Vishay-Dale	CRCW040233K0JNED	2
64	R84	RES, 1.2 M, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW06031M20JNEA	1
65	R89	RES, 200, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	Vishay-Dale	CRCW0402200RJNED	1
66	R91	RES, 22.1 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	Vishay-Dale	CRCW040222K1FKED	1
67	R92	RES, 121 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	Vishay-Dale	CRCW0402121KFKED	1
68	R93, R102, R110, R111	RES, 100 k, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	Vishay-Dale	CRCW0402100KJNED	4
69	R94, R96, R103, R109, R113	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW06030000Z0EA	5
70	R97	RES, 29.4 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	Vishay-Dale	CRCW040229K4FKED	1
71	R99, R100	RES, 3.24 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	Vishay-Dale	CRCW04023K24FKED	2
72	R104	RES, 1.87 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	Vishay-Dale	CRCW04021K87FKED	1
73	R106	RES, 4.99 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	Vishay-Dale	CRCW04024K99FKED	1
74	R107	RES, 23.2 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	Vishay-Dale	CRCW040223K2FKED	1
75	R108	RES, 12.1 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	Vishay-Dale	CRCW040212K1FKED	1
76	R119, R120	RES, 470, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	Vishay-Dale	CRCW0402470RJNED	2
77	S1	Switch, Slide, SPST 3 poles, SMT	CTS Electrocomponents	219-3LPST	1
78	S2, S3, S6	Switch, Slide, SPST 8 poles, SMT	CTS Electrocomponents	219-8MST	3
79	S4, S7, S8	SWITCH TACTILE SPST-NO 0.02A 15V, TH	Panasonic	EVQ-PAD04M	3
80	S5	Switch, 2 SPST, 0.15 A, 30 V, TH	Grayhill	78B02ST	1
81	SH-J1, SH-J2, SH-J3, SH-J4, SH-J5	Shunt, 2mm, Gold plated, Black	Samtec	2SN-BK-G	5
82	U1	99dB SNR Stereo ADC with Single-Ended Inputs, PW0014A (TSSOP-14)	Texas Instruments	PCM1808PWR	1
83	U2	ESD-Protection Array for High-Speed Data Interfaces, 4 Channels, -40 to +85 degC, 6-pin SON (DRY), Green (RoHS and no Sb/Br)	Texas Instruments	TPD4E004DRYRG4	1
84	U3	6-Bit Bidirectional Voltage-Level Translator with Auto Direction Sensing and +/-15-kV ESD Protect, PW0016A (TSSOP-16)	Texas Instruments	TXB0106PWR	1
85	U4	TCA9406 Dual Bidirectional 1-MHz I2C-BUS and SMBus Voltage Level-Translator, 1.65 to 3.6 V, -40 to 85 degC, 8-pin US8 (DCU), Green (RoHS and no Sb/Br)	Texas Instruments	TCA9406DCUR	1
86	U5	25 MHz Mixed Signal Microcontroller with 128 KB Flash, 8192 B SRAM and 63 GPIOs, -40 to 85 degC, 80-pin QFP (PN), Green (RoHS and no Sb/Br)	Texas Instruments	MSP430F5529IPN	1
87	U6	4.5V to 18V Input, 2A Synchronous Step-Down Converter, PWP0014E (TSSOP-14)	Texas Instruments	TPS54225PWPR	1
88	U7	1A Low Dropout Adjustable Regulator, NGN0008A (WSON-8)	Texas Instruments	LM2941LD/NOPB	1
89	U8	Single Output LDO, 500 mA, Adjustable 0.8 to 3.6 V Output, 0.8 to 5.5 V Input, with Programmable Soft Start, 10-pin SON (DRC), -40 to 125 degC, Green (RoHS and no Sb/Br)	Texas Instruments	TPS74701DRCR	1
90	U9	Dual Output LDO, 1 A, Fixed 1.8, 3.3 V Output, 2.7 to 10 V Input, 28-pin HTSSOP (PWP), -40 to 125 degC, Green (RoHS and no Sb/Br)	Texas Instruments	TPS767D318PWP	1

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Table 14. Bill of Materials (continued)

ITEM	DESIGNATOR	DESCRIPTION	MANUFACTURER	PART NUMBER	QTY
91	U10	Ultra-Low Jitter Programmable Oscillator with Internal EEPROM, SIA0008B (QFM-8)	Texas Instruments	LMK61E0M-SIAR	1
92	U11	DSI to FPD-Link III Bridge Serializer with HDCP, RTD0064F (VQFNP-64)	Texas Instruments	DS90UH941ASRTDRQ1 or DS90UB941ASRTDRQ1	1
93	Y1	OSC, 12.288 MHz, 3.3 Vdc, SMD	ECS Inc.	ECS-8FA3X-122.8-TR	1
94	Y2	Crystal, 24.000 MHz, 20pF, SMD	ECS Inc.	ECS-240-20-5PX-TR	1

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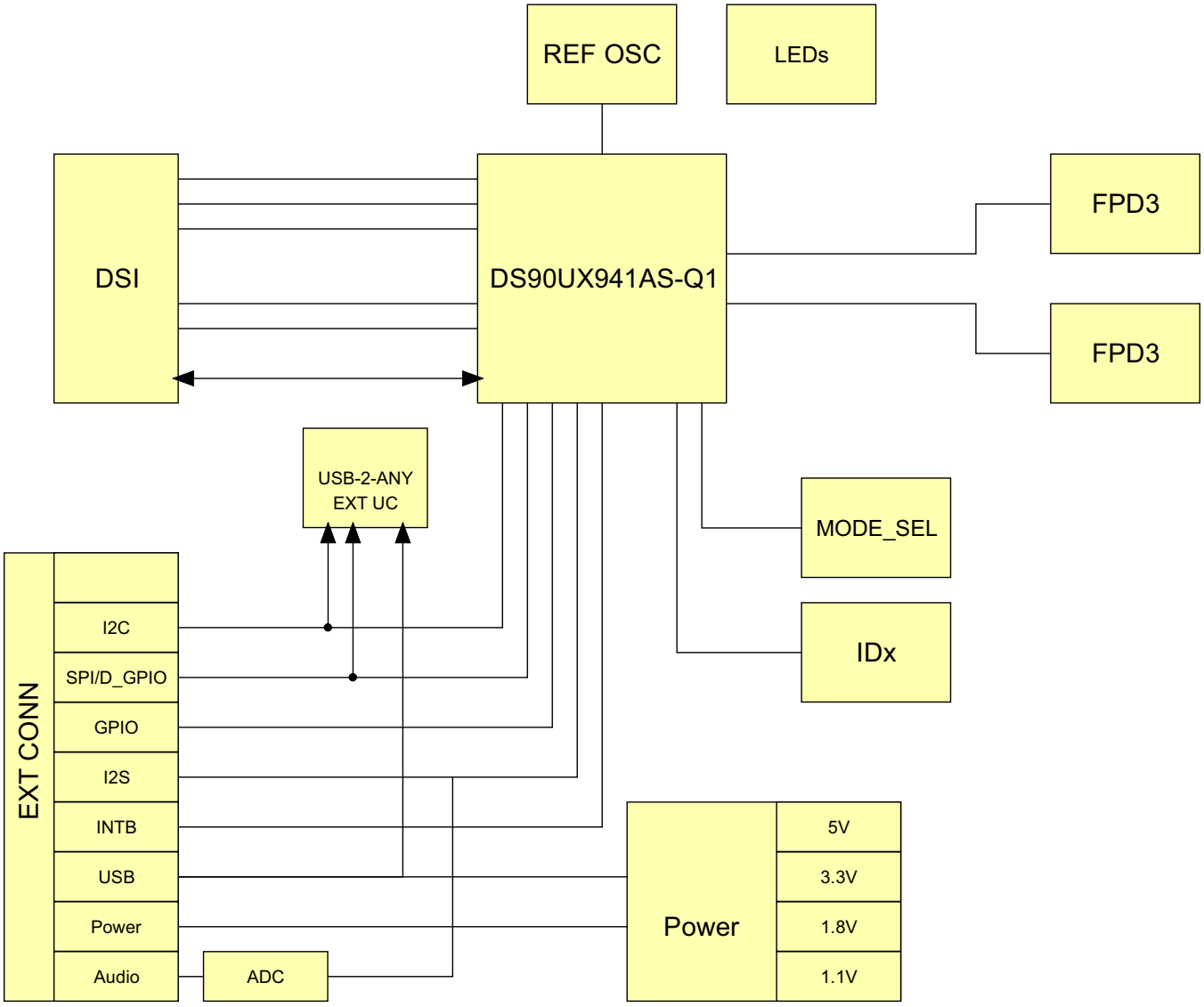


Figure 23. Top Level Schematic

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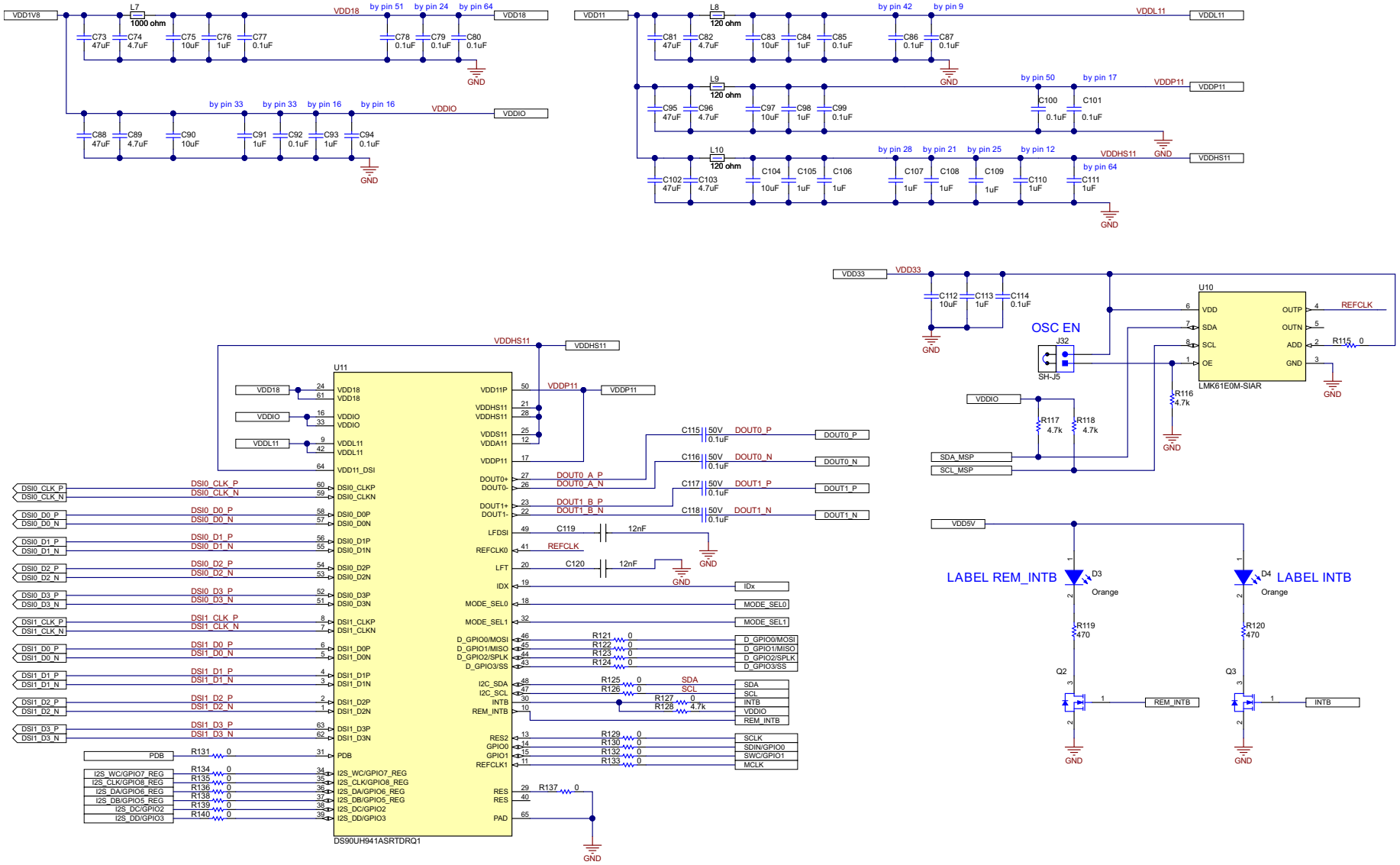


Figure 24. Main Schematic

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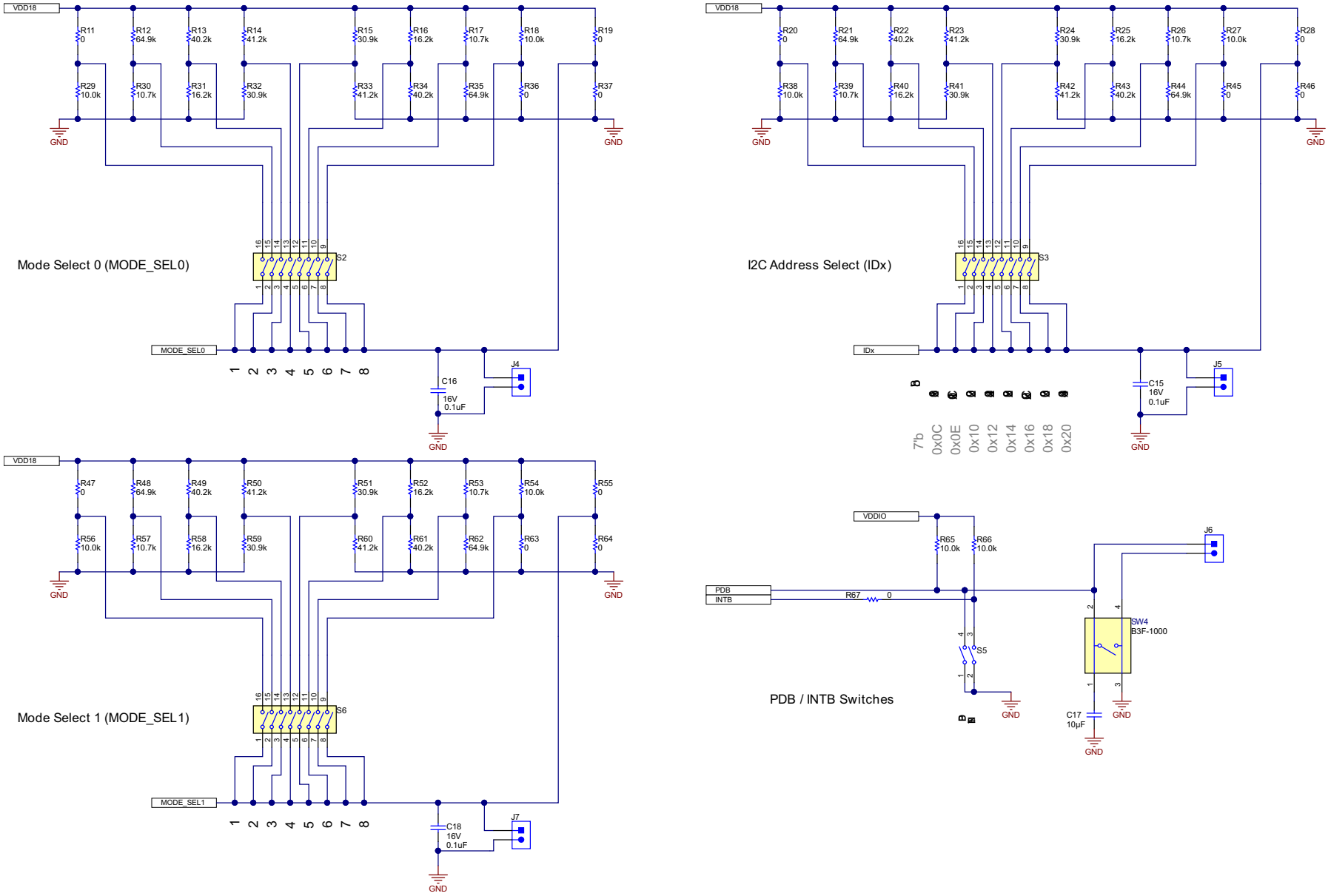


Figure 25. Configuration Schematic

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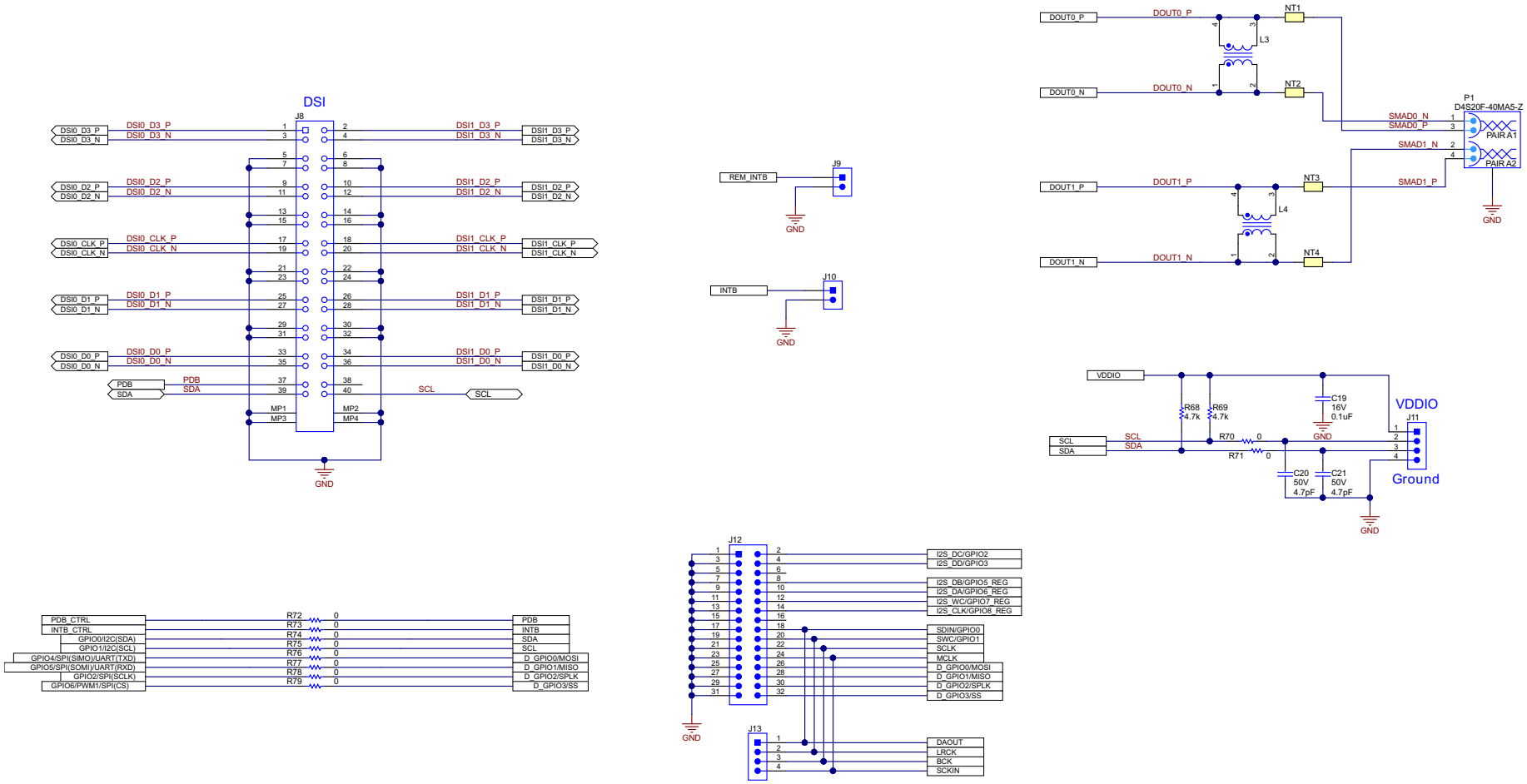


Figure 26. Schematic Connectors

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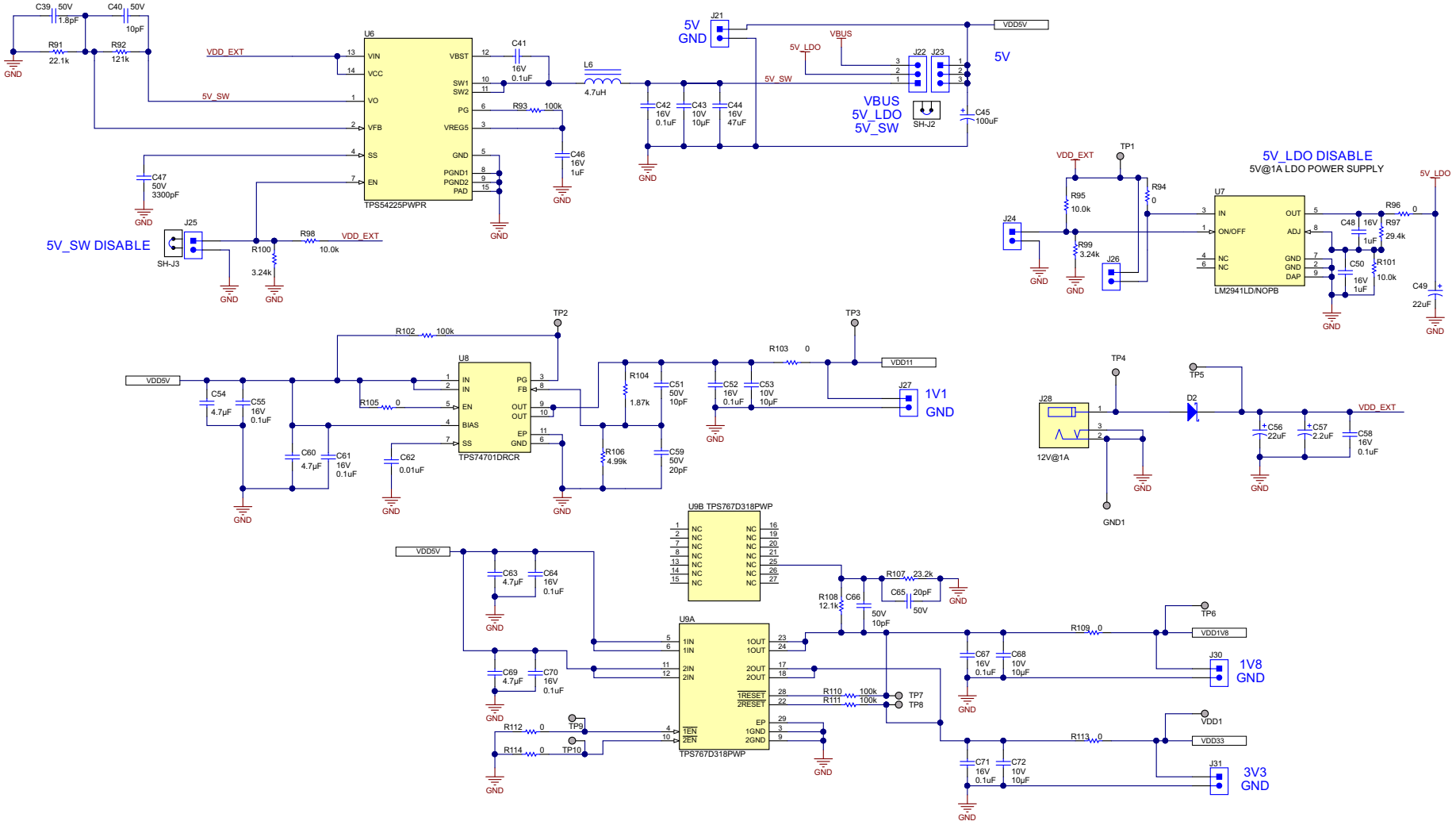


Figure 27. Power Schematic

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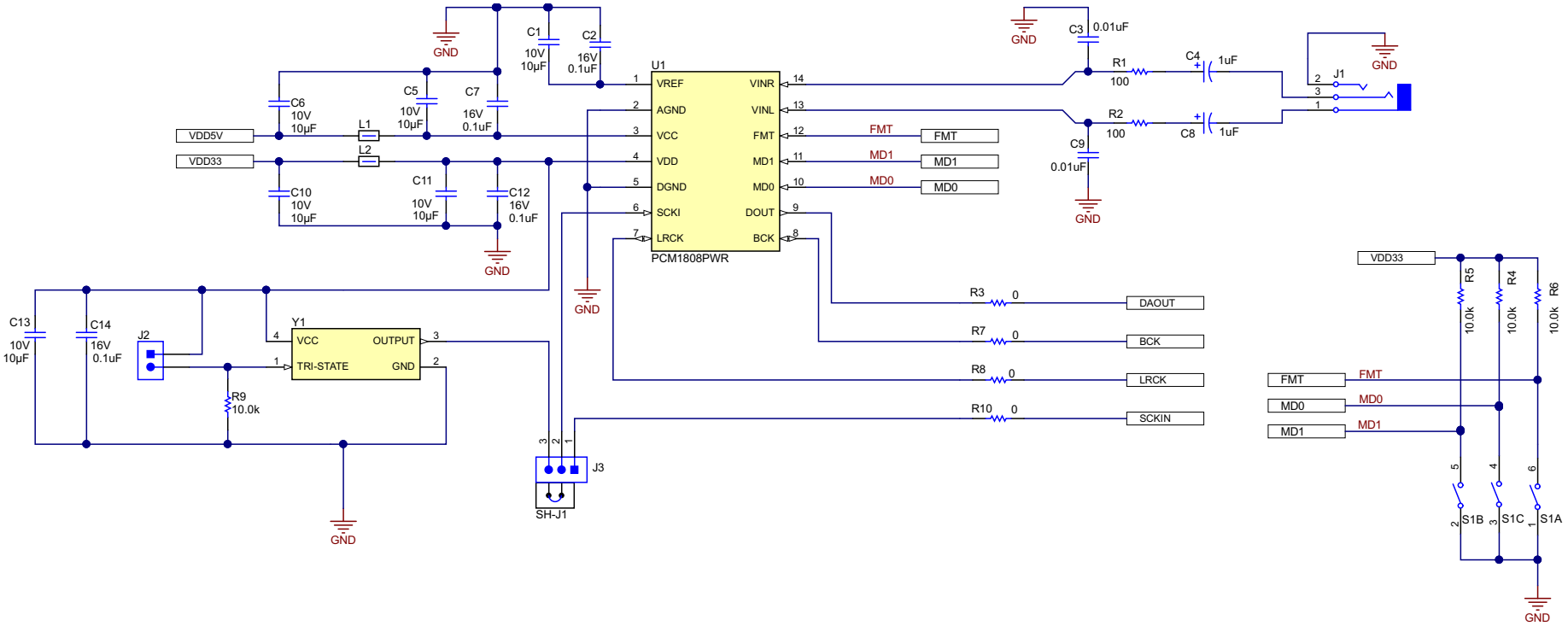


Figure 28. Audio Schematic

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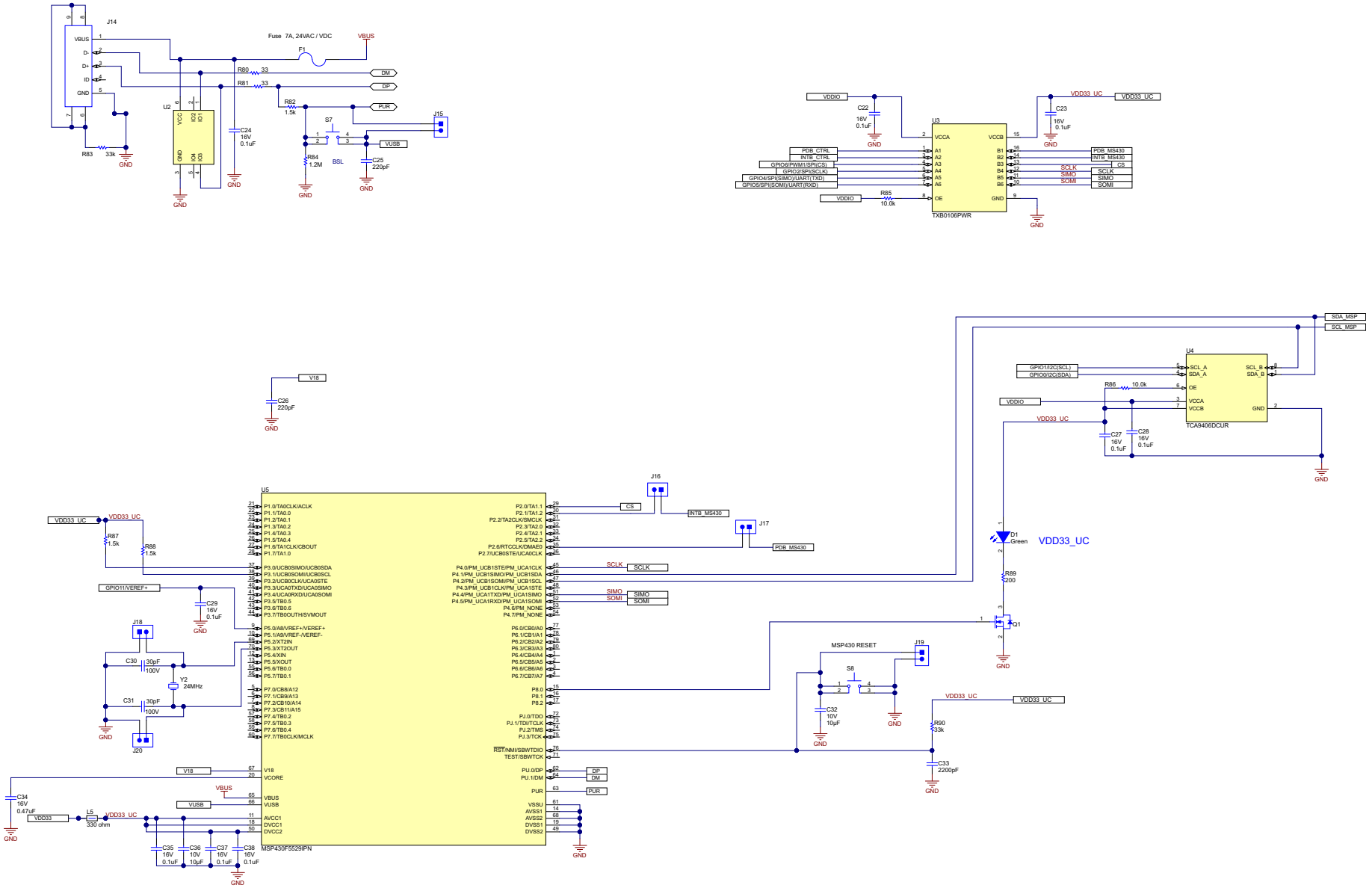


Figure 29. USB2Any Schematic

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Board Layout

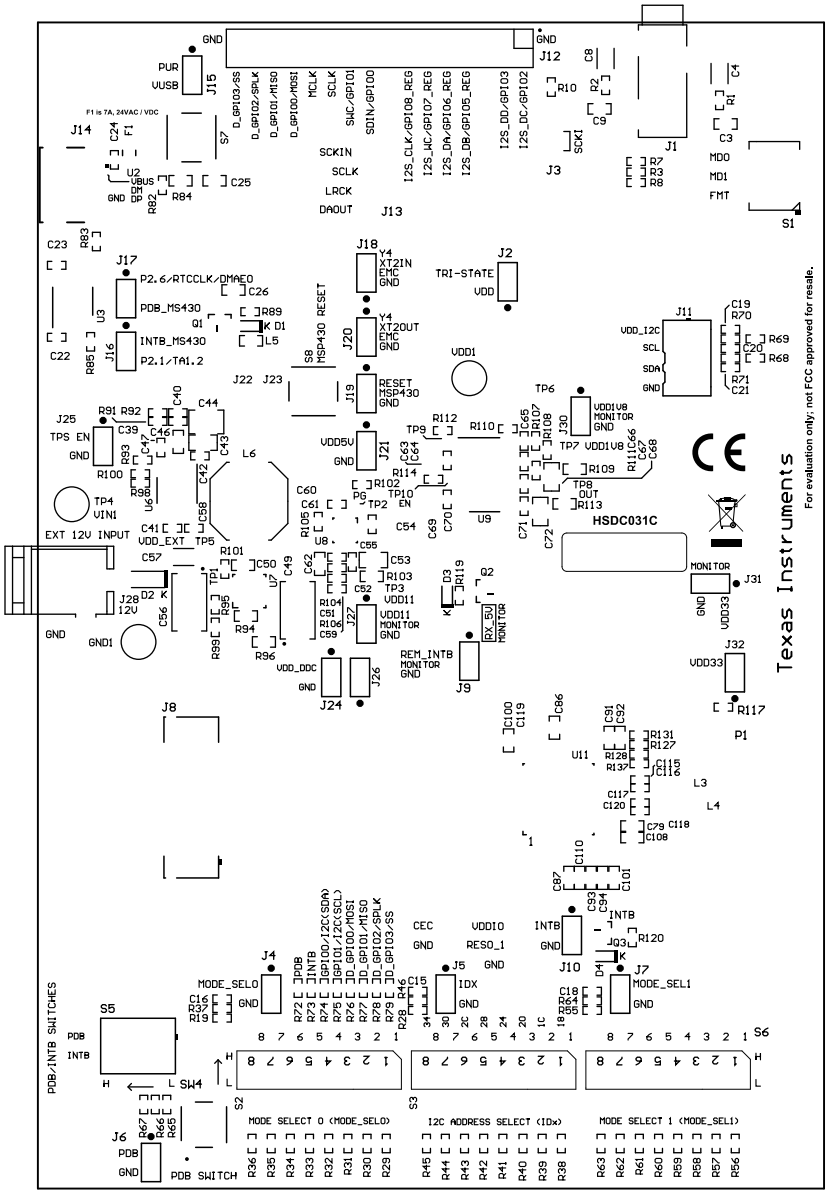


Figure 30. Top Overlay

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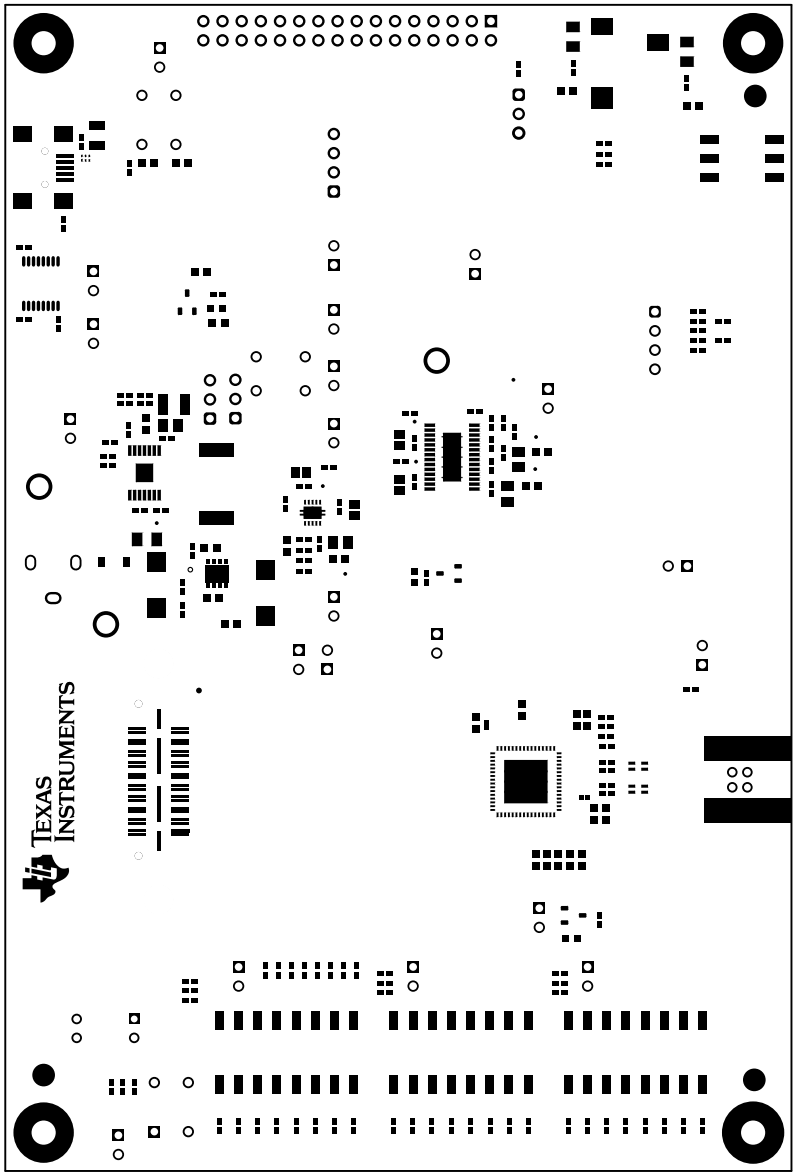


Figure 31. Top Solder

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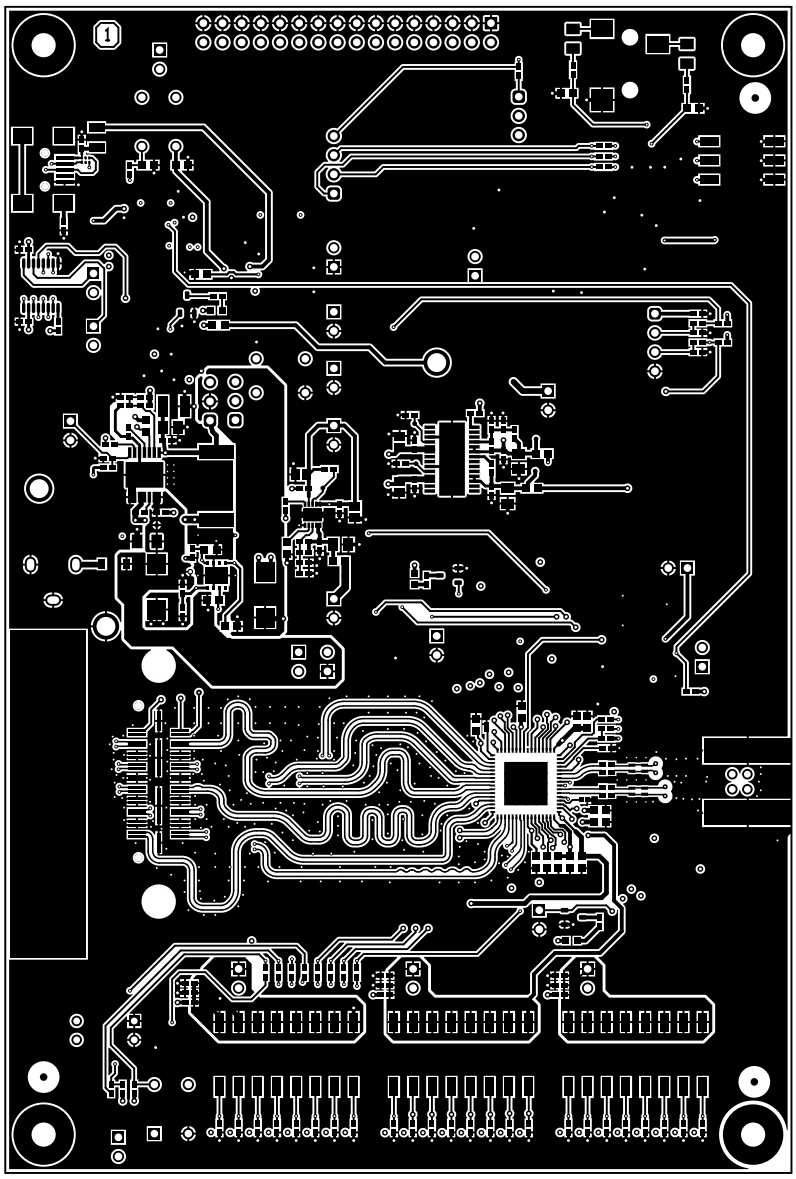


Figure 32. Layer1 Top

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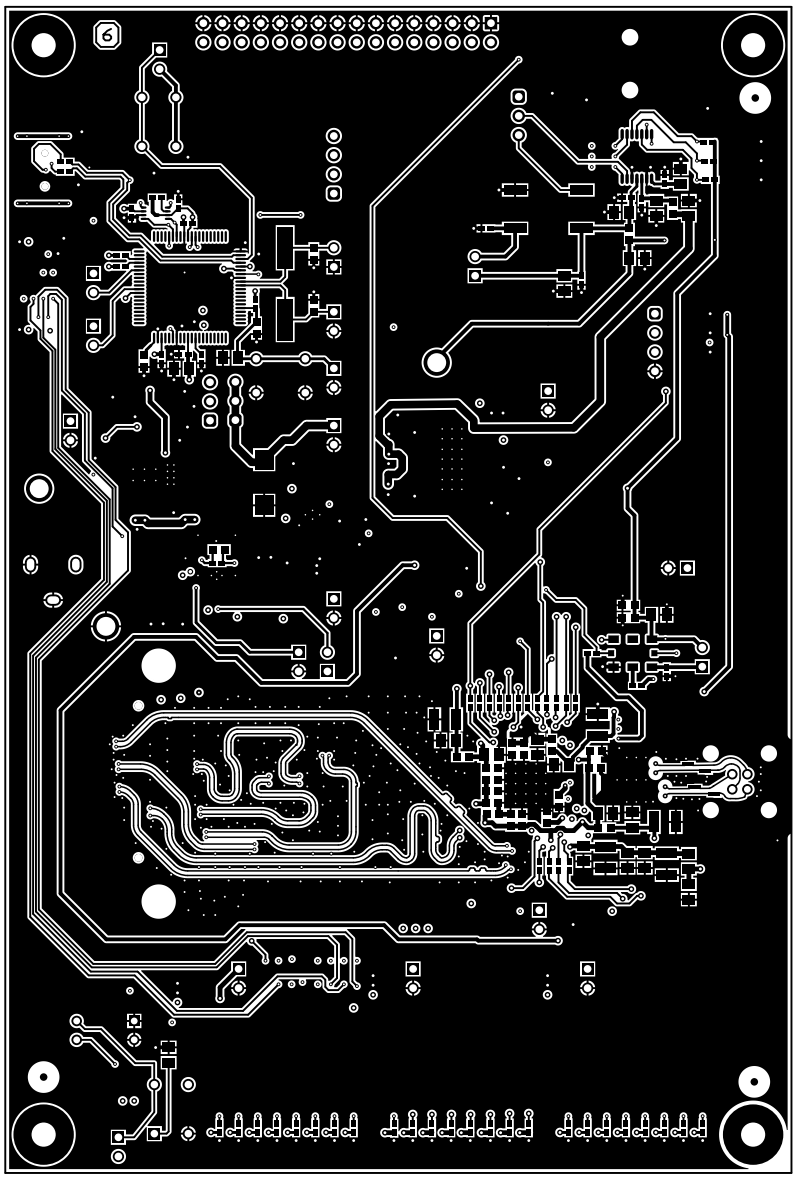


Figure 33. Layer 6 Bottom

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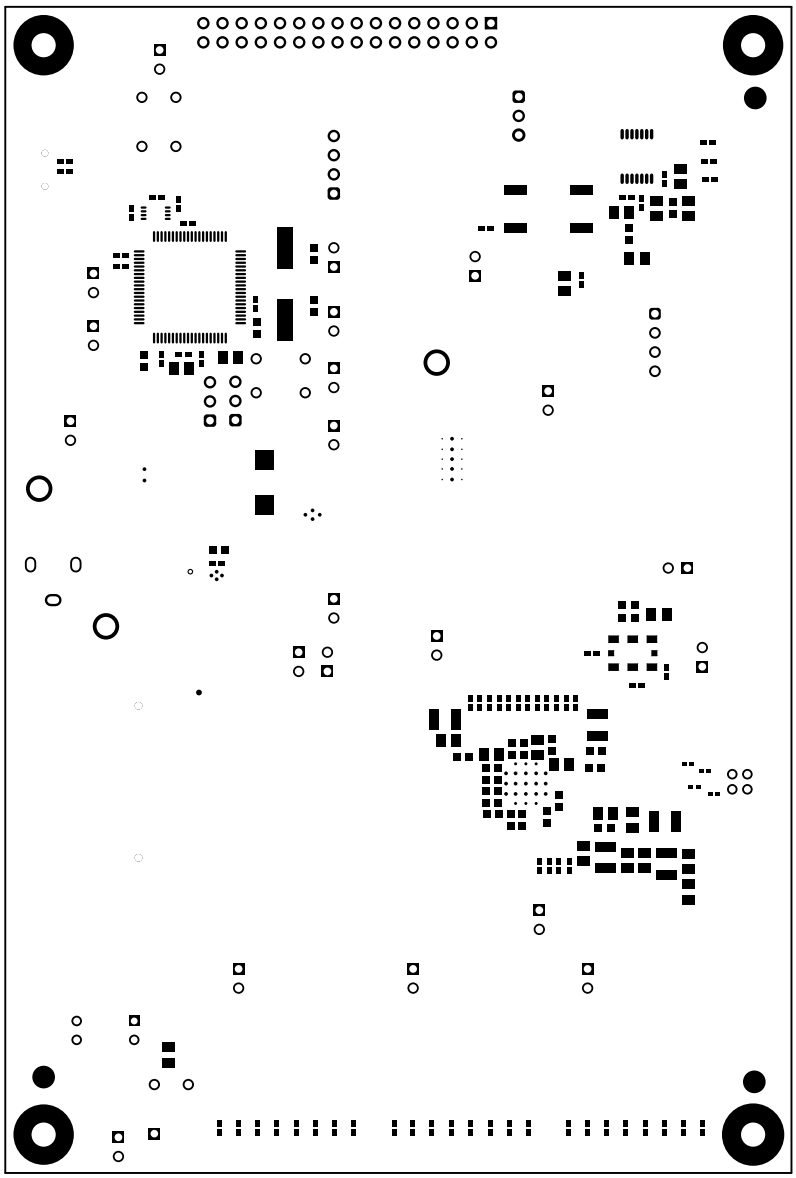


Figure 34. Layer6 Solder Bottom

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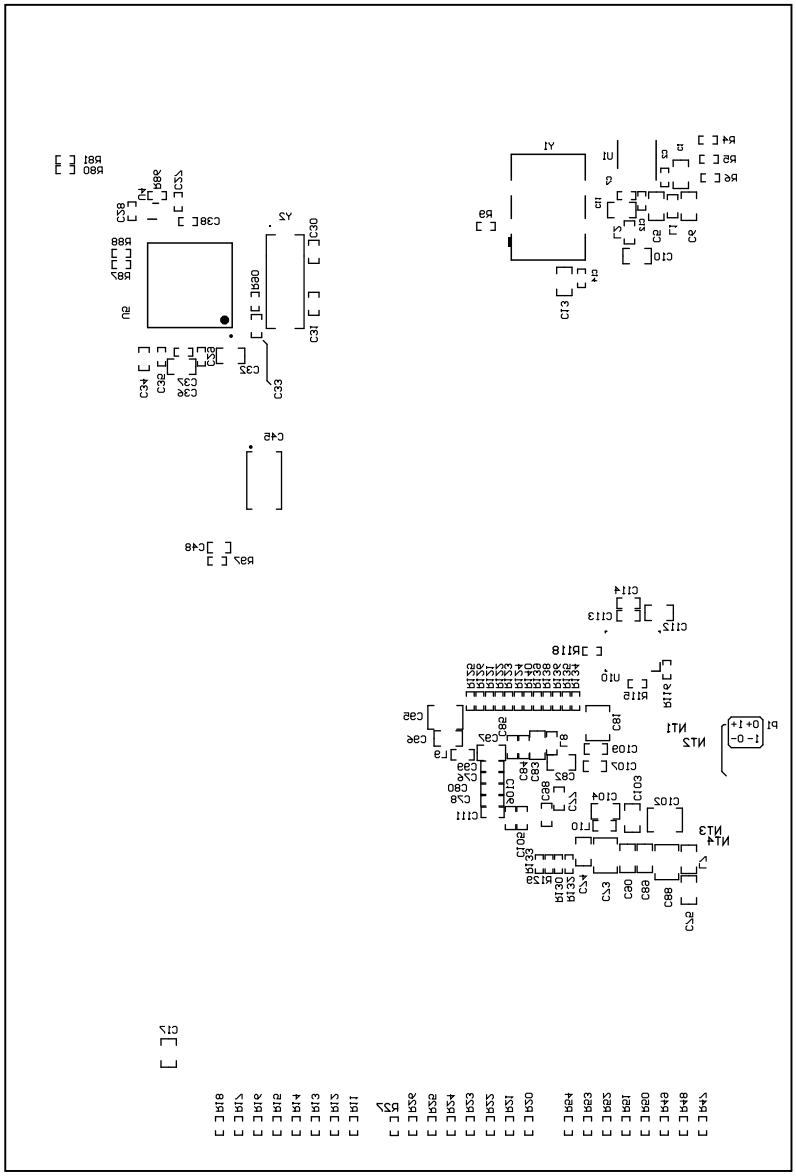
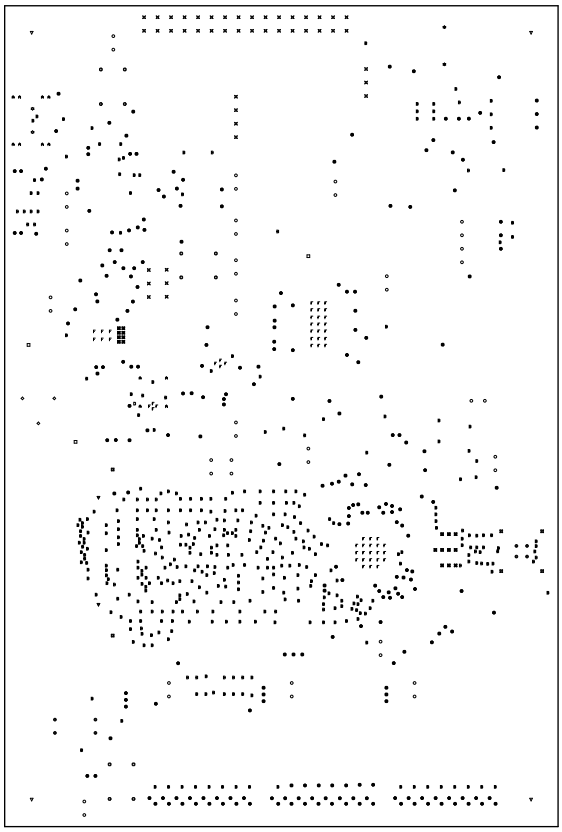


Figure 35. Layer6 Bottom Overlay

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DRILL TABLE:

Symbol	Quantity	Finished Hole Size	Plated	Hole Type	Drill Layer Pair	Hole Tolerance	Hole Length	Routed Path Length
	2	35.43mil (0.900mm)	NPTH	Round	Layer1 Top - Layer6 Bottom		-	-
	2	40.16mil (1.020mm)	NPTH	Round	Layer1 Top - Layer6 Bottom		-	-
	4	64.96mil (1.650mm)	NPTH	Round	Layer1 Top - Layer6 Bottom		-	-
	2	66.93mil (1.700mm)	NPTH	Round	Layer1 Top - Layer6 Bottom		-	-
	2	153,00mil (4,039mm)	NPTH	Round	Layer1 Top - Layer6 Bottom		-	-
F	56	7.87mil (0.200mm)	PTH	Round	Layer1 Top - Layer6 Bottom		-	-
	18	8.00mil (0.203mm)	PTH	Round	Layer1 Top - Layer6 Bottom		-	-
A	12	8.10mil (0.206mm)	PTH	Round	Layer1 Top - Layer6 Bottom		-	-
B	424	10.00mil (0.254mm)	PTH	Round	Layer1 Top - Layer6 Bottom		-	-
	259	15.00mil (0.381mm)	PTH	Round	Layer1 Top - Layer6 Bottom		-	-
D	1	17.72mil (0.450mm)	PTH	Round	Layer1 Top - Layer6 Bottom		-	-
	8	35.43mil (0.900mm)	PTH	Round	Layer1 Top - Layer6 Bottom		-	-
	12	39.37mil (1.000mm)	PTH	Round	Layer1 Top - Layer6 Bottom		-	-
	45	40.00mil (1.016mm)	PTH	Round	Layer1 Top - Layer6 Bottom		-	-
	46	40.16mil (1.020mm)	PTH	Round	Layer1 Top - Layer6 Bottom		-	-
	3	98.43mil (2.500mm)	PTH	Round	Layer1 Top - Layer6 Bottom		-	-
	4	125.98mil (3.200mm)	PTH	Round	Layer1 Top - Layer6 Bottom		-	-
	3	39.37mil (1.000mm)	PTH	Slot	Layer1 Top - Layer6 Bottom		62.99mil (1.600mm)	23.62mil (0.600mm)
	903 Total							

Slot definitions : Routed Path Length = Calculated from tool start centre position to tool end centre position.
Hole Length = Routed Path Length + Tool Size = Slot length as defined in the PCB layout

Figure 36. Drill Drawing

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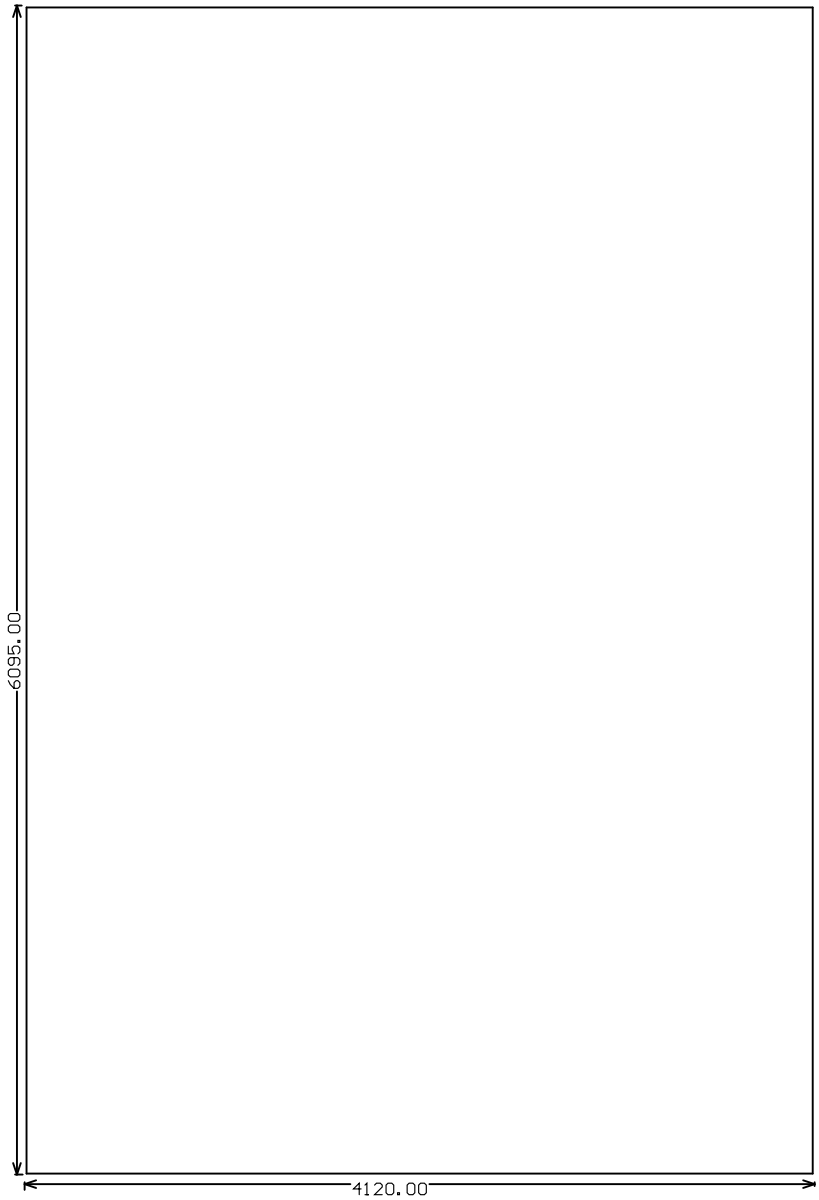


Figure 37. Board Dimensions

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Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (December 2018) to A Revision	Page
• Changed Typical Connection and Test Equipment Images	23
• Changed Bill of Materials	25
• Changed schematics, layouts and board shots	29

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FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

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Concerning EVMs Including Radio Transmitters:

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(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

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http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page

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If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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