DS90CP04 1.5 Gbps 4x4 LVDS Crosspoint Switch

Check for Samples: DS90CP04

FEATURES

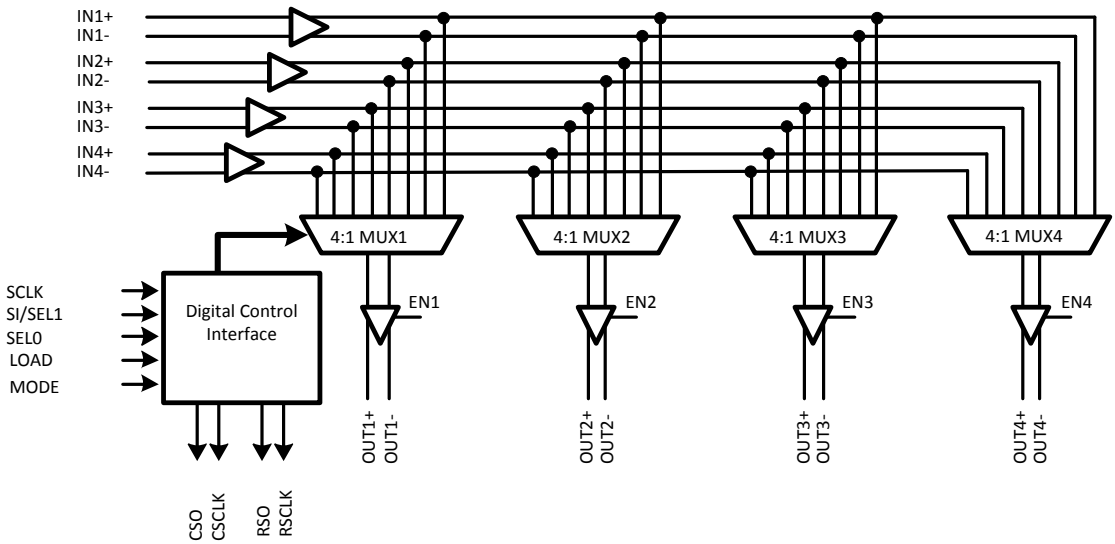
- **DC - 1.5 Gbps Low Jitter, Low Skew Operation**
- **Pin and Serial Interface Configurable, Fully Differential, Non-blocking Architecture**
- **Wide Input Common Mode Voltage Range Enables Easy Interface to LVDS/LVPECL/2.5V-CML Drivers**
- **TRI-STATE LVDS Outputs**
- **Serial Control Interface with Read-back Capability**
- **Double Register Loading**
- **Single +2.5V Supply**
- **Small 6x6 mm WQFN-32 Space Saving Package**
- **Fabricated with Advanced CMOS Process Technology**

DESCRIPTION

DS90CP04 is a 4x4 digital cross-point switch with broadside input and output pins for efficient board layout. It utilizes Low Voltage Differential Swing (LVDS) technology for low power, high-speed operation. Data paths are fully differential from input to output for low noise. The non-blocking architecture allows connections of any input to any output or outputs. The switch matrix consists of four differential 4:1 multiplexes. Each output channel connects to one of the four inputs common to all multiplexers.

A simple serial control interface or a configuration select port is activated by the state of the MODE pin. When utilizing the serial control interface a single load command will update the new switch configuration for all outputs simultaneously.

Functional Block Diagrams



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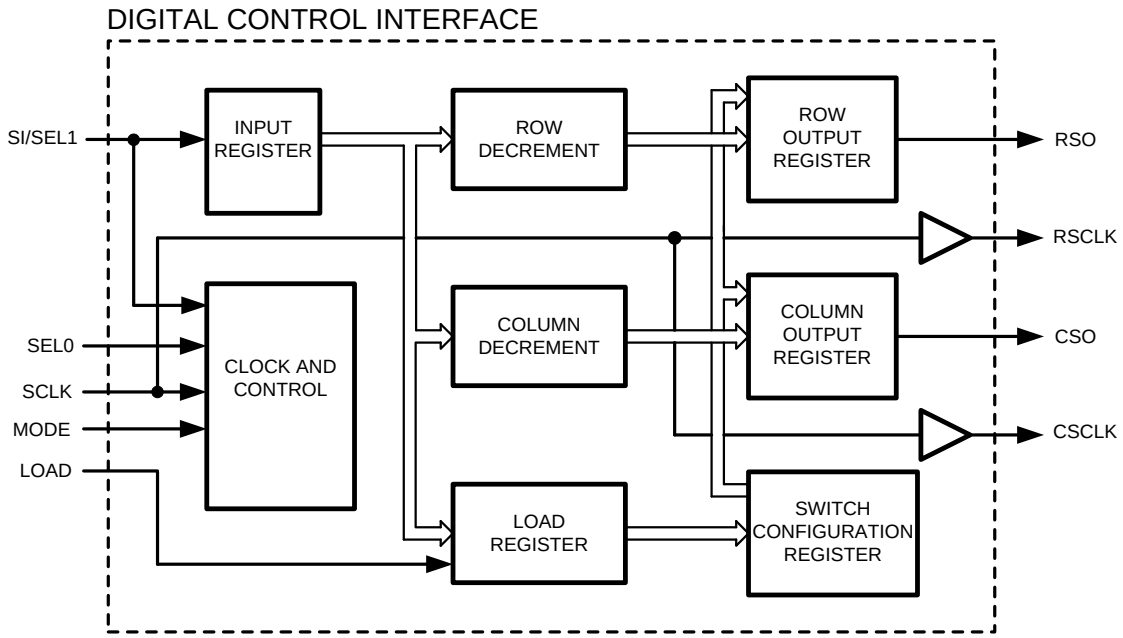


Figure 1. Functional Block Diagram

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Connection Diagram

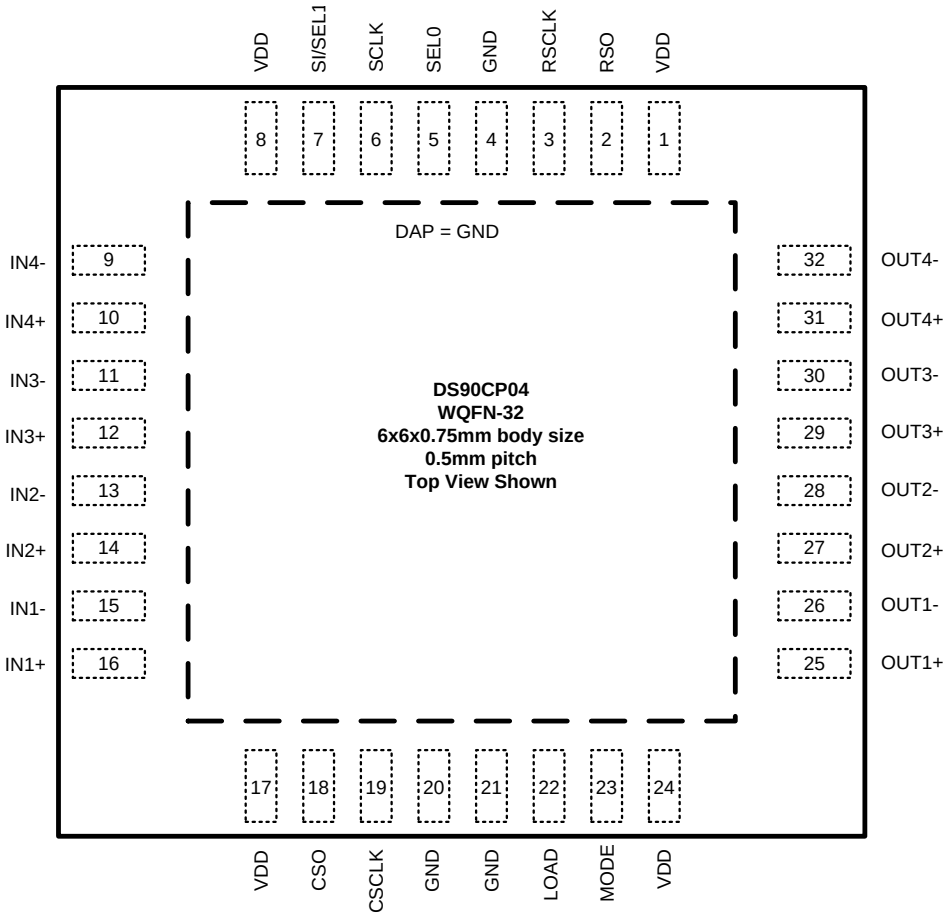


Figure 2. Connection Diagram - 32 Pin (Top View)
See Package Number NJE0032A

PIN DESCRIPTIONS

Pin Name	Pin Number	I/O, Type	Description
DIFFERENTIAL INPUTS COMMON TO ALL MUXES			
IN1+ IN1−	16 15	I, LVDS	Inverting and non-inverting differential inputs.
IN2+ IN2−	14 13	I, LVDS	Inverting and non-inverting differential inputs.
IN3+ IN3−	12 11	I, LVDS	Inverting and non-inverting differential inputs.
IN4+ IN4−	10 9	I, LVDS	Inverting and non-inverting differential inputs.
SWITCHED DIFFERENTIAL OUTPUTS			
OUT1+ OUT1−	25 26	O, LVDS	Inverting and non-inverting differential outputs. OUT1± can be connected to any one pair IN1±, IN2±, IN3±, or IN4±
OUT2+ OUT2−	27 28	O, LVDS	Inverting and non-inverting differential outputs. OUT2± can be connected to any one pair IN1±, IN2±, IN3±, or IN4±
OUT3+ OUT3−	29 30	O, LVDS	Inverting and non-inverting differential outputs. OUT3± can be connected to any one pair IN1±, IN2±, IN3±, or IN4
OUT4+ OUT4−	31 32	O, LVDS	Inverting and non-inverting differential outputs. OUT4± can be connected to any one pair IN1±, IN2±, IN3±, or IN4±

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PIN DESCRIPTIONS (continued)

Pin Name	Pin Number	I/O, Type	Description
DIGITAL CONTROL INTERFACE			
SCLK	6	I, LVCMOS	Control clock to latch in programming data at SI. SCLK can be 0 MHz to 100 MHz. SCLK should be burst of clock pulses active only while accessing the device. After completion of programming, SCLK should be kept at logic low to minimize potential noise injection into the high-speed differential data paths.
SI / SEL1	7	I, LVCMOS	Programming data to select the switch configuration. Data is latched into the input buffer register at the rising edge of SCLK.
SEL0	5	I, LVCMOS	Programming data to select the switch configuration.
CSO RSO	18 2	O, LVCMOS	With MODE low, control data is shifted out at CSO (RSO) for cascading to the next device in the serial chain. The control data at CSO (RSO) is identical to that shifted in at SI with the exception of the device column (row) address being decremented by one internally before propagating to the next device in the chain. CSO (RSO) is clocked out at the rising edge of SCLK.
CSCLK RSCLK	19 3	O, LVCMOS	With MODE low, these pins function as a buffered control clock from SCLK. CSCLK (RSCLK) is used for cascading the serial control bus to the next device in the serial chain.
LOAD	22	I, LVCMOS	When LOAD is high and SCLK makes a LH transition, the device transfers the programming data in the load register into the configuration registers. The new switch configuration for all outputs takes effect. LOAD needs to remain high for only one SCLK cycle to complete the process, holding LOAD high longer repeats the transfer to the configuration register.
MODE	23	I, LVCMOS	When MODE is low, the SCLK is active and a buffered SCLK signal is present at the CLKOUT output. When MODE is high, the SCLK signal is uncoupled from register and state machine internals. Internal registers will see an active low signal until MODE is brought Low again.
POWER			
V_{DD}	1, 8, 17, 24	I, Power	V_{DD} = 2.5V ±5%. At least 4 low ESR 0.01 µF bypass capacitors should be connected from V_{DD} to GND plane.
GND	4, 20, 21, DAP	I, Power	Ground reference to LVDS and CMOS circuitry. DAP is the exposed metal contact at the bottom of the WQFN-32 package. The DAP is used as the primary GND connection to the device. It should be connected to the ground plane with at least 4 vias for optimal AC and thermal performance.

Serial Interface Truth Table

LOAD	MODE	SCLK	Resulting Action
0	0	LH	The current state on SI is clocked into the input shift register.
0	1	LH	Uncouples SCLK input from internal registers and state machine inputs. The RSCLK and CSCLK outputs will drive an active Low signal until MODE is brought Low again. See Configuration Select Truth Table below.
LH	0	X	Loads OUT1–OUT4 configuration information from last valid frame. Places contents of load register into the configuration register. The switch configuration is updated asynchronously from the SCLK input.
1	1	LH	Uncouples SCLK input from internal registers and state machine inputs. The RSCLK and CSCLK outputs will drive an active Low signal until MODE is brought Low again. See Configuration Select Truth Table below.

Configuration Select Truth Table

MODE	SEL1	SEL0	Resulting Action
0	X	X	The SEL0/1 pins only function in configuration select mode. See below.
1	0	0	Distribution: IN1 - OUT1 OUT2 OUT3 OUT4
1	0	1	Distribution: IN2 - OUT1 OUT2 OUT3 OUT4
1	1	0	Redundancy: IN1 - OUT1 OUT2 and IN3 - OUT3 OUT4
1	1	1	Broadside: IN1 - OUT1, IN2 - OUT2, IN3 - OUT3, IN4 - OUT4

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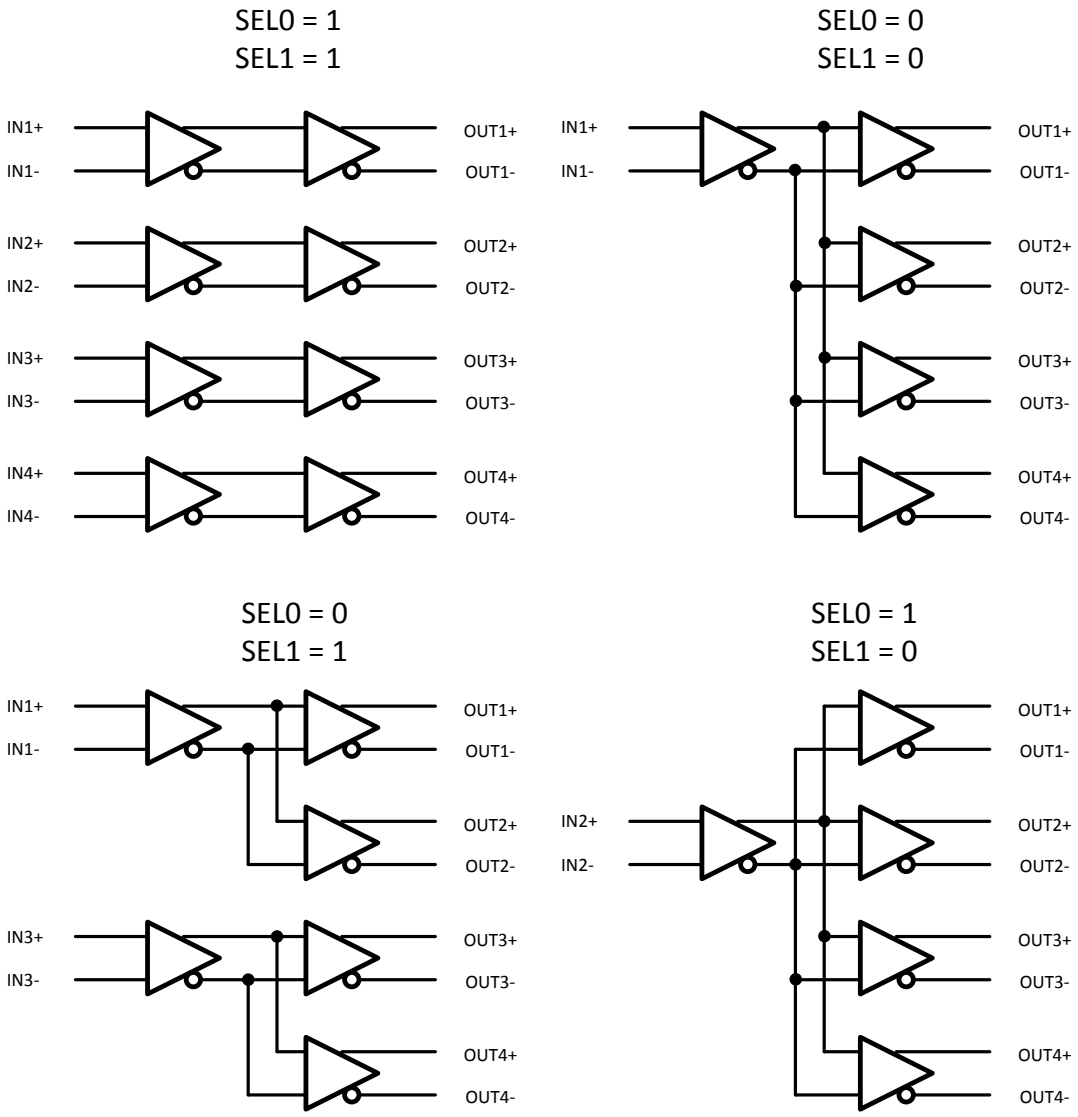


Figure 3. DS90CP04 Configuration Select Decode

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

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Absolute Maximum Ratings (1)(2)

Supply Voltage (V_{DD})	−0.3V to +3V
CMOS/TTL Input Voltage	−0.3V to (V_{DD} +0.3V)
LVDS Receiver Input Voltage	−0.3V to +3.3V
LVDS Driver Output Voltage	−0.3V to +3V
LVDS Output Short Circuit Current	40mA
Junction Temperature	+150°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 4 sec.)	+260°C
Maximum Package Power Dissipation at 25°C	
WQFN-32	3200 mW
Derating above 25°C	38 mW/°C
Thermal Resistance, θ_{JA}	26.4°C/W
ESD Rating	
HBM, 1.5 kΩ, 100 pF	
LVDS Outputs	>1.0 kV
LVDS Inputs	>1.5 kV
All Other Pins	>4.0 kV
EIAJ, 0Ω, 200 pF	>100V

(1) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
(2) "Absolute Maximum Ratings" are the ratings beyond which the safety of the device cannot be ensured. They are not meant to imply that the device should be operated at these limits.

Recommended Operating Conditions

	Min	Typ	Max	Unit
Supply Voltage (V_{DD}– GND)	2.375	2.5	2.625	V
Receiver Input Voltage	0.05		3.3	V
Operating Free Air Temperature	−40	25	85	°C
Junction Temperature			110	°C

Electrical Characteristics

Over recommended operating supply and temperature ranges unless other specified. (1)

Symbol	Parameter	Conditions	Min	Typ (2)	Max	Units
LVCMOS/LVTTL DC SPECIFICATIONS (SCLK, SI/SEL1, SEL0, LOAD, MODE , CSCLK, RSCLK, CSO, RSO)						
V_{IH}	High Level Input Voltage		1.7		V_{DD}	V
V_{IL}	Low Level Input Voltage		GND		0.7	V
I_{IH}	High Level Input Current	$V_{IN} = V_{DD} = V_{DDMAX}$	−10		+10	µA
I_{IL}	Low Level Input Current	$V_{IN} = V_{SS}$, $V_{DD} = V_{DDMAX}$	−10		+10	µA
C_{IN1}	Input Capacitance	Any Digital Input Pin to V_{SS}		3.5		pF
C_{OUT1}	Output Capacitance	Any Digital Output Pin to V_{SS}		5.5		pF
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA	−1.5	−0.8		V
V_{OH}	High Level Output Voltage	I_{OH} = −4.0 mA, $V_{DD} = V_{DDMIN}$	1.9			V
		I_{OH} = −100 µA, V_{DD} = 2.5V	2.4			V
V_{OL}	Low Level Output Voltage	I_{OL} = 4.0 mA, $V_{DD} = V_{DDMIN}$			0.4	V
		I_{OL} = 100 µA, V_{DD} = 2.5V			0.1	V
LVDS INPUT DC SPECIFICATIONS (IN1±, IN2±, IN3±, IN4±)						

(1) "Absolute Maximum Ratings" are the ratings beyond which the safety of the device cannot be ensured. They are not meant to imply that the device should be operated at these limits.
(2) Typical parameters are measured at V_{DD} = 2.5V, T_A = 25°C. They are for reference purposes, and are not production-tested.

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Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges unless other specified. (1)

Symbol	Parameter	Conditions	Min	Typ (2)	Max	Units
V_{TH}	Differential Input High Threshold (3)	V_{CM} = 0.05V or 1.2V or 2.45V, V_{DD} = 2.5V		0	50	mV
V_{TL}	Differential Input Low Threshold	V_{CM} = 0.05V or 1.2V or 2.45V, V_{DD} = 2.5V	−50	0		mV
V_{ID}	Differential Input Voltage	V_{DD} = 2.5V, V_{CM} = 0.05V to 2.45V	100		V_{DD}	mV
V_{CMR}	Common Mode Voltage Range	V_{ID} = 100 mV, V_{DD} = 2.5V	0.05		3.25	V
C_{IN2}	Input Capacitance	IN+ or IN− to V_{SS}		3.5		pF
I_{IN}	Input Current	V_{IN} = 2.5V, V_{DD} = V_{DDMAX} or 0V	−10		+10	µA
		V_{IN} = 0V, V_{DD} = V_{DDMAX} or 0V	−10		+10	µA
LVDS OUTPUT DC SPECIFICATIONS (OUT1±, OUT2±, OUT3±, OUT4±)						
V_{OD}	Differential Output Voltage (3)	R_L = 100Ω between OUT+ and OUT− (see Figure 4)	250	400	475	mV
ΔV_{OD}	Change in V_{OD} between Complementary States		−35		35	mV
V_{OS}	Offset Voltage (4)		1.125	1.25	1.375	V
ΔV_{OS}	Change in V_{OS} between Complementary States		−35		35	mV
I_{OZ}	Output TRI-STATE Current	TRI-STATE Output V_{OUT} = V_{DD} or V_{SS}	−10		+10	µA
I_{OFF}	Power Off Leakage Current	V_{DD} = 0V, V_{OUT} = 2.5V or GND	−10		+10	µA
I_{OS}	Output Short Circuit Current, One Complementary Output	OUT+ or OUT− Short to GND		−15	-40	mA
		OUT+ or OUT− Short to V_{DD}		15	40	mA
I_{OSB}	Output Short Circuit Current, both Complementary Outputs	OUT+ and OUT− Short to GND		−15	-30	mA
		OUT+ and OUT− Short to V_{CM}		15	30	mA
C_{OUT2}	Output Capacitance	OUT+ or OUT− to GND when TRI-STATE		5.5		pF
SUPPLY CURRENT						
I_{CCD}	Total Supply Current	All inputs and outputs enabled, terminated with differential load of 100Ω between OUT+ and OUT-.		220	300	mA
I_{CCZ}	TRI-STATE Supply Current	TRI-STATE All Outputs		10	20	mA
SWITCHING CHARACTERISTICS—LVDS OUTPUTS ((5), (6), (7))						
t_{LHT}	Differential Low to High Transition Time	Use an alternating 1 and 0 pattern at 200 Mb/s, measure between 20% and 80% of V_{OD}.	100	135	160	ps
t_{HLT}	Differential High to Low Transition Time		100	135	160	ps
t_{PLHD}	Differential Low to High Propagation Delay	Use an alternating 1 and 0 pattern at 200 Mb/s, measure at 50% V_{OD} between input to output.	500	750	1200	ps
t_{PHLD}	Differential High to Low Propagation Delay		500	750	1200	ps
t_{SKD1}	Pulse Skew	$\lvert t_{PLHD} - t_{PHLD} \rvert$		0	30	ps

(3) Differential output voltage V_{OD} is defined as |OUT+–OUT−|. Differential input voltage V_{ID} is defined as |IN+–IN−|.
(4) Output offset voltage V_{OS} is defined as the average of the LVDS single-ended output voltages at logic high and logic low states.
(5) Differential output voltage V_{OD} is defined as |OUT+–OUT−|. Differential input voltage V_{ID} is defined as |IN+–IN−|.
(6) Characterized from any input to any one differential LVDS output running at the specified data rate and data pattern, with all other 3 channels running K28.5 pattern at 1.25 Gb/s asynchronously to the channel under test. Jitter is not production-tested, but ensured through characterization on sample basis. Random Jitter is measured peak to peak with a histogram including 1000 histogram window hits. K28.5 pattern is repeating bit streams of (0011111010 1100000101). This deterministic jitter or DJ pattern is measured to a histogram mean with a sample size of 350 hits. Like RJ the Total Jitter or TJ is measured peak to peak with a histogram including 3500 window hits.
(7) The LVCMOS input and output AC specifications may also be verified and tested using an input attenuation network instead of a power splitter.

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Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges unless other specified. (1)

Symbol	Parameter	Conditions	Min	Typ (2)	Max	Units
t_{SKCC}	Output Channel to Channel Skew	Difference in propagation delay (t_{PLHD} or t_{PHLD}) among all output channels in Broadcast mode (any one input to all outputs).	0	50	100	ps
t_{JIT}	Jitter (6)	Alternating 1 and 0 Pattern				
		750 MHz		1.6	2.5	psrms
		1.25 GHz		1.6	2.5	psrms
		K28.5 Pattern				
		1.5 Gb/s		10	40	psp-p
		2.5 Gb/s		27	60	psp-p
		PRBS 2^{23}-1 Pattern				
		1.5 Gb/s		25	40	psp-p
		2.5 Gb/s		40	70	psp-p
t_{ON}	LVDS Output Enable Time	Time from LOAD = LH or SELx to OUT± change from TRI-STATE to active.	50	150	300	ns
t_{OFF}	LVDS Output Disable Time	Time from LOAD = LH or SELx to OUT± change from active to TRI-STATE.		3	5	ns
t_{SW}	LVDS Switching Time	Time from LOAD = LH to new switch configuration effective for OUT±.		50	150	ns
t_{SEL}	SELx to OUT±	Configuration select to new data at OUT±.		50	150	ns
SWITCHING CHARACTERISTICS — Serial control Interface (8)						
F_{SCLK}	SCLK Clock Frequency		0		100	MHz
T_{DCCLK}	CSCLK Duty Cycle RSCLK Duty Cycle	Input SCLK Duty Cycle set at 50%	45		55	%
t_S	SI–SCLK or MODE–SCLK Setup Time	From SI or MODE Input Data to SCLK Rising Edge	1.5			ns
t_H	SCLK–SI or SCLK–MODE Hold Time	From SCLK Rising Edge to SI or MODE Input Data	1			ns
t_{DSO}	SCLK to RSO or CSO Delay	From SCLK to RSO or CSO	1.5		4	ns
t_{DSCLK}	SCLK to RSCLK or CSCLK Delay	From SCLK to RSCLK or CSCLK	4.0		8.5	ns
t_{DSDIF}	|SCLK to RSCLK or CSCLK–SCLK to RSO or CSO|	Propagation Delay Difference between t_{DSO} and t_{DSCLK}	1.5		4.5	ns
T_{RISE}	Logic Low to High Transition Time	20% to 80% at RSO, CSO, RSCLK, or CSCLK		1.5		ns
T_{FALL}	Logic High to Low Transition Time	80% to 20% at RSO, CSO, RSCLK, or CSCLK		1.5		ns

(8) Output offset voltage V_{OS} is defined as the average of the LVDS single-ended output voltages at logic high and logic low states.

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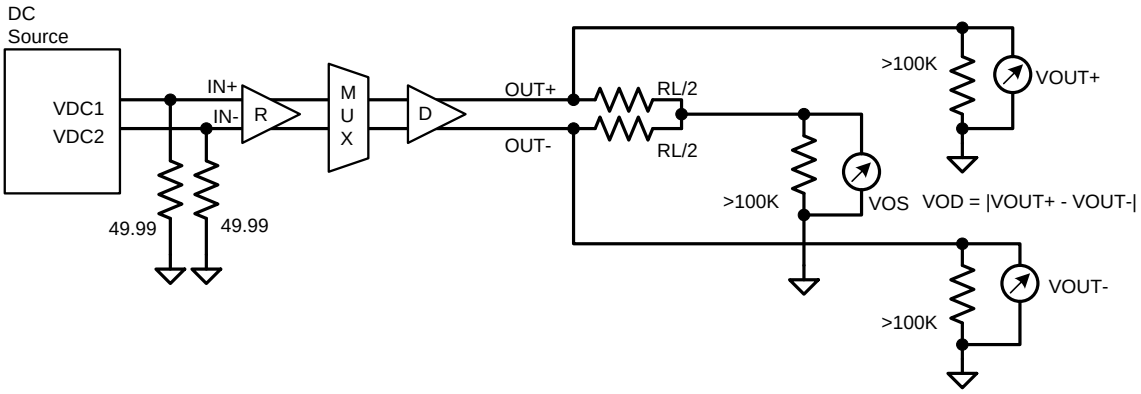


Figure 4. Differential Driver DC Test Circuit

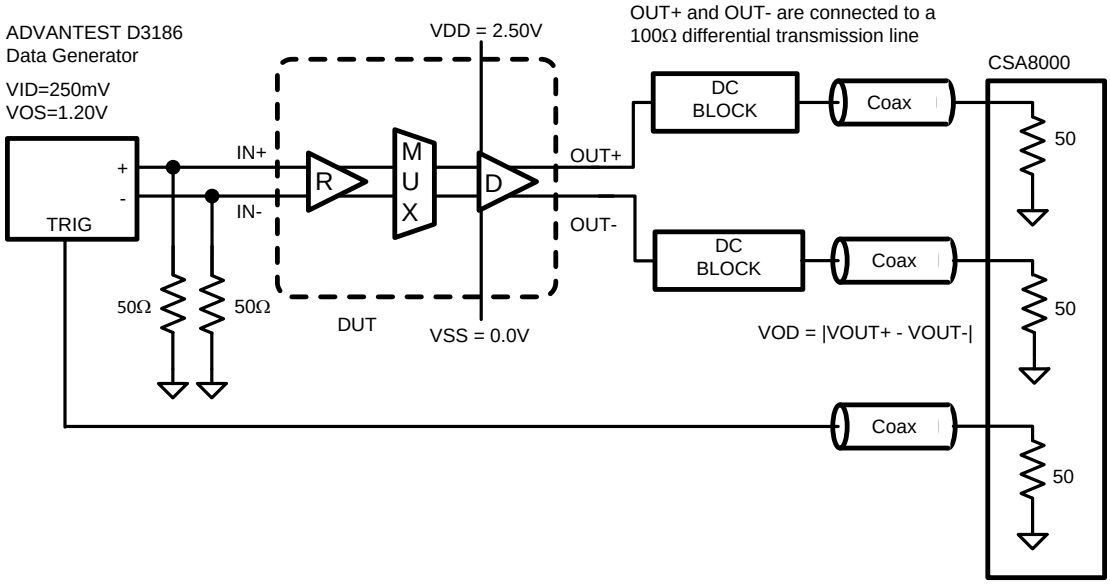


Figure 5. Differential Driver AC Test Circuit

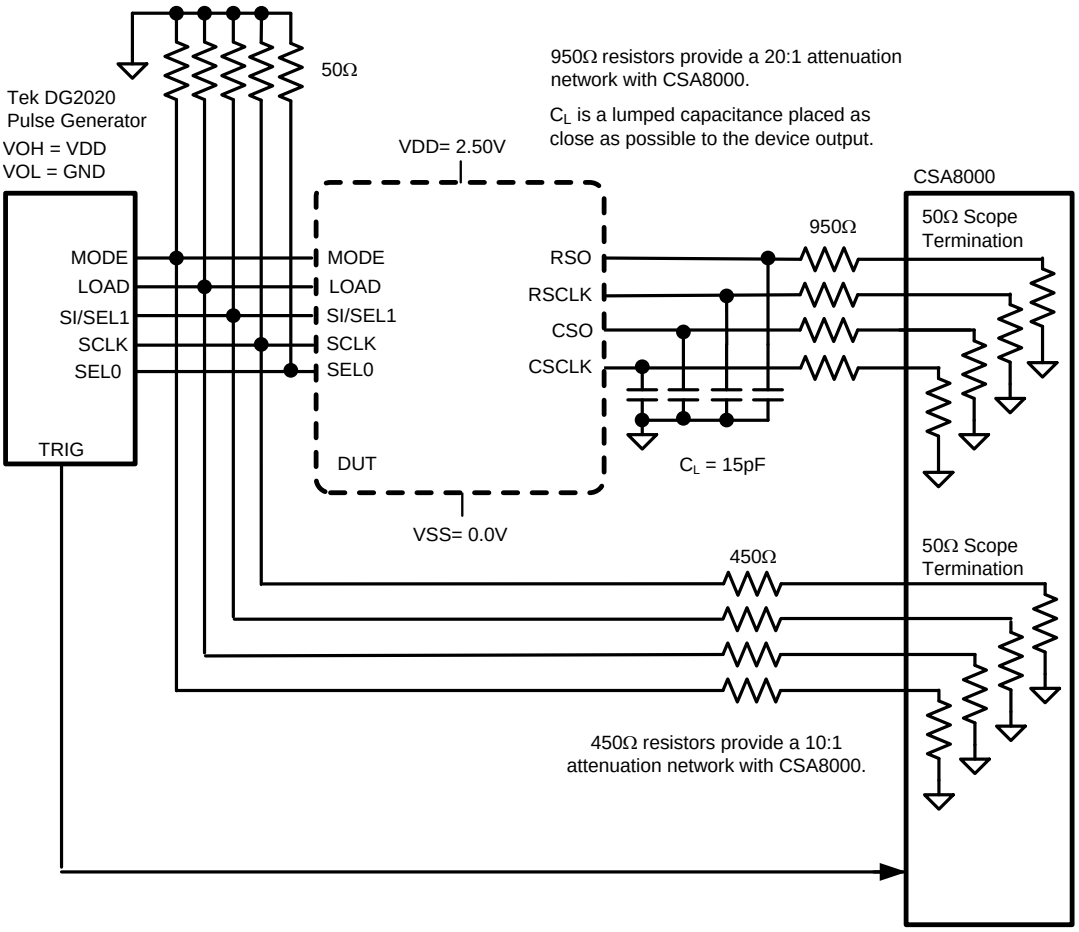


Figure 6. LVCMOS Driver AC Test Circuit (9)

(9) The LVCMOS input and output AC specifications may also be verified and tested using an input attenuation network instead of a power splitter.

Parameter Measurement Information

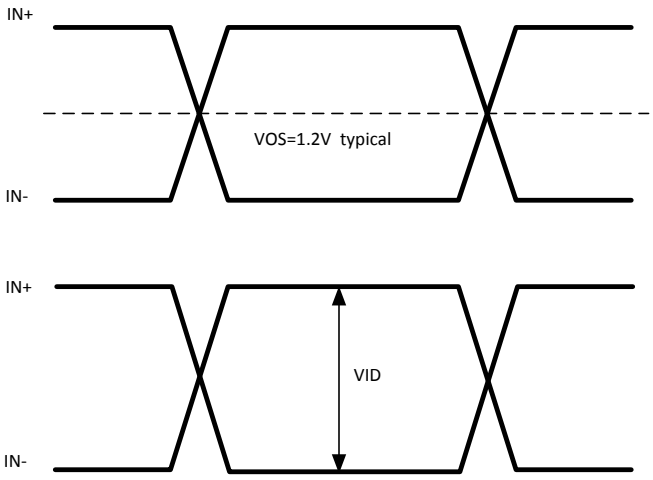


Figure 7. LVDS Signals

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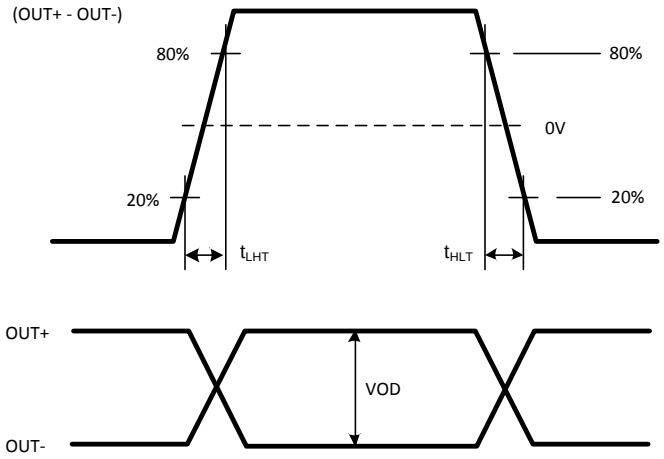


Figure 8. LVDS Output Transition Time

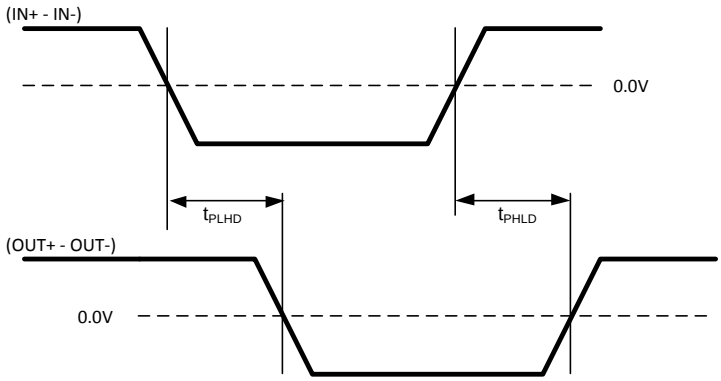


Figure 9. LVDS Output Propagation Delay

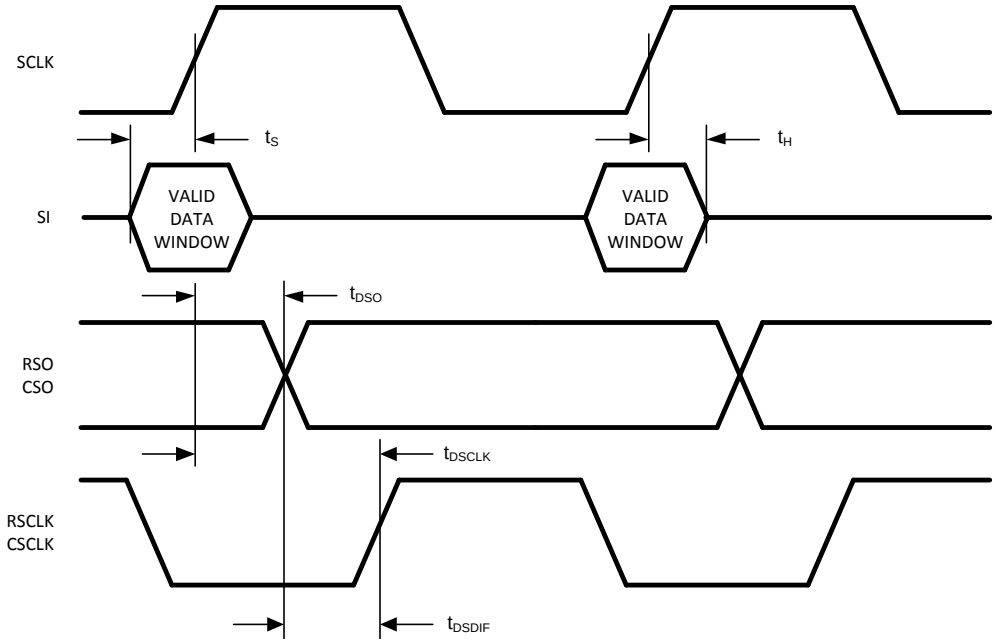


Figure 10. Serial Interface Propagation Delay and Input Timing Waveforms

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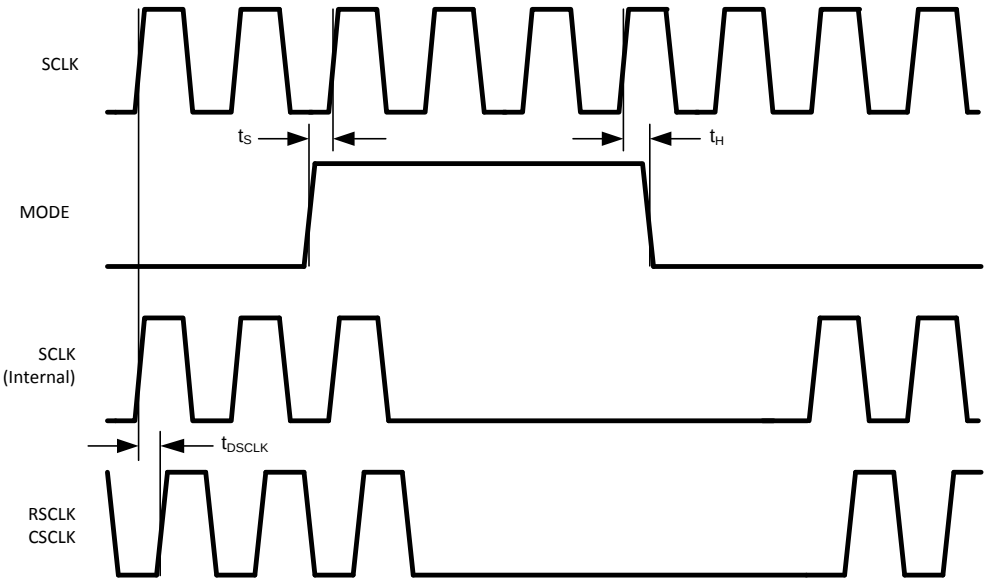


Figure 11. Serial Interface— MODE Timing and Functionality

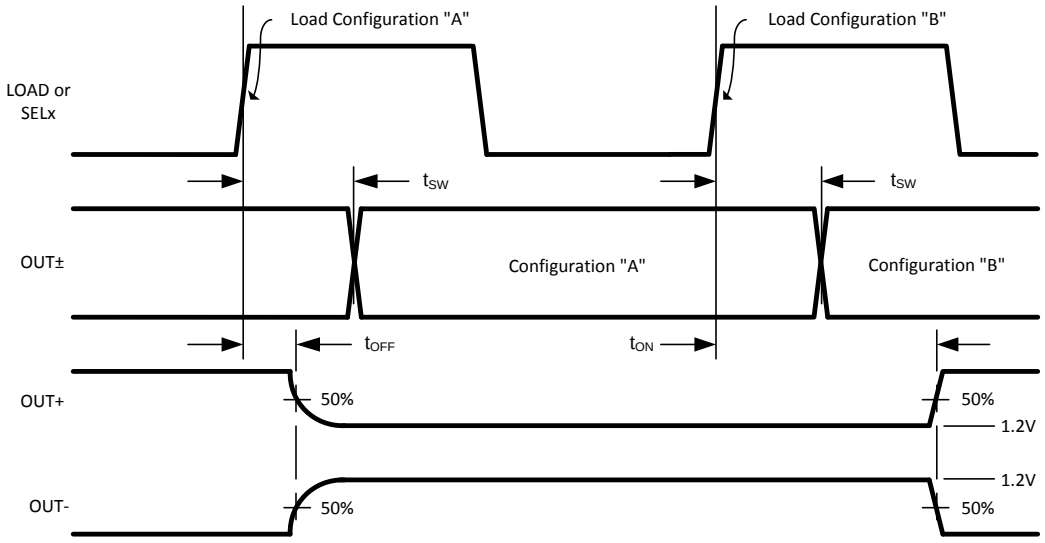


Figure 12. Configuration and Output Enable/Disable Timing

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FUNCTIONAL DESCRIPTIONS

Programming with the Serial Interface

The configuration of the internal multiplexer is programmed through a simple serial interface consisting of serial clock SCLK and serial input data line SI. The serial interface is designed for easy expansion to larger switch array. A replicated output serial interface (RSCLK, RSO) is provided for propagating the control data to the downstream device in the row of an array of DS90CP04 devices in a matrix. A similar replicated serial interface (CSCLK, CSO) is provided for propagating the control data to the downstream devices in the first column of the device matrix. Through this scheme, user can program all the devices in the matrix through one serial control bus (SCLK and SI) with the use of the feed-through replicated control bus at RSCLK and RSO, CSCLK and CSO.

To program the configuration of the switch, a 30-bit control word is sent to the device. The first 6 bits shift the start frame into SI. The only two valid start frames are 1F'h for a configuration load and 1E'h for a configuration read. The start frame is followed by the row and column addresses of the device to be accessed, as well as the switch configuration of the four channels of the device. Table 1 and Table 2 are the bit definitions of the control word. D29 is the first bit that shifts into SI.

Table 1. 30-Bit Control Word

Bit	Bit Length	Descriptions
D29–D24	6	The start frame for control word synchronization (01 1111'b = LOAD).
D23–D18	6	Specify the row address of the device to be access. The serial interface can access up to 64 devices in the row.
D17–D12	6	Specify the column address of the device to be access. The serial interface can access up to 64 devices in the column.
D11–D9	3	Specify the switch configuration for Output 1. See Table 2.
D8–D6	3	Specify the switch configuration for Output 2. See Table 2.
D5–D3	3	Specify the switch configuration for Output 3. See Table 2.
D2–D0	3	Specify the switch configuration for Output 4. See Table 2.

Table 2. Switch Configuration Data

MSB		LSB	OUT1± Connects to	OUT2± Connects to	OUT3± Connects to	OUT4± Connects to
0	0	0	Output 1 Tri-Stated	Output 2 Tri-Stated	Output 3 Tri-Stated	Output 4 Tri-Stated
0	0	1	IN1±	IN1±	IN1±	IN1±
0	1	0	IN2±	IN2±	IN2±	IN2±
0	1	1	IN3±	IN3±	IN3±	IN3±
1	0	0	IN4±	IN4±	IN4±	IN4±
1	0	1	Invalid.			
1	1	0	Use of these invalid combinations may cause loss of synchronization.			
1	1	1				

Row and Column Addressing

The upper left device in an array of NxN devices is assigned row address 0, and column address 0. The devices to its right have column addresses of 1 to N, whereas devices below it have row addresses of 1 to N. The Serial Control Interface (SCLK and SI) is connected to the first device with the row and column addresses of 0. The Serial Control Interface shifts in a control word containing the row and column address of the device it wants to access. When the control data propagates through each device, the control word's address is internally decremented by one before it is sent to the next row or column device. When the control data is sent out the column interface (CSO and CSCLK) the row address is decremented by one. Similarly, when the column address data is shifted out the row interface (RSO and RSCLK) the column address is decremented by one. By the time the control word reaches the device it has been intended to program, both the row and column addresses have been decremented to 0.

Each device constantly checks for the receipt of a frame start (D29-24=01 1111'b or 01 1110'b). When it detects the proper start frame string, and the row and column addresses it receives are both 0, the device responds by storing the switch configuration data of the 30-bit control word into its load register.

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Each device in the array is sequentially programmed through the serial interface. When programming is completed for the entire array, LOAD is pulsed high and the load register's content is transferred to the configuration register of each device. The LOAD pulse must wait until the final bit of the control word has been placed into the "load" register. This timing is ensured to take place two clock cycles after programming has been completed.

Due to internal shift registers additional SCLK cycles will be necessary to complete array programming. It takes 7 clock (SCLK) positive edge transitions for the control data to appear at RSO and CSO for its near neighbor. Users must provide the correct number of clock transitions for the control data word to reach its destination in the array. Table 3 shows an example of the control data words for a 4 device serial chain with connections (OUT1=IN1, OUT2=IN2, OUT16=IN16). To program the array, it requires four 30-bit control words to ripple through the serial chain and reach their destinations. In order to completely program the array in the 120 clock cycles associated with the 30-bit control words it is important to program the last device in the chain first. The following programming data pushes the initial data through the chain into the correct devices.

Read-Back Switch Configuration

The DS90CP04 is put into read-back mode by sending a special “Read” start frame (01 1110'b). Upon receipt of the special read start frame the configuration register information is transferred into the shift register and output at both RSO and CSO in the OUT1 to OUT4 bit segments of the read control word. Each time the read-back data from a device passes through its downstream device, its default address (11 1111'b) is internally decremented by one. The “relative” column address emerges at RSO of the last device in the row and is used to determine (11 1111'b - N) the column of the sending device. Similarly, the row address emerges at CSO of the sending device. After inserting the channel configuration information in the “read” control word, the device will automatically revert to write mode, ready to accept a new control word at SI.

Table 4 shows an example of reading back the configuration registers of 4 devices in the first row of a 4x4 device array. Again, due to internal shift registers additional SCLK cycles will be necessary to complete the array read. It takes 4x30 SCLK clock cycles to shift out 4 30-bit configuration registers plus 7 SCLK cycles per device to account for device latency making for a total SCLK count of 148. The serialized read data is sampled at RSO and synchronized with RSCLK of the last device in the row. The user is recommended to backfill with all 0's at SI after the four reads have been shifted in.

Table 3. Example to Program a 4 Device Array

Frame D29:D24	Row Address D23:D18	Column Address D17:D12	OUT1 D11:D9	OUT2 D8:D6	OUT3 D5:D3	OUT4 D2:D0	Number of SCLK Cycles	Control Word Destination Device in Array Row, Column
01 1111	00 0000	00 0011	001	010	011	100	30	0, 3
01 1111	00 0000	00 0010	001	010	011	100	30	0, 2
01 1111	00 0000	00 0001	001	010	011	100	30	0, 1
01 1111	00 0000	00 0000	001	010	011	100	30	0, 0
Shift in configuration information from device furthest from system SI input first to minimize array latency during the programming process.								
The 2 clock cycle delay ensures all channel information has reached the “load” register and all switches are ready to be configured.							2	

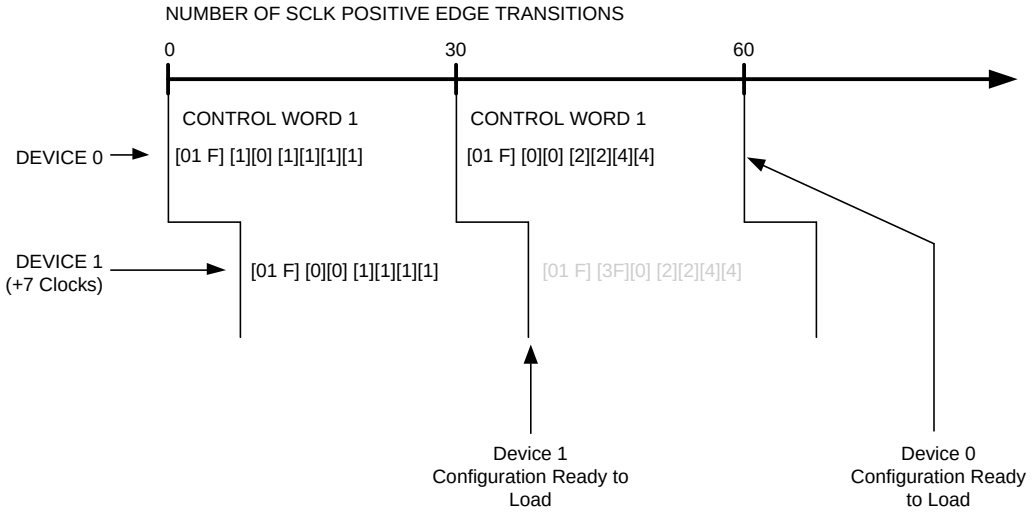
Table 4. A Read-Back Example from a 4 Device Array

Frame D29:D24	Row Address D23:D18	Column Address D17:D12	OUT1 D11:D9	OUT2 D8:D6	OUT3 D5:D3	OUT4 D2:D0	Number of SCLK Cycles	Descriptions
01 1110	00 0000	11 1111	000	000	000	000	30	Read-Back (R,C)=0, 3
01 1110	00 0000	11 1110	000	000	000	000	30	Read-Back (R,C)=0, 2
01 1110	00 0000	11 1101	000	000	000	000	30	Read-Back (R,C)=0, 1
01 1110	00 0000	11 1100	001	010	011	100	30	Read-Back (R,C)=0, 0

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Switch Expansion For Minimum Programming Latency

Programming data ripples through the array through RSO and RSCLK in the row and CSO and CSCLK in the first column. LOAD pins of all devices are electrically tied together and driven by the same “load” signal. To prevent excessive stub length in the array from affecting the signal quality of LOAD, it is recommended that the load signal is distributed to each row or column in large crosspoint array applications.



Programming Example

CONFIGURATION WRITE

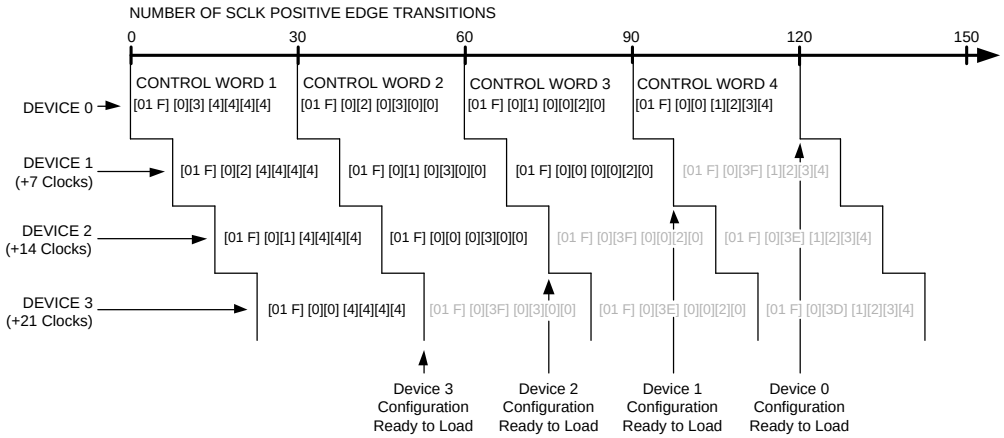
30 Bit Control Word: [WRITE FRAME] [ROW ADDRESS][COLUMN ADDRESS] [OUT1][OUT2][OUT3][OUT4]

ARRAY WRITE

[01 1111] [0][1] [1][1][1][1] //*Array position 1, Broadcast IN1 *//

[01 1111] [0][0] [2][2][4][4] //*Array position 0, Connect IN2 to OUT1 and 2, IN4 to OUT3 and OUT4 *//

LOAD = H and SCLK = LH



DEVICE 0 WRITE PROGRAMMING SEQUENCE

SCLK Number	Event Description
6	Device 0 (R=0, C=0) detects “WRITE” frame of first Control Word.
18	Device 0 (R=0, C=0) sees Row = 1, Column = 0 of first Control Word. The Row address of the first Control Word is decremented by 1 (Row Address = 0) and sent out RSO.
36	Device 0 (R=0, C=0) detects “WRITE” frame of second Control Word.
48	Device 0 (R=0, C=0) sees Row = 0, Column = 0 of second Control Word. This is a valid configuration write address, Device 1 prepares to receive configuration information.
60	Device 0 (R=0, C=0) has received configuration information and is waiting for a LOAD.

DEVICE 1 WRITE PROGRAMMING SEQUENCE

SCLK Number	Event Description
13	Device 1 (R=1, C=0) detects “WRITE” frame of first Control Word.
25	Device 1 (R=1,C=0) sees Row = 0, Column = 0 of first Control Word. This is a valid configuration write address, Device 1 prepares to receive configuration information.
37	Device 1 (R=1,C=0) has received configuration information and is waiting for a LOAD.
43	Device 1 (R=1, C=0) detects “WRITE” frame of second Control Word.
55	Device 1 (R=1,C=0) sees Row = 3F, Column = 0 of second Control Word. The Row address of the second Control Word is decremented by 1 (Row Address = 3E) and sent out RSO.

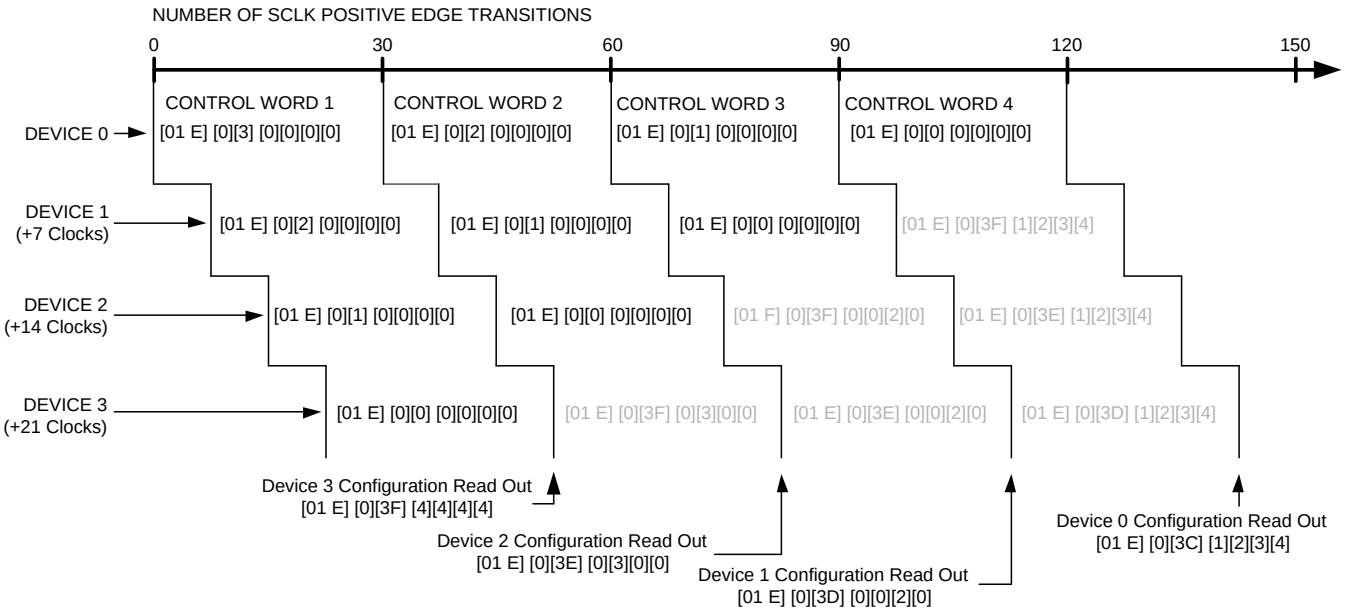
CONFIGURATION READ

30 Bit Control Word: [READ FRAME] [ROW ADDRESS][COLUMN ADDRESS] [OUT1][OUT2][OUT3][OUT4]

ARRAY WRITE

[01 1110] [1][0] [0][0][0][0] //*Array position 1, Return Configuration Information *//

[01 1110] [0][0] [0][0][0][0] //*Array position 0, Return Configuration Information *//



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DEVICE 0 READ PROGRAMMING SEQUENCE

SCLK Number	Event Description
6	Device 0 (R=0, C=0) detects “READ” frame of first Control Word.
18	Device 0 (R=0,C=0) sees Row = 1, Column = 0 of first Control Word. The Row address of the first Control Word is decremented by 1 (Row Address = 0) and sent out RSO.
36	Device 0 (R=0,C=0) detects "READ" frame of second Control Word.
48	Device 0 (R=0,C=0) sees Row = 0, Column = 0 of second Control Word. This is a valid configuration read address, Device 0 prepares to transmit configuration information. The Row address of the last Control Word is decremented by 1 (Row Address = 3F) and sent out RSO.
60	Device 0 (R=0,C=0) has transmitted configuration information.
74	Finished transmitting configuration information at Array Output (RSO of Device 1).

DEVICE 1 READ PROGRAMMING SEQUENCE

SCLK Number	Event Description
13	Device 1 (R=1, C=0) detects “READ” frame of first Control Word.
25	Device 1 (R=1,C=0) sees Row = 0, Column = 0 of first Control Word. This is a valid configuration read address, Device 1 prepares to transmit configuration information. The Row address of the last Control Word is decremented by 1 (Row Address = 3F) and sent out RSO.
37	Device 1 (R=1,C=0) has transmitted configuration information at Array Output (RSO of Device 1).

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REVISION HISTORY

Changes from Revision H (April 2013) to Revision I	Page
• Changed layout of National Data Sheet to TI format	17

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS90CP04TLQ	NRND	WQFN	NJE	32	250	TBD	Call TI	Call TI	-40 to 85	90CP04T	
DS90CP04TLQ/NOPB	ACTIVE	WQFN	NJE	32	250	Green (RoHS & no Sb/Br)	SN	Level-3-260C-168 HR	-40 to 85	90CP04T	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

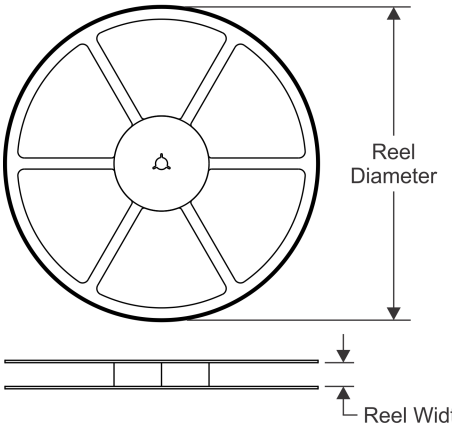
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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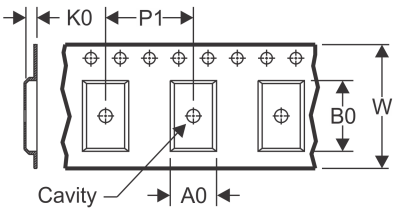
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

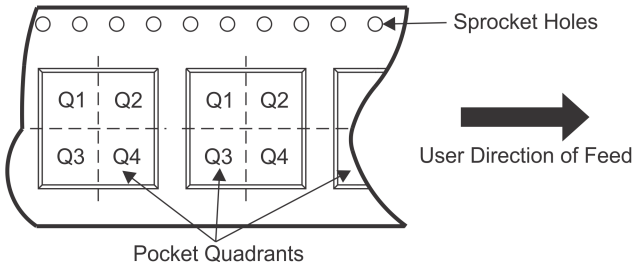


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

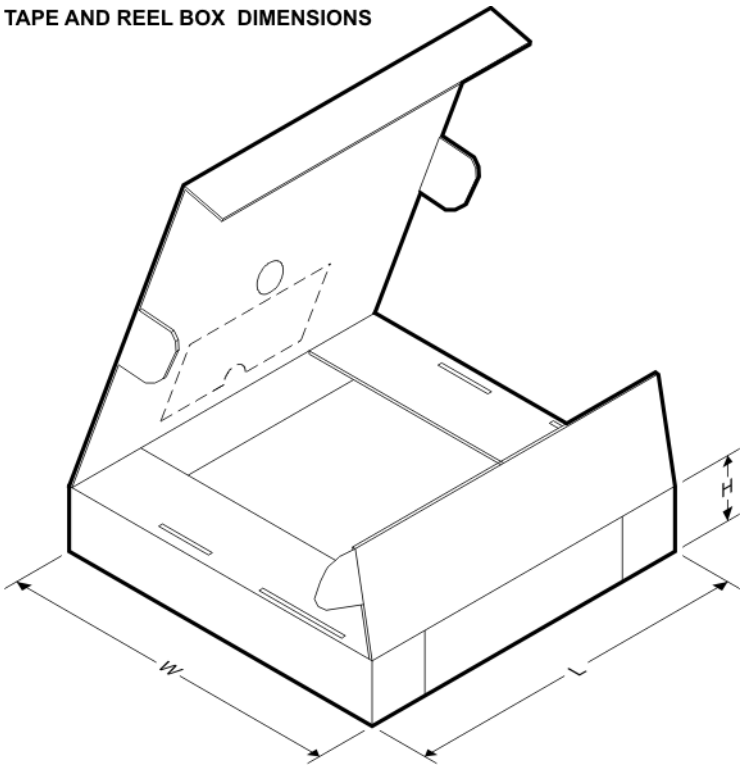
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

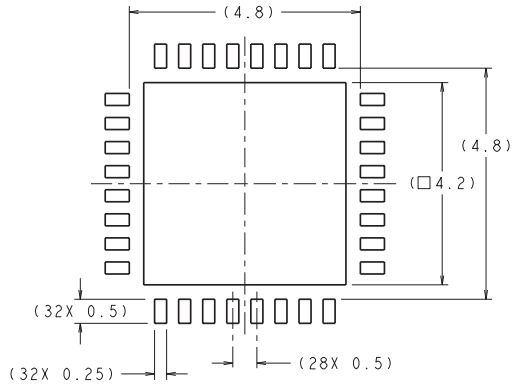
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS90CP04TLQ	WQFN	NJE	32	250	178.0	16.4	6.3	6.3	1.5	12.0	16.0	Q1
DS90CP04TLQ/NOPB	WQFN	NJE	32	250	178.0	16.4	6.3	6.3	1.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



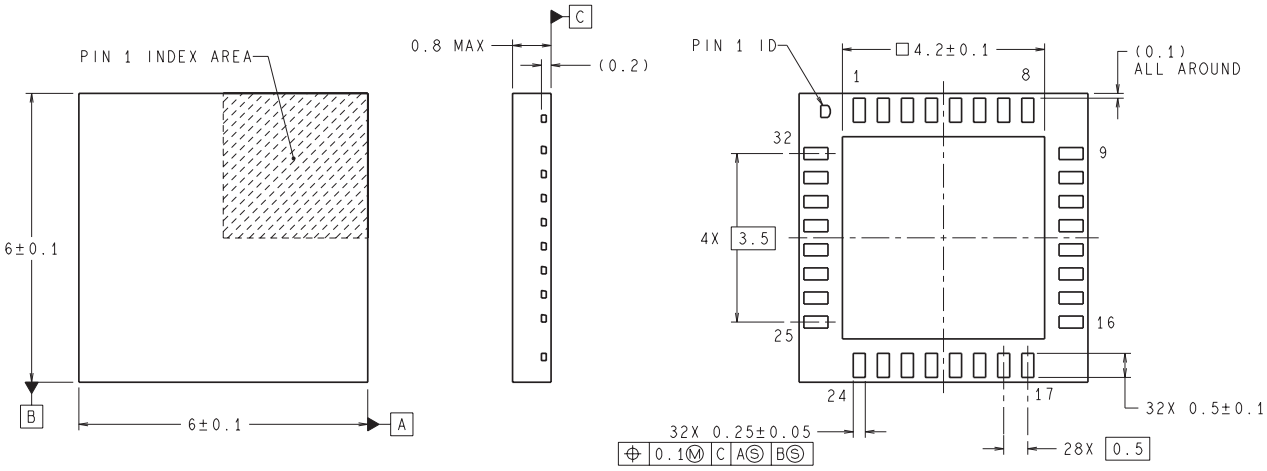
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS90CP04TLQ	WQFN	NJE	32	250	210.0	185.0	35.0
DS90CP04TLQ/NOPB	WQFN	NJE	32	250	210.0	185.0	35.0



RECOMMENDED LAND PATTERN
1:1 RATIO WITH PKG SOLDER PADS

DIMENSIONS ARE IN MILLIMETERS



LQA32A (REV A)

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