DS90C3201 3.3V 8 MHz to 135 MHz Dual FPD-Link Transmitter

Check for Samples: DS90C3201

FEATURES

- **Up to 9.45Gbit/s data throughput**
- **8 MHz to 135 MHz input clock support**
- **Supports up to QXGA panel resolutions**
- **Supports HDTV resolutions and frame rates up to 1920 x 1080p**
- **LVDS 30-bit, 24-bit or 18-bit color data outputs**
- **Supports single pixel and dual pixel interfaces**
- **Supports spread spectrum clocking**
- **Two-wire serial communication interface**
- **Programmable clock edge and control strobe select**
- **Power down mode**
- **+3.3V supply voltage**
- **128-pin TQFP**
- **Compliant to TIA/EIA-644-A-2001 LVDS Standard**

DESCRIPTION

The DS90C3201 is a 3.3V single/dual FPD-Link 10-bit color transmitter is designed to be used in Liquid Crystal Display TVs, LCD Monitors, Digital TVs, and Plasma Display Panel TVs. The DS90C3201 is designed to interface between the digital video processor and the display device using the low-power, low-EMI LVDS (Low Voltage Differential Signaling) interface. The DS90C3201 converts up to 70 bits of LVCMOS/LVTTL data into ten LVDS data streams. The transmitter can be programmed clocking data with rising edge or falling edge clock. Optional two-wire serial programming allows fine tuning in development and production environments. At a transmitted clock frequency of 135 MHz, 70 bits of LVCMOS/LVTTL data are transmitted at an effective rate of 945 Mbps per LVDS channel. Using a 135 MHz clock, the data throughput is 9.45Gbit/s (945Mbytes/s). This allows the dual 10-bit LVDS Transmitter to support HDTV resolutions.

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Block Diagram

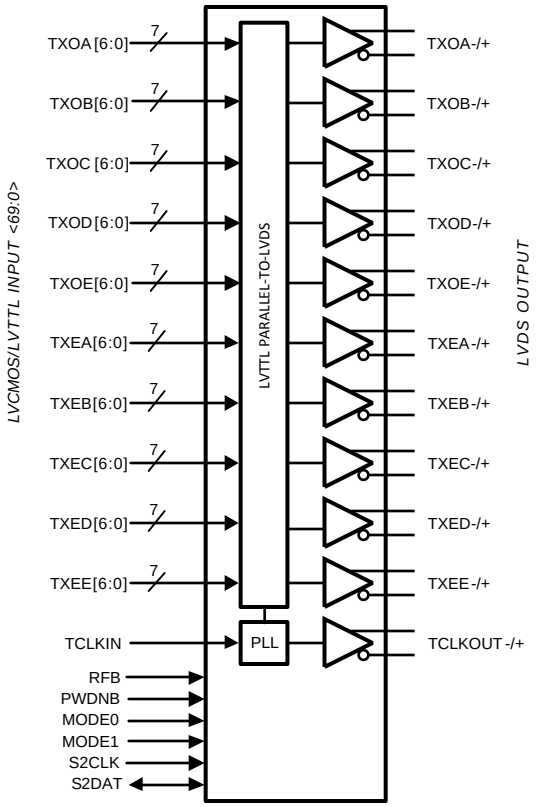


Figure 1. Transmitter Block Diagram

Typical Application Diagram

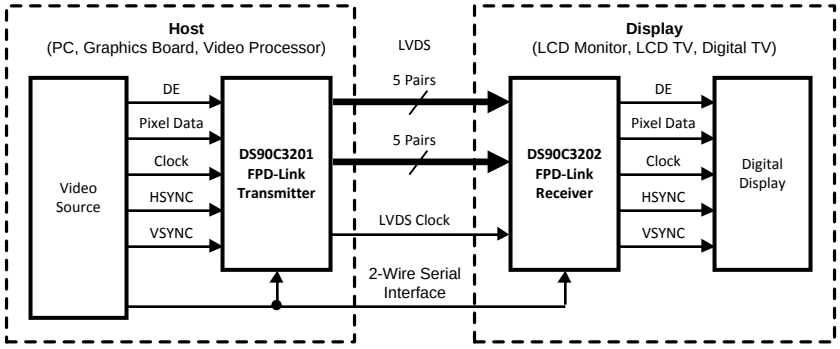


Figure 2. LCD Panel Application Diagram

Functional Description

The DS90C3201 and DS90C3202 are a dual 10-bit color Transmitter and Receiver FPD-Link chipset designed to transmit data at clocks speeds from 8 to 135 MHz. DS90C3201 and DS90C3202 are designed to interface between the digital video processor and the display using a LVDS interface. The DS90C3201 transmitter serializes 2 channels of video data (10-bit each for RGB for each channel, totaling 60 bits) and control signals (HSYNC, VSYNC, DE and two user-defined signals) along with clock signal to 10 channels of LVDS signals and transmits them. The DS90C3202 receiver converts 10 channels of LVDS signals into parallel signals and outputs

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2 channels of video data (10-bit each for RGB for each channel, totaling 60 bits) and control signals (HSYNC, VSYNC, DE and two user-defined signals) along with clock signal. The dual high speed LVDS channels supports single pixel in-single pixel out and dual pixel in-dual pixel out transmission modes. The FPD-Link chipset is suitable for a variety of display applications including LCD Monitors, LCD TV, Digital TV, and DLP TV, and Plasma Display Panels.

Using a true 10-bit color depth system, the 30-bit RGB color produces over 1.07 billion colors to represent High Definition (HD) displays in their most natural color, surpassing the maximum 16.7 million colors achieved by 6/8-bit color conventionally used for large-scale LCD televisions and LCD monitors.

LVDS TRANSMITTER

The LVDS Transmitter serializes LVCMOS/LVTTL RGB video data and control signal timing into LVDS data streams.

SINGLE PIXEL AND DUAL PIXEL INTERFACE

The DS90C3201 LVDS ports support two modes: Single Pixel mode (30-bit LVDS output) and Dual Pixel mode (2 x 30-bit LVDS output). For Single Pixel mode, the Odd LVDS ports for 10-bit RGB data are utilized. For the Dual Pixel mode, both Odd and Even LVDS ports are utilized for 10-bit RGB data.

SELECTABLE INPUT DATA STROBE

The Transmitter input data edge strobe can be latched on the rising or falling edges of input clock signal. The dedicated RFB pin is used to program input strobe select on the rising edge of TCLK IN or the falling edge of TCLK IN.

2-WIRE SERIAL COMMUNICATION INTERFACE

Optional Two-wire serial interface programming allows fine tuning in development and production environments. The Two-wire serial interface provides several capabilities to reduce EMI and to customize output timing. These capabilities are selectable/programmable via Two-wire serial interface: Programmable LVDS Swing Control, Adjustable Input Setup/Hold Control, Input/Output Channel Control.

PROGRAMMABLE LVDS SWING CONTROL

Programmable LVDS amplitude (V_{OD}) and LVDS offset voltage (V_{OS}) of the differential signals can be adjusted for better impedance matching for noise and EMI reduction. The low level LVDS swing mode and offset voltage can be controlled via Two-wire serial interface.

ADJUSTABLE INPUT SETUP/HOLD CONTROL

Programmable LVCMOS/LVTTL Data Input Setup and Hold Times can be adjusted with respect to TCLK IN for convenient interface with a variety of graphic controllers and video processors. Feature is controlled via Two-wire serial interface.

INPUT/OUTPUT CHANNEL CONTROL

Full independent control for input/output channels can be disabled to minimize power supply line noise and overall power dissipation. Feature is configured via Two-wire serial interface.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)

Supply Voltage (V_{DD})		−0.3V to +4V
LVCMOS/LVTTL Input Voltage		−0.3V to (V_{DD} + 0.3V)
LVCMOS/LVTTL Output Voltage		−0.3V to (V_{DD} + 0.3V)
LVDS Output Voltage		−0.3V to (V_{DD} + 0.3V)
LVDS Short Circuit Duration		Continuous
Junction Temperature		+150°C
Storage Temperature		−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)		+260°C
Maximum Package Power Dissipation Capacity at 25°C	128 TQFP Package	1.4W
Package Derating		25.6mW/°C above +25°C
ESD Rating	HBM, 1.5kΩ, 100pF	> 2 kV
	EIAJ, 0Ω, 200pF	> 200 V

(1) "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be ensured. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

Recommended Operating Conditions

	Min	Nom	Max	Unit
Supply Voltage (V_{DD})	3.15	3.3	3.6	V
Operating Free Air Temperature (T_A)	0	+25	+70	°C
Supply Noise Voltage (V_{P-P})			±100	mV_{P-P}
Transmitter Input Range	0		V_{DD}	V
Input Clock Frequency (f)	8		135	MHz
TCLKIN Period (T_{CIP})	7.4		125	ns

Electrical Characteristics (1) (2) (3)

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
LVCMOS/LVTTL DC SPECIFICATIONS (Tx inputs, control inputs)						
V_{IH}	High Level Input Voltage		2.0		V_{DD}	V
V_{IL}	Low Level Input Voltage		0		0.8	V
V_{CL}	Input Clamp Voltage	I_{CL} = −18mA		−0.8	−1.5	V
I_{IN}	Input Current	0V ≤ V_{IN} ≤ V_{DD}			+10	µA
		V_{IN} = 0V	−10	0		µA
LVDS TRANSMITTER DC SPECIFICATIONS						
V_{OD}	Differential Output Voltage (Programmable register)	R_L = 100Ω, Register addr 28d/1ch bit [5] (TXE) = 0b, bit [4] (TXO) = 0b (Default)	200	400	620	mV
		R_L = 100Ω, Register addr 28d/1ch bit [5] (TXE) = 1b, bit [4] (TXO) = 1b	100	250	400	mV
ΔV_{OD}	Change in V_{OD} between complimentary output states	R_L = 100Ω			50	mV

(1) Typical values are given for V_{DD} = 3.3V and T_A = +25°C.
(2) Current into device pins is defined as positive. Current out of device pins is defined as negative. Voltages are referenced to ground unless otherwise specified.
(3) The Minimum and Maximum Limits are based on statistical analysis of the device performance over process, voltage and temperature ranges. This parameter is functional tested only on Automatic Test Equipment (ATE).

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Electrical Characteristics [1] [2] [3] (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{OS}	Offset Voltage (Programmable register)	R_L = 100Ω, Register addr 28d/1ch bit [3:2] (TXE) = 00b, bit [1:0] (TXO) = 00b, (Default)		1.0	1.2	1.5	V
		R_L = 100Ω, Register addr 28d/1ch bit [3:2] (TXE) = 01b, bit [1:0] (TXO) = 01b		0.8	1.0	1.2	V
		R_L = 100Ω, Register addr 28d/1ch bit [3:2] (TXE) = 10b, bit [1:0] (TXO) = 10b		0.6	0.8	1.0	V
ΔV_{OS}	Change in V_{OS} between complimentary output states					50	mV
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V				−50	mA
TRANSMITTER SUPPLY CURRENT							
ICCTW	Transmitter Supply Current, Worst Case (Figure 4, Figure 6) [4]	R_L = 100Ω, C_L = 5pF, Worst Case Pattern, Default Register Settings	f = 8 MHz	20	60	95	mA
			f = 135 MHz	65	150	235	mA
ICCTG	Transmitter Supply Current, Incremental Test Pattern (Figure 5 Figure 6) [5]	R_L = 100Ω, C_L = 5pF, Worst Case Pattern, Default Register Settings	f = 8 MHz	15	55	90	mA
			f = 135 MHz	40	110	175	mA
ICCTZ	Transmitter Supply Current, Power Down	PDWNB = Low, R_L = 100Ω, C_L = 5pF, Default Register Settings				2	mA

(4) The worst case test pattern produces a maximum toggling of digital circuits, LVDS I/O and LVCMOS/LVTTL I/O.
(5) The incremental test pattern tests device power consumption for a “typical” LCD display pattern.

Recommended Transmitter Input Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit
T_{CIT}	TCLK IN Transition Time (Figure 8)			(1)	ns
T_{CIP}	TCLK IN Period (Figure 9)	7.4	T	125.0	ns
T_{CIH}	TCLK IN High Time (Figure 9)	$0.30T_{CIP}$	$0.50T_{CIP}$	$0.70T_{CIP}$	ns
T_{CIL}	TCLK IN Low Time (Figure 9)	$0.30T_{CIP}$	$0.50T_{CIP}$	$0.70T_{CIP}$	ns
T_{XIT}	TxIN Transition Time	(1)		(1)	ns
$TJIT_{RMS}$	TCLK IN Jitter (RMS)		±200		ps

(1) Less than 5ns or 30% of TCIP, whichever is less.

Transmitter Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit
LLHT	LVDS Low-to-High Transition Time (Figure 7)		0.6	1.5	ns
LHLT	LVDS High-to-Low Transition Time (Figure 7)		0.6	1.5	ns
TPPos1	Transmitter Output Pulse Position for bit 1 (1st bit) (Figure 15)	−0.2	0	+0.2	UI (1)
TPPos0	Transmitter Output Pulse Position for bit 0 (2nd bit) (Figure 15)	1 UI − 0.2	1	1 UI + 0.2	UI (1)
TPPos6	Transmitter Output Pulse Position for bit 6 (3rd bit) (Figure 15)	2 UI − 0.2	2	2 UI + 0.2	UI (1)
TPPos5	Transmitter Output Pulse Position for bit 5 (4th bit) (Figure 15)	3 UI − 0.2	3	3 UI + 0.2	UI (1)
TPPos4	Transmitter Output Pulse Position for bit 4 (5th bit) (Figure 15)	4 UI − 0.2	4	4 UI + 0.2	UI (1)

(1) A Unit Interval (UI) is defined as 1/7th of an ideal clock period (TCIP/7). E.g. For an 11.76ns clock period (85MHz), 1 UI = 1.68ns (Figure 13)

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Transmitter Switching Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter		Min	Typ	Max	Unit
TPPos3	Transmitter Output Pulse Position for bit 3 (6th bit) (Figure 15)		5 UI − 0.2	5	5 UI + 0.2	UI (1)
TPPos2	Transmitter Output Pulse Position for bit 2 (7th bit) (Figure 15)		6 UI − 0.2	6	6 UI + 0.2	UI (1)
TSTC	Required TxIN Setup to TCLK IN (Figure 9) Register addr 26d/19h bit [2:0] = 000b (Default)		1.5	0.69		ns
THTC	Required TxIN Hold to TCLK IN (Figure 9) Register addr 26d/19h bit [2:0] = 000b (Default)		1.5	0.70		ns
TSTC/THTC Programmable adjustment	Register addr 26d/19h bit [2:0] = 001b (Figure 14) Decrease TSTC ~400ps from Default; Increase THTC ~400ps from Default			0.5/ 1.0		ns
	Register addr 26d/19h bit [2:0] = 010b, Decrease TSTC ~800ps from default; Increase THTC ~800ps from Default			0/ 1.5		ns
	Register addr 26d/19h bit [2:0] = 011b, Decrease TSTC ~1200ps from Default; Increase THTC ~1200ps from Default			-0.5/ 2.0		ns
	Register addr 26d/19h bit [2:0] = 111b, Increase TSTC ~800ps from Default; Decrease THTC ~800ps from Default			1.5/ 0		ns
	Register addr 26d/19h bit [2:0] = 110b, Increase TSTC ~600ps from Default; Decrease THTC ~600ps from Default			1.4/ 0		ns
	Register addr 26d/19h bit [2:0] = 101b, Increase TSTC ~400ps from Default; Decrease THTC ~400ps from Default			1.1/ 0.3		ns
	Register addr 26d/19h bit [2:0] = 100b, Increase TSTC ~200ps from Default; Decrease THTC ~200ps from Default			0.9/ 0.5		ns
TCCD	Transmitter TCLKIN (LVTTL) to CLKOUT (LVDS) Latency (Figure 9) (2)	f = 135 MHz	10		20	ns
		f = 85 MHz (3)	20		30	ns
		f = 65 MHz (3)	25		40	ns
		f = 40 MHz (3)	40		50	ns
		f = 25 MHz (3)	60		70	ns
		f = 8 MHz	180		200	ns
TPPLS	Transmitter Phase Lock Loop Set (Figure 10)				10	ms
TPDD	Transmitter Powerdown Delay (Figure 11)				100	ns

(2) The typical transmitter TCCD latency is: 1.786*T + 4.19 ns – 2 UI, where T = TCLK IN period.
(3) Specification is ensured by characterization.

Two-Wire Serial Communication Interface

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SC}	S2CLK Clock Frequency				400	kHz
SC:LOW	Clock Low Period	R_P = 4.7KΩ, C_L = 50pF	1.5			us
SC:HIGH	Clock High Period	R_P = 4.7KΩ, C_L = 50pF	0.6			us
SCD:TR	S2CLK and S2DAT Rise Time	R_P = 4.7KΩ, C_L = 50pF			0.3	us
SCD:TF	S2CLK and S2DAT Fall Time	R_P = 4.7KΩ, C_L = 50pF			0.3	us
SU:STA	Start Condition Setup Time	R_P = 4.7KΩ, C_L = 50pF	0.6			us
HD:STA	Start Condition Hold Time	R_P = 4.7KΩ, C_L = 50pF	0.6			us
HD:STO	Stop Condition Hold Time	R_P = 4.7KΩ, C_L = 50pF	0.6			us
SC:SD	Clock Falling Edge to Data	R_P = 4.7KΩ, C_L = 50pF	0			us
SD:SC	Data to Clock Rising Edge	R_P = 4.7KΩ, C_L = 50pF	0.1			us
SCL:SD	S2CLK Low to S2DAT Data Valid	R_P = 4.7KΩ, C_L = 50pF	0.1		0.9	us

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Two-Wire Serial Communication Interface (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
BUF	Bus Free Time	R_P = 4.7KΩ, C_L = 50pF	13			us

AC Timing Diagrams

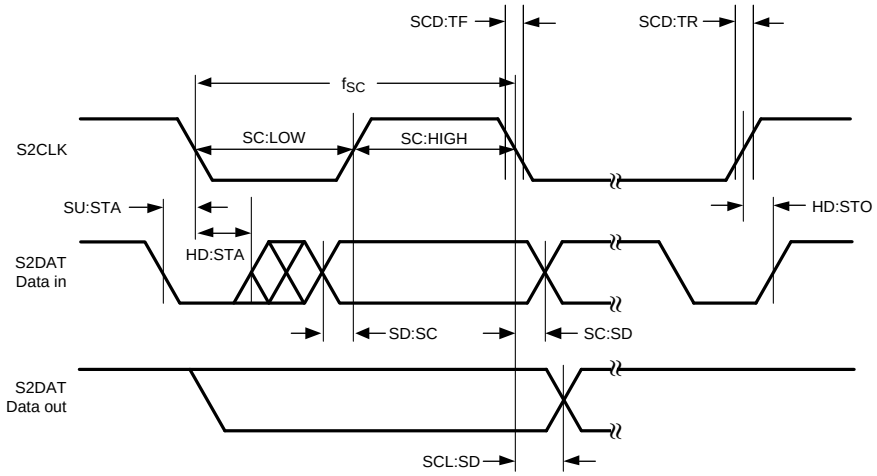


Figure 3. Two-Wire Serial Communication Interface Timing Diagram

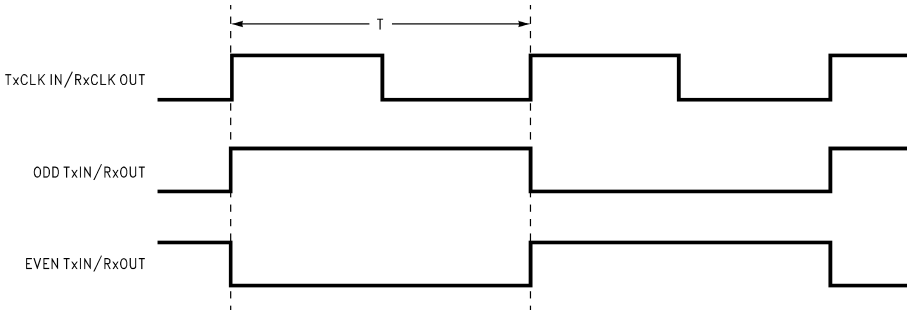


Figure 4. "Worst Case" Test Pattern

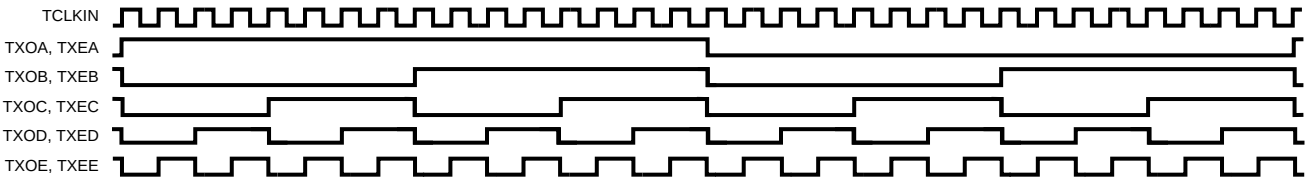


Figure 5. Incremental Test Pattern

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AC Timing Diagrams (continued)

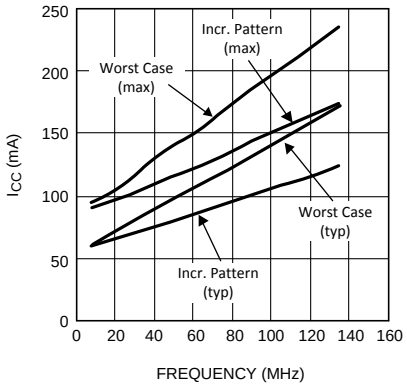


Figure 6. Typical and Max ICC with Worst Case and Incremental Test Pattern

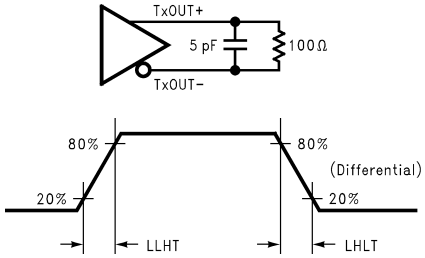


Figure 7. LVDS Transition Times

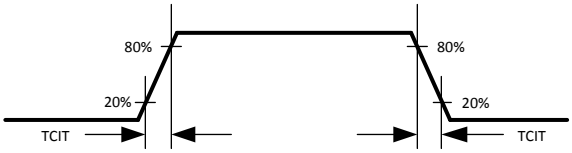


Figure 8. Input Clock Transition Time

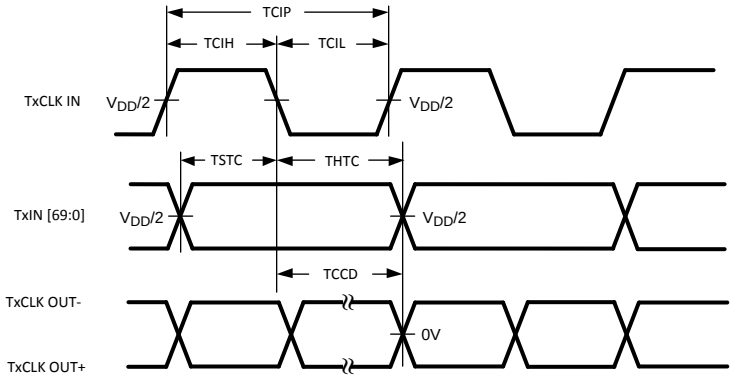


Figure 9. Input Setup/Hold Time, High/Low Time, and Clock In to Clock Out Latency

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AC Timing Diagrams (continued)

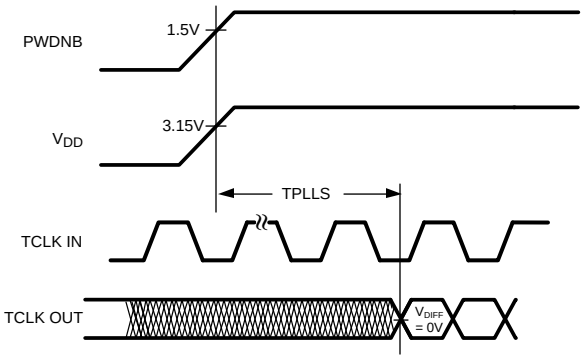


Figure 10. Phase Lock Loop Set Time

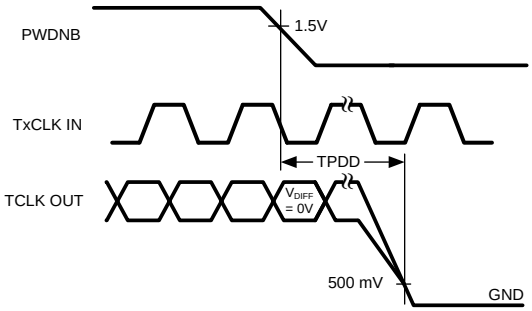


Figure 11. Transmitter Powerdown Delay

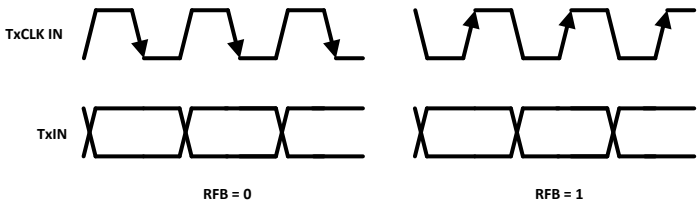


Figure 12. LVTLL Input Programmable Strobe Select

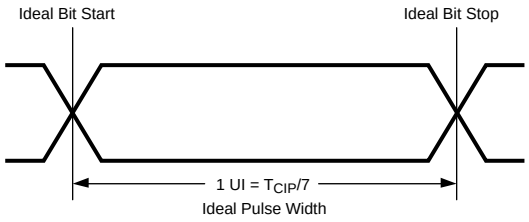


Figure 13. Serializer Ideal Pulse Width

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AC Timing Diagrams (continued)

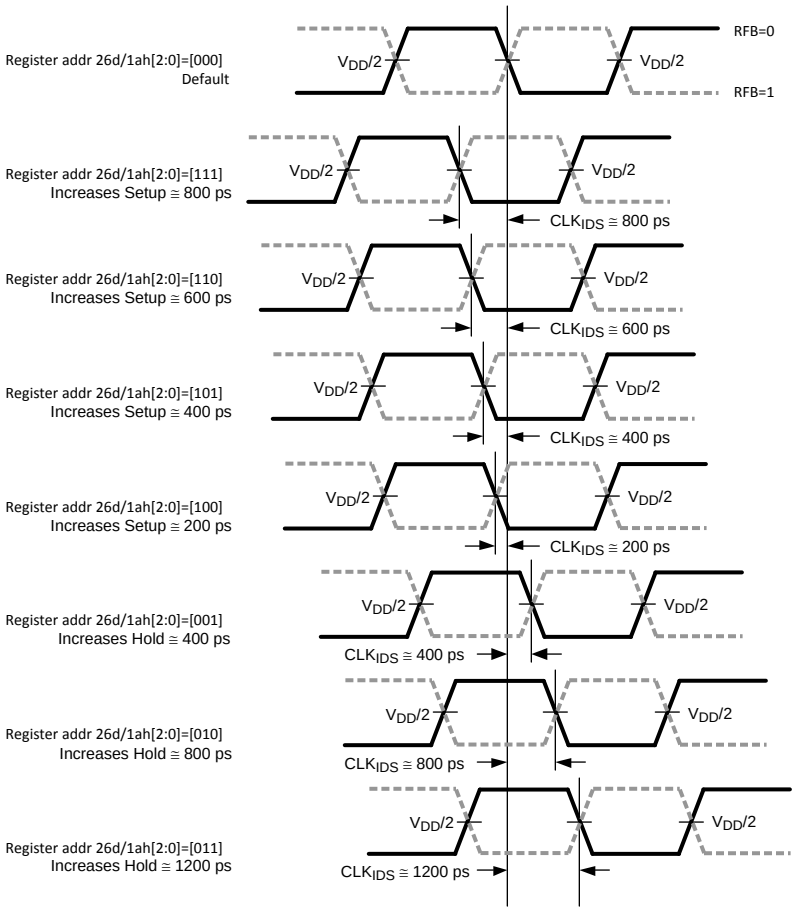


Figure 14. User Programmable Internal Clock Delay Adjustment for Input Data Setup/Hold Optimization Input Data Sampling Clock ($TCLK_{IDS}$)

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AC Timing Diagrams (continued)

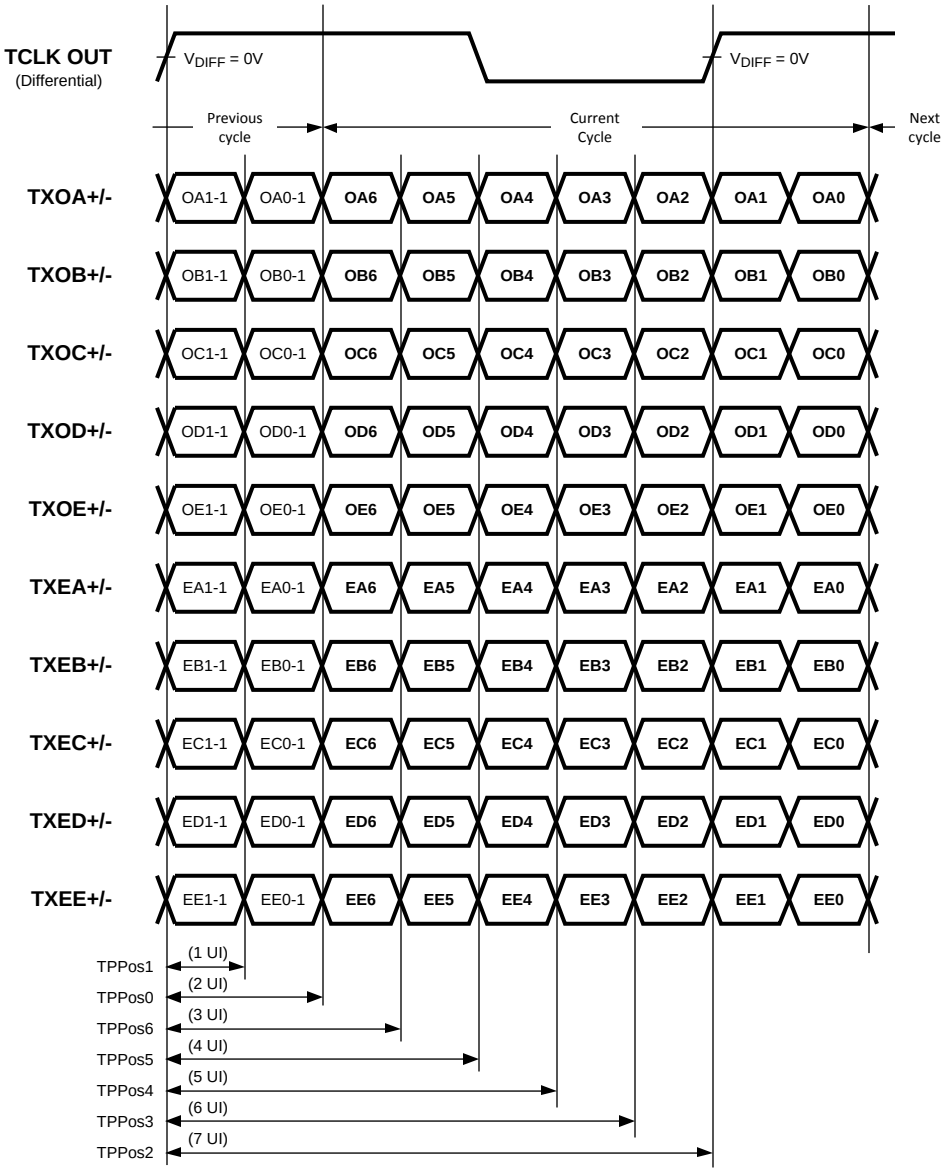


Figure 15. LVDS Input Mapping and Ideal Transmitter Pulse Position

PIN ASSIGNMENTS

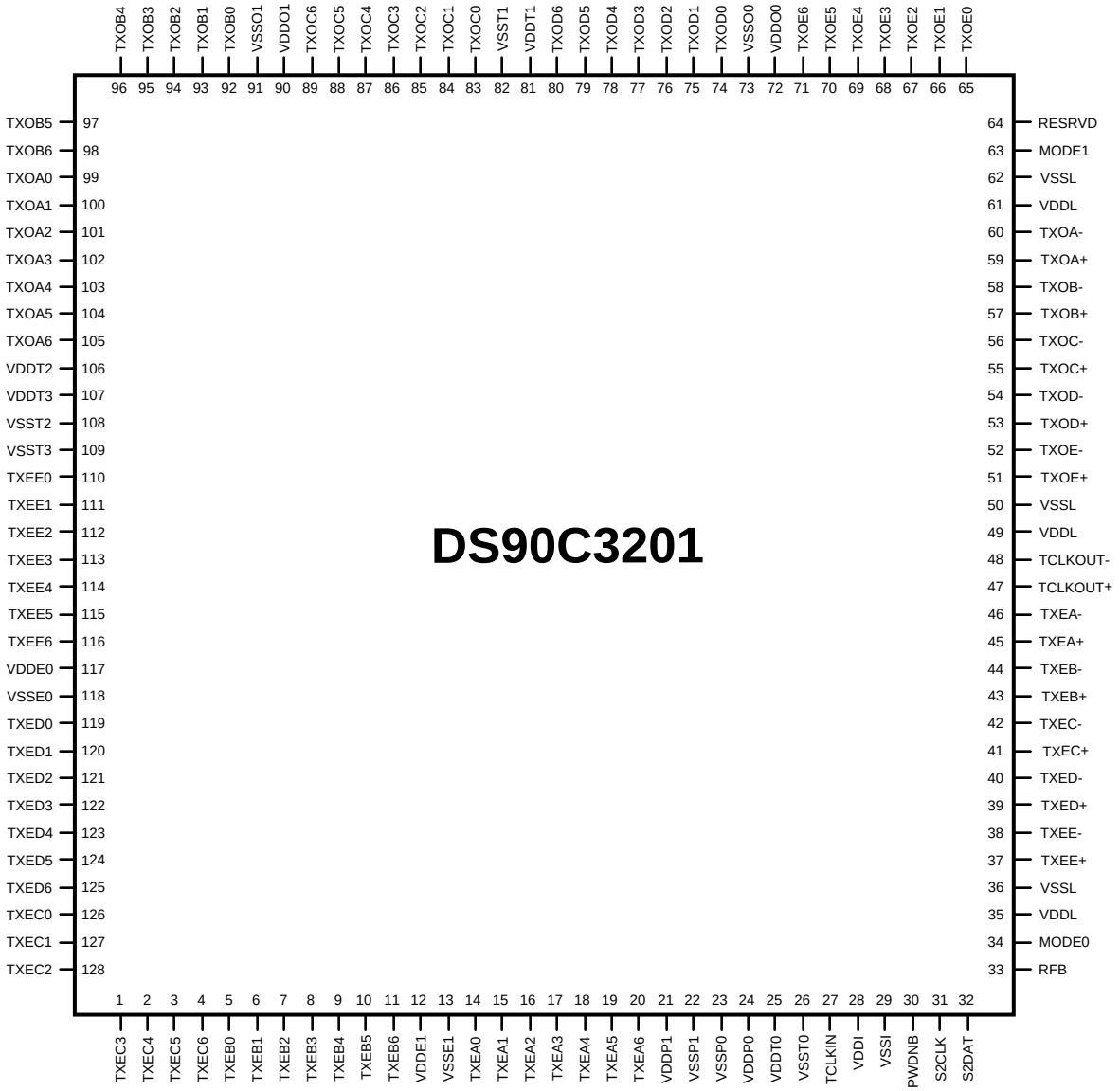


Figure 16. DS90C3201 Transmitter

DS90C3201 PIN DESCRIPTIONS

Pin No.	Pin Name	I/O	Pin Type	Description
1	TXEC3	I/P	LVTTL I/P (pulldown)	LVTTL level data input
2	TXEC4	I/P	LVTTL I/P (pulldown)	LVTTL level data input
3	TXEC5	I/P	LVTTL I/P (pulldown)	LVTTL level data input
4	TXEC6	I/P	LVTTL I/P (pulldown)	LVTTL level data input
5	TXEB0	I/P	LVTTL I/P (pulldown)	LVTTL level data input
6	TXEB1	I/P	LVTTL I/P (pulldown)	LVTTL level data input
7	TXEB2	I/P	LVTTL I/P (pulldown)	LVTTL level data input
8	TXEB3	I/P	LVTTL I/P (pulldown)	LVTTL level data input
9	TXEB4	I/P	LVTTL I/P (pulldown)	LVTTL level data input
10	TXEB5	I/P	LVTTL I/P (pulldown)	LVTTL level data input

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DS90C3201 PIN DESCRIPTIONS (continued)

Pin No.	Pin Name	I/O	Pin Type	Description
11	TXEB6	I/P	LVTTL I/P (pulldown)	LVTTL level data input
12	VDDE1	VDD	DIGITAL	Power supply for digital circuitry
13	VSSE1	GND	DIGITAL	Ground pin for digital circuitry
14	TXEA0	I/P	LVTTL I/P (pulldown)	LVTTL level data input
15	TXEA1	I/P	LVTTL I/P (pulldown)	LVTTL level data input
16	TXEA2	I/P	LVTTL I/P (pulldown)	LVTTL level data input
17	TXEA3	I/P	LVTTL I/P (pulldown)	LVTTL level data input
18	TXEA4	I/P	LVTTL I/P (pulldown)	LVTTL level data input
19	TXEA5	I/P	LVTTL I/P (pulldown)	LVTTL level data input
20	TXEA6	I/P	LVTTL I/P (pulldown)	LVTTL level data input
21	VDDP1	VDD	PLL	Power supply for PLL circuitry
22	VSSP1	GND	PLL	Ground pin for PLL circuitry
23	VSSP0	GND	PLL	Ground pin for PLL circuitry
24	VDDP0	VDD	PLL	Power supply for PLL circuitry
25	VDDT0	VDD	TX LOGIC	Power supply for logic
26	VSST0	GND	TX LOGIC	Ground pin for logic
27	TCLKIN	I/P	LVTTL I/P (pulldown)	LVTTL level data clock input
28	VDDI	VDD	DIGITAL	Power supply for digital circuitry
29	VSSI	GND	DIGITAL	Ground pin for digital circuitry
30	PWDNB	I/P	LVTTL I/P (pulldown)	Powerdown Bar (Active LOW) 0 = DEVICE DISABLED 1 = DEVICE ENABLED
31	S2CLK	I/P	DIGITAL	Two-wire Serial interface - clock
32	S2DAT	I/OP	DIGITAL	Two-wire Serial interface - data
33	RFB	VDD	LVTTL I/P (pulldown)	Rising Falling Bar (Figure 12) 0 = FALLING EDGE 1 = RISING EDGE
34	MODE0	I/P	LVTTL I/P (pulldown)	“EVEN” bank enable 0 = LVDS EVEN OUTPUTS DISABLED 1 = LVDS EVEN OUTPUTS ENABLED
35	VDDL	VDD	ANALOG	Power supply for analog circuitry
36	VSSL	GND	ANALOG	Ground pin for analog circuitry
37	TXEE+	O/P	LVDS O/P	Positive LVDS differential data output
38	TXEE -	O/P	LVDS O/P	Negative LVDS differential data output
39	TXED+	O/P	LVDS O/P	Positive LVDS differential data output
40	TXED -	O/P	LVDS O/P	Negative LVDS differential data output
41	TXEC+	O/P	LVDS O/P	Positive LVDS differential data output
42	TXEC -	O/P	LVDS O/P	Negative LVDS differential data output
43	TXEB+	O/P	LVDS O/P	Positive LVDS differential data output
44	TXEB -	O/P	LVDS O/P	Negative LVDS differential data output
45	TXEA+	O/P	LVDS O/P	Positive LVDS differential data output
46	TXEA -	O/P	LVDS O/P	Negative LVDS differential data output
47	TCLKOUT+	O/P	LVDS O/P	Positive LVDS differential data output
48	TCLKOUT -	O/P	LVDS O/P	Negative LVDS differential data output
49	VDDL	VDD	ANALOG	Power supply for analog circuitry
50	VSSL	GND	ANALOG	Ground pin for analog circuitry
51	TXOE+	O/P	LVDS O/P	Positive LVDS differential data output
52	TXOE -	O/P	LVDS O/P	Negative LVDS differential data output
53	TXOD+	O/P	LVDS O/P	Positive LVDS differential data output

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DS90C3201 PIN DESCRIPTIONS (continued)

Pin No.	Pin Name	I/O	Pin Type	Description
54	TXOD -	O/P	LVDS O/P	Negative LVDS differential data output
55	TXOC+	O/P	LVDS O/P	Positive LVDS differential data output
56	TXOC -	O/P	LVDS O/P	Negative LVDS differential data output
57	TXOB+	O/P	LVDS O/P	Positive LVDS differential data output
58	TXOB -	O/P	LVDS O/P	Negative LVDS differential data output
59	TXOA+	O/P	LVDS O/P	Positive LVDS differential data output
60	TXOA -	O/P	LVDS O/P	Negative LVDS differential data output
61	VDDL	VDD	ANALOG	Power supply for analog circuitry
62	VSSL	GND	ANALOG	Ground pin for analog circuitry
63	MODE1	I/P	LVTTL I/P (pulldown)	“ODD” bank enable 0 = LVDS ODD OUTPUTS DISABLED 1 = LVDS ODD OUTPUTS ENABLED
64	RESRVD	I/P	LVTTL I/P (pulldown)	Tie to VSS for correct functionality
65	TXOE0	I/P	LVTTL I/P (pulldown)	LVTTL level data input
66	TXOE1	I/P	LVTTL I/P (pulldown)	LVTTL level data input
67	TXOE2	I/P	LVTTL I/P (pulldown)	LVTTL level data input
68	TXOE3	I/P	LVTTL I/P (pulldown)	LVTTL level data input
69	TXOE4	I/P	LVTTL I/P (pulldown)	LVTTL level data input
70	TXOE5	I/P	LVTTL I/P (pulldown)	LVTTL level data input
71	TXOE6	I/P	LVTTL I/P (pulldown)	LVTTL level data input
72	VDDO0	VDD	DIGITAL	Power supply for digital circuitry
73	VSSO0	GND	DIGITAL	Ground pin for digital circuitry
74	TXOD0	I/P	LVTTL I/P (pulldown)	LVTTL level data input
75	TXOD1	I/P	LVTTL I/P (pulldown)	LVTTL level data input
76	TXOD2	I/P	LVTTL I/P (pulldown)	LVTTL level data input
77	TXOD3	I/P	LVTTL I/P (pulldown)	LVTTL level data input
78	TXOD4	I/P	LVTTL I/P (pulldown)	LVTTL level data input
79	TXOD5	I/P	LVTTL I/P (pulldown)	LVTTL level data input
80	TXOD6	I/P	LVTTL I/P (pulldown)	LVTTL level data input
81	VDDT1	VDD	TX LOGIC	Power supply for logic
82	VSST1	GND	TX LOGIC	Ground pin for logic
83	TXOC0	I/P	LVTTL I/P (pulldown)	LVTTL level data input
84	TXOC1	I/P	LVTTL I/P (pulldown)	LVTTL level data input
85	TXOC2	I/P	LVTTL I/P (pulldown)	LVTTL level data input
86	TXOC3	I/P	LVTTL I/P (pulldown)	LVTTL level data input
87	TXOC4	I/P	LVTTL I/P (pulldown)	LVTTL level data input
88	TXOC5	I/P	LVTTL I/P (pulldown)	LVTTL level data input
89	TXOC6	I/P	LVTTL I/P (pulldown)	LVTTL level data input
90	VDDO1	VDD	DIGITAL	Power supply for digital circuitry
91	VSSO1	GND	DIGITAL	Ground pin for digital circuitry
92	TXOB0	I/P	LVTTL I/P (pulldown)	LVTTL level data input
93	TXOB1	I/P	LVTTL I/P (pulldown)	LVTTL level data input
94	TXOB2	I/P	LVTTL I/P (pulldown)	LVTTL level data input
95	TXOB3	I/P	LVTTL I/P (pulldown)	LVTTL level data input
96	TXOB4	I/P	LVTTL I/P (pulldown)	LVTTL level data input
97	TXOB5	I/P	LVTTL I/P (pulldown)	LVTTL level data input
98	TXOB6	I/P	LVTTL I/P (pulldown)	LVTTL level data input
99	TXOA0	I/P	LVTTL I/P (pulldown)	LVTTL level data input

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DS90C3201 PIN DESCRIPTIONS (continued)

Pin No.	Pin Name	I/O	Pin Type	Description
100	TXOA1	I/P	LVTTL I/P (pulldown)	LVTTL level data input
101	TXOA2	I/P	LVTTL I/P (pulldown)	LVTTL level data input
102	TXOA3	I/P	LVTTL I/P (pulldown)	LVTTL level data input
103	TXOA4	I/P	LVTTL I/P (pulldown)	LVTTL level data input
104	TXOA5	I/P	LVTTL I/P (pulldown)	LVTTL level data input
105	TXOA6	I/P	LVTTL I/P (pulldown)	LVTTL level data input
106	VDDT2	VDD	TX LOGIC	Power supply for logic
107	VDDT3	VDD	TX LOGIC	Power supply for logic
108	VSST2	GND	TX LOGIC	Ground pin for logic
109	VSST3	GND	TX LOGIC	Ground pin for logic
110	TXEE0	I/P	LVTTL I/P (pulldown)	LVTTL level data input
111	TXEE1	I/P	LVTTL I/P (pulldown)	LVTTL level data input
112	TXEE2	I/P	LVTTL I/P (pulldown)	LVTTL level data input
113	TXEE3	I/P	LVTTL I/P (pulldown)	LVTTL level data input
114	TXEE4	I/P	LVTTL I/P (pulldown)	LVTTL level data input
115	TXEE5	I/P	LVTTL I/P (pulldown)	LVTTL level data input
116	TXEE6	I/P	LVTTL I/P (pulldown)	LVTTL level data input
117	VDDE0	VDD	DIGITAL	Power supply for digital circuitry
118	VSSE0	GND	DIGITAL	Ground pin for digital circuitry
119	TXED0	I/P	LVTTL I/P (pulldown)	LVTTL level data input
120	TXED1	I/P	LVTTL I/P (pulldown)	LVTTL level data input
121	TXED2	I/P	LVTTL I/P (pulldown)	LVTTL level data input
122	TXED3	I/P	LVTTL I/P (pulldown)	LVTTL level data input
123	TXED4	I/P	LVTTL I/P (pulldown)	LVTTL level data input
124	TXED5	I/P	LVTTL I/P (pulldown)	LVTTL level data input
125	TXED6	I/P	LVTTL I/P (pulldown)	LVTTL level data input
126	TXEC0	I/P	LVTTL I/P (pulldown)	LVTTL level data input
127	TXEC1	I/P	LVTTL I/P (pulldown)	LVTTL level data input
128	TXEC2	I/P	LVTTL I/P (pulldown)	LVTTL level data input

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APPLICATION INFORMATION

Two-Wire Serial Communication Interface Description

The DS90C3201 operates as a slave on the Serial Bus, so the S2CLK line is an input (no clock is generated by the DS90C3201) and the S2DAT line is bi-directional. DS90C3201 has a fixed 7bit slave address. The address is not user configurable in anyway.

A zero in front of the register address is required. For example, to access register 0x0Fh, “0F” is the correct way of accessing the register.

COMMUNICATING WITH THE DS90C3201 CONTROL REGISTERS

There are 32 data registers (one byte each) in the DS90C3201, and can be accessed through 32 addresses. All registers are predefined as read only or read and write. The DS90C3201 slave state machine does not require an internal clock and it supports only byte read and write. Page mode is not supported. The 7-bit binary address is 0111111 All seven bits are hardwired internally.

Reading the DS90C3201 can take place either of three ways:

1. If the location latched in the data register addresses is correct, then the read can simply consist of a slave address byte, followed by retrieving the data byte.
2. If the data register address needs to be set, then a slave address byte, data register address will be sent first, then the master will repeat start, send the slave address byte and data byte to accomplish a read.
3. When performing continuous read operations, another write (or read) instruction in between reads needs to be completed in order for the two-wire serial interface module to read repeatedly.

The data byte has the most significant bit first. At the end of a read, the DS90C3201 can accept either Acknowledge or No Acknowledge from the Master (No Acknowledge is typically used as a signal for the slave that the Master has read its last byte).

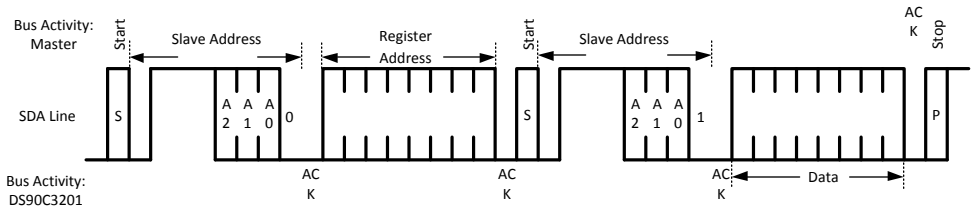


Figure 17. Byte Read

The master must generate a Start by sending the 7-bit slave address plus a 0 first, and wait for acknowledge from DS90C3201. When DS90C3201 acknowledges (the 1st ACK) that the master is calling, the master then sends the data register address byte and waits for acknowledge from the slave. When the slave acknowledges (the 2nd ACK), the master repeats the “Start” by sending the 7-bit slave address plus a 1 (indicating that READ operation is in progress) and waits for acknowledge from DS90C3201. After the slave responds (the 3rd ACK), the slave sends the data to the bus and waits for acknowledge from the master. When the master acknowledges (the 4th ACK), it generates a “Stop”. This completes the “ READ”.

A **Write** to the DS90C3201 will always include the slave address, data register address byte, and a data byte.

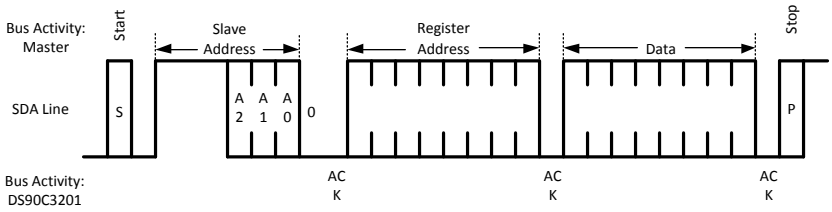


Figure 18. Byte Write

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The master must generate a “Start” by sending the 7-bit slave address plus a 0 and wait for acknowledge from DS90C3201. When DS90C3201 acknowledges (the 1st ACK) that the master is calling, the master then sends the data register address byte and waits for acknowledge from the slave. When the slave acknowledges (the 2nd ACK), the master sends the data byte and wait for acknowledge from the slave. When the slave acknowledges (the 3rd ACK), the master generates a “ Stop”. This completes the “WRITE”.

DS90C3201 Two-Wire Serial Interface Register Table

Table 1. DS90C3201 Two-Wire Serial Interface Register Table

Address	R/W	RESET	Bit #	Description	Default Value
0d/0h	R	PWDN	[7:0]	Vender ID low byte[7:0] = 05h	0000_0101
1d/1h	R	PWDN	[7:0]	Vender ID high byte[15:8] =13h	0001_0011
2d/2h	R	PWDN	[7:0]	Device ID low byte[7:0] = 27h	0010_0111
3d/3h	R	PWDN	[7:0]	Device ID high byte 15:8] = 67h	0110_0111
4d/4h	R	PWDN	[7:0]	Device revision [7:0] = 00h to begin with	0000_0000
5d/5h	R	PWDN	[7:0]	Low frequency limit, 8Mhz = 8h	0000_1000
6d/6h	R	PWDN	[7:0]	High frequency limit 135Mhz = 87h = 0000_0000_1000_0111	1000_0111
7d/7h	R	PWDN	[7:0]	Reserved	0000_0000
8d/8h	R	PWDN	[7:0]	Reserved	0000_0000
9d/9h	R	PWDN	[7:0]	Reserved	0000_0000
10d/ah	R	PWDN	[7:0]	Reserved	0000_0000
11d/bh	R	PWDN	[7:0]	Reserved	0000_0000
20d/14h	R/W	PWDN	[7:0]	Reserved	0000_0000
21d/15h	R/W	PWDN	[7:0]	Reserved	0000_0000
22d/16h	R/W	PWDN	[7:0]	Reserved	0000_0000
23d/17h	R/W	PWDN	[7:0]	Reserved	0000_0000
24d/18h	R/W	PWDN	[7:0]	Reserved	0000_0000
25d/19h	R/W	PWDN	[7:0]	Reserved	0000_0000
26d/1ah	R/W	PWDN	[7:3]	Reserved	0000_0000
			[2:0]	LVTTL input delay control for TCLK channel, 000 is Default which means no delays add to TCLK, two buffer delay per step adjustment for Tsetup; while single buffer step adjustment for Thold	
				[111]: move internal clock early by 4 buffer delays (increases setup time)	
				[110]: move internal clock early by 3 buffer delays (increases setup time)	
				[101]: move internal clock early by 2 buffer delays (increases setup time)	
				[100]: move internal clock early by 1 buffer delays (increases setup time)	
				[001]: move internal clock late by 2 buffer delays (increases hold time)	
				[010]: move internal clock late by 4 buffer delays (increases hold time)	
				[011]: move internal clock late by 6 buffer delays (increases hold time)	
				[000]: Default	
27d/1bh	R/W	PWDN	[7:0]	Reserved	0000_0000

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Table 1. DS90C3201 Two-Wire Serial Interface Register Table (continued)

Address	R/W	RESET	Bit #	Description	Default Value
28d/1ch	R/W	PWDN	[7]	Vod adjustment for TCLK channel 0: TCLK Vod is the same as TXE EVEN BANK (Default) 1: TCLK Vod is the same as TXO ODD BANK	0000_0000
			[6]	Vos adjustment for TCLK channel 0: TCLK Vos is the same as TXE EVEN BANK (Default) 1: TCLK Vos is the same as TXO ODD BANK	
			[5]	Vod adjustment for TXE EVEN BANK 0: Vod set at 400mV (Default) 1: Vod set at 250mv	
			[4]	Vod adjustment for TXO ODD BANK 0: Vod set at 400mV (Default) 1: Vod set at 250mv	
			[3:2]	Vos adjustment for TXE EVEN BANK 11: NA 10: LVDS DR O/P Vos set at 0.8V 01: LVDS DR O/P Vos set at 1.0V 00: LVDS DR O/P Vos set at 1.2V (Default)	
			[1:0]	Vos adjustment for TXO ODD BANK 11: NA 10: LVDS DR O/P Vos set at 0.8V 01: LVDS DR O/P Vos set at 1.0V 00: LVDS DR O/P Vos set at 1.2V (Default)	
29d/1dh	R/W	PWDN	[7:5]	Reserved	0000_0000
			[4]	I/O disable control for TXE EVEN BANK channel E, 1: Disable, 0: Enable (Default)	
			[3]	I/O disable control for TXE EVEN BANK channel D, 1: Disable, 0: Enable (Default)	
			[2]	I/O disable control for TXE EVEN BANK channel C, 1: Disable, 0: Enable (Default)	
			[1]	I/O disable control for TXE EVEN BANK channel B, 1: Disable, 0: Enable (Default)	
			[0]	I/O disable control for TXE EVEN BANK channel A, 1: Disable, 0: Enable (Default)	
30d/1eh	R/W	PWDN	[7:5]	Reserved	0000_0000
			[4]	I/O disable control for TXO ODD BANK channel E, 1: Disable, 0: Enable (Default)	
			[3]	I/O disable control for TXO ODD BANK channel D, 1: Disable, 0: Enable (Default)	
			[2]	I/O disable control for TXO ODD BANK channel C, 1: Disable, 0: Enable (Default)	
			[1]	I/O disable control for TXO ODD BANK channel B, 1 Disable, 0: Enable (Default)	
			[0]	I/O disable control for TXO ODD BANK channel A, 1: Disable, 0: Enable (Default)	
31d/1fh	R/W	PWDN	[7:6]	11: LVDS O/Ps available as long as "NO CLK" is at HIGH regardless PLL lock or not	0000_0000
				10: LVDS O/Ps available after 1K of TCLK cycles detected & PLL generated strobes are within 0.5UI respect to REFCLK	
				01: LVDS O/Ps available after 2K of TCLK cycles detected	
				00: Default ; LVDS O/Ps available after 1K of TCLK cycles detected	
			[5]	0: Default; to select the size of wait counter between 1K or 2K, Default is 1K	
			[0:4]	Reserved	

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REVISION HISTORY

Changes from Revision C (April 2013) to Revision D	Page
• Changed layout of National Data Sheet to TI format	18

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
DS90C3201VS/NOPB	ACTIVE	TQFP	PDT	128	90	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	0 to 70	DS90C3201VS	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

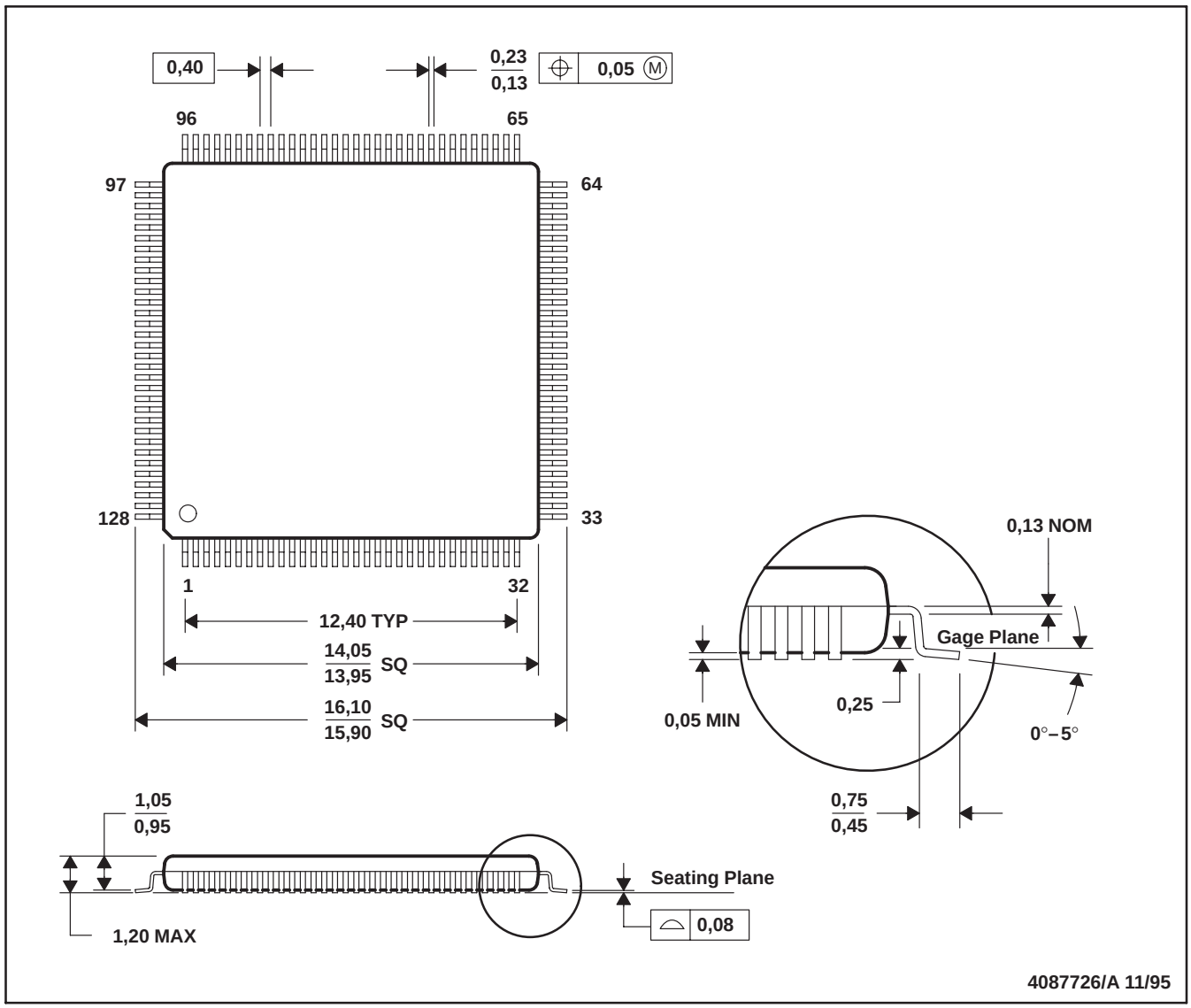
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.

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