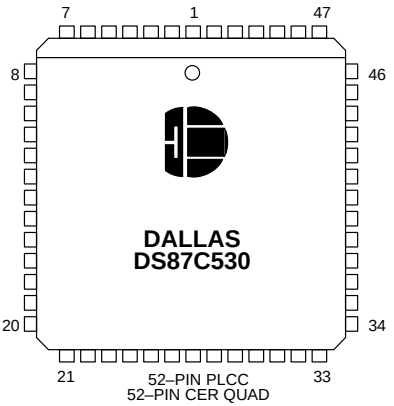
DALLAS SEMICONDUCTOR

DS87C530
EPROM Micro with Real Time Clock

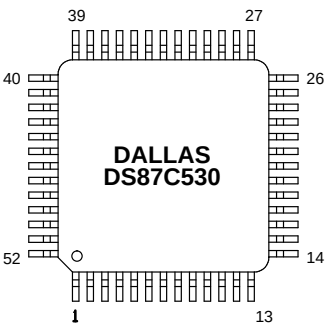
FEATURES

- 80C52 Compatible
  - 8051 Instruction set
  - Four 8–bit I/O ports
  - Three 16–bit timer/counters
  - 256 bytes scratchpad RAM
- Large On–chip Memory
  - 16KB EPROM (OTP)
  - 1KB extra on–chip SRAM for MOVX
- **ROMSIZE™ Feature**
  - Selects effective on–chip ROM size from 0 to 16KB
  - Allows access to entire external memory map
  - Dynamically adjustable by software
  - Useful as boot block for external Flash
- Nonvolatile Functions
  - **On–chip Real Time Clock w/ Alarm Interrupt**
  - **Battery backup support of 1KB SRAM**
- High–Speed Architecture
  - 4 clocks/machine cycle (8051 = 12)
  - Runs DC to 33 MHz clock rates
  - Single–cycle instruction in 121 ns
  - Dual data pointer
  - Optional variable length MOVX to access fast/slow RAM /peripherals
- Power Management Mode
  - Programmable clock source saves power
  - Runs from (crystal/64) or (crystal/1024)
  - Provides automatic hardware and software exit
- EMI Reduction Mode disables ALE
- High integration controller includes:
  - Power–fail reset
  - Early–warning power–fail interrupt
  - Programmable Watchdog timer
- Two full–duplex hardware serial ports
- 14 total interrupt sources with 6 external

PACKAGE OUTLINE



52–PIN PLCC
52–PIN CER QUAD



52–PIN TQFP OUTLINE

DESCRIPTION

The DS87C530 is an 8051 compatible microcontroller based on the Dallas High Speed core. It uses four clocks per instruction cycle instead of 12 used by the standard 8051. It also provides a unique mix of peripherals not widely available on other processors. They include an on–chip Real Time Clock (RTC) and battery back up support for an on–chip 1K x 8 SRAM. The new Power Management Mode allows software to select reduced power operation while still processing.

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A combination of high performance microcontroller core, real time clock, battery backed SRAM, and power management makes the DS87C530 ideal for instruments and portable applications. It also provides several peripherals found on other Dallas High–Speed Microcontrollers. These include two independent serial ports, two data pointers, on–chip power monitor with brown–out detection and a watchdog timer.

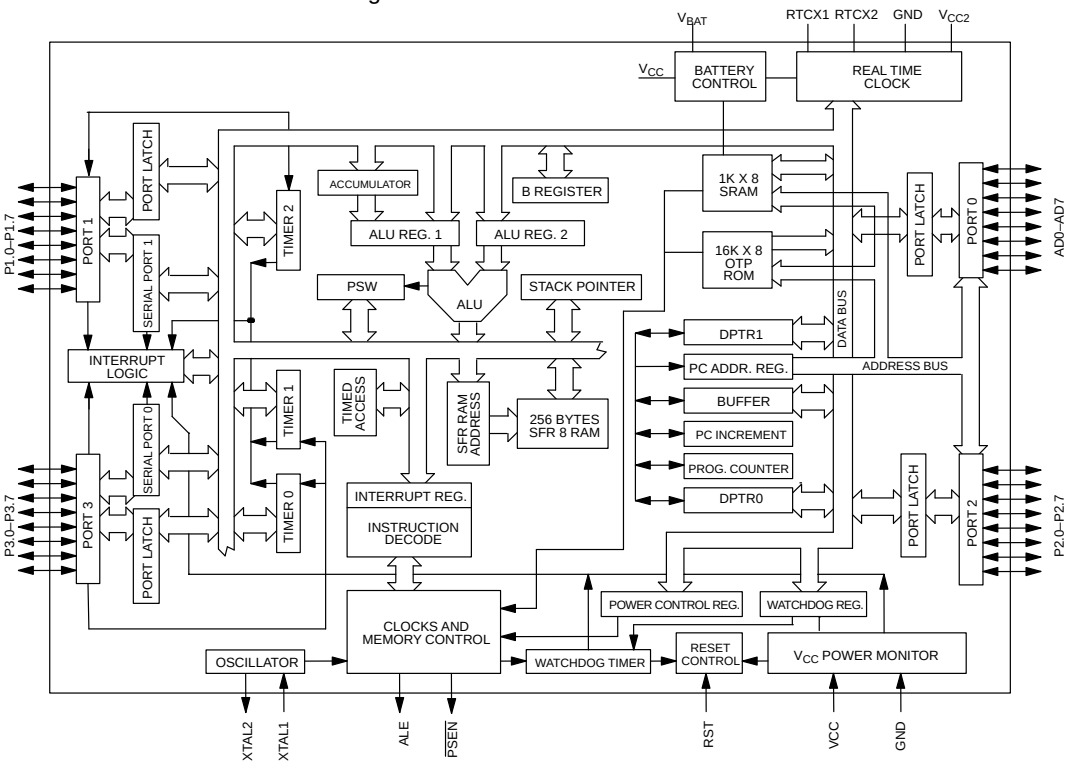
Power Management Mode (PMM) allows software to select a slower CPU clock. While default operation uses four clocks per machine cycle, the PMM runs the processor at 64 or 1024 clocks per cycle. There is a corresponding drop in power consumption when the processor slows.

Note: The DS87C530 is a monolithic device. A user must supply an external battery or super–cap and a 32.768 KHz timekeeping crystal to have permanently powered timekeeping or nonvolatile RAM. The DS87C530 provides all the support and switching circuitry needed to manage these resources.

ORDERING INFORMATION

PART NUMBER	PACKAGE	MAX. CLOCK SPEED	TEMPERATURE RANGE
DS87C530–QCL	52–pin PLCC	33 MHz	0°C to 70°C
DS87C530–QNL	52–pin PLCC	33 MHz	–40°C to +85°C
DS87C530–KCL	52–pin windowed CERQUAD	33 MHz	0°C to 70°C
DS87C530–ECL	52–PIN TQFP	33 MHz	0°C to 70°C
DS87C530–ENL	52–PIN TQFP	33 MHz	–40°C to +85°C

DS87C530 BLOCK DIAGRAM Figure 1



PIN DESCRIPTION Table 1

PLCC	TQFP	SIGNAL NAME	DESCRIPTION
52	45	V_{CC}	**V_{CC} – +5V**. Processor power supply.
1,25	18, 46	GND	**GND** – Processor digital circuit ground.
29	22	V_{CC2}	**V_{CC2}** – +5V Real Time Clock supply.
26	19	GND2	**GND2** – Real Time Clock circuit ground.
12	5	RST	**RST – Input**. The RST input pin contains a Schmitt voltage input to recognize external active high Reset inputs. The pin also employs an internal pull–down resistor to allow for a combination of wired OR external Reset sources. An RC is not required for power–up, as the DS87C530 provides this function internally.
23 24	16 17	XTAL2 XTAL1	**XTAL1, XTAL2** – The crystal oscillator pins XTAL1 and XTAL2 provide support for parallel resonant, AT cut crystals. XTAL1 acts also as an input if there is an external clock source in place of a crystal. XTAL2 serves as the output of the crystal amplifier.
38	31	PSEN	**$\overline{\text{PSEN}}$ – Output**. The Program Store Enable output. This signal is commonly connected to optional external ROM memory as a chip enable. $\overline{\text{PSEN}}$ will provide an active low pulse and is driven high when external ROM is not being accessed.
39	32	ALE	**ALE – Output**. The Address Latch Enable output functions as a clock to latch the external address LSB from the multiplexed address/data bus on Port 0. This signal is commonly connected to the latch enable of an external 373 family transparent latch. ALE has a pulse width of 1.5 XTAL1 cycles and a period of four XTAL1 cycles. ALE is forced high when the DS87C530 is in a Reset condition. ALE can be disabled by writing ALEOFF=1 (PMR.Z). When ALEOFF=1, ALE is forced high. ALE operates independently of ALEOFF during external memory accesses.
50 49 48 47 46 45 44 43	43 42 41 40 39 38 37 36	P0.0 (AD0) P0.1 (AD1) P0.2 (AD2) P0.3 (AD3) P0.4 (AD4) P0.5 (AD5) P0.6 (AD6) P0.7 (AD7)	**Port 0 (AD0–7) – I/O**. Port 0 is an open–drain 8–bit bi–directional I/O port. As an alternate function Port 0 can function as the multiplexed address/data bus to access off–chip memory. During the time when ALE is high, the LSB of a memory address is presented. When ALE falls to a logic 0, the port transitions to a bi–directional data bus. This bus is used to read external ROM and read/write external RAM memory or peripherals. When used as a memory bus, the port provides active high drivers. The reset condition of Port 0 is tri–state. Pull–up resistors are required when using Port 0 as an I/O port.
3–10	48–52, 1–3	P1.0 – P1.7	**Port 1 – I/O**. Port 1 functions as both an 8–bit bi–directional I/O port and an alternate functional interface for Timer 2 I/O, new External Interrupts, and new Serial Port 1. The reset condition of Port 1 is with all bits at a logic 1. In this state, a weak pull–up holds the port high. This condition also serves as an input mode, since any external circuit that writes to the port will overcome the weak pull–up. When software writes a 0 to any port pin, the DS87C530 will activate a strong pull–down that remains on until either a 1 is written or a reset occurs. Writing a 1 after the port has been at 0 will cause a strong transition driver to turn on, followed by a weaker sustaining pull–up. Once the momentary strong driver turns off, the port again becomes the output high (and input) state. The alternate modes of Port 1 are outlined as follows.

PLCC	TQFP	SIGNAL NAME	DESCRIPTION
			Port **Alternate** **Function**
3	48		P1.0 T2 External I/O for Timer/Counter 2
4	49		P1.1 T2EX Timer/Counter 2 Capture/Reload Trigger
5	50		P1.2 RXD1 Serial Port 1 Input
6	51		P1.3 TXD1 Serial Port 1 Output
7	52		P1.4 $\overline{INT2}$ External Interrupt 2 (Positive Edge Detect)
8	1		P1.5 $\overline{INT3}$ External Interrupt 3 (Negative Edge Detect)
9	2		P1.6 $\overline{INT4}$ External Interrupt 4 (Postive Edge Detect)
10	3		P1.7 $\overline{INT5}$ External Interrupt 5 (Negative Edge Detect)
30 31 32 33 34 35 36 37	23 24 25 26 27 28 29 30	P2.0 (AD8) P2.1 (AD9) P2.2 (AD10) P2.3 (AD11) P2.4 (AD12) P2.5 (AD13) P2.6 (AD14) P2.7 (AD15)	**Port 2 (A8–15) – I/O**. Port 2 is a bi–directional I/O port. The reset condition of Port 2 is logic high. In this state, a weak pull–up holds the port high. This condition also serves as an input mode, since any external circuit that writes to the port will overcome the weak pull–up. When software writes a 0 to any port pin, the DS87C530 will activate a strong pull–down that remains on until either a 1 is written or a reset occurs. Writing a 1 after the port has been at 0 will cause a strong transition driver to turn on, followed by a weaker sustaining pull–up. Once the momentary strong driver turns off, the port again becomes both the output high and input state. As an alternate function Port 2 can function as MSB of the external address bus. This bus can be used to read external ROM and read/write external RAM memory or peripherals.
15–22	8–15	P3.0 – P3.7	**Port 3 – I/O.** Port 3 functions as both an 8–bit bi–directional I/O port and an alternate functional interface for External Interrupts, Serial Port 0, Timer 0 and 1 Inputs, and $\overline{RD}$ and $\overline{WR}$ strobes. The reset condition of Port 3 is with all bits at a logic 1. In this state, a weak pull–up holds the port high. This condition also serves as an input mode, since any external circuit that writes to the port will overcome the weak pull–up. When software writes a 0 to any port pin, the DS87C530 will activate a strong pull–down that remains on until either a 1 is written or a reset occurs. Writing a 1 after the port has been at 0 will cause a strong transition driver to turn on, followed by a weaker sustaining pull–up. Once the momentary strong driver turns off, the port again becomes both the output high and input state. The alternate modes of Port 3 are outlined below.
			Port **Alternate Mode**
15	8		P3.0 RXD0 Serial Port 0 Input
16	9		P3.1 TXD0 Serial Port 0 Output
17	10		P3.2 $\overline{INT0}$ External Interrupt 0
18	11		P3.3 $\overline{INT1}$ External Interrupt 1
19	12		P3.4 T0 Timer 0 External Input
20	13		P3.5 T1 Timer 1 External Input
21	14		P3.6 $\overline{WR}$ External Data Memory Write Strobe
22	15		P3.7 $\overline{RD}$ External Data Memory Read Strobe
42	35	$\overline{EA}$	**$\overline{EA}$ – Input.** Connect to ground to force the DS87C530 to use an external ROM. The internal RAM is still accessible as determined by register settings. Connect $\overline{EA}$ to V_{CC} to use internal ROM.
51	44	V_{BAT}	**V_{BAT} – Input.** Connect to the power source that maintains SRAM and RTC when $V_{CC} < V_{BAT}$. May be connected to a 3V lithium battery or a super–cap. See the electrical specifications for details.

PLCC	TQFP	SIGNAL NAME	DESCRIPTION
27, 28	20, 21	RTCX2, RTCX1	**RTCX2, RTCX1 – Timekeeping crystal**. Connect a 32.768 KHz crystal between RTCX2 and RTCX1 to supply the time–base for the real time clock. The DS87C530 supports both 6 pF and 12.5 pF load capacitance crystals as selected by an SFR bit described below. To prevent noise from affecting the RTC, the RTCX2 and RTCX1 pin should be guard–ringed with GND2.
2, 11, 13, 14, 40, 41	4, 6, 7, 33, 34, 47	NC	**NC – Reserved.** These pins should not be connected. They are reserved for use with future devices in the family.

COMPATIBILITY

The DS87C530 is a fully static CMOS 8051 compatible microcontroller designed for high performance. While remaining familiar to 8051 users, it has many new features. In general, software written for existing 8051 based systems works without modification on the DS87C530. The exception is critical timing since the High Speed Micro performs its instructions much faster than the original for any given crystal selection. The DS87C530 runs the standard 8051 instruction set. It is not pin compatible with other 8051s due to the time-keeping crystal.

The DS87C530 provides three 16–bit timer/counters, full–duplex serial port (2), 256 bytes of direct RAM plus 1KB of extra MOVX RAM. I/O ports have the same operation as a standard 8051 product. Timers will default to a 12 clock per cycle operation to keep their timing compatible with original 8051 systems. However, timers are individually programmable to run at the new 4 clocks per cycle if desired. The PCA is not supported.

The DS87C530 provides several new hardware features implemented by new Special Function Registers. A summary of these SFRs is provided below.

PERFORMANCE OVERVIEW

The DS87C530 features a high speed 8051 compatible core. Higher speed comes not just from increasing the clock frequency, but from a newer, more efficient design.

This updated core does not have the dummy memory cycles that are present in a standard 8051. A conventional 8051 generates machine cycles using the clock frequency divided by 12. In the DS87C530, the same machine cycle takes four clocks. Thus the fastest instruction, 1 machine cycle, executes three times faster for the same crystal frequency. Note that these are identical instructions. The majority of instructions on the DS87C530 will see the full 3 to 1 speed improvement. Some instructions will get between 1.5 and 2.4 to 1 improvement. All instructions are faster than the original 8051.

The numerical average of all opcodes gives approximately a 2.5 to 1 speed improvement. Improvement of individual programs will depend on the actual instructions used. Speed sensitive applications would make the most use of instructions that are three times faster. However, the sheer number of 3 to 1 improved opcodes makes dramatic speed improvements likely for any code. These architecture improvements and 0.8 µm CMOS produce a peak instruction cycle in 121 ns (8.25 MIPs). The Dual Data Pointer feature also allows the user to eliminate wasted instructions when moving blocks of memory.

INSTRUCTION SET SUMMARY

All instructions in the DS87C530 perform the same functions as their 8051 counterparts. Their effect on bits, flags, and other status functions is identical. However, the timing of each instruction is different. This applies both in absolute and relative number of clocks.

For absolute timing of real–time events, the timing of software loops can be calculated using a table in the High–Speed Microcontroller User's Guide. However, counter/timers default to run at the older 12 clocks per increment. In this way, timer–based events occur at the standard intervals with software executing at higher speed. Timers optionally can run at 4 clocks per increment to take advantage of faster processor operation.

The relative time of two instructions might be different in the new architecture than it was previously. For example, in the original architecture, the "MOVX A, @DPTR" instruction and the "MOV direct, direct" instruction used

two machine cycles or 24 oscillator cycles. Therefore, they required the same amount of time. In the DS87C530, the MOVX instruction takes as little as two machine cycles or eight oscillator cycles but the “MOV direct, direct” uses three machine cycles or 12 oscillator cycles. While both are faster than their original counterparts, they now have different execution times. This is because the DS87C530 usually uses one instruction cycle for each instruction byte. The user concerned with precise program timing should examine the timing of each instruction for familiarity with the changes. Note that a machine cycle now requires just four clocks, and provides one ALE pulse per cycle. Many instructions require only one cycle, but some require five. In the original architecture, all were one or two cycles except for MUL and DIV. Refer to the High–Speed Microcontroller User’s Guide for details and individual instruction timing.

SPECIAL FUNCTION REGISTER LOCATIONS Table 2

** Functions not present in the 80C52 are in bold*

REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	ADDRESS
P0	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0	80h
SP									81h
DPL									82h
DPH									83h
DPL1									84h
DPH1									85h
DPS	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**SEL**	86h
PCON	SMOD_0	**SMOD0**	–	–	GF1	GF0	STOP	IDLE	87h
TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	88h
TMOD	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0	89h
TL0									8Ah
TL1									8Bh
TH0									8Ch
TH1									8Dh
CKCON	**WD1**	**WD0**	**T2M**	**T1M**	**T0M**	**MD2**	**MD1**	**MD0**	8Eh
P1	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0	90h
EXIF	**IE5**	**IE4**	**IE3**	**IE2**	**XT/RG**	**RGMD**	**RGSL**	**BGS**	91h
TRIM	**E4K**	**X12/$\overline{6}$**	**TRM2**	**$\overline{\text{TRM2}}$**	**TRM1**	**$\overline{\text{TRM1}}$**	**TRM0**	**$\overline{\text{TRM0}}$**	96h
SCON0	SM0/FE_0	SM1_0	SM2_0	REN_0	TB8_0	RB8_0	TI_0	RI_0	98h
SBUF0									99h
P2	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0	A0h
IE	EA	ES1	ET2	ES0	ET1	EX1	ET0	EX0	A8h
SADDR0									A9h
SADDR1									AAh
P3	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0	B0h
IP	–	PS1	PT2	PS0	PT1	PX1	PT0	PX0	B8h
SADEN0									B9h

REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	ADDRESS
SADEN1									BAh
SCON1	**SM0/FE_1**	**SM1_1**	**SM2_1**	**REN_1**	**TB8_1**	**RB8_1**	**TI_1**	**RI_1**	C0h
SBUF1									C1h
ROMSIZE	**–**	**–**	**–**	**–**	**–**	**RMS2**	**RMS1**	**RMS0**	C2h
PMR	**CD1**	**CD0**	**SWB**	**–**	**XTOFF**	**ALEOFF**	**DME1**	**DME0**	C4h
STATUS	**PIP**	**HIP**	**LIP**	**XTUP**	**SPTA1**	**SPRA1**	**SPTA0**	**SPRA0**	C5h
TA									C7h
T2CON	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$	C8h
T2MOD	–	–	–	–	–	–	T2OE	DCEN	C9h
RCAP2L									CAh
RCAP2H									CBh
TL2									CCh
TH2									CDh
PSW	CY	AC	F0	RS1	RS0	OV	FL	P	D0h
WDCON	**SMOD_1**	**POR**	**EPFI**	**PFI**	**WDIF**	**WTRF**	**EWT**	**RWT**	D8h
ACC									E0h
EIE	**–**	**–**	**ERTCI**	**EWDI**	**EX5**	**EX4**	**EX3**	**EX2**	E8h
B									F0h
RTASS									F2h
RTAS	0	0							F3h
RTAM	0	0							F4h
RTAH	0	0	0						F5h
EIP	**–**	**–**	**PRTCI**	**PWDI**	**PX5**	**PX4**	**PX3**	**PX2**	F8h
RTCC	**SSCE**	**SCE**	**MCE**	**HCE**	**RTCRE**	**RTCWE**	**RTCIF**	**RTCE**	F9h
RTCSS									FAh
RTCS	0	0							FBh
RTCM	0	0							FCh
RTCH									FDh
RTCD0									FEh
RTCD1									FFh

NONVOLATILE FUNCTIONS

The DS87C530 provides two functions that are permanently powered if a user supplies an external energy source. These are an on–chip real time clock and a nonvolatile SRAM. The chip contains all related functions and controls. The user must supply a backup source and a 32.768 KHz timekeeping crystal.

REAL TIME CLOCK

The on–chip Real Time Clock (RTC) keeps time of day and calendar functions. Its timebase is a 32.768 KHz crystal between pins RTCX1 and RTCX2. The RTC maintains time to 1/256 of a second. It also allows a user to read (and write) seconds, minutes, hours, day of the week, and date. The clock organization is shown in Figure 2.

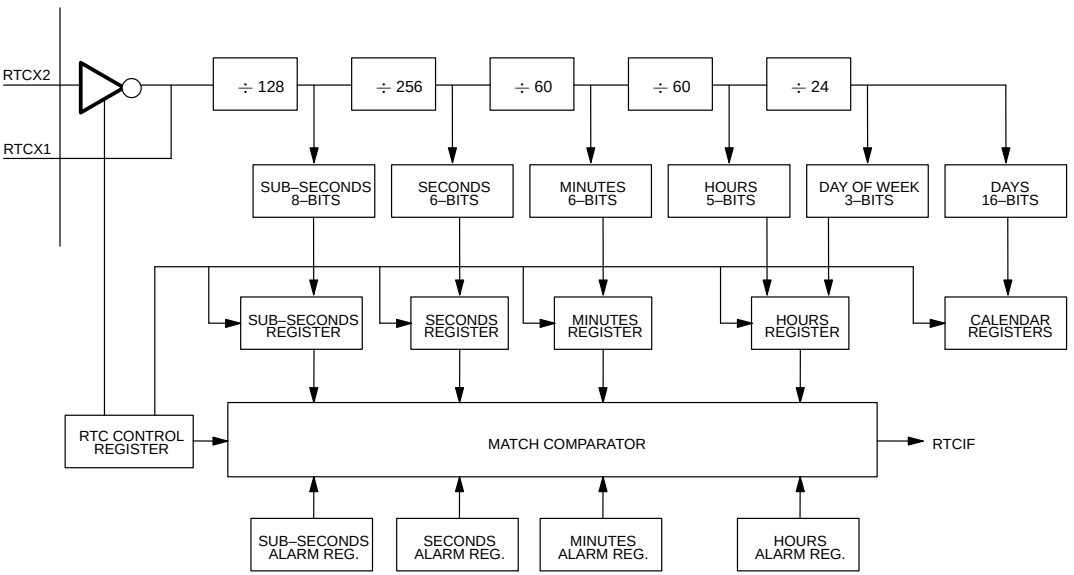
Timekeeping registers allow easy access to commonly needed time values. For example, software can simply check the elapsed number of minutes by reading one register. Alternately, it can read the complete time of day, including subseconds, in only four registers. The calendar stores its data in binary form. While this requires software translation, it allows complete flexibility as to the exact value. A user can start the calendar with a variety of selections since it is simply a 16–bit binary number of days. This number allows a total range of 179 years beginning from 0000.

The RTC features a programmable alarm condition. A user selects the alarm time. When the RTC reaches the selected value, it sets a flag. This will cause an interrupt if enabled, even in Stop mode. The alarm consists of a comparator that matches the user value against the RTC actual value. A user can select a match for one or more of the sub–seconds, seconds, minutes, or hours. This allows an interrupt automatically to occur once per second, once per minute, once per hour, or once per day. Enabling interrupts with no match will generate an interrupt 256 times per second.

Software enables the timekeeper oscillator using the RTC Enable bit in the RTC Control register (F9h). This starts the clock. It can disable the oscillator to preserve the life of the backup energy–source if unneeded. Values in the RTC Control register are maintained by the backup source through power failure. Once enabled, the RTC maintains time for the life of the backup source even when V_{CC} is removed.

The RTC will maintain an accuracy of ±2 minutes per month at 25°C. Under no circumstances are negative voltages, of any amplitude, allowed on any pin while the device is in data retention mode ($V_{CC} < V_{BAT}$). Negative voltages will shorten battery life, possibly corrupting the contents of internal SRAM and the RTC.

REAL TIME CLOCK Figure 2



NONVOLATILE RAM

The 1K x 8 on–chip SRAM can be nonvolatile. An external backup energy–source will maintain the SRAM contents through power failure. This allows the DS87C530 to log data or to store configuration settings. Internal switching circuits will detect the loss of V_{CC} and switch SRAM power to the backup source on the V_{BAT} pin. The 256 bytes of direct RAM are not affected by this circuit and are volatile.

CRYSTAL AND BACKUP SOURCES

To use the unique functions of the DS87C530, two external components are needed. These are a 32.768 KHz timekeeping crystal and a backup energy–source. The following describes guidelines for choosing these devices.

Timekeeping Crystal

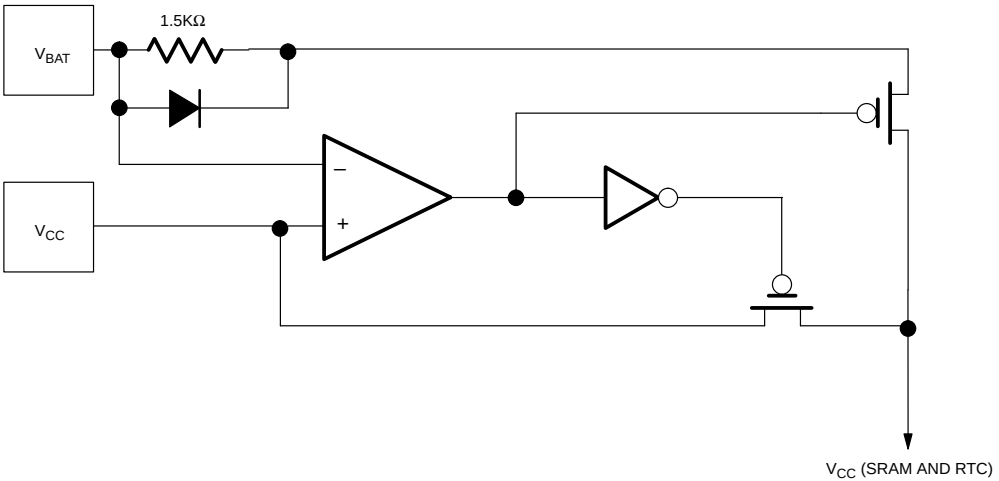
The DS87C530 can use a standard 32.768 KHz crystal as the RTC time base. There are two versions of standard crystals available, with 6 pF and 12.5 pF load capacitance. The tradeoff is that the 6 pF uses less power, giving longer life while V_{CC} is off, but is more sensitive to noise and board layout. The 12.5 pF crystal uses more power, giving a shorter battery backed life, but produces a more robust oscillator. Bit 6 in the RTC Trim register (TRIM; 96h) must be programmed to specify the crystal type for the oscillator. When TRIM.6 = 1, the circuit expects a 12.5 pF crystal. When TRIM.6 = 0, it expects a 6 pF crystal. As mentioned above, this bit will be nonvolatile so these choices will remain while the backup source is present. A guard ring (connected to the Real Time Clock ground) should encircle the RTCX1 and RTCX2 pins.

Backup Energy Source

The DS87C530 uses an external energy source to maintain timekeeping and SRAM data without V_{CC}. This source can be either a battery or 0.47 F super cap and should be connected to the V_{BAT} pin. The nominal battery voltage is 3V. The V_{BAT} pin will not source current. Therefore, a super cap requires an external resistor and diode to supply charge.

The backup lifetime is a function of the battery capacity and the data retention current drain. This drain is specified in the electrical specifications. The circuit loads the V_{BAT} only when V_{CC} has fallen below V_{BAT}. Thus the actual lifetime depends not only on the current and battery capacity, but also on the portion of time without power. A very small lithium cell provides a lifetime of more than 10 years.

INTERNAL BACKUP CIRCUIT Figure 3



IMPORTANT APPLICATION NOTE

The pins on the DS87C530 are generally as resilient as other CMOS circuits. They have no unusual susceptibility to electrostatic discharge (ESD) or other electrical transients. **However, no pin on the DS87C530 should ever be taken to a voltage below ground.** Negative voltages on any pin can turn on internal parasitic diodes that draw current directly from the battery. If a device pin is connected to the "outside world" where it may be handled or come in contact with electrical noise, protection should be added to prevent the device pin from going below -0.3V. Some power supplies can give a small undershoot on power up, which should be prevented. Application Note 93, "Design Guidelines for Microcontrollers Incorporating NVRAM", discusses how to protect the DS87C530 against these conditions.

MEMORY RESOURCES

Like the 8051, the DS87C530 uses three memory areas. These are program (ROM), data (RAM), and scratchpad RAM (registers). The DS87C530 contains on–chip quantities of all three areas.

The total memory configuration of the DS87C530 is 16KB of ROM, 1KB of data SRAM and 256 bytes of scratchpad or direct RAM. The 1KB of data space SRAM is read/write accessible and is memory mapped. This on–chip SRAM is reached by the MOVX instruction. It is not used for executable memory. The scratchpad area is 256 bytes of register mapped RAM and is identical to the RAM found on the 80C52. There is no conflict or overlap among the 256 bytes and the 1KB as they use different addressing modes and separate instructions.

OPERATIONAL CONSIDERATION

The erasure window should be covered without regard to the programmed/unprogrammed state of the EPROM. Otherwise, the device may not meet the AC and DC parameters listed in the datasheet.

PROGRAM MEMORY ACCESS

On–chip ROM begins at address 0000h and is contiguous through 3FFFh (16KB). Exceeding the maximum address of on–chip ROM will cause the DS87C530 to access off–chip memory. However, the maximum on–chip decoded address is selectable by software using the ROMSIZE™ feature. Software can cause the DS87C530 to behave like a device with less on–chip memory. This is beneficial when overlapping external memory, such as Flash, is used.

The maximum memory size is dynamically variable. Thus a portion of memory can be removed from the memory map to access off–chip memory, then restored to access on–chip memory. In fact, all of the on–chip memory can be removed from the memory map allowing the full 64KB memory space to be addressed from off–chip memory. ROM addresses that are larger than the selected maximum are automatically fetched from outside the part via Ports 0 and 2. A depiction of the ROM memory map is shown in Figure 4.

The ROMSIZE register is used to select the maximum on–chip decoded address for ROM. Bits RMS2, RMS1, RMS0 have the following affect:

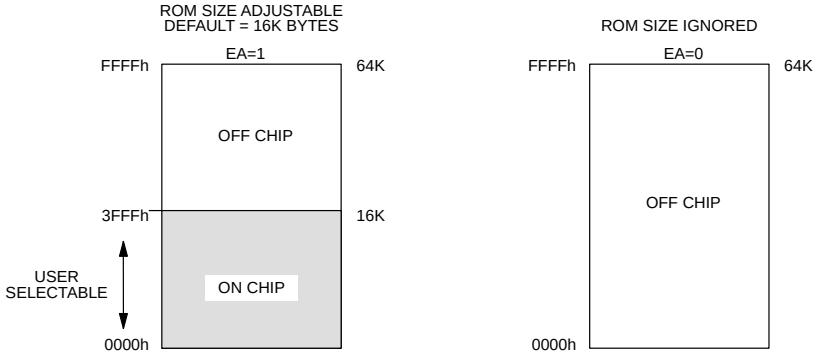
RMS2	RMS1	RMS0	Maximum on–chip ROM Address
0	0	0	0KB
0	0	1	1KB
0	1	0	2KB
0	1	1	4KB
1	0	0	8KB
1	0	1	16KB (default)
1	1	0	Invalid – reserved
1	1	1	Invalid – reserved

The reset default condition is a maximum on–chip ROM address of 16KB. Thus no action is required if this feature is not used. When accessing external program memory, the first 16KB would be inaccessible. To select a smaller effective ROM size, software must alter bits RMS2–RMS0. Altering these bits requires a Timed Access procedure as explained below.

Care should be taken so that changing the ROMSIZE register does not corrupt program execution. For example, assume that a DS87C520 is executing instructions from internal program memory near the 12KB boundary (~3000h) and that the ROMSIZE register is currently configured for a 16KB internal program space. If software reconfigures the ROMSIZE register to 4KB (0000h–0FFFh) in the current state, the device will immediately jump to external program execution because program code from 4KB to 16KB (1000h–3FFFh) is no longer located on–chip. This could result in code misalignment and execution of an invalid instruction. The recommended method is to modify the ROMSIZE register from a location in memory that will be internal (or external) both before and after the operation. In the above example, the instruction which modifies the ROMSIZE register should be located below the 4KB (1000h) boundary, so that it will be unaffected by the memory modification. The same precaution should be applied if the internal program memory size is modified while executing from external program memory.

Off–chip memory is accessed using the multiplexed address/data bus on P0 and the MSB address on P2. While serving as a memory bus, these pins are not I/O ports. This convention follows the standard 8051 method of expanding on–chip memory. Off–chip ROM access also occurs if the $\overline{EA}$ pin is a logic 0. $\overline{EA}$ overrides all bit settings. The $\overline{PSEN}$ signal will go active (low) to serve as a chip enable or output enable when Ports 0 and 2 fetch from external ROM.

ROM MEMORY MAP Figure 4



DATA MEMORY ACCESS

Unlike many 8051 derivatives, the DS87C530 contains on–chip data memory. It also contains the standard 256 bytes of RAM accessed by direct instructions. These areas are separate. The MOVX instruction accesses the on–chip data memory. Although physically on–chip, software treats this area as though it was located off–chip. The 1KB of SRAM is between address 0000h and 03FFh.

Access to the on–chip data RAM is optional under software control. When enabled by software, the data SRAM is between 0000h and 03FFh. Any MOVX instruction that uses this area will go to the on–chip RAM while enabled. MOVX addresses greater than 03FFh automatically go to external memory through Ports 0 and 2.

When disabled, the 1KB memory area is transparent to the system memory map. Any MOVX directed to the space between 0000h and FFFFh goes to the expanded bus on Ports 0 and 2. This also is the default condition. This default allows the DS87C530 to drop into an existing system that uses these addresses for other hardware and still have full compatibility.

The on–chip data area is software selectable using two bits in the Power Management Register at location C4h. This selection is dynamically programmable. Thus access to the on–chip area becomes transparent to reach off–chip devices at the same addresses. The control bits are DME1 (PMR.1) and DME0 (PMR.0). They have the following operation:

DATA MEMORY ACCESS CONTROL Table 3

DME1	DME0	DATA MEMORY ADDRESS	MEMORY FUNCTION
0	0	0000h – FFFFh	External Data Memory **Default condition*
0	1	0000h – 03FFh 0400h – FFFFh	Internal SRAM Data Memory External Data Memory
1	0	Reserved	Reserved
1	1	0000h – 03FFh 0400h – FFFBh FFFCh FFFDh–FFFh	Internal SRAM Data Memory Reserved – no external access Read access to the status of lock bits Reserved – no external access

Notes on the status byte read at FFFCh with DME1, 0 = 1, 1: Bits 2–0 reflect the programmed status of the security lock bits LB2–LB0. They are individually set to a logic 1 to correspond to a security lock bit that has been programmed. These status bits allow software to verify that the part has been locked before running if desired. The bits are read only.

Note: After internal MOVX SRAM has been initialized, changing bits DEM0/1 will have no affect on the contents of the SRAM.

STRETCH MEMORY CYCLE

The DS87C530 allows software to adjust the speed of off–chip data memory access. The micro is capable of performing the MOVX in as few as two instruction cycles. The on–chip SRAM uses this speed and any MOVX instruction directed internally uses two cycles. However, the time can be stretched for interface to external devices. This allows access to both fast memory and slow memory or peripherals with no glue logic. Even in high–speed systems, it may not be necessary or desirable to perform off–chip data memory access at full speed. In addition, there are a variety of memory mapped peripherals such as LCDs or UARTs that are slow.

The Stretch MOVX is controlled by the Clock Control Register at SFR location 8Eh as described below. It allows the user to select a Stretch value between zero and seven. A Stretch of zero will result in a two machine cycle MOVX. A Stretch of seven will result in a MOVX of nine machine cycles. Software can dynamically change this value depending on the particular memory or peripheral.

On reset, the Stretch value will default to a one resulting in a three cycle MOVX for any external access. Therefore, off–chip RAM access is not at full speed. This is a convenience to existing designs that may not have fast RAM in place. Internal SRAM access is always at full speed regardless of the Stretch setting. When desiring maximum speed, software should select a Stretch value of zero. When using very slow RAM or peripherals, select a larger Stretch value. Note that this affects data memory only and the only way to slow program memory (ROM) access is to use a slower crystal.

Using a Stretch value between one and seven causes the microcontroller to stretch the read/write strobe and all related timing. Also, setup and hold times are increased by 1 clock when using any Stretch greater than 0. This results in a wider read/write strobe and relaxed interface timing, allowing more time for memory/peripherals to respond. The timing of the variable speed MOVX is in the Electrical Specifications. Table 4 shows the resulting strobe widths for each Stretch value. The memory Stretch uses the Clock Control Special Function Register at SFR location 8Eh. The Stretch value is selected using bits CKCON.2–0. In the table, these bits are referred to as M2 through M0. The first Stretch (default) allows the use of common 120 ns RAMs without dramatically lengthening the memory access.

DATA MEMORY CYCLE STRETCH VALUES Table 4

CKCON.2–0				$\overline{RD}$ OR $\overline{WR}$ STROBE	STROBE WIDTH TIME
M2	M1	M0	MEMORY CYCLES	WIDTH IN CLOCKS	@ 33 MHz
0	0	0	2 (forced internal)	2	60 ns
0	0	1	3 (default external)	4	121 ns
0	1	0	4	8	242 ns
0	1	1	5	12	364 ns
1	0	0	6	16	485 ns
1	0	1	7	20	606 ns
1	1	0	8	24	727 ns
1	1	1	9	28	848 ns

DUAL DATA POINTER

The timing of block moves of data memory is faster using the DS87C530 Dual Data Pointer (DPTR). The standard 8051 DPTR is a 16–bit value that is used to address off–chip data RAM or peripherals. In the DS87C530, the standard data pointer is called DPTR, located at SFR addresses 82h and 83h. These are the standard locations. Using DPTR requires no modification of standard code. The new DPTR at SFR 84h and 85h is called DPTR1. The DPTR Select bit (DPS) chooses the active pointer. Its location is the lsb of the SFR location 86h. No other bits in register 86h have any effect and are 0. The user switches between data pointers by toggling the lsb of register 86h. The increment (INC) instruction is the fastest way to accomplish this. All DPTR–related instructions use the currently selected DPTR for any activity. Therefore it takes only one instruction to switch from a source to a destination address. Using the Dual Data Pointer saves code from needing to save source and destination addresses when doing a block move. The software simply switches between DPTR and 1 once software loads them. The relevant register locations are as follows.

DPL	82h	Low byte original DPTR
DPH	83h	High byte original DPTR
DPL1	84h	Low byte new DPTR
DPH1	85h	High byte new DPTR
DPS	86h	DPTR Select (lsb)

POWER MANAGEMENT

Along with the standard Idle and power down (Stop) modes of the standard 80C52, the DS87C530 provides a new Power Management Mode. This mode allows the processor to continue functioning, yet to save power compared with full operation. The DS87C530 also features several enhancements to Stop mode that make it more useful.

POWER MANAGEMENT MODE (PMM)

Power Management Mode offers a complete scheme of reduced internal clock speeds that allow the CPU to run software but to use substantially less power. During default operation, the DS87C530 uses four clocks per machine cycle. Thus the instruction cycle rate is (Clock/4). At 33 MHz crystal speed, the instruction cycle speed is 8.25 MHz (33/4). In PMM, the microcontroller continues to operate but uses an internally divided version of the clock source. This creates a lower power state without external components. It offers a choice of two reduced instruction cycle speeds (and two clock sources – discussed below). The speeds are (Clock/64) and (Clock/1024).

Software is the only mechanism to invoke the PMM. Table 5 illustrates the instruction cycle rate in PMM for several common crystal frequencies. Since power consumption is a direct function of operating speed, PMM 1 eliminates most of the power consumption while still allowing a reasonable speed of processing. PMM 2 runs very slowly and provides the lowest power consumption without stopping the CPU. This is illustrated in Table 6.

Note that PMM provides a lower power condition than Idle mode. This is because in Idle, all clocked functions such as timers run at a rate of crystal divided by 4. Since wake–up from PMM is as fast as or faster than from Idle and PMM allows the CPU to operate (even if doing NOPs), there is little reason to use Idle mode in new designs.

INSTRUCTION CYCLE RATE Table 5

CRYSTAL SPEED	FULL OPERATION (4 CLOCKS)	PMM 1 (64 CLOCKS)	PMM 2 (1024 CLOCKS)
1.8432 MHz	460.8 KHz	28.8 KHz	1.8 KHz
11.0592 MHz	2.765 MHz	172.8 KHz	10.8 KHz
22 MHz	5.53 MHz	345.6 KHz	21.6 KHz
25 MHz	6.25 MHz	390.6 KHz	24.4 KHz
33 MHz	8.25 MHz	515.6 KHz	32.2 KHz

OPERATING CURRENT ESTIMATES IN PMM Table 6

CRYSTAL SPEED	FULL OPERATION (4 CLOCKS)	PMM 1 (64 CLOCKS)	PMM 2 (1024 CLOCKS)
1.8432 MHz	3.1 mA	1.2 mA	1.0 mA
3.57 MHz	5.3 mA	1.6 mA	1.1 mA
11.0592 MHz	15.5 mA	4.8 mA	4.0 mA
16 MHz	21 mA	7.1 mA	6.0 mA
22 MHz	25.5 mA	8.3 mA	6.5 mA
25 MHz	31 mA	9.7 mA	8.0 mA
33 MHz	36 mA	12.0 mA	10.0 mA

CRYSTALESS PMM

A major component of power consumption in PMM is the crystal amplifier circuit. The DS87C530 allows the user to switch CPU operation to an internal ring oscillator and turn off the crystal amplifier. The CPU would then have a clock source of approximately 2–4 MHz, divided by either 4, 64, or 1024. The ring is not accurate, so software can not perform precision timing. However, this mode allows an additional saving of between 0.5 and 6.0 mA depending on the actual crystal frequency. While this saving is of little use when running at 4 clocks per instruction cycle, it makes a major contribution when running in PMM1 or PMM2.

PMM OPERATION

Software invokes the PMM by setting the appropriate bits in the SFR area. The basic choices are divider speed and clock source. There are three speeds (4, 64, and 1024) and two clock sources (crystal, ring). Both the decisions and the controls are separate. Software will typically select the clock speed first. Then, it will perform the switch to ring operation if desired. Lastly, software can disable the crystal amplifier if desired.

There are two ways of exiting PMM. Software can remove the condition by reversing the procedure that invoked PMM or hardware can (optionally) remove it. To resume operation at a divide by 4 rate under software control, simply select 4 clocks per cycle, then crystal based operation if relevant. When disabling the crystal as the time base in favor of the ring oscillator, there are timing restrictions associated with restarting the crystal operation. Details are described below.

There are three registers containing bits that are concerned with PMM functions. They are Power Management Register (PMR; C4h), Status (STATUS; C5h), and External Interrupt Flag (EXIF; 91h)

Clock Divider

Software can select the instruction cycle rate by selecting bits CD1 (PMR.7) and CD0 (PMR.6) as follows:

CD1	CD0	Cycle rate
0	0	Reserved
0	1	4 clocks (default)
1	0	64 clocks
1	1	1024 clocks

The selection of instruction cycle rate will take effect after a delay of one instruction cycle. Note that the clock divider choice applies to all functions including timers. Since baud rates are altered, it will be difficult to conduct serial communication while in PMM. There are minor restrictions on accessing the clock selection bits. The processor must be running in a 4 clock state to select either 64 (PMM1) or 1024 (PMM2) clocks. This means software cannot go directly from PMM1 to PMM2 or visa versa. It must return to a 4 clock rate first.

Switchback

To return to a 4 clock rate from PMM, software can simply select the CD1 and CD0 clock control bits to the 4 clocks per cycle state. However, the DS87C530 provides several hardware alternatives for automatic Switchback. If Switchback is enabled, then the DS87C530 will automatically return to a 4 clock per cycle speed when an interrupt occurs from an enabled, valid external interrupt source. A Switchback will also occur when a UART detects the beginning of a serial start bit if the serial receiver is enabled (REN=1). Note the beginning of a start bit does not generate an interrupt; this occurs on reception of a complete serial word. The automatic Switchback on detection of a start bit allows hardware to correct baud rates in time for a proper serial reception. A switchback will also occur when a byte is written to the SBUF0 or SBUF1 for transmission.

Switchback is enabled by setting the SWB bit (PMR.5) to a 1 in software. For an external interrupt, Switchback will occur only if the interrupt source could really generate the interrupt. For example, if $\overline{\text{INT0}}$ is enabled but has a low priority setting, then Switchback will not occur on $\overline{\text{INT0}}$ if the CPU is servicing a high priority interrupt.

Status

Information in the Status register assists decisions about switching into PMM. This register contains information about the level of active interrupts and the activity on the serial ports.

The DS87C530 supports three levels of interrupt priority. These levels are Power–fail, High, and Low. Bits STATUS.7–5 indicate the service status of each level. If PIP (Power–fail Interrupt Priority; STATUS.7) is a 1, then the processor is servicing this level. If either HIP

(High Interrupt Priority; STATUS.6) or LIP (Low Interrupt Priority; STATUS.5) is high, then the corresponding level is in service.

Software should not rely on a lower priority level interrupt source to remove PMM (Switchback) when a higher level is in service. Check the current priority service level before entering PMM. If the current service level locks out a desired Switchback source, then it would be advisable to wait until this condition clears before entering PMM.

Alternately, software can prevent an undesired exit from PMM by entering a low priority interrupt service level before entering PMM. This will prevent other low priority interrupts from causing a Switchback.

Status also contains information about the state of the serial ports. Serial Port Zero Receive Activity (SPRA0; STATUS.0) indicates a serial word is being received on Serial Port 0 when this bit is set to a 1. Serial Port Zero Transmit Activity (SPTA0; STATUS.1) indicates that the serial port is still shifting out a serial transmission. STATUS.2 and STATUS.3 provide the same information for Serial Port 1, respectively. These bits should be interrogated before entering PMM1 or PMM2 to ensure that no serial port operations are in progress. Changing the clock divisor rate during a serial transmission or reception will corrupt the operation.

Crystal/Ring Operation

The DS87C530 allows software to choose the clock source as an independent selection from the instruction cycle rate. The user can select crystal–based or ring oscillator–based operation under software control. Power–on reset default is the crystal (or external clock) source. The ring may save power depending on the actual crystal speed. To save still more power, software can then disable the crystal amplifier. This process requires two steps. Reversing the process also requires two steps.

The XT/$\overline{RG}$ bit (EXIF.3) selects the crystal or ring as the clock source. Setting XT/$\overline{RG}$ = 1 selects the crystal. Setting XT/$\overline{RG}$ = 0 selects the ring. The RGMD (EXIF.2) bit serves as a status bit by indicating the active clock source. RGMD = 0 indicates the CPU is running from the crystal. RGMD = 1 indicates it is running from the ring. When operating from the ring, disable the crystal amplifier by setting the XTOFF bit (PMR.3) to a 1. This can only be done when XT/$\overline{RG}$ = 0.

When changing the clock source, the selection will take effect after a one instruction cycle delay. This applies to changes from crystal to ring and vise versa. However, this assumes that the crystal amplifier is running. In most cases, when the ring is active, software previously disabled the crystal to save power. If ring operation is being used and the system must switch to crystal operation, the crystal must first be enabled. Set the XTOFF bit to a 0. At this time, the crystal oscillation will begin. The DS87C530 then provides a warm–up delay to make certain that the frequency is stable. Hardware will set the XTUP bit (STATUS.4) to a 1 when the crystal is ready for use. Then software should write XT/$\overline{RG}$ to a 1 to begin operating from the crystal. Hardware prevents writing XT/$\overline{RG}$ to a 1 before XTUP = 1. The delay between XTOFF = 0 and XTUP = 1 will be 65,536 crystal clocks in addition to the crystal cycle startup time.

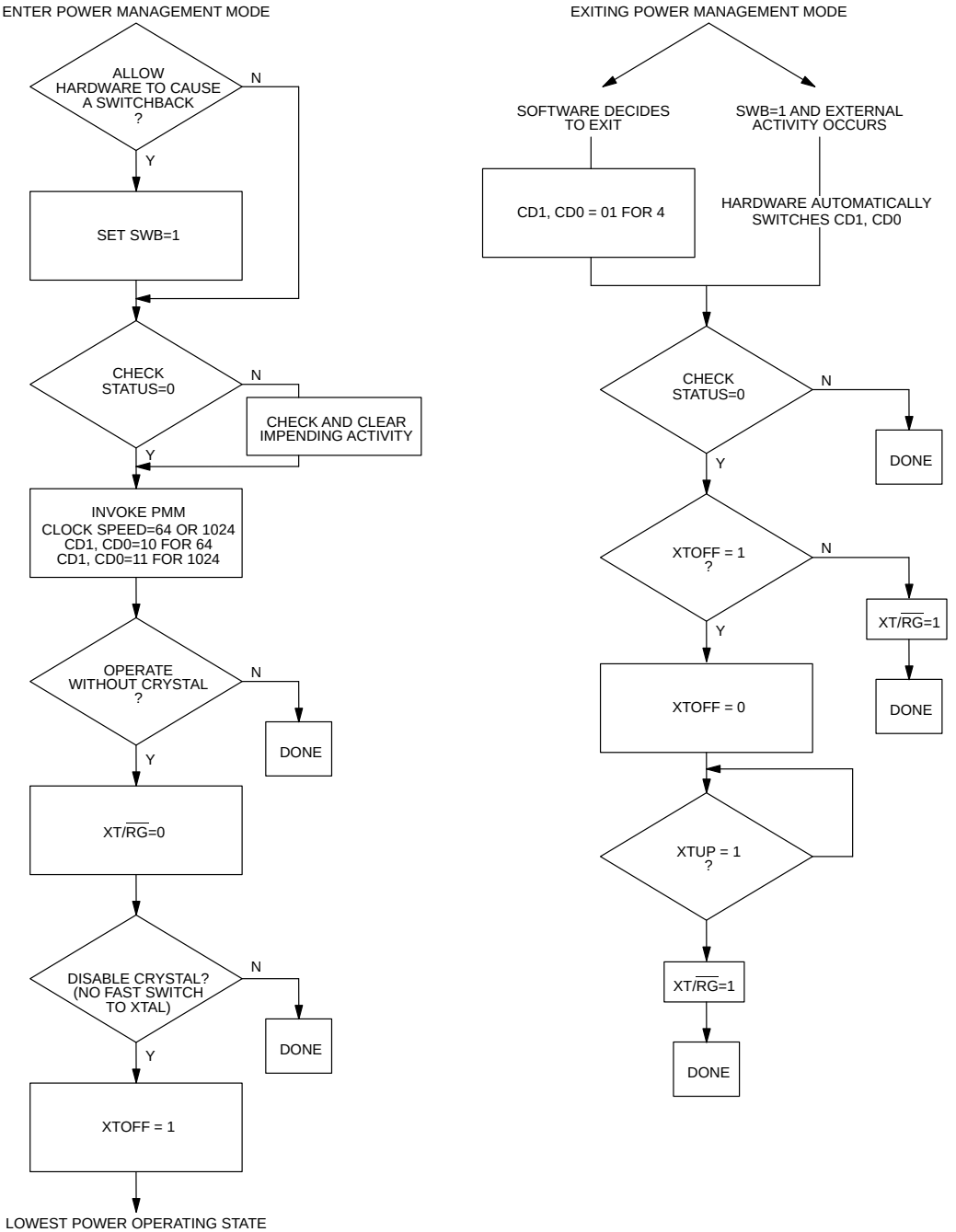
Switchback has no effect on the clock source. If software selects a reduced clock divider and enables the ring, a Switchback will only restore the divider speed. The ring will remain as the time base until altered by software. If there is serial activity, Switchback usually occurs with enough time to create proper baud rates. This is not true if the crystal is off and the CPU is running from the ring. If sending a serial character that wakes the system from crystaless PMM, then it should be a dummy character of no importance with a subsequent delay for crystal startup.

The following table is a summary of the bits relating to PMM and its operation. The flow chart below illustrates a typical decision set associated with PMM.

PMM CONTROL AND STATUS BIT SUMMARY Table 7

BIT NAME	LOCATION	FUNCTION	RESET	WRITE ACCESS
XT/$\overline{RG}$	EXIF.3	Control. XT/$\overline{RG}$=1, runs from crystal or external clock; XT/$\overline{RG}$=0, runs from internal ring oscillator.	X	0 to 1 only when XTUP=1 and XTOFF=0
RGMD	EXIF.2	Status. RGMD=1, CPU clock = ring; RGMD=0, CPU clock = crystal.	0	None
CD1, CD0	PMR.7, PMR.6	Control. CD1,0=01, 4 clocks; CS1,0=10, PMM1; CD1,0=11, PMM2.	0, 1	Write CD1,0=10 or 11 only from CD1,0=01
SWB	PMR.5	Control. SWB=1, hardware invokes switchback to 4 clocks, SWB=0, no hardware switchback.	0	Unrestricted
XTOFF	PMR.3	Control. Disables crystal operation after ring is selected.	0	1 only when XT/$\overline{RG}$=0
PIP	STATUS.7	Status. 1 indicates a power–fail interrupt in service.	0	None
HIP	STATUS.6	Status. 1 indicates high priority interrupt in service.	0	None
LIP	STATUS.5	Status. 1 indicates low priority interrupt in service.	0	None
XTUP	STATUS.4	Status. 1 indicates that the crystal has stabilized.	1	None
SPTA1	STATUS.3	Status. Serial transmission on serial port 1.	0	None
SPRA1	STATUS.2	Status. Serial word reception on serial port 1.	0	None
SPTA0	STATUS.1	Status. Serial transmission on serial port 0.	0	None
SPRA0	STATUS.0	Status. Serial word reception on serial port 0.	0	None

INVOKING AND CLEARING PMM Figure 3



IDLE MODE

Setting the lsb of the Power Control register (PCON; 87h) invokes the Idle mode. Idle will leave internal clocks, serial ports and timers running. Power consumption drops because the CPU is not active. Since clocks are running, the Idle power consumption is a function of crystal frequency. It should be approximately 1/2 of the operational power at a given frequency. The CPU can exit the Idle state with any interrupt or a reset. Idle is available for backward software compatibility. The system can now reduce power consumption to below Idle levels by using PMM1 or PMM2 and running NOPs.

STOP MODE ENHANCEMENTS

Setting bit 1 of the Power Control register (PCON; 87h) invokes the Stop mode. Stop mode is the lowest power state since it turns off all internal clocking. The I_{CC} of a standard Stop mode is approximately 1 µA but is specified in the Electrical Specifications. The CPU will exit Stop mode from an external interrupt or a reset condition. Internally generated interrupts (timer, serial port, watchdog) are not useful since they require clocking activity. One exception is that a real time clock interrupt can cause the device to exit Stop mode. This provides a very power efficient way of performing infrequent yet periodic tasks.

The DS87C530 provides two enhancements to the Stop mode. As documented below, the DS87C530 provides a band–gap reference to determine Power–fail Interrupt and Reset thresholds. The default state is that the band–gap reference is off while in Stop mode. This allows the extremely low power state mentioned above. A user can optionally choose to have the band–gap enabled during Stop mode. With the band–gap reference enabled, PFI and Power–fail reset are functional and are a valid means for leaving Stop mode. This allows software to detect and compensate for a brown–out or power supply sag, even when in Stop mode.

In Stop mode with the band–gap enabled, I_{CC} will be approximately 50 µA compared with 1 µA with the band–gap off. If a user does not require a Power–fail Reset or Interrupt while in Stop mode, the band–gap can remain disabled. Only the most power sensitive applications should turn off the band–gap, as this results in an uncontrolled power down condition.

The control of the band–gap reference is located in the Extended Interrupt Flag register (EXIF; 91h). Setting BGS (EXIF.0) to a 1 will keep the band–gap reference enabled during Stop mode. The default or reset condition is with the bit at a logic 0. This results in the band–gap being off during Stop mode. Note that this bit has no control of the reference during full power, PMM, or Idle modes.

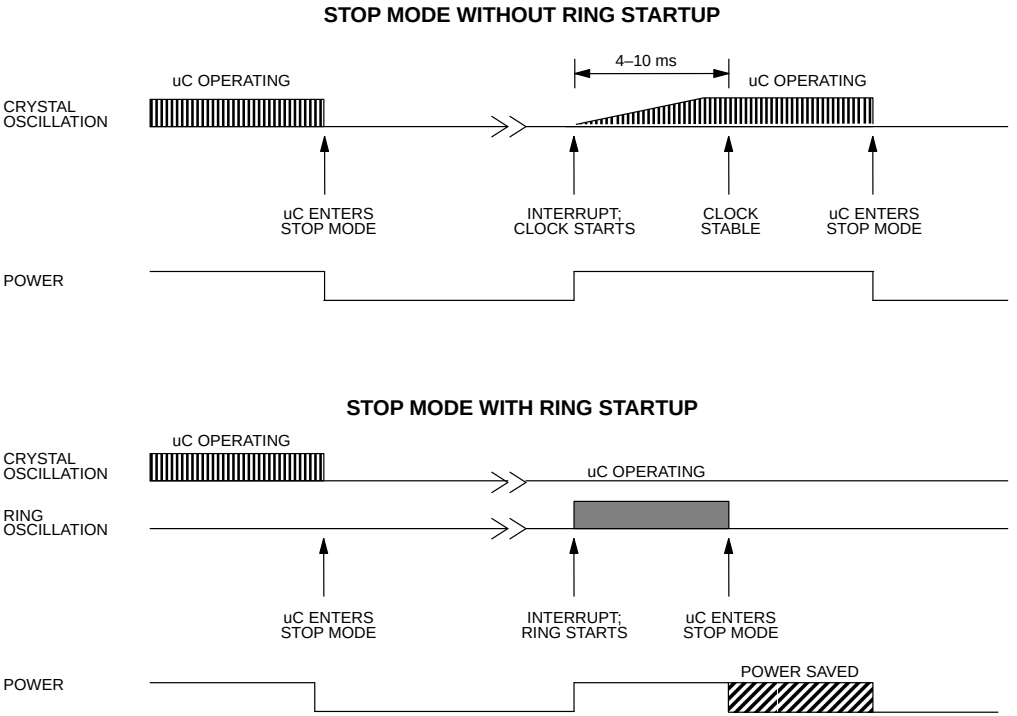
The second feature allows an additional power saving option while also making Stop easier to use. This is the ability to start instantly when exiting Stop mode. It is the internal ring oscillator that provides this feature. This ring can be a clock source when exiting Stop mode in response to an interrupt. The benefit of the ring oscillator is as follows.

Using Stop mode turns off the crystal oscillator and all internal clocks to save power. This requires that the oscillator be restarted when exiting Stop mode. Actual start–up time is crystal dependent, but is normally at least 4 ms. A common recommendation is 10 ms. In an application that will wake–up, perform a short operation, then return to sleep, the crystal start–up can be longer than the real transaction. However, the ring oscillator will start instantly. Running from the ring, the user can perform a simple operation and return to sleep before the crystal has even started. If a user selects the ring to provide the start–up clock and the processor remains running, hardware will automatically switch to the crystal once a power–on reset interval (65536 clocks) has expired. Hardware uses this value to assure proper crystal start even though power is not being cycled.

The ring oscillator runs at approximately 2–4 MHz but will not be a precise value. Do not conduct real–time precision operations (including serial communication) during this ring period. Figure 4 shows how the operation would compare when using the ring, and when starting up normally. The default state is to exit Stop mode without using the ring oscillator.

The RGSL – Ring Select bit at EXIF.1 (EXIF; 91h) controls this function. When RGSL = 1, the CPU will use the ring oscillator to exit Stop mode quickly. As mentioned above, the processor will automatically switch from the ring to the crystal after a delay of 65,536 crystal clocks. For a 3.57 MHz crystal, this is approximately 18 ms. The processor sets a flag called RGMD– Ring Mode, located at EXIF.2, that tells software that the ring is being used. The bit will be a logic 1 when the ring is in use. Attempt no serial communication or precision timing while this bit is set, since the operating frequency is not precise.

RING OSCILLATOR EXIT FROM STOP MODE Figure 4



Note: Diagram assumes that the operation following Stop requires less than 18 ms to complete.

EMI REDUCTION

The DS87C530 allows software to reduce EMI. One of the major contributors to radiated noise in an 8051 based system is the toggling of ALE. The DS87C530 allows software to disable ALE when not used by setting the ALEOFF (PMR.2) bit to a 1. When ALEOFF = 1, ALE will still toggle during an off–chip MOVX. However, ALE will remain in a static when performing on–chip memory access. The default state of ALEOFF = 0 so ALE toggles with every instruction cycle.

PERIPHERAL OVERVIEW

The DS87C530 provides several of the most commonly needed peripheral functions in microcomputer–based systems. These new functions include a second serial port, Power–fail Reset, Power–fail Interrupt, and a programmable Watchdog Timer. These are described below, and more details are available in the High–Speed Microcontroller User's Guide.

SERIAL PORTS

The DS87C530 provides a serial port (UART) that is identical to the 80C52. In addition it includes a second hardware serial port that is a full duplicate of the standard one. This port optionally uses pins P1.2 (RXD1) and P1.3 (TXD1). It has duplicate control functions included in new SFR locations.

Both ports can operate simultaneously but can be at different baud rates or even in different modes. The second serial port has similar control registers (SCON1; C0h, SBUF1; C1h) to the original. The new serial port can only use Timer 1 for timer generated baud rates.

TIMER RATE CONTROL

There is one important difference between the DS87C530 and 8051 regarding timers. The original 8051 used 12 clocks per cycle for timers as well as for machine cycles. The DS87C530 architecture normally uses 4 clocks per machine cycle. However, in the area of timers and serial ports, the DS87C530 will default to 12 clocks per cycle on reset. This allows existing code with real–time dependencies such as baud rates to operate properly.

If an application needs higher speed timers or serial baud rates, the user can select individual timers to run at the 4 clock rate. The Clock Control register (CKCON; 8Eh) determines these timer speeds. When the relevant CKCON bit is a logic 1, the DS87C530 uses 4 clocks per cycle to generate timer speeds. When the bit is a 0, the DS87C530 uses 12 clocks for timer speeds. The reset condition is a 0. CKCON.5 selects the speed of Timer 2. CKCON.4 selects Timer 1 and CKCON.3 selects Timer 0. Unless a user desires very fast timing, it is unnecessary to alter these bits. Note that the timer controls are independent.

POWER–FAIL RESET

The DS87C530 uses a precision band–gap voltage reference to decide if V_{CC} is out of tolerance. While powering up, the internal monitor circuit maintains a reset state until V_{CC} rises above the V_{RST} level. Once above this level, the monitor enables the crystal oscillator and counts 65536 clocks. It then exits the reset state. This power–on reset (POR) interval allows time for the oscillator to stabilize.

A system needs no external components to generate a power–related reset. Anytime V_{CC} drops below V_{RST}, as in power–failure or a power drop, the monitor will generate and hold a reset. It occurs automatically, needing no action from the software. Refer to the Electrical Specifications for the exact value of V_{RST}.

POWER–FAIL INTERRUPT

The voltage reference that sets a precise reset threshold also generates an optional early warning Power–fail Interrupt (PFI). When enabled by software, the processor will vector to program memory address 0033h if V_{CC} drops below V_{PFW}. PFI has the highest priority. The PFI enable is in the Watchdog Control SFR (WDCON – D8h). Setting WDCON.5 to a logic 1 will enable the PFI. Application software can also read the PFI flag at WDCON.4. A PFI condition sets this bit to a 1. The flag is independent of the interrupt enable and software must manually clear it. If the PFI is enabled and the band–gap select bit (BGS) is set, a PFI will bring the device out of Stop mode.

WATCHDOG TIMER

To prevent software from losing control, the DS87C530 includes a programmable Watchdog Timer. The Watchdog is a free running timer that sets a flag if allowed to reach a preselected time–out. It can be (re)started by software.

A typical application is to select the flag as a reset source. When the Watchdog times out, it sets its flag which generates reset. Software must restart the timer before it reaches its time–out or the processor is reset.

Software can select one of four time–out values. Then, it restarts the timer and enables the reset function. After enabling the reset function, software must then restart the timer before its expiration or hardware will reset the CPU. Both the Watchdog Reset Enable and the Watchdog Restart control bits are protected by a “Timed Access” circuit. This prevents errant software from accidentally clearing the Watchdog. Time–out values are precise since they are a function of the crystal frequency as shown below in Table 8. For reference, the time periods at 33 MHz also are shown.

The Watchdog also provides a useful option for systems that do not require a reset circuit. It will set an interrupt flag 512 clocks before setting the reset flag. Software can optionally enable this interrupt source. The interrupt is independent of the reset. A common use of the interrupt is during debug, to show developers where the Watchdog times out. This indicates where the Watchdog must be restarted by software. The interrupt also can serve as a convenient time–base generator or can wake–up the processor from power saving modes.

The Watchdog function is controlled by the Clock Control (CKCON – 8Eh), Watchdog Control (WDCON – D8h), and Extended Interrupt Enable (EIE – E8h) SFRs. CKCON.7 and CKCON.6 are WD1 and WD0 respectively and they select the Watchdog time–out period as shown in Table 8.

WATCHDOG TIME–OUT VALUES Table 8

WD1	WD0	INTERRUPT TIME–OUT	TIME (33 MHz)	RESET TIME–OUT	TIME (33 MHz)
0	0	2^{17} clocks	3.9718 ms	2^{17} + 512 clocks	3.9874 ms
0	1	2^{20} clocks	31.77 ms	2^{20} + 512 clocks	31.79 ms
1	0	2^{23} clocks	254.20 ms	2^{23} + 512 clocks	254.21 ms
1	1	2^{26} clocks	2033.60 ms	2^{26} + 512 clocks	2033.62 ms

As shown above, the Watchdog Timer uses the crystal frequency as a time base. A user selects one of four counter values to determine the time–out. These clock counter lengths are 2^{17}= 131,072 clocks; 2^{20} = 1,048,576; 2^{23} = 8,388,608 clocks; and 2^{26} = 67,108,864 clocks. The times shown in Table 8 above are with a 33 MHz crystal frequency. Once the counter chain has completed a full interrupt count, hardware will set an interrupt flag. Regardless of whether the user enables this interrupt, there are then 512 clocks left until the reset flag is set. Software can enable the interrupt and reset individually. Note that the Watchdog is a free running timer and does not require an enable.

There are five control bits in special function registers that affect the Watchdog Timer and two status flags that report to the user. WDIF (WDCON.3) is the interrupt flag that is set at timer termination when there are 512 clocks remaining until the reset flag is set. WTRF (WDCON.2) is the flag that is set when the timer has completely timed out. This flag is normally associated with a CPU reset and allows software to determine the reset source. EWT (WDCON.1) is the enable for the Watchdog timer reset function. RWT (WDCON.0) is the bit that software uses to restart the Watchdog Timer. Setting this bit restarts the timer for another full interval. Application software must set this bit before the time–out. Both of these bits are protected by Timed Access discussed below. As mentioned previously, WD1 and 0 (CKCON .7 and 6) select the time–out. Finally, the user can enable the Watchdog Interrupt using EWDI (EIE.4). The Special Function Register map is shown above.

INTERRUPTS

The DS87C530 provides 14 interrupt sources with three priority levels. The Power–fail Interrupt (PFI) has the highest priority. Software can assign high or low priority to other sources. All interrupts that are new to the 8051 family, except for the PFI, have a lower natural priority than the originals.

INTERRUPT SOURCES AND PRIORITIES Table 9

NAME	DESCRIPTION	VECTOR	NATURAL PRIORITY	8051/DALLAS
PFI	Power Fail Interrupt	33h	1	DALLAS
$\overline{\text{INT0}}$	External Interrupt 0	03h	2	8051
TF0	Timer 0	0Bh	3	8051
$\overline{\text{INT1}}$	External Interrupt 1	13h	4	8051
TF1	Timer 1	1Bh	5	8051
SCON0	TI0 or RI0 from serial port 0	23h	6	8051
TF2	Timer 2	2Bh	7	8051
SCON1	TI1 or RI1 from serial port 1	3Bh	8	DALLAS
INT2	External Interrupt 2	43h	9	DALLAS
$\overline{\text{INT3}}$	External Interrupt 3	4Bh	10	DALLAS
INT4	External Interrupt 4	53h	11	DALLAS
$\overline{\text{INT5}}$	External Interrupt 5	5Bh	12	DALLAS
WDTI	Watchdog Time–Out Interrupt	63h	13	DALLAS
RTCI	Real Time Clock Interrupt	6Bh	14	DALLAS

TIMED ACCESS PROTECTION

It is useful to protect certain SFR bits from an accidental write operation. The Timed Access procedure stops an errant CPU from accidentally changing these bits. It requires that the following instructions precede a write of a protected bit.

```
MOV     0C7h, #0AAh
MOV     0C7h, #55h
```

Writing an AAh then a 55h to the Timed Access register (location C7h) opens a 3 cycle window for write access. The window allows software to modify a protected bit(s). If these instructions do not immediately precede the write operation, then the write will not take effect. The protected bits are:

EXIF.0	BGS	Band–gap Select
WDCON.6	POR	Power–on Reset flag
WDCON.1	EWT	Enable Watchdog Reset
WDCON.0	RWT	Restart Watchdog
WDCON.3	WDIF	Watchdog Interrupt Flag
ROMSIZE.2	RMS2	ROM size select 2
ROMSIZE.1	RMS1	ROM size select 1
ROMSIZE.0	RMS0	ROM size select 0
TRIM.7–0		All RTC trim functions
RTCC.2	RTCWE	RTC Write Enable
RTCC.0	RTCE	RTC Oscillator Enable

EPROM PROGRAMMING

The DS87C530 follows standards for a 16K byte EPROM version in the 8051 family. It is available in a UV erasable, ceramic windowed package and in plastic packages for one–time user–programmable versions. The part has unique signature information so programmers can support its specific EPROM options.

PROGRAMMING PROCEDURE

The DS87C530 should run from a clock speed between 4 and 6 MHz when programmed. The programming fixture should apply address information for each byte to the address lines and the data value to the data lines. The control signals must be manipulated as shown in Table 10. The diagram in Figure 5 shows the expected electrical connection for programming. Note that the programmer must apply addresses in demultiplexed fashion to Ports 1 and 2 with data on Port 0. Waveforms and timing are provided in the Electrical Specifications. Program the DS87C530 as follows:

1. Apply the address value,
2. Apply the data value,
3. Select the programming option from Table 10 using the control signals,
4. Increase the voltage on V_{PP} from 5V to 12.75V if writing to the EPROM,
5. Pulse the $\overline{PROG}$ signal five times for EPROM array and 25 times for encryption table, lock bits, and other EPROM bits,
6. Repeat as many times as necessary.

SECURITY OPTIONS

The DS87C530 employs a standard three–level lock that restricts viewing of the EPROM contents. A 64–byte Encryption Array allows the authorized user to verify memory by presenting the data in encrypted form.

Lock Bits

The security lock consists of three lock bits. These bits select a total of 4 levels of security. Higher levels provide increasing security but also limit application flexibility. Table 11 shows the security settings. Note that the programmer cannot directly read the state of the security lock. User software has access to this information as described in the Memory section.

Encryption Array

The Encryption Array allows an authorized user to verify EPROM without allowing the true memory to be dumped. During a verify, each byte is Exclusive NORed (XNOR) with a byte in the Encryption Array. This results in a true representation of the EPROM while the Encryption is unprogrammed (FFh). Once the Encryption Array is programmed in a non–FFh state, the verify value will be encrypted.

For encryption to be effective, the Encryption Array must be unknown to the party that is trying to verify memory. The entire EPROM also should be a non–FFh state or the Encryption Array can be discovered.

The Encryption Array is programmed as shown in Table 10. Note that the programmer can not read the array. Also note that the verify operation always uses the Encryption Array. The array has no impact while FFh. Simply programming the array to a non–FFh state will cause the encryption to function.

OTHER EPROM OPTIONS

The DS87C530 has user selectable options that must be set before beginning software execution. These options use EPROM bits rather than SFRs.

Program the EPROM selectable options as shown in Table 10. The Option Register sets or reads these selections. The bits in the Option Control Register have the following function:

Bit 7 –4 Reserved, program to a 1.

Bit 3 Watchdog POR default. Set=1; Watchdog reset function is disabled on power–up. Set=0; Watchdog reset function is enabled automatically.

Bit 2–0 Reserved. Program to a 1.

SIGNATURE

The Signature bytes identify the product and programming revision to EPROM programmers. This information is at programming addresses 30h, 31h, and 60h. This information is as follows::

Address	Value	Meaning
30h	DAh	Manufacturer
31h	30h	Model
60h	01h	Extension

EPROM PROGRAMMING MODES Table 10

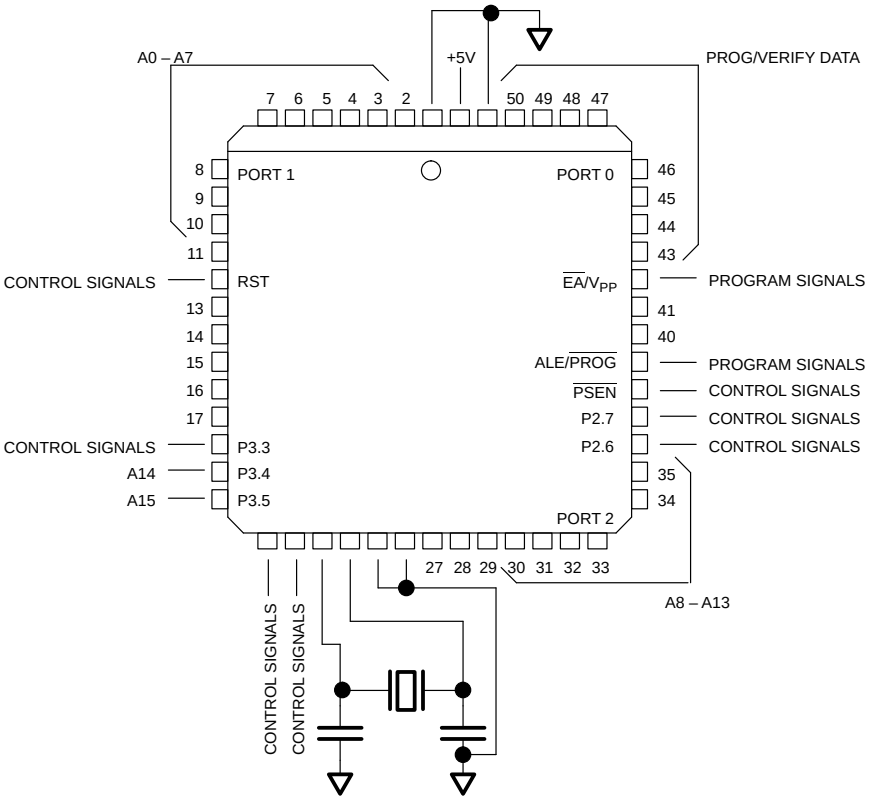
MODE		RST	$\overline{\text{PSEN}}$	ALE/$\overline{\text{PROG}}$	EA/VPP	P2.6	P2.7	P3.3	P3.6	P3.7
Program Code Data		H	L	PL	12.75V	L	H	H	H	H
Verify Code Data		H	L	H	H	L	L	L	H	H
Program Encryption Array Address 0–3Fh		H	L	PL	12.75V	L	H	H	L	H
Program Lock Bits	LB1	H	L	PL	12.75V	H	H	H	H	H
	LB2	H	L	PL	12.75V	H	H	H	L	L
	LB3	H	L	PL	12.75V	H	L	H	H	L
Program Option Register Address FCh		H	L	PL	12.75V	L	H	H	L	L
Read Signature or Option Registers 30, 31, 60, FCh		H	L	H	H	L	L	L	L	L

* PL indicates pulse to a logic low.

EPROM LOCK BITS Table 11

LEVEL	LOCK BITS			PROTECTION
	LB1	LB2	LB3	
1	U	U	U	No program lock. Encrypted verify if encryption table was programmed.
2	P	U	U	Prevent MOVC instructions in external memory from reading program bytes in internal memory. $\overline{\text{EA}}$ is sampled and latched on reset. Allow no further programming of EPROM.
3	P	P	U	Level 2 plus no verify operation. Also, prevent MOVX instructions in external memory from reading SRAM (MOVX) in internal memory.
4	P	P	P	Level 3 plus no external execution.

EPROM PROGRAMMING CONFIGURATION Figure 5



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC}=4.0V to 5.5V)

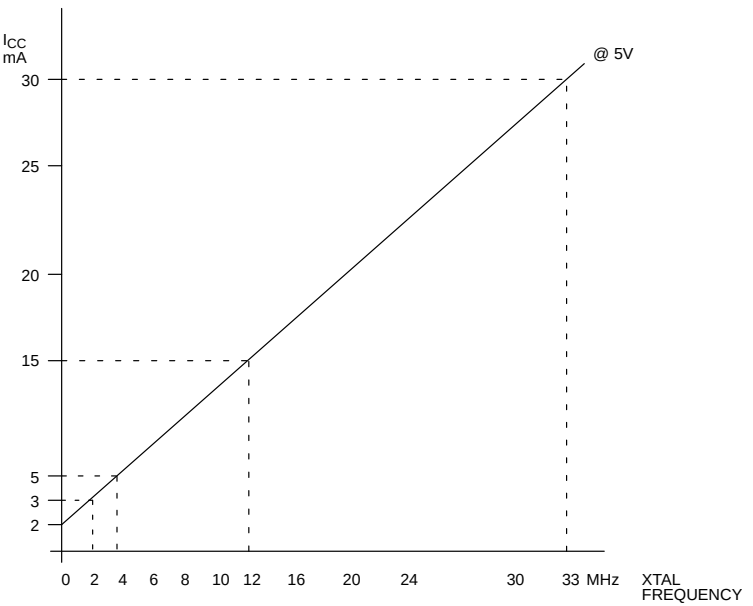
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Power–fail Warning	V_{PFW}	4.25	4.38	4.5	V	1
Minimum Operating Voltage	V_{RST}	4.0	4.13	4.25	V	1
Backup Battery Voltage	V_{BAT}	2.5	3.0	V_{CC}–0.7	V	
Supply Current Active Mode @ 33 MHz	I_{CC}		30		mA	2
Supply Current Idle Mode @ 33 MHz	I_{Idle}		15		mA	3
Supply Current Stop Mode, Band–gap Disabled	I_{Stop}		1		µA	4
Supply Current Stop Mode, Band–gap Enabled	I_{SPBG}		50		µA	4
Backup Supply Current, Data Retention Mode	I_{BAT}	0		0.5	µA	11
Input Low Level	V_{IL}	–0.3		+0.8	V	1
Input High Level	V_{IH}	2.0		V_{CC}+0.3	V	1
Input High Level XTAL1 and RST	V_{IH2}	3.5		V_{CC}+0.3	V	1
Output Low Voltage @ I_{OL}=1.6 mA	V_{OL1}		0.15	0.45	V	1
Output Low Voltage Ports 0, 2, ALE, and $\overline{PSEN}$ @ I_{OL}=3.2 mA	V_{OL2}		0.15	0.45	V	1
Output High Voltage Ports 1, 2, 3, ALE, $\overline{PSEN}$ @ I_{OH}=–50 µA	V_{OH1}	2.4			V	1,6
Output High Voltage Ports 1, 2, 3 @ I_{OH}= –1.5 mA	V_{OH2}	2.4			V	1, 7
Output High Voltage Port 0 in Bus Mode I_{OH}= –8 mA	V_{OH3}	2.4			V	1, 5
Input Low Current Ports 1, 2, 3 @ 0.45V	I_{IL}			–55	µA	
Transition Current from 1 to 0 Ports 1, 2, 3 @ 2V	I_{TL}			–650	µA	8
Input Leakage Port 0, $\overline{EA}$ pins, I/O Mode	I_L	–10		+10	µA	10
Input Leakage Port 0, Bus Mode	I_L	–300		+300	µA	9
RST Pull–down Resistance	R_{RST}	50		170	kΩ	

NOTES FOR DC ELECTRICAL CHARACTERISTICS:

All parameters apply to both commercial and industrial temperature operation unless otherwise noted.

1. All voltages are referenced to ground.
2. Active current is measured with a 33 MHz clock source driving XTAL1, V_{CC}=RST=5.5V, all other pins disconnected.
3. Idle mode current is measured with a 33 MHz clock source driving XTAL1, V_{CC}=5.5V, RST at ground, all other pins disconnected.
4. Stop mode current measured with XTAL1 and RST grounded, V_{CC}=5.5V, all other pins disconnected. This value is not guaranteed. Users that are sensitive to this specification should contact Dallas Semiconductor for more information.
5. When addressing external memory.
6. RST=V_{CC}. This condition mimics operation of pins in I/O mode. Port 0 is tristated in reset and when at a logic high state during I/O mode.
7. During a 0 to 1 transition, a one–shot drives the ports hard for two clock cycles. This measurement reflects port in transition mode.
8. Ports 1, 2, and 3 source transition current when being pulled down externally. It reaches its maximum at approximately 2V.
9. 0.45<V_{IN}<V_{CC}. Not a high impedance input. This port is a weak address holding latch in Bus Mode. Peak current occurs near the input transition point of the latch, approximately 2V.
10. 0.45<V_{IN}<V_{CC}. RST=V_{CC}. This condition mimics operation of pins in I/O mode.
11. V_{CC}=0V, V_{BAT}=3.3V. 32.768 KHz crystal with 12.5 pF load capacitance between RTCX1 and RTCX2 pins. RTCE bit set to 1.

TYPICAL I_{CC} VERSUS FREQUENCY Figure 6



AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC}=4.0V to 5.5V)

PARAMETER	SYMBOL	33 MHz		VARIABLE CLOCK		UNITS
		MIN	MAX	MIN	MAX	
Oscillator Frequency	$1/t_{CLCL}$	0	33	0	33	MHz
ALE Pulse Width	t_{LHLL}	40		$1.5t_{CLCL}-5$		ns
Port 0 Address Valid to ALE Low	t_{AVLL}	10		$0.5t_{CLCL}-5$		ns
Address Hold after ALE Low	t_{LLAX1}	10		$0.5t_{CLCL}-5$		ns
ALE Low to Valid Instruction In	t_{LLIV}		56		$2.5t_{CLCL}-20$	ns
ALE Low to $\overline{PSEN}$ Low	t_{LLPL}	10		$0.5t_{CLCL}-5$		ns
$\overline{PSEN}$ Pulse Width	t_{PLPH}	55		$2t_{CLCL}-5$		ns
$\overline{PSEN}$ Low to Valid Instr. In	t_{PLIV}		41		$2t_{CLCL}-20$	ns
Input Instruction Hold after $\overline{PSEN}$	t_{PXIX}	0		0		ns
Input Instruction Float after $\overline{PSEN}$	t_{PXIZ}		26		$t_{CLCL}-5$	ns
Port 0 Address to Valid Instr. In	t_{AVIV}		71		$3t_{CLCL}-20$	ns
Port 2 Address to Valid Instr. In	t_{AVIV2}		81		$3.5t_{CLCL}-25$	ns
$\overline{PSEN}$ Low to Address Float	t_{PLAZ}		0		0	ns

NOTES FOR AC ELECTRICAL CHARACTERISTICS:

All parameters apply to both commercial and industrial temperature range operation unless otherwise noted. All signals rated over operating temperature. All signals characterized with load capacitance of 80 pF except Port 0, ALE, $\overline{PSEN}$, $\overline{RD}$ and $\overline{WR}$ with 100 pF. Interfacing to memory devices with float times (turn off times) over 25 ns may cause contention. This will not damage the parts, but will cause an increase in operating current.

MOVX CHARACTERISTICS USING STRETCH MEMORY CYCLES (0°C to 70°C; V_{CC}=4.0V to 5.5V)

PARAMETER	SYMBOL	VARIABLE CLOCK		UNITS	STRETCH
		MIN	MAX		
Data Access ALE Pulse Width	t_{LHLL2}	$1.5t_{CLCL}$–5 $2t_{CLCL}$–5		ns	t_{MCS}=0 t_{MCS}>0
Address Hold after ALE Low for MOVX Write	t_{LLAX2}	$0.5t_{CLCL}$–5 t_{CLCL}–5		ns	t_{MCS}=0 t_{MCS}>0
$\overline{RD}$ Pulse Width	t_{RLRH}	$2t_{CLCL}$–5 t_{MCS}–10		ns	t_{MCS}=0 t_{MCS}>0
$\overline{WR}$ Pulse Width	t_{WLWH}	$2t_{CLCL}$–5 t_{MCS}–10		ns	t_{MCS}=0 t_{MCS}>0
$\overline{RD}$ Low to Valid Data In	t_{RLDV}		$2t_{CLCL}$–20 t_{MCS}–20	ns	t_{MCS}=0 t_{MCS}>0
Data Hold after Read	t_{RHDX}	0		ns	
Data Float after Read	t_{RHDZ}		t_{CLCL}–5 $2t_{CLCL}$–5	ns	t_{MCS}=0 t_{MCS}>0
ALE Low to Valid Data In	t_{LLDV}		$2.5t_{CLCL}$–20 t_{MCS}+t_{CLCL}–40	ns	t_{MCS}=0 t_{MCS}>0
Port 0 Address to Valid Data In	t_{AVDV1}		$3t_{CLCL}$–20 t_{MCS}+$1.5t_{CLCL}$–20	ns	t_{MCS}=0 t_{MCS}>0
Port 2 Address to Valid Data In	t_{AVDV2}		$3.5t_{CLCL}$–20 t_{MCS}+$2t_{CLCL}$–20	ns	t_{MCS}=0 t_{MCS}>0
ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	t_{LLWL}	$0.5t_{CLCL}$–5 t_{CLCL}–5	$0.5t_{CLCL}$+5 t_{CLCL}+5	ns	t_{MCS}=0 t_{MCS}>0
Port 0 Address to $\overline{RD}$ or $\overline{WR}$ Low	t_{AVWL1}	t_{CLCL}–5 $2t_{CLCL}$–5		ns	t_{MCS}=0 t_{MCS}>0
Port 2 Address to $\overline{RD}$ or $\overline{WR}$ Low	t_{AVWL2}	$1.5t_{CLCL}$–10 $2.5t_{CLCL}$–10		ns	t_{MCS}=0 t_{MCS}>0
Data Valid to $\overline{WR}$ Transition	t_{QVWX}	–5		ns	
Data Hold after Write	t_{WHQX}	t_{CLCL}–5 $2t_{CLCL}$–5		ns	t_{MCS}=0 t_{MCS}>0
$\overline{RD}$ Low to Address Float	t_{RLAZ}		$–0.5t_{CLCL}$–5	ns	
$\overline{RD}$ or $\overline{WR}$ High to ALE High	t_{WHLH}	0 t_{CLCL}–5	10 t_{CLCL}+5	ns	t_{MCS}=0 t_{MCS}>0

NOTE: t_{MCS} is a time period related to the Stretch memory cycle selection. The following table shows the value of t_{MCS} for each Stretch selection.

M2	M1	M0	MOVX CYCLES	t_{MCS}
0	0	0	2 machine cycles	0
0	0	1	3 machine cycles (default)	4 t_{CLCL}
0	1	0	4 machine cycles	8 t_{CLCL}
0	1	1	5 machine cycles	12 t_{CLCL}
1	0	0	6 machine cycles	16 t_{CLCL}
1	0	1	7 machine cycles	20 t_{CLCL}
1	1	0	8 machine cycles	24 t_{CLCL}
1	1	1	9 machine cycles	28 t_{CLCL}

EXTERNAL CLOCK CHARACTERISTICS

(0°C to 70°C; V_{CC}=4.0V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Clock High Time	t_{CHCX}	10			ns	
Clock Low Time	t_{CLCX}	10			ns	
Clock Rise Time	t_{CLCL}			5	ns	
Clock Fall Time	t_{CHCL}			5	ns	

SERIAL PORT MODE 0 TIMING CHARACTERISTICS

(0°C to 70°C; V_{CC}=4.0V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Serial Port Clock Cycle Time SM2=0, 12 clocks per cycle SM2=1, 4 clocks per cycle	t_{XLXL}		 $12t_{CLCL}$ $4t_{CLCL}$		 ns ns	
Output Data Setup to Clock Rising SM2=0, 12 clocks per cycle SM2=1, 4 clocks per cycle	t_{QVXH}		 $10t_{CLCL}$ $3t_{CLCL}$		 ns ns	
Output Data Hold from Clock Rising SM2=0, 12 clocks per cycle SM2=1, 4 clocks per cycle	t_{XHQX}		 $2t_{CLCL}$ t_{CLCL}		 ns ns	
Input Data Hold after Clock Rising SM2=0, 12 clocks per cycle SM2=1, 4 clocks per cycle	t_{XHDX}		 t_{CLCL} t_{CLCL}		 ns ns	
Clock Rising Edge to Input Data Valid SM2=0, 12 clocks per cycle SM2=1, 4 clocks per cycle	t_{XHDV}		 $11t_{CLCL}$ $3t_{CLCL}$		 ns ns	

EXPLANATION OF AC SYMBOLS

In an effort to remain compatible with the original 8051 family, this device specifies the same parameters as such devices, using the same symbols. For completeness, the following is an explanation of the symbols.

t	Time
A	Address
C	Clock
D	Input data
H	Logic level high
L	Logic level low
I	Instruction
P	$\overline{\text{PSEN}}$
Q	Output data
R	$\overline{\text{RD}}$ signal
V	Valid
W	$\overline{\text{WR}}$ signal
X	No longer a valid logic level
Z	Tristate

POWER CYCLE TIMING CHARACTERISTICS

(0°C to 70°C; V_{CC}=4.0V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Cycle Start–up Time	t_{CSU}		1.8		ms	1
Power–on Reset Delay	t_{POR}			65536	t_{CLCL}	2

NOTES FOR POWER CYCLE TIMING:

1. Start–up time for crystals varies with load capacitance and manufacturer. Time shown is for an 11.0592 MHz crystal manufactured by Fox.
2. Reset delay is a synchronous counter of crystal oscillations after crystal start–up. At 33 MHz, this time is 1.99 ms.

EPROM PROGRAMMING AND VERIFICATION

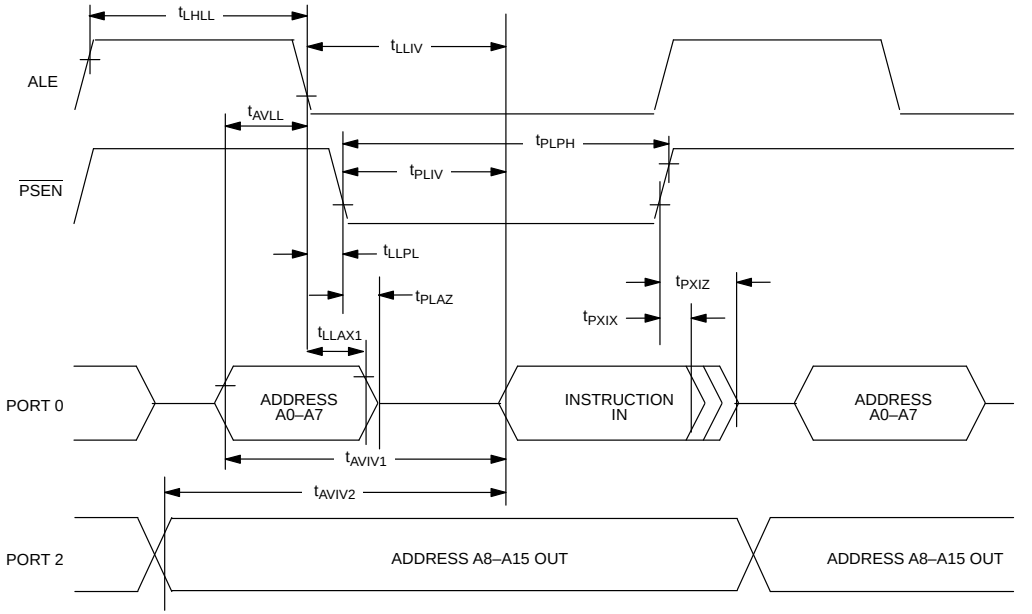
(21°C to 27°C; V_{CC}=4.5V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Programming Voltage	V_{PP}	12.5		13.0	V	1
Programming Supply Current	I_{PP}			50	mA	
Oscillator Frequency	$1/t_{CLCL}$	4		6	MHz	
Address Setup to $\overline{PROG}$ Low	t_{AVGL}	$48t_{CLCL}$				
Address Hold after $\overline{PROG}$	t_{GHAX}	$48t_{CLCL}$				
Data Setup to $\overline{PROG}$ Low	t_{DVGL}	$48t_{CLCL}$				
Data Hold after $\overline{PROG}$	t_{GHDX}	$48t_{CLCL}$				
Enable High to V_{PP}	t_{EHSH}	$48t_{CLCL}$				
V_{PP} Setup to $\overline{PROG}$ Low	t_{SHGL}	10			µs	
V_{PP} Hold after $\overline{PROG}$	t_{GHSL}	10			µs	
$\overline{PROG}$ Width	t_{GLGH}	90		110	µs	
Address to Data Valid	t_{AVQV}			$48t_{CLCL}$		
Enable Low to Data Valid	t_{ELQV}			$48t_{CLCL}$		
Data Float after Enable	t_{EHQZ}	0		$48t_{CLCL}$		
$\overline{PROG}$ High to $\overline{PROG}$ Low	t_{GHGL}	10			µs	

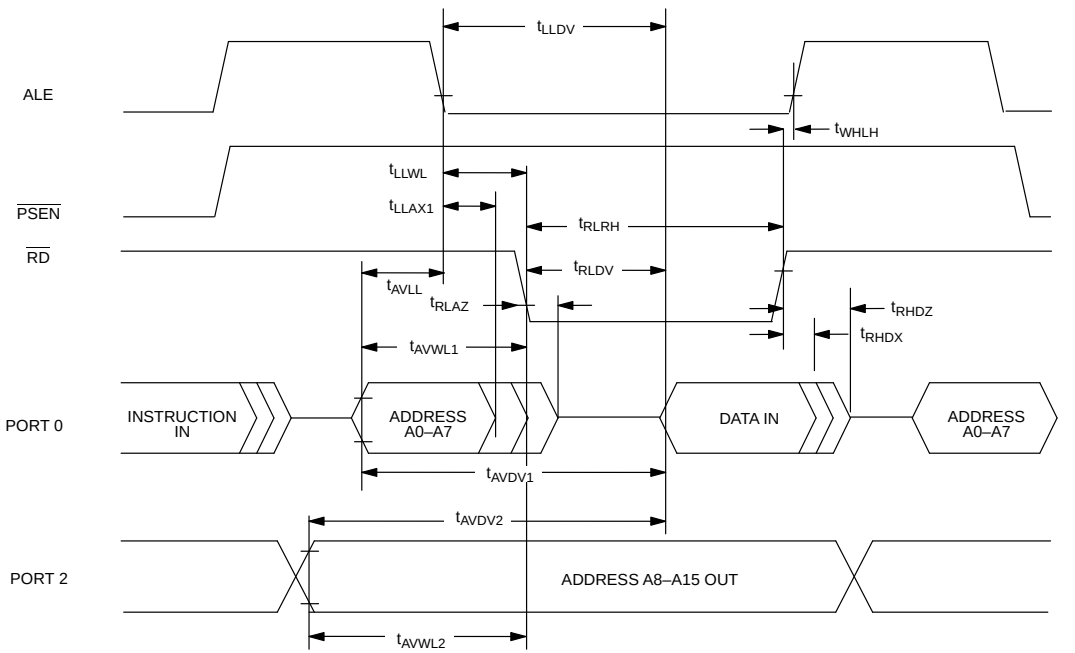
NOTE:

1. All voltages are referenced to ground.

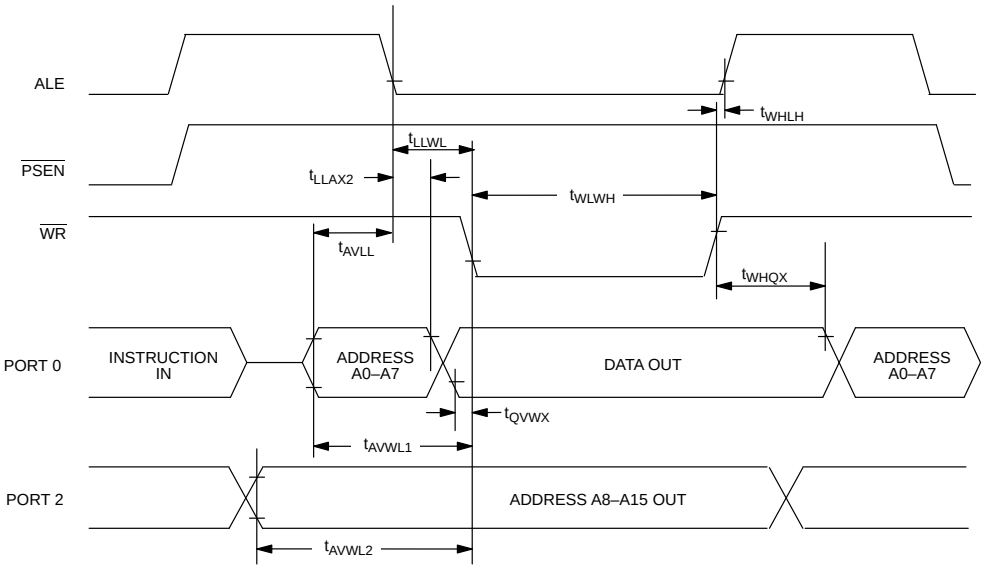
EXTERNAL PROGRAM MEMORY READ CYCLE



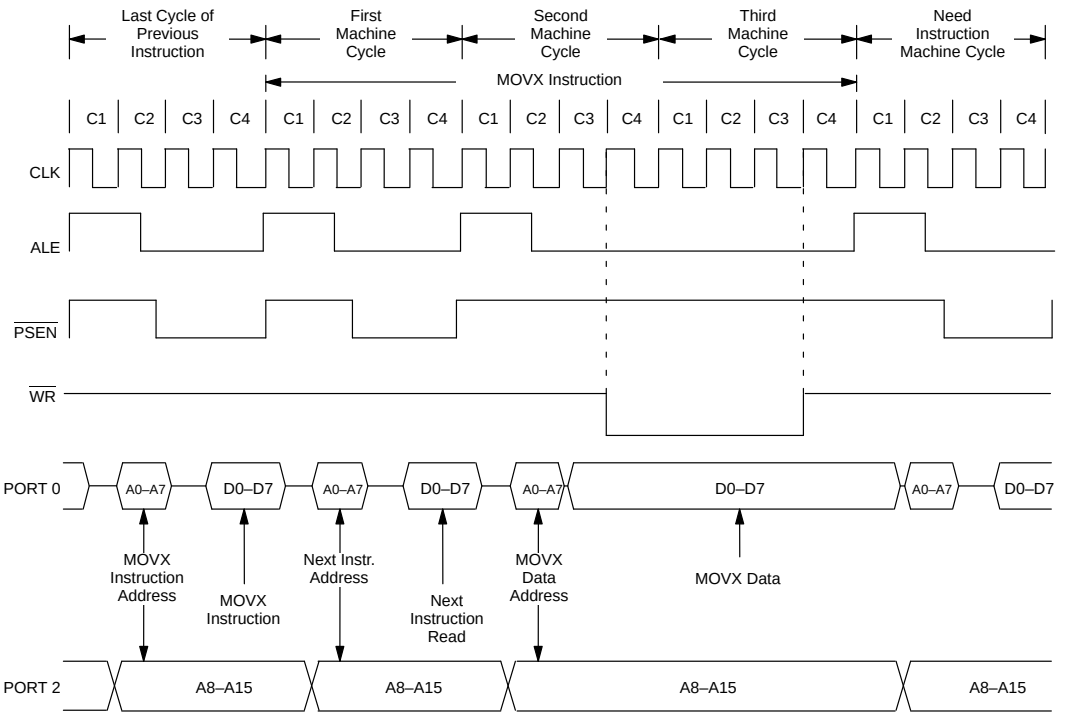
EXTERNAL DATA MEMORY READ CYCLE



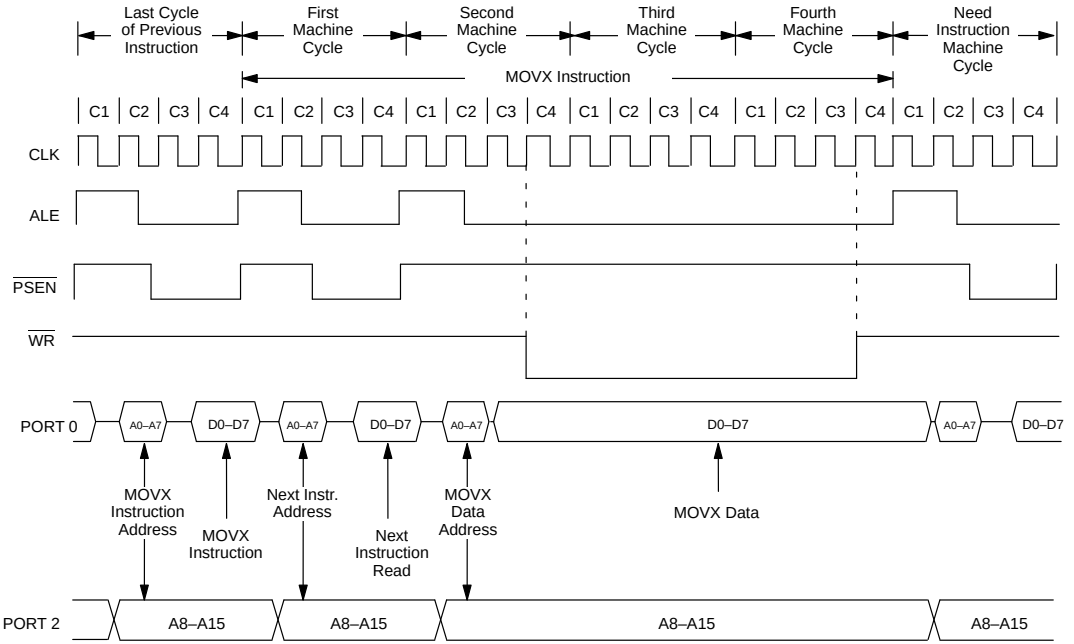
DATA MEMORY WRITE CYCLE



DATA MEMORY WRITE WITH STRETCH=1

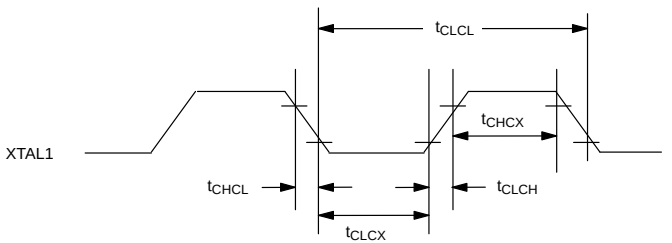


DATA MEMORY WRITE WITH STRETCH=2



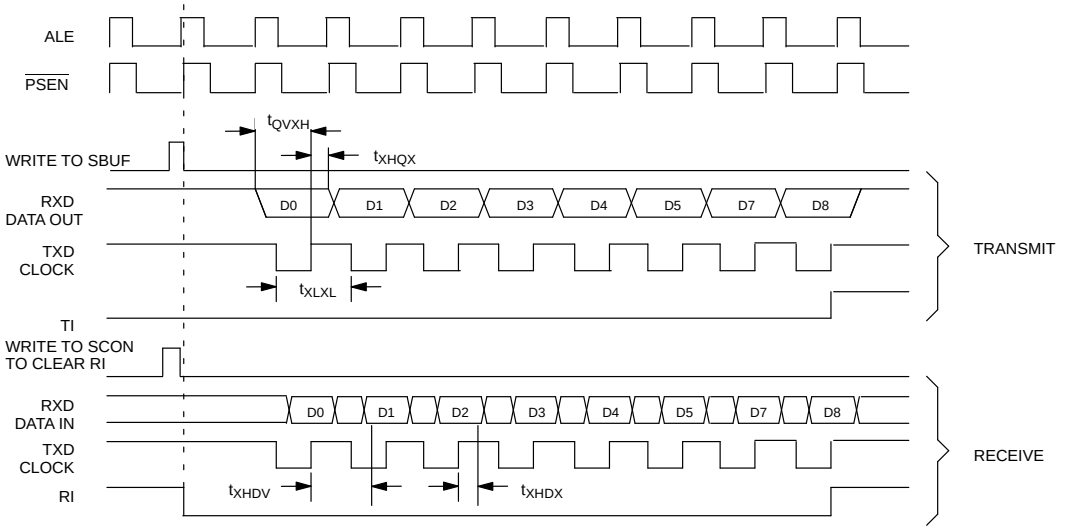
FOUR CYCLE DATA MEMORY WRITE
STRETCH VALUE=2

EXTERNAL CLOCK DRIVE

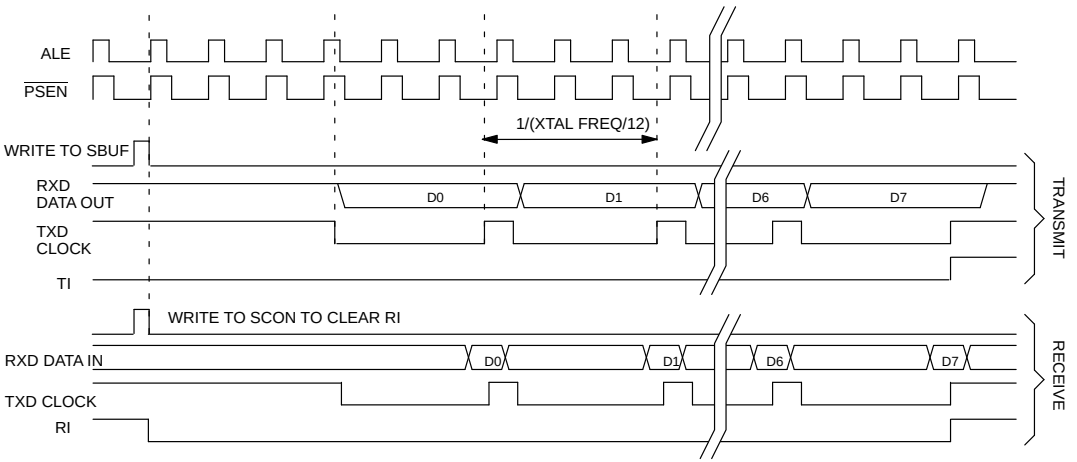


SERIAL PORT MODE 0 TIMING

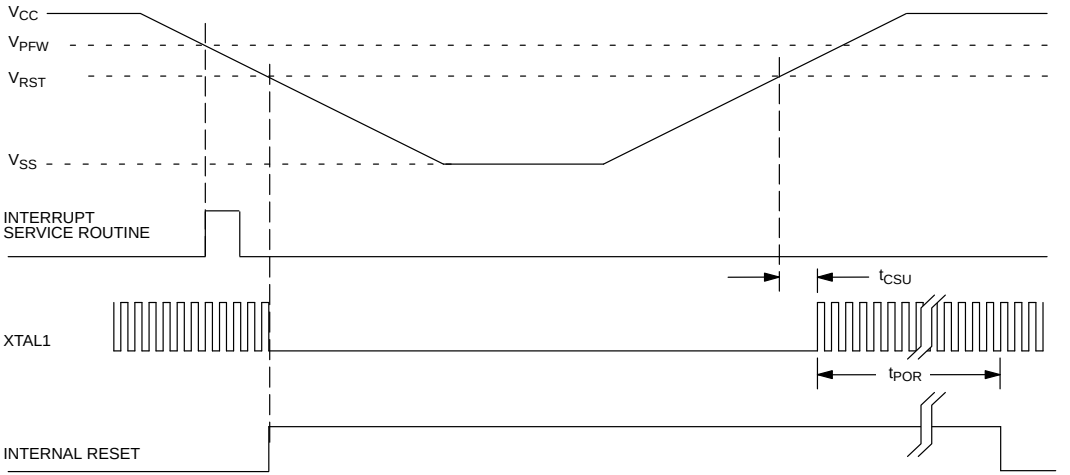
SERIAL PORT 0 (SYNCHRONOUS MODE)
HIGH SPEED OPERATION SM2=1=>TXD CLOCK=XTAL/4



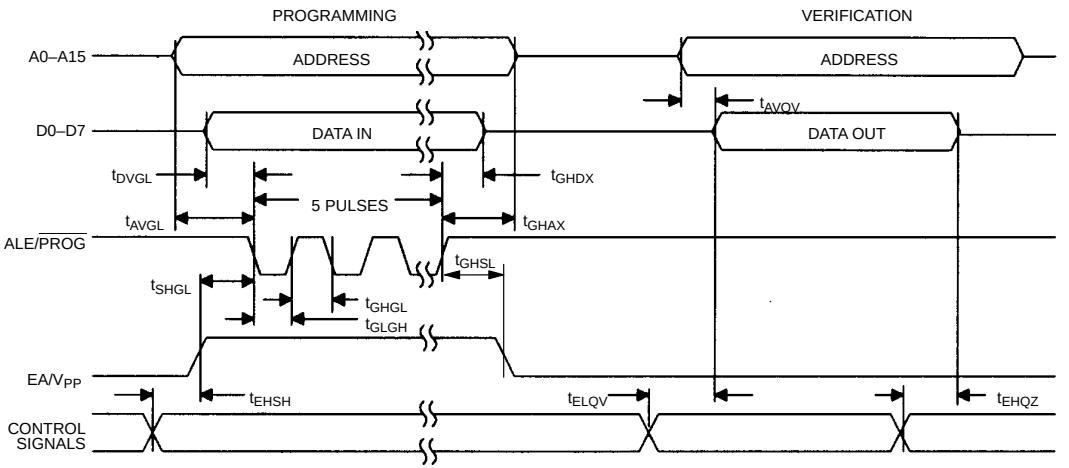
SERIAL PORT 0 (SYNCHRONOUS MODE)
SM2=0=>TXD CLOCK=XTAL/12



POWER CYCLE TIMING

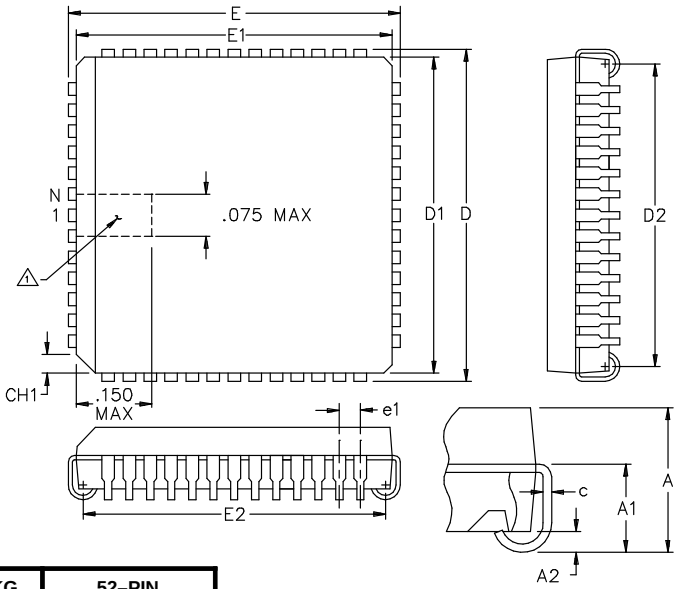


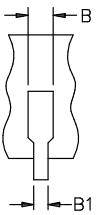
EPROM PROGRAMMING AND VERIFICATION WAVEFORMS



52–PIN PLCC

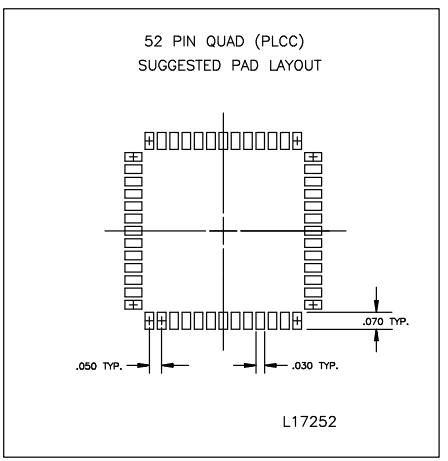
NOTE:
1. PIN–1 IDENTIFIER TO BE LOCATED IN ZONE INDICATED.
2. CONTROLLING DIMENSIONS ARE IN INCHES.



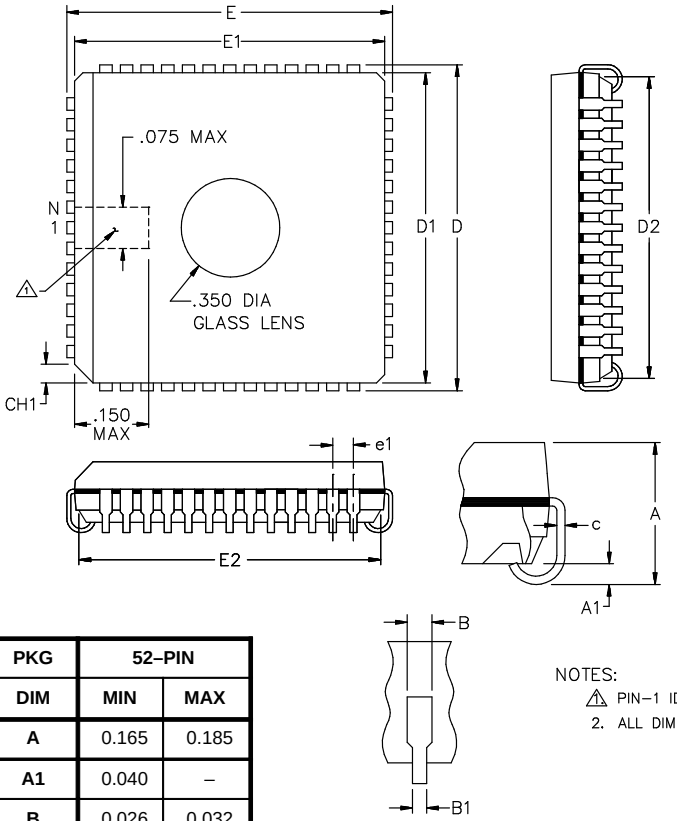


PKG	52–PIN	
DIM	MIN	MAX
A	0.165	0.180
A1	0.090	0.120
A2	0.020	–
B	0.026	0.032
B1	0.013	0.021
c	0.008	0.013
CH1	0.042	0.048
D	0.785	0.795
D1	0.750	0.756
D2	0.690	0.730
E	0.785	0.795
E1	0.750	0.756
E2	0.690	0.730
e1	0.050 BSC	
N	52	–

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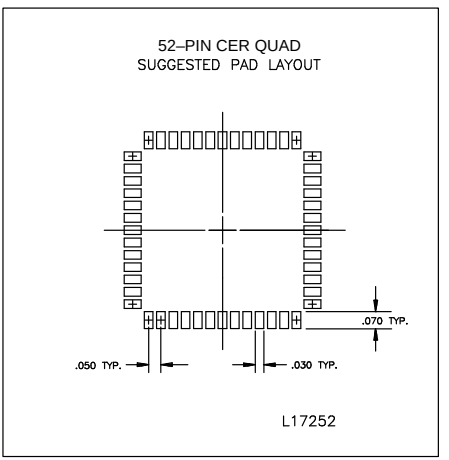
52–PIN CER QUAD



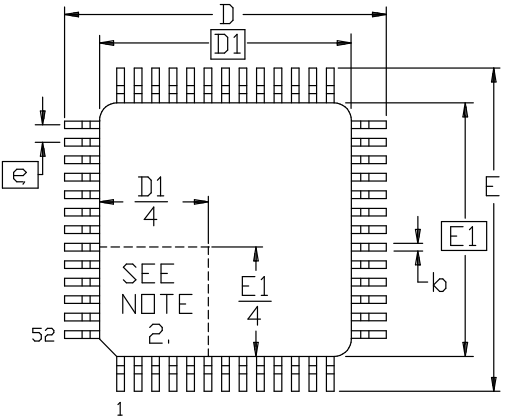
PKG	52–PIN	
DIM	MIN	MAX
A	0.165	0.185
A1	0.040	–
B	0.026	0.032
B1	0.013	0.021
c	0.008	0.013
CH1–45°	0.035	0.040
D	0.760	0.800
D1	0.740	0.770
D2	0.700	0.730
E	0.760	0.800
E1	0.740	0.770
E2	0.700	0.730
e1	0.050 BSC	
N	52	–

NOTES:
1. PIN–1 IDENTIFIER TO BE LOCATED IN ZONE INDICATED.
2. ALL DIMENSIONS SHOWN ARE IN INCHES.

56–G4007–001

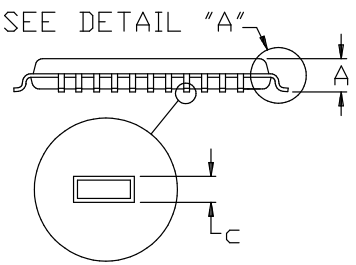


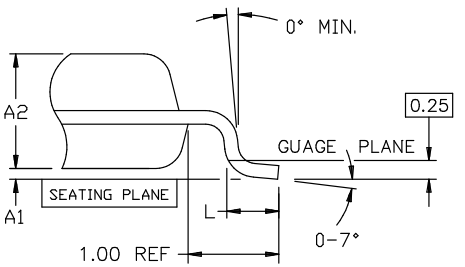
52–PIN TQFP



NOTES:

1. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH, BUT DO NOT INCLUDE MOLD PROTRUSION; ALLOWABLE PROTRUSION IS 0.254 MM ON D1 AND E1.
2. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
3. ALLOWABLE DAMBAR PROTRUSION IS 0.08 MM TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION. PROTRUSION NOT TO BE LOCATED ON LOWER RADIUS OR FOOT OF LEAD.

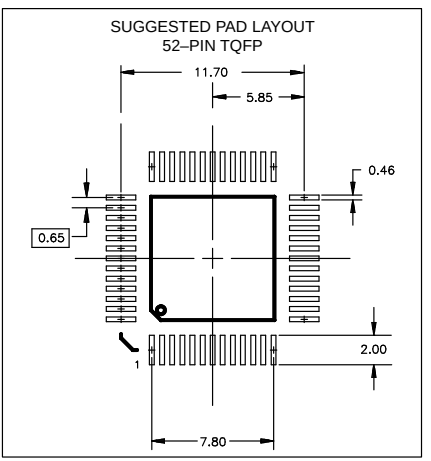




DETAIL A

DIMENSIONS ARE IN MILLIMETERS

PKG	52–PIN		
DIM	MIN	NOM	MAX
A	–	–	1.20
A1	0.05	0.10	0.15
A2	0.95	1.00	1.05
b	0.25	0.32	0.40
c	0.09	–	0.20
D	11.80	12.00	12.20
D1	10.00 BSC		
E	11.80	12.00	12.20
E1	10.00 BSC		
e	0.65 BSC		
L	0.45	0.60	0.75



DATA SHEET REVISION SUMMARY

The following represent the key differences between 06/08/95 and 02/20/97 version of the DS87C530 data sheet. Please review this summary carefully.

1. Update ALE pin description.
2. Add note pertaining to erasure window.
3. Add note pertaining to internal MOVX SRAM.
4. Change Note 6 from RST=5.5V to RST=V_{CC}.
5. Change Note 10 from RST=5.5V to RST=V_{CC}.
6. Change serial port mode 0 timing diagram label from t_{QVXL} to t_{QVXH}.
7. Add information pertaining to 52–pin TQFP package.