Rev 0; 10/08

HART Modem

DS8500

General Description

The DS8500 is a single-chip modem with Highway Addressable Remote Transducer (HART) capabilities and satisfies the HART physical layer requirements. The device integrates the modulation and demodulation of the 1200Hz/2200Hz FSK signal, has very low power consumption, and needs only a few external components due to the integrated digital signal processing. The input signal is sampled by an analog-to-digital converter (ADC), followed by a digital filter/demodulator. This architecture ensures reliable signal detection in noisy environments. The output digital-to-analog converter (DAC) generates a sine wave and provides a clean signal with phase-continuous switching between 1200Hz and 2200Hz. Low power is achieved by disabling the receive circuits during transmit and vice versa. The DS8500 is ideal for low-power process control transmitters.

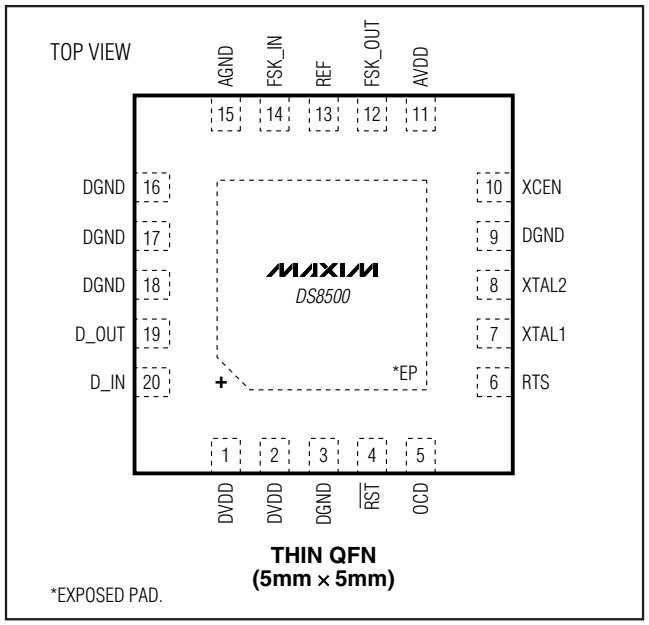
Applications

4–20mA Loop-Powered Transmitters for Temperature, Pressure, Flow, and Level Measurement

HART Multiplexers

HART Modem Interface Connectivity

Pin Configuration



Features

- **Single-Chip, Half-Duplex, 1200bps FSK Modulation and Demodulation**
- **Digital Signal Processing Provides Reliable Input Signal Detection in Noisy Conditions**
- **Sinusoidal Output Signal with Lowest Harmonic Distortion**
- **Few External Components Enable a Space-Saving Solution**
- **Standard Component 3.6864MHz Crystal**
- **Complies to HART Physical Layer Requirements**
- **2.7V to 3.6V Operating Voltage**
- **285µA (max) Current Consumption**
- **Space-Saving, 5mm x 5mm x 0.8mm, 20-Pin TQFN Package**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
DS8500-JND+	-40°C to +85°C	20 TQFN-EP*

+Denotes a lead-free/RoHS-compliant package.
**EP = Exposed pad.*

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

ABSOLUTE MAXIMUM RATINGS

Voltage Range on All Pins (including AVDD, DVDD) Relative to Ground .....-0.5V to +3.6V
Voltage Range on Any Pin Relative to Ground Except AVDD, DVDD .....-0.5V to (V_{DVDD} + 0.5V)

Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Soldering Temperature.....Refer to the IPC/JEDEC J-STD-020 Specification.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(V_{DVDD} = V_{AVDD} = 2.7V to 3.6V, T_A = -40°C to +85°C.) (Note 1)

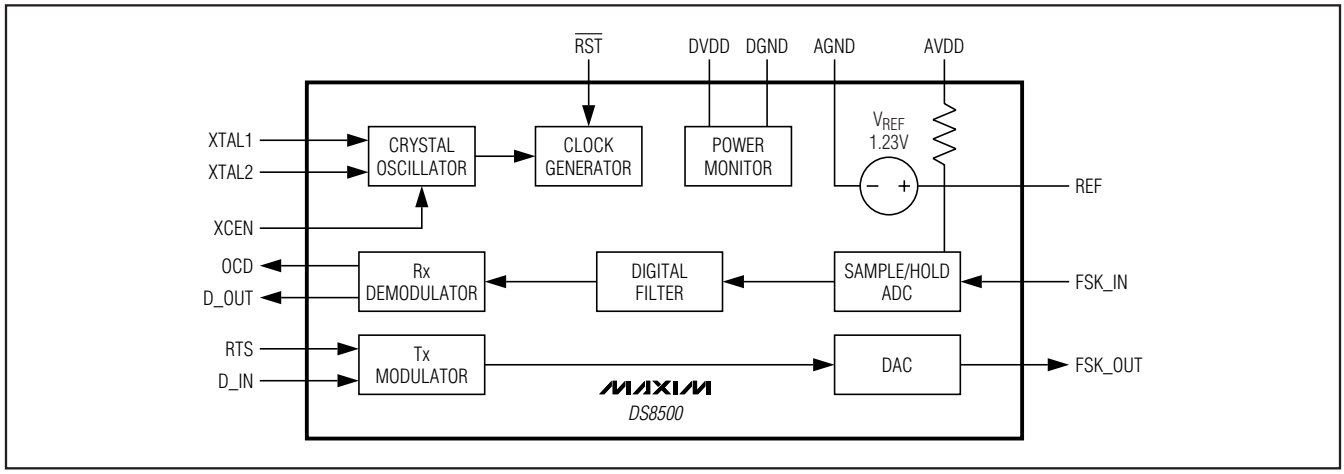
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Digital Supply Voltage	V_{DVDD}		2.7		3.6	V
Analog Supply Voltage	V_{AVDD}	V_{AVDD} = V_{DVDD}	2.7		3.6	V
Ground	GND	AGND = DGND	0		0	V
Digital Power-Fail Reset Voltage	V_{RST}	Monitors V_{DVDD}	2.59	2.64	2.69	V
Active Current	I_{DD}	V_{AVDD} = V_{DVDD} = 2.7V (Note 2)			285	µA
Input Low Voltage	V_{IL}		DGND		0.30 x V_{DVDD}	V
Input High Voltage	V_{IL}		0.75 x V_{DVDD}		V_{DVDD}	V
Output Low Voltage	V_{OL}	I_{OL} = 4mA	DGND		0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4mA	0.8 x V_{DVDD}			V
I/O Pin Capacitance	C_{IO}	Guaranteed by design (Note 3)			15	pF
$\overline{RST}$ Pullup Resistance	R_{RST}		19		45	kΩ
Input Leakage Current XTAL, $\overline{RST}$	I_{ILRX}		-30		+30	µA
Input Leakage Current All Other Pins	I_{IL}		-2		+2	µA
Input Low Current for $\overline{RST}$	I_{IL1}	V_{IN} = 0.4V			170	µA
CLOCK SOURCE						
External Clock Frequency	f_{HFIN}		-1%	3.6864	+1%	MHz
VOLTAGE REFERENCE						
Internal Reference Voltage	V_{REF}			1.23		V
FSK INPUT						
Input Voltage Range at FSK_IN			0		V_{REF}	V
FSK OUTPUT						
Output Voltage at FSK_OUT	V_{OUT}	AC-coupled max 30kΩ load	400	500	600	mV_{P-P}
Frequency of FSK_OUT (Note 4)		For a mark	-1%	1200	+1%	kHz
		For a space	-1%	2200	+1%	

Note 1: Specifications to -40°C are guaranteed by design and are not production tested.
Note 2: Active currents are measured when the device is driven by an external clock XCEN = 1 condition.
Note 3: Guaranteed by design and not production tested.
Note 4: Accuracy is guaranteed based on the external crystal or clock provided.

Pin Description

PIN	NAME	FUNCTION
1, 2	DVDD	Digital Supply Voltage
3, 9, 16, 17, 18	DGND	Digital Ground
4	$\overline{RST}$	Active-Low Reset, Digital Input/Output. This pin includes an internal pullup resistor and is driven low as an output when an internal reset condition occurs.
5	OCD	Carrier Detect, Digital Output. A logic-high indicates a valid carrier detection on FSK_IN. OCD = 1 when FSK_IN amplitude is greater than 120mV$_{P-P}$. OCD = 0 when FSK_IN amplitude is less than 80mV$_{P-P}$.
6	RTS	Request to Send, Digital Input. When set high, the device is put into the demodulator mode. A logic-low puts the device into modulator mode.
7	XTAL1	Crystal Pin or Input for External Clock at 3.6864MHz
8	XTAL2	Crystal Pin or Output of the Crystal Amplifier
10	XCEN	External Clock Enable, Digital Input. When set high, this pin allows the user to drive an external clock signal through XTAL1. When in this mode, XTAL2 should be left unconnected. An external crystal must be connected between XTAL1 and XTAL2 when set low.
11	AVDD	Analog Supply Voltage
12	FSK_OUT	FSK Out, Analog Output. Output of the modulator. Provides a phase-continuous, FSK-modulated output signal (1200Hz and 2200Hz output frequencies) to the 4mA to 20mA current loop interface circuit.
13	REF	Reference, Analog Output. The internal voltage reference is provided as output. This pin must be connected to a 0.1µF capacitor.
14	FSK_IN	FSK In, Analog Input. Input for the FSK-modulated HART receive signal from the 4mA to 20mA current loop interface circuit.
15	AGND	Analog Ground
19	D_OUT	Digital Data Out, Digital Output. Output from the demodulator.
20	D_IN	Digital Data In, Digital Input. Input to the modulator.

Block Diagram



HART Modem

Introduction to HART

HART is a backward-compatible enhancement to existing 4mA to 20mA instrumentation networks that allows two-way, half-duplex, digital communication with a microcontroller-based field device. The digital signal is encoded on top of the existing instrumentation signal. Communication is accomplished through a series of commands and responses dependent on the specific protocol and network topology. The DS8500 does not implement any portion of the communication protocol; it only handles the modulation and demodulation of the encoded information. Digital data is encoded using frequency-shift keying (FSK), which is illustrated in Figure 1. A “1” is identified as a mark symbol and is represented with a center frequency of 1.2kHz. A “0” is identified as a space symbol and is represented with a center frequency of 2.2kHz. This allows a throughput of 1.2kbps, with each symbol occupying an 833µs slot.

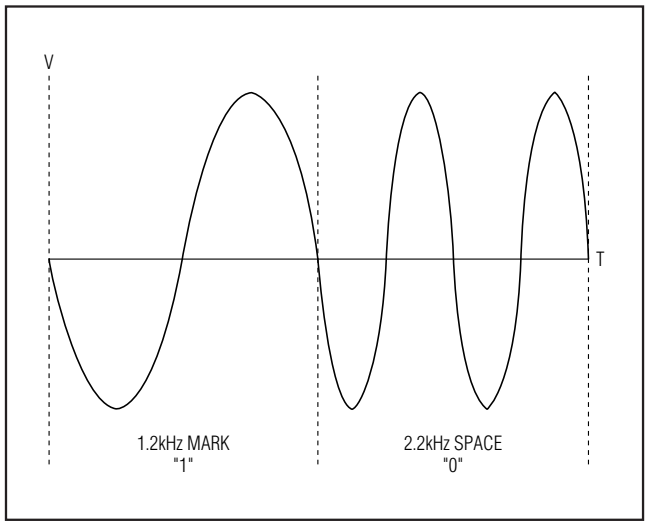


Figure 1. HART FSK Signal

Functional Description

The DS8500 modem chip consists of a demodulator, carrier detect, digital filter, ADC for input signal conversion, a modulator and DAC for output signal generation, and receive and transmit state machine blocks to perform the HART communication. The *Block Diagram* illustrates the interface between various blocks of circuitry.

The input HART signal’s noise interference is attenuated by a one-pole highpass filter that is external to the chip; the attenuated signal is digitized by the ADC and filtered by the receive state machine. The transmit state machine modulates the input to the HART-compliant signal with the help of the modulator and the DAC.

Modulator

The modulator performs the FSK modulation of the digital data at the D_IN input. The FSK-modulated sinusoidal signal is present at the FSK_OUT output as illustrated in Figure 1. The modulator is enabled by RTS being a logic-low. The modulation is done between 1200Hz (mark) or 2200Hz (space) depending on the logic level of the input signal. The modulator preserves a continuous phase when switching between frequencies to minimize the bandwidth of the transmitted signal.

Figure 2 illustrates an example waveform of the DS8500 in modulate mode. The data to be modulated is presented in a UART format (start, 8 data bits, parity, stop bit) at D_IN. FSK_OUT shows the modulated output.

Demodulator

The demodulator accepts an FSK signal at the FSK_IN input and reproduces the original modulating signal at the D_OUT output. The HART signal should be presented as an 11-bit UART character with a start, data, parity, and stop bits for proper operation of the demodulator block. The nominal bit rate of the D_OUT signal is 1200 bits per second. A simple RC filter is sufficient for anti-aliasing. Figure 3 illustrates an example waveform of the DS8500 in demodulate mode.

Applications Information

Figure 4 shows the typical application circuit. As the DS8500 integrates a digital filter, only a simple passive RC filter is required in front of the ADC. R3 and C3 implement a lowpass filter with a 10kHz cutoff frequency; C2 and R2/R1 implement a highpass filter with a 480Hz cutoff frequency. The resistor-divider formed by R1 and R2 provides an input bias voltage of $V_{REF}/2$ to the ADC input (R1 = R2).

The output DAC provides a sine-wave signal, and C4 provides the AC-coupled signal output from the DS8500. The typical value of C4 can be anything greater than 20nF based on the application.

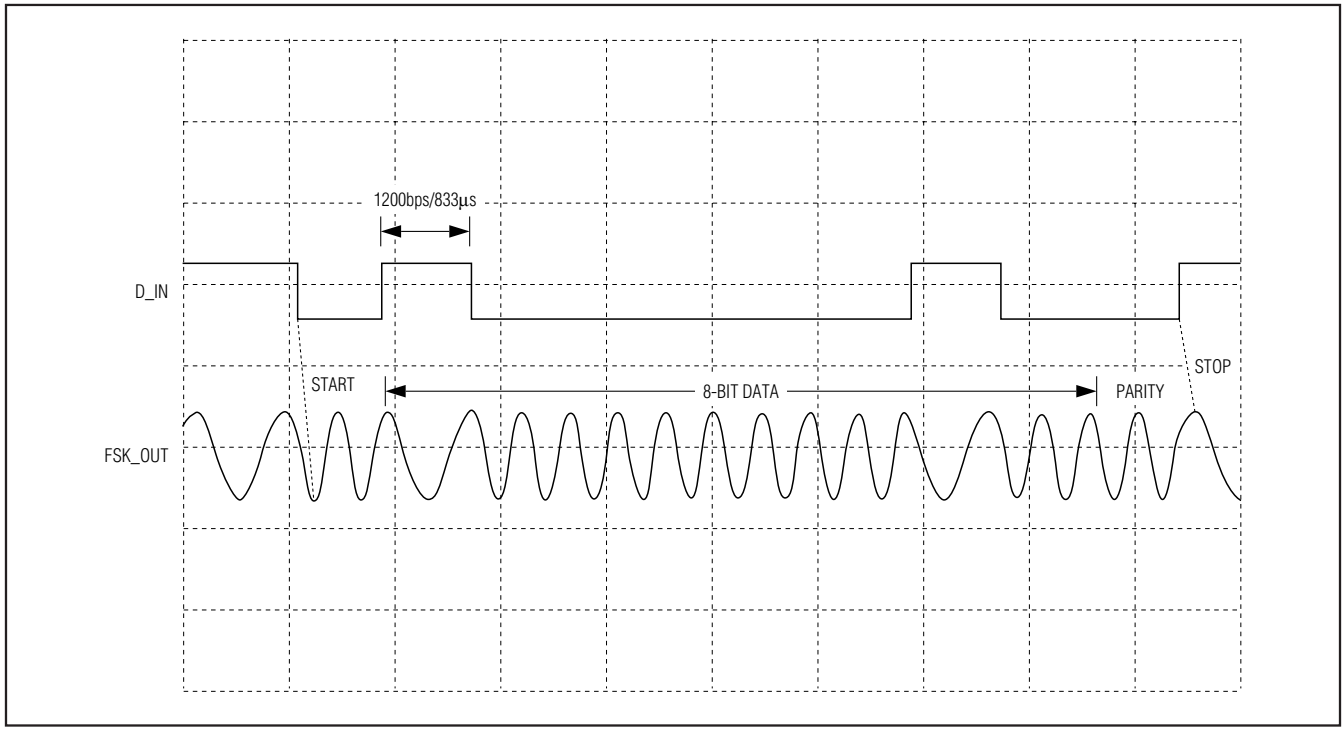


Figure 2. Actual DS8500 Modulator Waveform

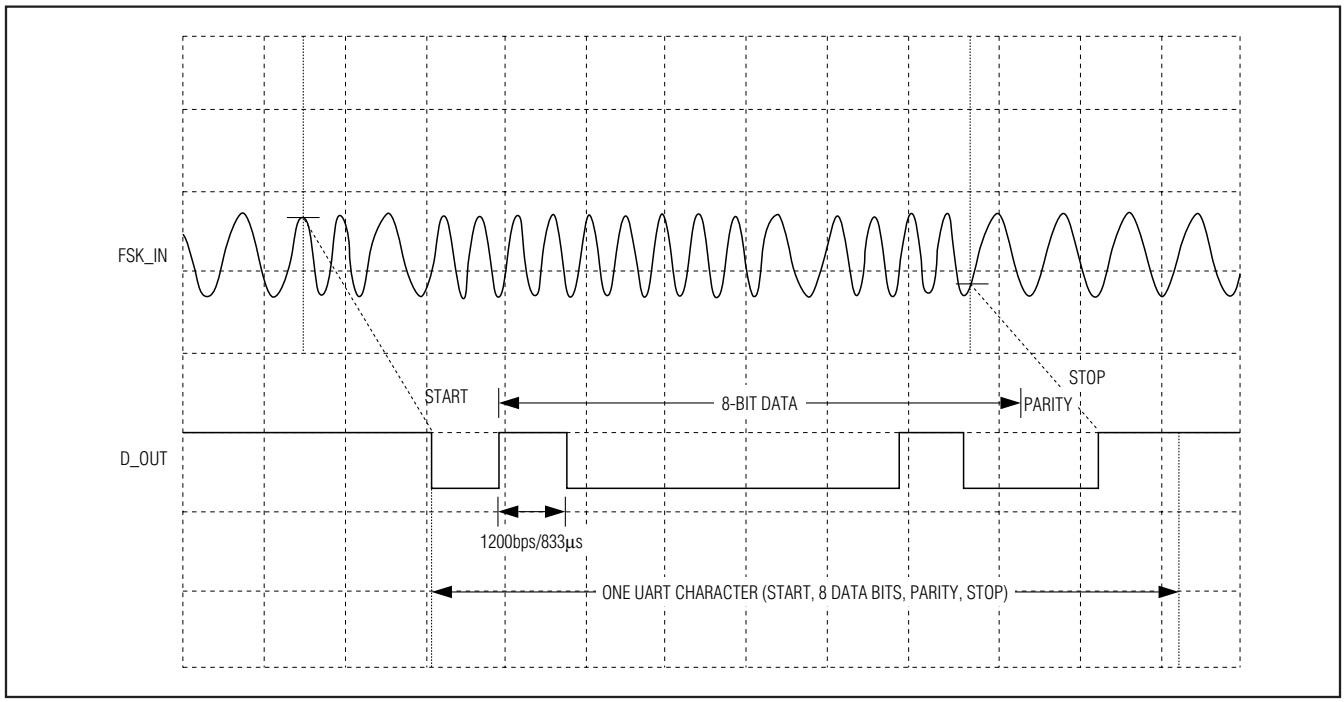


Figure 3. Actual DS8500 Demodulator Waveform

HART Modem

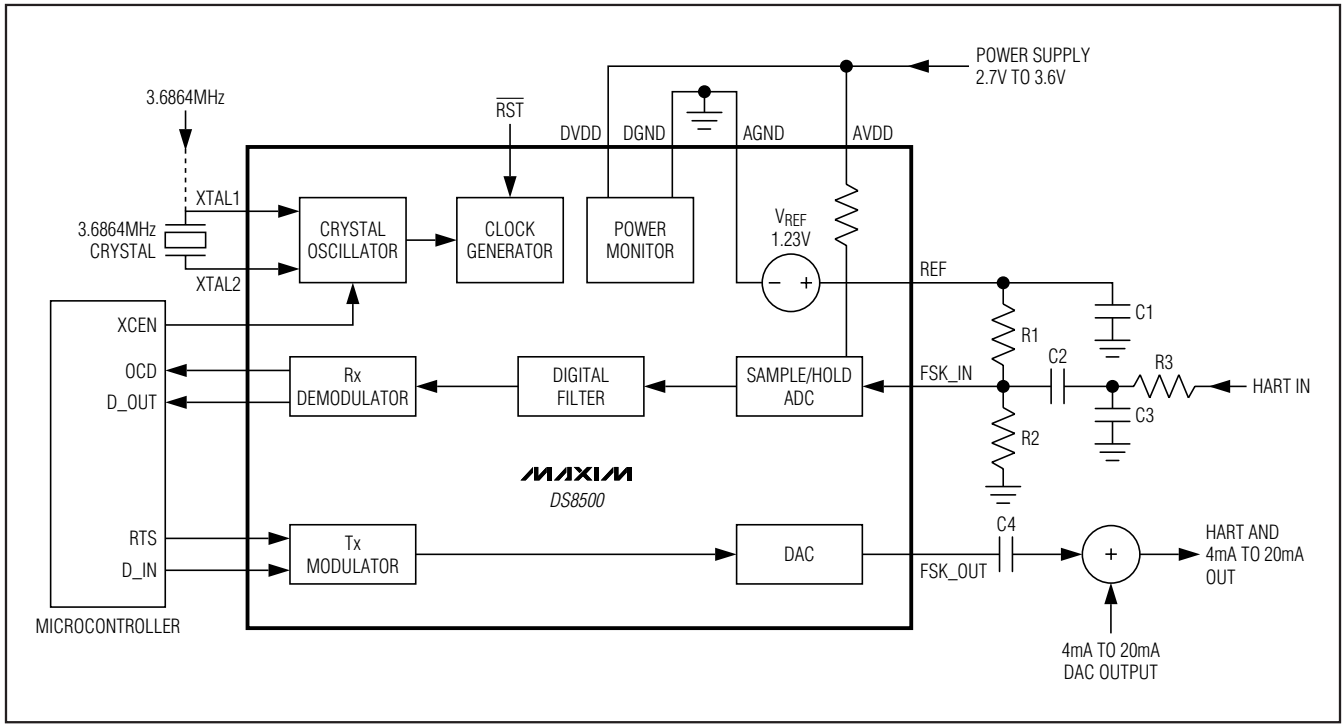


Figure 4. Typical Application Circuit

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
20 TQFN	T2055+3	**21-0140**

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