DS80PCI402EVK User's Guide

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1. Introduction:

The DS80PCI402EVK is a 4 channel SMA evaluation kit. It provides a complete high bandwidth platform to evaluate the signal integrity and signal conditioning features of the Texas Instruments DS80PCI402SQ – 2.5 Gbps / 5.0 Gbps / 8.0 Gbps 8 Channel PCI Express Repeater with Equalization and De-Emphasis.

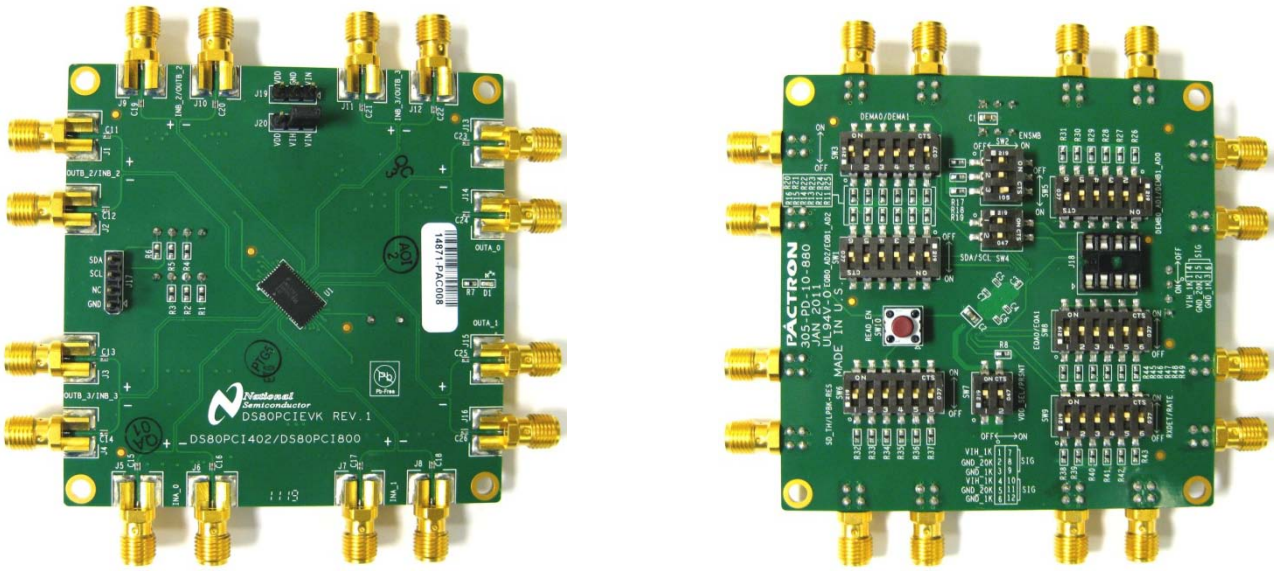


Figure 1. DS80PCI402EVK (TOP / BOTTOM VIEW)

Table 1. Switches to set the 4-level input control pins

4 – level Input Settings	Setting for 3 pin switches (3-2-1)
0 – Tie 1k ohm to GND	**ON** – OFF – OFF
R – Tie 20k ohm to GND	OFF – **ON** – OFF
F – FLOAT (open)	OFF – OFF – OFF
1 – Tie 1k ohm to VIH	OFF – OFF – **ON**

The following switches are used to set the input condition for the 4-level inputs:
SW1, SW2, SW3, SW5, SW6, SW8, SW9.
There are 3 switches connected to an input signal pin. Each switch when set to the ON position sets the pin to one of the 4-level setting. The 6 pin switches are assigned similar to the 3 pin switches. The only difference is 2 signal pins are connected and thus 6-5-4 is for the one signal pin and 3-2-1 is for another signal pin. Please note only 1 switch at the ON position is allowed.

Table 2. Connection and Control Description

Component	Name	Function
J9 to J12 J5 to J8	IN_B2+, IN_B2-, IN_B3+, IN_B3-, IN_A0+, IN_A0-, IN_A1+, IN_A1-	High speed differential inputs.
J1 to J4 J13 to J16	OUT_B2+, OUT_B2-, OUT _B3+, OUT_B3-, OUT _A0+, OUT_A0-, OUT _A1+, OUT_A1-	High speed differential outputs.
J19	VIN or VDD	DC Power – VIN or VDD to DS80PCI402SQ
J20	VIN or VDD	Jumper – VIN or VDD to VIH power
J17	SDA, SCL	Optional SMBUS access pins. See the datasheet for additional information on SMBUS.
J18	EEPROM	Optional socket for EEPROM
SW1	EQB[1:0] or AD[3:2]	PIN MODE – EQ control for channel B inputs SMBUS MODE – AD[3:2] device address bits
SW2	ENSMB	ENSMB = LOW – PIN MODE ENSMB = HIGH – SMBUS (slave mode) ENSMB = FLOAT – SMBUS (master mode – load configuration from EEPROM)
SW3	DEMA[1:0]	PIN MODE – DE control for channel A outputs
SW4	SDA/SCL	“ON” position connects SDA and SCL lines to the device pin.
SW5	DEMB[1:0] or AD[1:0]	PIN MODE – DE control for channel B outputs SMBUS MODE – AD[1:0] device address bits
SW6	SD_TH and LPBK - RES	SD_TH – Signal detect threshold level (FLOAT = Default level) LPBK function for PCI402 and RESERVED for PCI800 (FLOAT = Normal operation)
SW7	VDD_SEL and PRSNT	VDD_SEL – Enable or disable the internal 3.3V to 2.5V regulator. PRSNT – Enable or disable the device (LOW – Enables the device)
SW8	EQA[1:0]	PIN MODE – EQ control for channel A inputs
SW9	RXDET and RATE	RXDET – Input internal 50 ohm to VDD terminations RXDET = F (AUTO RX Detect), RXDET = 1 (50 ohm input termination). RATE = 0 (GEN1,2) = 2.5G / 5.0G. RATE = R (GEN3) = 8.0G. RATE = F (AUTO Detect). The RATE auto detect circuit requires the idle and active signal which occurs during the link training negotiation.
SW10	READ_EN	ENSMB = FLOAT – SMBUS (master mode – load configuration from EEPROM) SW6: SD_TH becomes the READ_EN pin. To start the loading at power up, set SW6 pin 3 to “ON” position (pull to GND). To manually control the start, set SW6 pin 1 to “ON” position (pull to VDD) and push the SW10 button for the high to low transition to start the loading. When the loading is complete the LED – D1 light should turn OFF.

2. Setup:

2.1. Connect J19: VIN = 3.3V or VDD = 2.5V and GND

For VIN = 3.3V:

Set SW7 pin1 (VDD_SEL) to the ON position (enable internal LDO regulator) and float VDD at J19.

For VDD = 2.5V:

Set SW7 pin1 (VDD_SEL) to the OFF positions (disable internal LDO regulator) and float VIN at J19.

2.2. Set jumper – J20 for VIH connection to VIN or VDD

2.3. Connect 50 Ohm SMA cables to the board

The input signals J1 to J8 can be connected from a pattern generator.

The output signals J9 to J16 can be connected to a scope.

Top 2 – B channel: J9 – IN_B2+, J10 – IN_B2- → J1 – OUT_B2+, J2 – OUT_B2-
J11 – IN_B3+, J12 – IN_B3- → J3 – OUT_B3+, J4 – OUT_B3-

Bottom 2 – A channel: J5 – IN_A0+, J6 – IN_A0- → J13 – OUT_A0+, J14 – OUT_A0-
J7 – IN_A1+, J8 – IN_A1- → J15 – OUT_A1+, J16 – OUT_A1-

2.4. Set the control pins for normal operation

SW7 – PRSNT = 0 (enables the device): set switch pin2 to the ON position.

SW9 – RXDET = F (continuous receiver detection): set switches (3-2-1) = (OFF-OFF-OFF).
RXDET = 1 (50 ohm input termination): set switches (3-2-1) = (OFF-OFF-**ON**).

SW9 – RATE = 1 (GEN3 mode with DEM control): set switches (6-5-4) = (OFF-OFF-**ON**).
RATE = F (enable rate detection for GEN1,2,3 with DEM control): set switches (6-5-4) to (OFF-OFF-OFF).
RATE = R (GEN3 mode without DEM control): set switches (6-5-4) = (OFF-**ON**-OFF).
RATE = 0 (GEN1,2 mode with DEM control): set switches (6-5-4) = (**ON**-OFF-OFF).

SW6 – SD_TH = F (default signal detect threshold level): set switches (3-2-1) = (OFF-OFF-OFF).

SW6 – LPBK = F (normal operation): set switches (6-5-4) = (OFF-OFF-OFF).

2.5. Set the input equalization level

For external pin mode control of the equalization level:

Set ENSMB = 0 (1kohm to GND) by using the SW2 (3-2-1) = (**ON**-OFF-OFF).

SW4 pin1,2 must be set to the OFF positions, so the SMBUS signals are disconnected.

Refer to Table 1 for information on the 3 switch settings for the 4 level input.

Example:

Set EQB[1:0] with SW1 for the B bank of inputs (top 2 right inputs of DS80PCI402).

SW1 (6-5-4), (3-2-1) = (OFF-**ON**-OFF), (OFF-**ON**-OFF) = EQB[1:0] = R,R = 14.6 dB at 4 GHz (level 6).

Set EQA[1:0] with SW8 for the A bank of inputs (bottom 2 left inputs of DS80PCI402).

SW8 (6-5-4), (3-2-1) = (OFF-**ON**-OFF), (OFF-**ON**-OFF) = EQA[1:0] = R,R = 14.6 dB at 4 GHz (level 6).

Table 3: 16 EQ settings when in pin mode

Level	EQA/B[1:0]	SW1 - EQB[1:0] SW8 - EQA[1:0]						EQ (dB) at 4 GHz
		6	5	4	3	2	1	
1	0, 0	**ON**	OFF	OFF	**ON**	OFF	OFF	4.9
2	0, R	**ON**	OFF	OFF	OFF	**ON**	OFF	7.9
3	0, F	**ON**	OFF	OFF	OFF	OFF	OFF	9.9
4	0, 1	**ON**	OFF	OFF	OFF	OFF	**ON**	11.0
5	R, 0	OFF	**ON**	OFF	**ON**	OFF	OFF	14.3
6	R, R	OFF	**ON**	OFF	OFF	**ON**	OFF	14.6
7	R, F	OFF	**ON**	OFF	OFF	OFF	OFF	17.0
8	R ,1	OFF	**ON**	OFF	OFF	OFF	**ON**	18.5
9	F ,0	OFF	OFF	OFF	**ON**	OFF	OFF	18.0
10	F, R	OFF	OFF	OFF	OFF	**ON**	OFF	22.0
11	F, F	OFF	OFF	OFF	OFF	OFF	OFF	24.4
12	F, 1	OFF	OFF	OFF	OFF	OFF	**ON**	25.8
13	1, 0	OFF	OFF	**ON**	**ON**	OFF	OFF	27.4
14	1, R	OFF	OFF	**ON**	OFF	**ON**	OFF	29.0
15	1, F	OFF	OFF	**ON**	OFF	OFF	OFF	31.4
16	1, 1	OFF	OFF	**ON**	OFF	OFF	**ON**	32.7

2.6. Set the output VOD and De-emphasis level

For external pin mode control for the VOD and De-emphasis level:
Set ENSMB = 0 (1kohm to GND) by using the SW2 (3-2-1) = (**ON**-OFF-OFF).
SW4 pin1,2 must be set to the OFF positions, so the SMBUS signals are disconnected.
Refer to Table 1 for information on the 3 switch settings for the 4 level input.

Example:
Set DEMB[1:0] with SW5 for the B bank of outputs (top 2 left outputs of DS80PCI402).
SW5 (6-5-4), (3-2-1) = (**ON**-OFF-OFF), (OFF-OFF-**ON**) = DEMB[1:0] = 0,1 (VOD=1.0V, DE=0 dB).
Set DEMA[1:0] with SW3 for the A bank of outputs (bottom 2 right outputs of DS80PCI402).
SW3 (6-5-4), (3-2-1) = (**ON**-OFF-OFF), (OFF-OFF-**ON**) = DEMA1:0] = 0,1 (VOD=1.0V, DE=0 dB).

Table 4: 16 settings of VOD and DE when in pin mode

Level	DEMA/B[1:0]	SW5 - DEMB[1:0] SW3 - DEMA[1:0]						GEN1,2	
		6	5	4	3	2	1	VOD (Vp-p)	DE (dB)
1	0, 0	**ON**	OFF	OFF	**ON**	OFF	OFF	0.8	0
2	0, R	**ON**	OFF	OFF	OFF	**ON**	OFF	0.9	0
3	0, F	**ON**	OFF	OFF	OFF	OFF	OFF	0.9	-3.5
4	0, 1	**ON**	OFF	OFF	OFF	OFF	**ON**	1.0	0
5	R, 0	OFF	**ON**	OFF	**ON**	OFF	OFF	1.0	-3.5
6	R, R	OFF	**ON**	OFF	OFF	**ON**	OFF	1.0	-6
7	R, F	OFF	**ON**	OFF	OFF	OFF	OFF	1.1	0
8	R ,1	OFF	**ON**	OFF	OFF	OFF	**ON**	1.1	-3.5
9	F ,0	OFF	OFF	OFF	**ON**	OFF	OFF	1.1	-6
10	F, R	OFF	OFF	OFF	OFF	**ON**	OFF	1.2	0
11	F, F	OFF	OFF	OFF	OFF	OFF	OFF	1.2	-3.5
12	F, 1	OFF	OFF	OFF	OFF	OFF	**ON**	1.2	-6
13	1, 0	OFF	OFF	**ON**	**ON**	OFF	OFF	1.3	0
14	1, R	OFF	OFF	**ON**	OFF	**ON**	OFF	1.3	-3.5
15	1, F	OFF	OFF	**ON**	OFF	OFF	OFF	1.3	-6
16	1, 1	OFF	OFF	**ON**	OFF	OFF	**ON**	1.3	-9

2.7 SMBUS mode control of the EQ, VOD and De-emphasis level:

Set ENSMB = 1 (1kohm to VIH) by using the SW2 (3-2-1) = (OFF-OFF-**ON)**.
Set SW4 pin1,2 to the ON position so the SMBUS signals are connected.
Set SW3 pin1 thru pin6 switches to the OFF position so they do not connect to the SDA and SCL line.
Set the SW1 and SW5 for the AD[3:0] pins. AD[3:0]=0000 sets device slave address = B0'hex.
Connect SDA, SCL and GND to J17. Please refer to datasheet for register map for EQ, VOD and DEM.

3. Bill of Materials for DS80PCI402EVK

Item	Qty	Reference	Digikey PN	Manufacture PN	Descriptions
1	1	C1	445-3448-1-ND	C1608Y5V0J106Z	CAP CER 10UF 6.3V Y5V 0603
2	1	C2	445-1322-1-ND	C1608X5R0J105K	CAP CER 1.0UF 6.3V X5R 10% 0603
3	1	C3,C4,C5,C6,C7	445-4711-1-ND	C0603X5R0J104M	CAP CER .10UF 6.3V X5R 0201
4	16	C11,C12,C13,C14,C15,C16	587-2483-1-ND	LMK063BJ224MP-F	CAP CER .22UF 10V X5R 20% 0201
		C17,C18,C19,C20,C21,C22,			
		C23,C24,C25,C26			
5	1	D1	511-1592-1-ND	SML-P12PTT86	LED GREEN 0.2MM 13MCD 0402 SMD
6	16	J1,J2,J3,J4,J5,J6,J7,J8,	J801-ND	142-0761-881	CONN JACK SMA 50 OHMS PC MOUNT
		J9,J10,J11,J12,J13,J14,			
		J15,J16			
7	1	J17	WM6504-ND	22-28-4043	CONN HEADER 4POS .100 VERT GOLD
8	2	J19,J20	WM6503-ND	22-28-4033	CONN HEADER 3POS .100 VERT GOLD
9	1	J18	3M5473-ND	4808-3004-CP	SOCKET IC OPEN FRAME 8POS .3"
10	31	R1,R2,R3,R4,R8,R11,R13,	P1.00KLCT-ND	ERJ-2RKF1001X	RES 1.00K OHM 1/10W 1% 0402 SMD
		R14,R16,R17,R19,R20,R22,			
		R23,R25,R26,R28,R29,R31,			
		R32,R34,R35,R37,R38,R40,			
		R41,R43,R44,R46,R47,R49			
11	1	R7	P220LCT-ND	ERJ-2RKF2200X	RES 220 OHM 1/10W 1% 0402 SMD
12	13	R12,R15,R18,R21,R24,R27,	P20.0KLCT-ND	ERJ-2RKF2002X	RES 20.0K OHM 1/10W 1% 0402 SMD
		R30,R33,R36,R39,R42,R45,			
		R48			
13	2	R5,R6	P4.70KLCT-ND	ERJ-2RKF4701X	RES 4.70K OHM 1/10W 1% 0402 SMD
14	6	SW1,SW3,SW5,SW6,SW8, SW9	CT2196MST-ND	219-6MST	SWITCH TAPE SEAL 6 POS SMD
15	1	SW2	CT2193MST-ND	219-3MST	SWITCH TAPE SEAL 3 POS SMD
16	2	SW4,SW7	CT2192MST-ND	219-2MST	SWITCH TAPE SEAL 2 POS SMD
17	1	SW10	P12225SCT-ND	EVQ-21505R	SWITCH LT 6MM 160GF 5MM HEIGHT
18	1	U1	NA	DS80PCI402SQ	PCIE REPEATER

4. Schematic

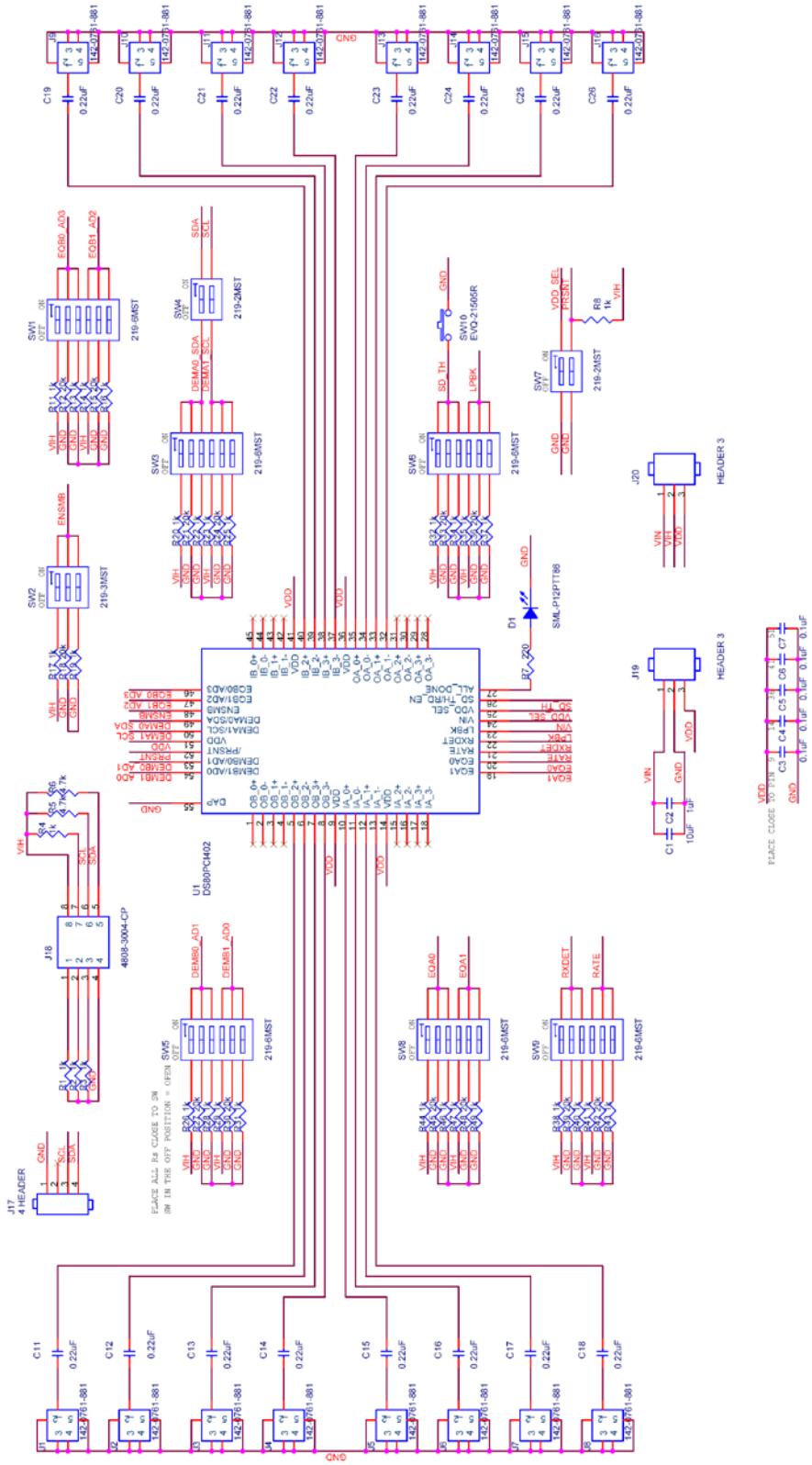


Figure 2. DS80PCI402EVK Schematic

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For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant

Caution
This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

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This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

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Concerning EVMs including radio transmitters
This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concerning EVMs including detachable antennas
Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication.

This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Cet appareil numérique de la classe A ou B est conforme à la norme NMB-003 du Canada.

Les changements ou les modifications pas expressément approuvés par la partie responsable de la conformité ont pu vider l'autorité de l'utilisateur pour actionner l'équipement.

Concernant les EVMs avec appareils radio
Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concernant les EVMs avec antennes détachables
Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but

de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante.

Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

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This development kit is NOT certified as Confirming to Technical Regulations of Radio Law of Japan

If you use this product in Japan, you are required by Radio Law of Japan to follow the instructions below with respect to this product:

1. Use this product in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use this product only after you obtained the license of Test Radio Station as provided in Radio Law of Japan with respect to this product, or
3. Use of this product only after you obtained the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to this product. Also, please do not transfer this product, unless you give the same notice above to the transferee. Please note that if you could not follow the instructions above, you will be subject to penalties of Radio Law of Japan.

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3. You will employ reasonable safeguards to ensure that your use of the EVM will not result in any property damage, injury or death, even if the EVM should fail to perform as described or expected.
4. You will take care of proper disposal and recycling of the EVM's electronic components and packing materials.

Certain Instructions. It is important to operate this EVM within TI's recommended specifications and environmental considerations per the user guidelines. Exceeding the specified EVM ratings (including but not limited to input and output voltage, current, power, and environmental ranges) may cause property damage, personal injury or death. If there are questions concerning these ratings please contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, some circuit components may have case temperatures greater than 60°C as long as the input and output are maintained at a normal ambient operating temperature. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors which can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during normal operation, please be aware that these devices may be very warm to the touch. As with all electronic evaluation tools, only qualified personnel knowledgeable in electronic measurement and diagnostics normally found in development environments should use these EVMs.

Agreement to Defend, Indemnify and Hold Harmless. You agree to defend, indemnify and hold TI, its licensors and their representatives harmless from and against any and all claims, damages, losses, expenses, costs and liabilities (collectively, "Claims") arising out of or in connection with any use of the EVM that is not in accordance with the terms of the agreement. This obligation shall apply whether Claims arise under law of tort or contract or any other legal theory, and even if the EVM fails to perform as described or expected.

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