Rev 2; 10/08

DALLAS SEMICONDUCTOR MAXIM

# Two/Four-Channel, I²C Adjustable Current DAC



## General Description

The DS4402 and DS4404 contain two and four I²C adjustable current DACs, respectively, that are each capable of sinking or sourcing current. Each output has 31 sink and 31 source settings that are programmed by the I²C interface. External resistors set the full-scale range and step size of each output.

## Applications

Power-Supply Adjustment

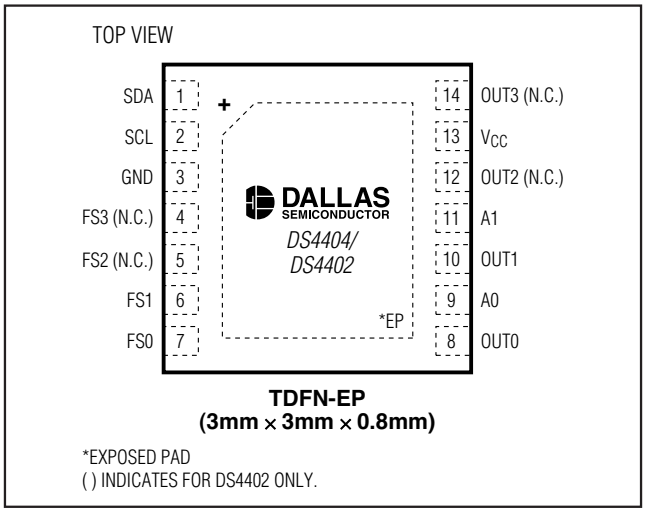
Power-Supply Margining

Adjustable Current Sink or Source

## Features

- **Two (DS4402) or Four (DS4404) Current DACs**
- **Full-Scale Range for Each DAC Determined by External Resistors**
- **31 Settings Each for Sink and Source Modes**
- **I²C-Compatible Serial Interface**
- **Two Three-Level Address Pins Allow Nine Devices on Same I²C Bus**
- **Low Cost**
- **Small Package (14-Pin TDFN)**
- **-40°C to +85°C Temperature Range**
- **2.7V to 5.5V Operation**

## Pin Configuration




**TDFN-EP**
**(3mm × 3mm × 0.8mm)**

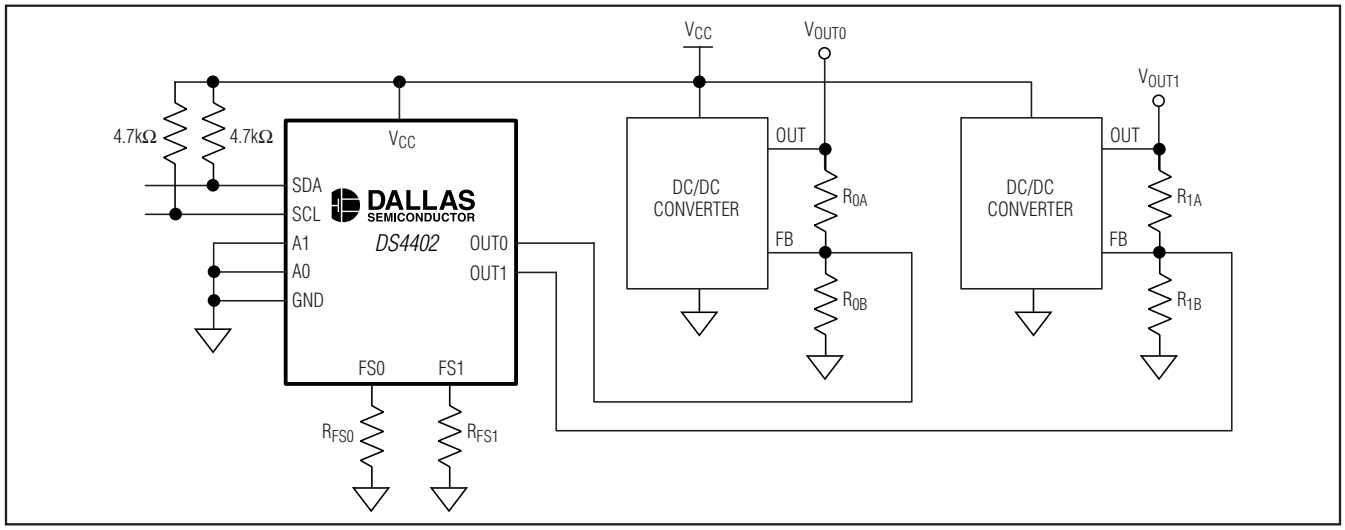
*EXPOSED PAD
( ) INDICATES FOR DS4402 ONLY.

## Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE |
|---|---|---|
| **DS4402**N+ | -40°C to +85°C | 14 TDFN-EP* |
| DS4402N+T&R | -40°C to +85°C | 14 TDFN-EP* |
| **DS4404**N+ | -40°C to +85°C | 14 TDFN-EP* |
| DS4404N+T&R | -40°C to +85°C | 14 TDFN-EP* |

*+Denotes a lead-free/RoHS-compliant package.*
*T&R = Tape and reel.*
**EP = Exposed pad.*

## Typical Operating Circuit






***For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.***

# Two/Four-Channel, I²C Adjustable Current DAC

## ABSOLUTE MAXIMUM RATINGS

Voltage Range on $V_{CC}$, SDA, and SCL Relative to Ground.....-0.5V to +6.0V
Voltage Range on A0, A1, FS0, FS1, FS2, FS3, OUT0, OUT1, OUT2, and OUT3 Relative to Ground .....-0.5V to ($V_{CC}$ + 0.5V) (Not to exceed 6.0V.)
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-55°C to +125°C
Soldering Temperature .....Refer to IPC/JEDEC J-STD-020 Specification

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## RECOMMENDED OPERATING CONDITIONS

($T_A$ = -40°C to +85°C.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | (Note 1) | 2.7 | | 5.5 | V |
| Input Logic 1 (SDA, SCL, A0, A1) | $V_{IH}$ | | 0.7 x $V_{CC}$ | | $V_{CC}$ + 0.3 | V |
| Input Logic 0 (SDA, SCL, A0, A1) | $V_{IL}$ | | -0.3 | | 0.3 x $V_{CC}$ | V |

## DC ELECTRICAL CHARACTERISTICS

($V_{CC}$ = +2.7V to +5.5V, $T_A$ = -40°C to +85°C.)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Supply Current | $I_{CC}$ | $V_{CC}$ = 5.5V (Note 2) | DS4402 | | | 500 | µA |
| | | | DS4404 | | | 500 | |
| Input Leakage (SDA, SCL) | $I_{IL}$ | $V_{CC}$ = 5.5V | | | | 1 | µA |
| Output Leakage (SDA) | $I_L$ | | | | | 1 | µA |
| Output Current Low (SDA) | $I_{OL}$ | $V_{OL}$ = 0.4V | | 3 | | | mA |
| | | $V_{OL}$ = 0.6V | | 6 | | | |
| Address Input Resistors | $R_{IN}$ | | | | 240 | | kΩ |
| Reference Voltage | $V_{REF}$ | | | | 1.23 | | V |
| I/O Capacitance | $C_{I/O}$ | | | | | 10 | pF |

## OUTPUT CURRENT CHARACTERISTICS

($V_{CC}$ = +2.7V to +5.5V, $T_A$ = -40°C to +85°C.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Output Voltage for Sinking Current | $V_{OUT:SINK}$ | (Note 3) | 0.5 | | $V_{CC}$ | V |
| Output Voltage for Sourcing Current | $V_{OUT:SOURCE}$ | (Note 3) | 0 | | $V_{CC}$ - 0.5 | V |
| Full-Scale Sink Output Current | $I_{OUT:SINK}$ | (Note 3) | 0.5 | | 2.0 | mA |
| Full-Scale Source Output Current | $I_{OUT:SOURCE}$ | (Note 3) | -2.0 | | -0.5 | mA |
| Output-Current Full-Scale Accuracy | $I_{OUT:FS}$ | +25°C, $V_{CC}$ = 4.0V; using ideal $R_{FS}$ resistor | | 2.5 | 5.0 | % |
| Output-Current Temperature Drift | $I_{OUT:TC}$ | (Note 4) | | 70 | | ppm/°C |

## OUTPUT CURRENT CHARACTERISTICS (continued)

($V_{CC}$ = +2.7V to +5.5V, $T_A$ = -40°C to +85°C.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Output-Current Power-Supply Rejection Ratio | | DC | | 0.33 | | %/V |
| Output Leakage Current at Zero Current Setting | $I_{ZERO}$ | | -1 | | +1 | µA |
| Output-Current Differential Linearity | DNL | (Note 5) | | | 0.5 | LSB |
| Output-Current Integral Linearity | INL | (Note 6) | | | 1 | LSB |

## I²C AC ELECTRICAL CHARACTERISTICS

($V_{CC}$ = +2.7V to +5.5V, $T_A$ = -40°C to +85°C.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| SCL Clock Frequency | $f_{SCL}$ | (Note 7) | 0 | | 400 | kHz |
| Bus Free Time Between STOP and START Conditions | $t_{BUF}$ | | 1.3 | | | µs |
| Hold Time (Repeated) START Condition | $t_{HD:STA}$ | | 0.6 | | | µs |
| Low Period of SCL | $t_{LOW}$ | | 1.3 | | | µs |
| High Period of SCL | $t_{HIGH}$ | | 0.6 | | | µs |
| Data Hold Time | $t_{DH:DAT}$ | | 0 | | 0.9 | µs |
| Data Setup Time | $t_{SU:DAT}$ | | 100 | | | ns |
| START Setup Time | $t_{SU:STA}$ | | 0.6 | | | µs |
| SDA and SCL Rise Time | $t_R$ | (Note 8) | $20 + 0.1C_B$ | | 300 | ns |
| SDA and SCL Fall Time | $t_F$ | (Note 8) | $20 + 0.1C_B$ | | 300 | ns |
| STOP Setup Time | $t_{SU:STO}$ | | 0.6 | | | µs |
| SDA and SCL Capacitive Loading | $C_B$ | (Note 8) | | | 400 | pF |

**Note 1:** All voltages with respect to ground. Currents entering the IC are specified positive, and currents exiting the IC are negative.

**Note 2:** Supply current specified with all outputs set to zero current setting with all inputs (except A1 and A0, which can be open) driven to well-defined logic levels. SDA and SCL are connected to $V_{CC}$. Excludes current through $R_{FS}$ resistors ($I_{RFS}$). Total current including $I_{RFS}$ is $I_{CC}$ + (2 x $I_{RFS}$).

**Note 3:** The output-voltage full-scale current ranges must be satisfied to ensure the device meets its accuracy and linearity specifications.

**Note 4:** Temperature drift excludes drift caused by external resistor.

**Note 5:** Differential linearity is defined as the difference between the expected incremental current increase with respect to position and the actual increase. The expected incremental increase is the full-scale range divided by 31.

**Note 6:** Integral linearity is defined as the difference between the expected value as a function of the setting and the actual value. The expected value is a straight line between the zero and the full-scale values proportional to the setting.

**Note 7:** Timing shown is for fast-mode (400kHz) operation. This device is also backward compatible with I²C standard-mode timing.

**Note 8:** $C_B$—total capacitance of one bus line in pF.

# Two/Four-Channel, I²C Adjustable Current DAC

## Pin Description

| PIN | | NAME | FUNCTION |
|---|---|---|---|
| DS4404 | DS4402 | | |
| 1 | 1 | SDA | I²C Serial Data. Input/output for I²C data. |
| 2 | 2 | SCL | I²C Serial Clock. Input for I²C clock. |
| 3 | 3 | GND | Ground |
| 4 | — | FS3 | Full-Scale Calibration Input. A resistor to ground on these pins determines the full-scale current for each output. FS0 controls OUT0, FS1 controls OUT1, etc. (DS4402 has only two inputs: FS0 and FS1.) |
| 5 | — | FS2 | |
| 6 | 6 | FS1 | |
| 7 | 7 | FS0 | |
| 8 | 8 | OUT0 | Current Output. Sinks or sources the current determined by the I²C interface and the resistance connected to FSx. (DS4402 has only two outputs: OUT0 and OUT1.) |
| 10 | 10 | OUT1 | |
| 12 | — | OUT2 | |
| 14 | — | OUT3 | |
| 9, 11 | 9, 11 | A0, A1 | Address Select Inputs. Tri-level inputs ($V_{CC}$, GND, N.C.) determine the I²C slave address. See the *Detailed Description* section for the nine available device addresses. |
| 13 | 13 | $V_{CC}$ | Power Supply |
| — | 4, 5, 12, 14 | N.C. | No Connection |
| — | — | EP | Exposed Pad. Leave floating or connect to GND. |

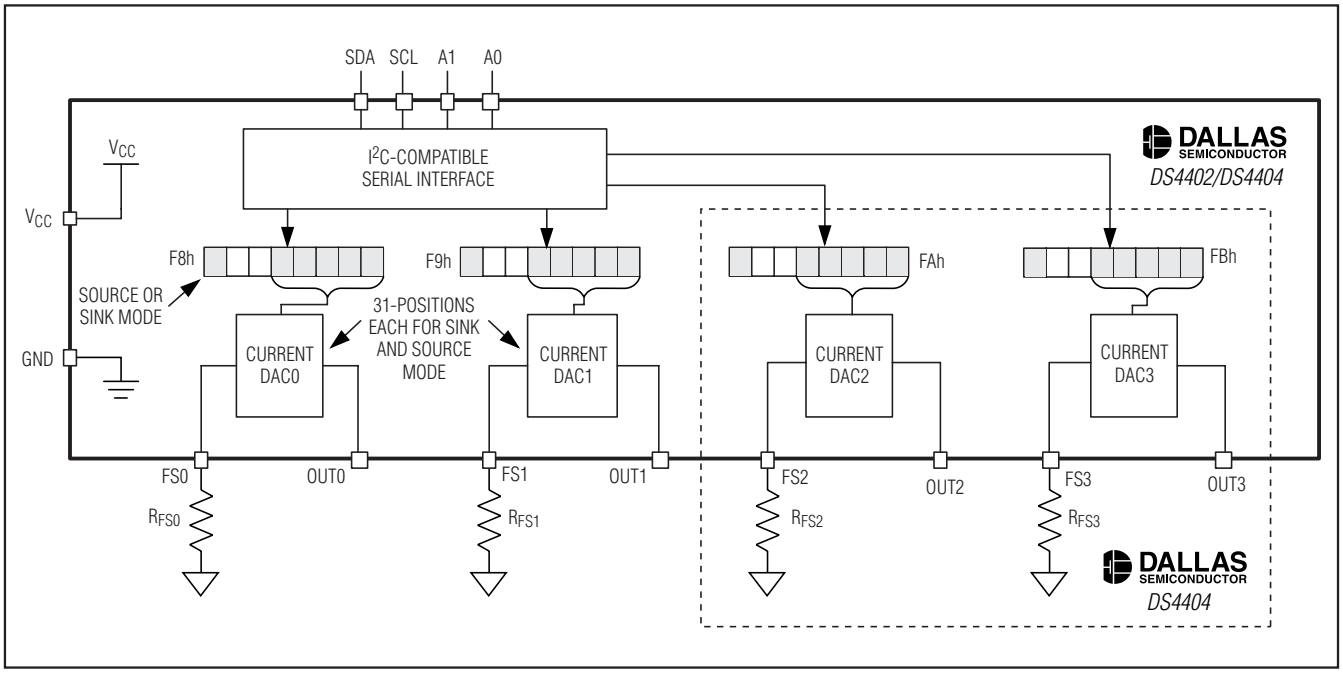



*Figure 1. Functional Diagram*

## Detailed Description

The DS4402/DS4404 contain two/four I²C adjustable current sources (Figure 1) that are each capable of sinking and sourcing current. Each output has 31 sink and 31 source settings that are programmed through the I²C interface. The full-scale ranges (and corresponding step sizes) of the outputs are determined by external resistors that adjust the output currents over a 4:1 range. The formula to determine the external resistor values ($R_{FS}$) for each of the outputs is given by:

**Equation 1:**

$$R_{FS} = (V_{REF} / I_{FS}) \times (31 / 4)$$

where $I_{FS}$ = desired full-scale current

On power-up, the DS4402/DS4404 output zero current. This is done to prevent it from sinking or sourcing an incorrect current before the system host controller has had a chance to modify the device's setting.

As a source for biasing instrumentation or other circuits, the DS4402/DS4404 provide a simple and inexpensive current source with an I²C interface for control. The adjustable full-scale range allows the application to get the most out of its 5-bit sink or source resolution.

When used in adjustable power-supply applications (see the *Typical Operating Circuit*), the DS4402/DS4404 do not affect the initial power-up supply voltage because it defaults to providing zero output current on power-up. As it sources or sinks current into the feedback voltage node, it changes the amount of output voltage required by the regulator to reach its steady state operating point. By using the external resistor to set the output current range, the devices provide flexibility for adjusting the impedances of the feedback network or the range over which the power supply can be controlled or margined.

### I²C Slave Address

The DS4402/DS4404 respond to one of nine I²C slave addresses determined by the two tri-level address inputs. The three input states are connected to $V_{CC}$, connected to ground, or disconnected. To sense the disconnected state (Figure 2), the address inputs have weak internal resistors that pull the pins to mid-supply.

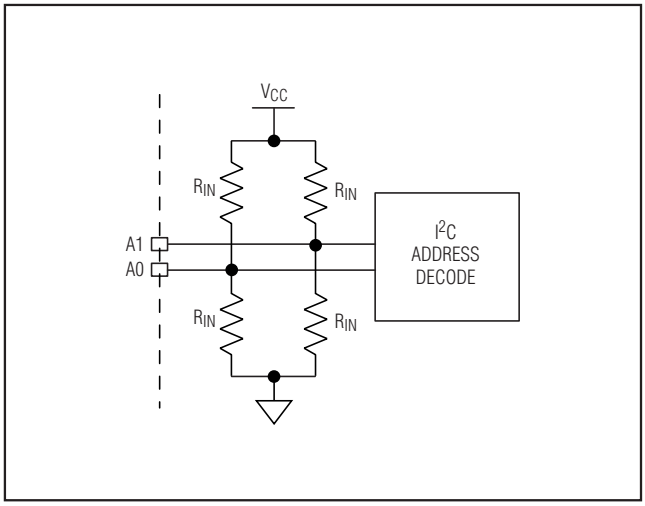



*Figure 2. I²C Address Inputs*

Table 1 lists the slave address determined by the address input combinations.

### Table 1. Slave Addresses

| A1 | A0 | SLAVE ADDRESS (HEXADECIMAL) |
|---|---|---|
| GND | GND | 90h |
| GND | $V_{CC}$ | 92h |
| $V_{CC}$ | GND | 94h |
| $V_{CC}$ | $V_{CC}$ | 96h |
| N.C. | GND | 98h |
| N.C. | $V_{CC}$ | 9Ah |
| GND | N.C. | 9Ch |
| $V_{CC}$ | N.C. | 9Eh |
| N.C. | N.C. | A0h |

# Two/Four-Channel, I²C Adjustable Current DAC

### Memory Organization

To control the DS4402/DS4404's current sources, write to the memory addresses listed in Table 2.

## Table 2. Memory Addresses

| MEMORY ADDRESS (HEXADECIMAL) | CURRENT SOURCE |
|---|---|
| F8h | OUT0 |
| F9h | OUT1 |
| FAh* | OUT2* |
| FBh* | OUT3* |

**Only for DS4404.*

The format of each output control register is given by:

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| S | X | X | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |

Where:

| BIT | NAME | FUNCTION | POWER-ON DEFAULT |
|---|---|---|---|
| S | Sign Bit | Determines if DAC sources or sinks current. For sink S = 0, for source S = 1. | 0b |
| X | Reserved | Reserved. Both bits read zero. | 00b |
| $D_X$ | Data | 5-Bit Data Word Controlling DAC Output. Setting 00000b outputs zero current regardless of the state of the sign bit. | 00000b |

Example: $I_{FS0}$ = 800µA, and register F8h is written to a value of 92h. Calculate the value of external resistance required, and the magnitude of the output current with this register setting.

$$R_{FS} = (V_{REF} / 800\mu A) \times (31 / 4) = 11.9k\Omega$$

The MSB of the output register is 1, so the output is sourcing the value corresponding to position 12h (18 decimal). The magnitude of the output current is equal to:

$$800\mu A \times (18 / 31) = 465\mu A$$

## I²C Serial Interface Description

### I²C Definitions

The following terminology is commonly used to describe I²C data transfers:

**Master Device:** The master device controls the slave devices on the bus. The master device generates SCL clock pulses, START and STOP conditions.

**Slave Devices:** Slave devices send and receive data at the master's request.

**Bus Idle or Not Busy:** Time between STOP and START conditions when both SDA and SCL are inactive and in their logic-high states. When the bus is idle it often initiates a low-power mode for slave devices.

**START Condition:** A START condition is generated by the master to initiate a new data transfer with a slave. Transitioning SDA from high to low while SCL remains high generates a START condition. See Figure 3 for applicable timing.

**STOP Condition:** A STOP condition is generated by the master to end a data transfer with a slave. Transitioning SDA from low to high while SCL remains high generates a STOP condition. See Figure 3 for applicable timing.

**Repeated START Condition:** The master can use a repeated START condition at the end of one data transfer to indicate that it will immediately initiate a new data transfer following the current one. Repeated STARTs are commonly used during read operations to identify a specific memory address to begin a data transfer. A repeated START condition is issued identically to a normal START condition. See Figure 3 for applicable timing.

**Bit Write:** Transitions of SDA must occur during the low state of SCL. The data on SDA must remain valid and unchanged during the entire high pulse of SCL, plus the setup and hold time requirements (Figure 3). Data is shifted into the device during the rising edge of the SCL.

**Bit Read:** At the end of a write operation, the master must release the SDA bus line for the proper amount of setup time (Figure 3) before the next rising edge of SCL during a bit read. The device shifts out each bit of data on SDA at the falling edge of the previous SCL pulse and the data bit is valid at the rising edge of the current SCL pulse. Remember that the master generates all SCL clock pulses, including when it is reading bits from the slave.

**Acknowledgement (ACK and NACK):** An Acknowledgement (ACK) or Not Acknowledge (NACK) is always the ninth bit transmitted during a byte transfer. The device receiving data (the master during a read or the slave during a write operation) performs an ACK by transmitting a zero during the ninth bit. A device performs a NACK by transmitting a one during the ninth bit. Timing for the ACK and NACK is identical to all other bit writes (Figure 4). An ACK is the acknowledgment that the device is properly receiving data. A NACK is used to terminate a read sequence or as an indication that the device is not receiving data.

**Byte Write:** A byte write consists of 8 bits of information transferred from the master to the slave (most significant bit first) plus a 1-bit acknowledgement from the slave to the master. The 8 bits transmitted by the master are done according to the bit-write definition, and the acknowledgement is read using the bit-read definition.

**Byte Read:** A byte read is an 8-bit information transfer from the slave to the master plus a 1-bit ACK or NACK from the master to the slave. The 8 bits of information that are transferred (most significant bit first) from the slave to the master are read by the master using the bit read definition above, and the master transmits an ACK using the bit write definition to receive additional data bytes. The master must NACK the last byte read to terminated communication so the slave will return control of SDA to the master.

**Slave Address Byte:** Each slave on the I²C bus responds to a slave address byte sent immediately following a START condition. The slave address byte contains the slave address in the most significant 7 bits and the R/$\overline{W}$ bit in the least significant bit. The DS4402/DS4404s' slave address is determined by the state of the A0 and A1 address pins. Table 1 describes the addresses corresponding to the state of A0 and A1.

When the R/$\overline{W}$ bit is 0 (such as in A0h), the master is indicating it will write data to the slave. If R/$\overline{W}$ = 1 (A1h in this case), the master is indicating it wants to read from the slave. If an incorrect slave address is written, the DS4402/DS4404 assume the master is communicating with another I²C device and ignore the communication until the next START condition is sent.

**Memory Address:** During an I²C write operation, the master must transmit a memory address to identify the memory location where the slave is to store the data. The memory address is always the second byte transmitted during a write operation following the slave address byte.

### I²C Communication

**Writing to a Slave:** The master must generate a START condition, write the slave address byte (R/$\overline{W}$ = 0), write the memory address, write the byte of data, and generate a STOP condition. Remember that the master must read the slave's acknowledgement during all byte-write operations.

**Reading from a Slave:** To read from the slave, the master generates a START condition, writes the slave address byte with R/$\overline{W}$ = 1, reads the data byte with a NACK to indicate the end of the transfer, and generates a STOP condition.

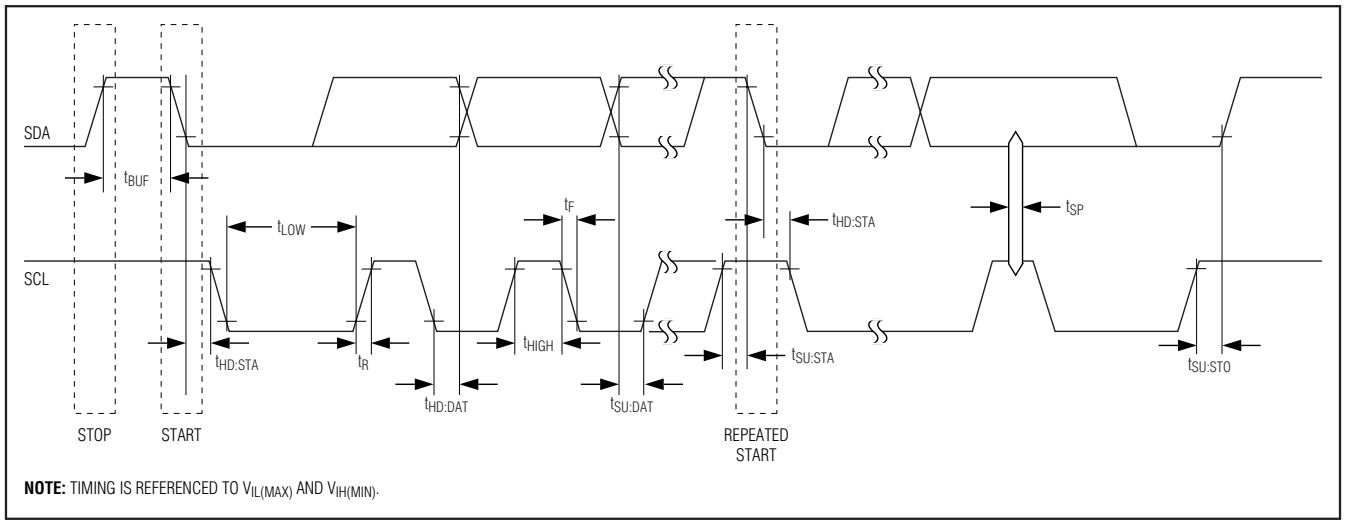



*Figure 3. I²C Timing Diagram*

# Two/Four-Channel, I²C Adjustable Current DAC

## Applications Information

### Example Calculations for an Adjustable Power Supply

Using the typical circuit, assuming a typical output voltage of 2.0V, a feedback voltage of 0.8V, R1 = 500Ω, and R2 = 333Ω, to adjust or margin the supply 20% requires a full-scale current equal to [(0.2 x 2.0V) / 500Ω = 800µA]. Using Equation 1, $R_{FS}$ can be calculated [$R_{FS} = (V_{REF} / 800\mu A) \times (31 / 4) = 11.9k\Omega$]. The current DAC in this configuration allows the output voltage to be stepped linearly from 1.6V to 2.4V using 63 settings. This corresponds to a resolution of 12.7mV/step.

### Power-Supply Feedback Voltage

The feedback voltage for adjustable power supplies must be between 0.5V and $V_{CC}$ - 0.5V for the DS4402/DS4404 to properly sink/source currents for adjusting the voltage.

### I²C Reset on Address Change

In addition to defining the I²C slave address, the DS4402/DS4404 address select inputs have an alternate function. Changing the address select inputs resets the I²C interface. This function aborts the current transaction and puts the SDA driver into a high-impedance state. This hardware reset function should never be required because it is achievable through software, but it does provide an alternative way of resetting the I²C interface, if needed.

### $V_{CC}$ Decoupling

To achieve the best results when using the DS4402/DS4404, decouple the power supply with a 0.01µF or 0.1µF capacitor. Use a high-quality ceramic surface-mount capacitor if possible. Surface-mount components minimize lead inductance, which improves performance, and ceramic capacitors tend to have adequate high-frequency response for decoupling applications.

### Layout Considerations

Care should be taken to ensure that traces underneath the DS4402/DS4404 do not short with the exposed pad. The exposed pad should be connected to the signal ground, or can be left floating.

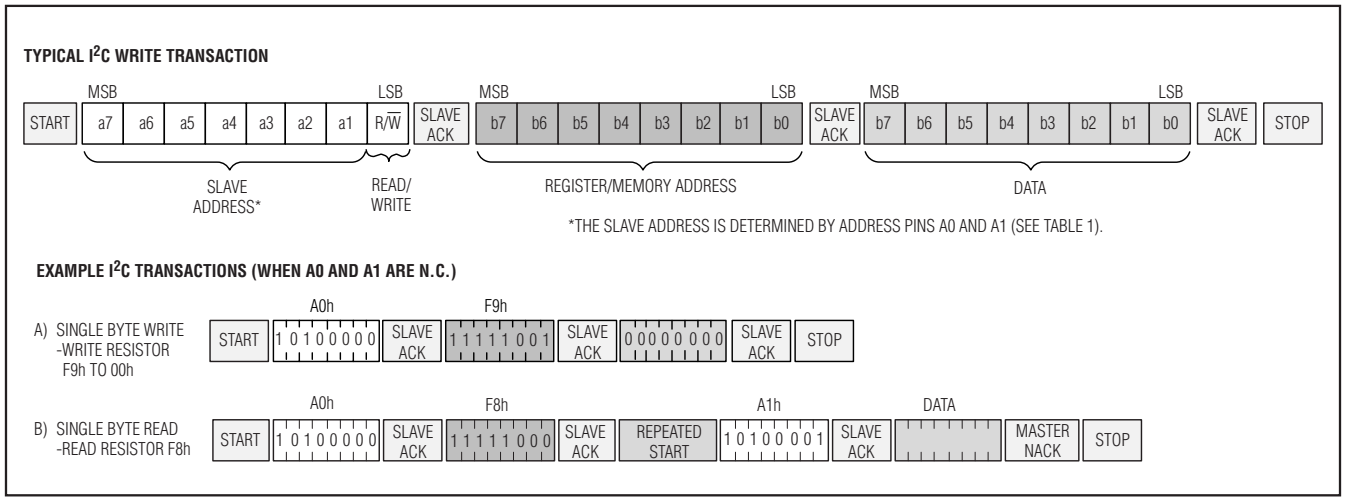



*Figure 4. I²C Communication Examples*

## Chip Information

TRANSISTOR COUNT: 10,992

## Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

| PACKAGE TYPE | PACKAGE CODE | DOCUMENT NO. |
|---|---|---|
| 14 TDFN-EP | T1433+1 | 21-0137 |

## Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|---|---|---|---|
| 0 | 4/06 | Initial release. | — |
| 1 | 8/06 | In the *Features*, corrected the operating range from 1.7V to 5.5V to 2.7V to 5.5V. | 1 |
| 2 | 10/08 | Added the I/O capacitance ($C_{I/O}$) parameter to the *DC Electrical Characteristics* table. | 2 |

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