Rev 2; 10/08

DS3234

# Extremely Accurate SPI Bus RTC with Integrated Crystal and SRAM

## General Description

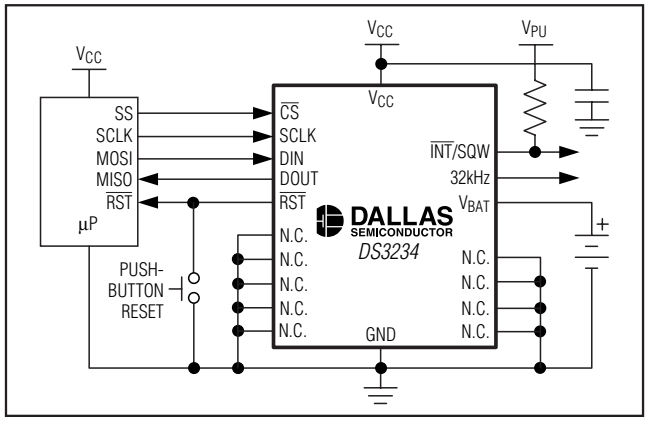
The DS3234 is a low-cost, extremely accurate SPI™ bus real-time clock (RTC) with an integrated temperature-compensated crystal oscillator (TCXO) and crystal. The DS3234 incorporates a precision, temperature-compensated voltage reference and comparator circuit to monitor $V_{CC}$. When $V_{CC}$ drops below the power-fail voltage ($V_{PF}$), the device asserts the $\overline{RST}$ output and also disables read and write access to the part when $V_{CC}$ drops below both $V_{PF}$ and $V_{BAT}$. The $\overline{RST}$ pin is monitored as a pushbutton input for generating a µP reset. The device switches to the backup supply input and maintains accurate timekeeping when main power to the device is interrupted. The integration of the crystal resonator enhances the long-term accuracy of the device as well as reduces the piece-part count in a manufacturing line. The DS3234 is available in commercial and industrial temperature ranges, and is offered in an industry-standard 300-mil, 20-pin SO package.

The DS3234 also integrates 256 bytes of battery-backed SRAM. In the event of main power loss, the contents of the memory are maintained by the power source connected to the $V_{BAT}$ pin. The RTC maintains seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The clock operates in either the 24-hour or 12-hour format with AM/PM indicator. Two programmable time-of-day alarms and a programmable square-wave output are provided. Address and data are transferred serially by an SPI bidirectional bus.

## Applications

Servers
Telematics
Utility Power Meters
GPS

## Typical Operating Circuit




*SPI is a trademark of Motorola, Inc.*
*UL is a registered trademark of Underwriters Laboratories, Inc.*

## Features

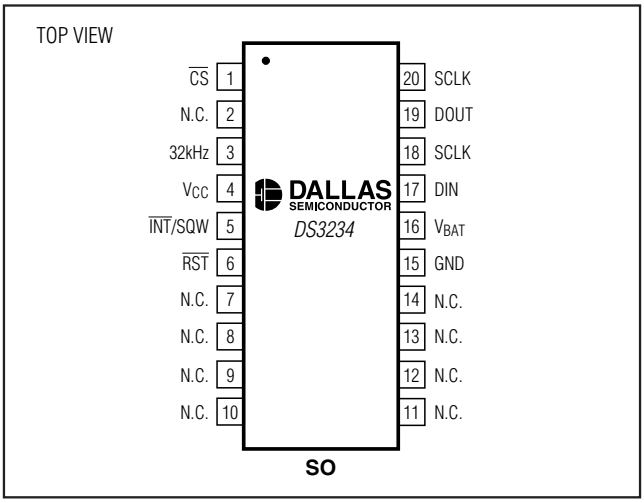
- **Accuracy ±2ppm from 0°C to +40°C**
- **Accuracy ±3.5ppm from -40°C to +85°C**
- **Battery Backup Input for Continuous Timekeeping**
- **Operating Temperature Ranges**
  **Commercial: 0°C to +70°C**
  **Industrial: -40°C to +85°C**
- **Low-Power Consumption**
- **Real-Time Clock Counts Seconds, Minutes, Hours, Day, Date, Month, and Year with Leap Year Compensation Valid Up to 2099**
- **Two Time-of-Day Alarms**
- **Programmable Square-Wave Output**
- **4MHz SPI Bus Supports Modes 1 and 3**
- **Digital Temp Sensor Output: ±3°C Accuracy**
- **Register for Aging Trim**
- **$\overline{RST}$ Input/Output**
- **300-Mil, 20-Pin SO Package**
- **Underwriters Laboratories (UL®) Recognized**

## Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE | TOP MARK |
|---|---|---|---|
| DS3234S# | 0°C to +70°C | 20 SO | DS3234S |
| DS3234SN# | -40°C to +85°C | 20 SO | DS3234SN |

*# Denotes a RoHS-compliant device that may include lead that is exempt under the RoHS requirements. Lead finish is JESD97 Category e3, and is compatible with both lead-based and lead-free soldering processes. A "#" anywhere on the top mark denotes a RoHS-compliant device.*

## Pin Configuration






**For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.**

# Extremely Accurate SPI Bus RTC with Integrated Crystal and SRAM

## ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin Relative to Ground.....-0.3V to +6.0V
Operating Temperature Range
(noncondensing) .....-40°C to +85°C
Junction Temperature.....+125°C
Storage Temperature Range .....-40°C to +85°C
Soldering Temperature
(leads, 10s) .....+260°C/10s
Soldering Temperature (reflow, 2 times max) .....See IPC/JEDEC J-STD-020 Specification

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## RECOMMENDED DC OPERATING CONDITIONS

($T_A$ = -40°C to +85°C, unless otherwise noted.) (Notes 1, 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | | 2.0 | 3.3 | 5.5 | V |
| | $V_{BAT}$ | | 2.0 | 3.0 | 3.8 | |
| Logic 1 Input $\overline{CS}$, SCLK, DIN | $V_{IH}$ | | 0.7 x $V_{CC}$ | | $V_{CC}$ + 0.3 | V |
| Logic 0 Input $\overline{CS}$, SCLK, DIN, $\overline{RST}$ | $V_{IL}$ | 2.0V ≤ $V_{CC}$ ≤ 3.63V | -0.3 | | +0.2 x $V_{CC}$ | V |
| | | 3.63V < $V_{CC}$ ≤ 5.5V | -0.3 | | +0.7 | |

## ELECTRICAL CHARACTERISTICS

($V_{CC}$ = 2.0V to 5.5V, $V_{CC}$ = active supply (see Table 1), $T_A$ = -40°C to +85°C, unless otherwise noted.) (Typical values are at **$V_{CC}$ = 3.3V, $V_{BAT}$ = 3.0V**, and $T_A$ = +25°C, unless otherwise noted. TCXO operation guaranteed from 2.3V to 5.5V on $V_{CC}$ and 2.3V to 3.8V on $V_{BAT}$.) (Notes 1, 2)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Active Supply Current | $I_{CCA}$ | SCLK = 4MHz, BSY = 0 (Notes 3, 4) | $V_{CC}$ = 3.63V | | | 400 | µA |
| | | | $V_{CC}$ = 5.5V | | | 700 | |
| Standby Supply Current | $I_{CCS}$ | $\overline{CS}$ = $V_{IH}$, 32kHz output off, SQW output off (Note 4) | $V_{CC}$ = 3.63V | | | 120 | µA |
| | | | $V_{CC}$ = 5.5V | | | 160 | |
| Temperature Conversion Current | $I_{CCSCONV}$ | SPI bus inactive, 32kHz output off, SQW output off | $V_{CC}$ = 3.63V | | | 500 | µA |
| | | | $V_{CC}$ = 5.5V | | | 600 | |
| Power-Fail Voltage | $V_{PF}$ | | | 2.45 | 2.575 | 2.70 | V |
| $V_{BAT}$ Leakage Current | $I_{BATLKG}$ | | | | 25 | 100 | nA |
| **($V_{CC}$ = 2.0V to 5.5V, $T_A$ = -40°C to +85°C, unless otherwise noted.) (Notes 1 and 2)** | | | | | | | |
| Logic 1 Output, 32kHz<br>$I_{OH}$ = -500µA<br>$I_{OH}$ = -250µA<br>$I_{OH}$ = -125µA | $V_{OH}$ | $V_{CC}$ > 3.63V,<br>3.63V > $V_{CC}$ > 2.7V,<br>2.7V > ($V_{CC}$ or $V_{BAT}$) > 2.0V<br>(BB32kHz = 1) | | 0.85 x $V_{CC}$ | | | V |

## ELECTRICAL CHARACTERISTICS (continued)

($V_{CC}$ = 2.0V to 5.5V, $V_{CC}$ = active supply (see Table 1), $T_A$ = -40°C to +85°C, unless otherwise noted.) (Typical values are at **$V_{CC}$ = 3.3V, $V_{BAT}$ = 3.0V**, and $T_A$ = +25°C, unless otherwise noted. TCXO operation guaranteed from 2.3V to 5.5V on $V_{CC}$ and 2.3V to 3.8V on $V_{BAT}$.) (Notes 1, 2)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Logic 0 Output, 32kHz | $V_{OL}$ | $I_{OL}$ = 1mA | | | | 0.4 | V |
| Logic 1 Output, DOUT | $V_{OH}$ | $I_{OH}$ = -1.0mA | | 0.85 x $V_{CC}$ | | | V |
| Logic 0 Output, DOUT, $\overline{INT}$/SQW | $V_{OL}$ | $I_{OL}$ = 3mA | | | | 0.4 | V |
| Logic 0 Output, $\overline{RST}$ | $V_{OL}$ | $I_{OL}$ = 1.0mA | | | | 0.4 | V |
| Output Leakage Current 32kHz, $\overline{INT}$/SQW, DOUT | $I_{LO}$ | Output high impedance | | -1 | 0 | +1 | µA |
| Input Leakage DIN, $\overline{CS}$, SCLK | $I_{LI}$ | | | -1 | | +1 | µA |
| $\overline{RST}$ Pin I/O Leakage | $I_{OL}$ | $\overline{RST}$ high impedance (Note 5) | | -200 | | +10 | µA |
| **TCXO ($V_{CC}$ = 2.3V to 5.5V, $V_{BAT}$ = 2.3V to 3.8V, $T_A$ = -40°C to +85°C, unless otherwise noted.) (Notes 1 and 2)** | | | | | | | |
| Output Frequency | $f_{OUT}$ | $V_{CC}$ = 3.3V or $V_{BAT}$ = 3.3V | | | 32.768 | | kHz |
| Frequency Stability vs. Temperature | $\Delta f/f_{OUT}$ | $V_{CC}$ = 3.3V or $V_{BAT}$ = 3.3V | 0°C to +40°C | -2 | | +2 | ppm |
| | | | -40°C to 0°C and +40°C to +85°C | -3.5 | | +3.5 | |
| Frequency Stability vs. Voltage | Δf/V | | | | 1 | | ppm/V |
| Trim Register Frequency Sensitivity per LSB | Δf/LSB | Specified at: | -40°C | | 0.7 | | ppm |
| | | | +25°C | | 0.1 | | |
| | | | +70°C | | 0.4 | | |
| | | | +85°C | | 0.8 | | |
| Temperature Accuracy | Temp | | | -3 | | +3 | °C |
| Crystal Aging | $\Delta f/f_{OUT}$ | After reflow, not production tested | First year | | ±1.0 | | ppm |
| | | | 0–10 years | | ±5.0 | | |

## ELECTRICAL CHARACTERISTICS

(**$V_{CC}$ = 0V, $V_{BAT}$ = 2.0V to 3.8V**, $T_A$ = -40°C to +85°C, unless otherwise noted.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Timekeeping Battery Current (Note 4) | $I_{BATT}$ | $\overline{EOSC}$ = 0, BBSQW = 0, CRATE1 = CRATE0 = 0 | $V_{BAT}$ = 3.4V | | 1.5 | 2.3 | µA |
| | | | $V_{BAT}$ = 3.8V | | 1.5 | 2.5 | |
| Temperature Conversion Current | $I_{BATTC}$ | $\overline{EOSC}$ = 0, BBSQW = 0 | | | | 400 | µA |
| Data-Retention Current | $I_{BATTDR}$ | $\overline{EOSC}$ = 1 | | | | 100 | nA |

# Extremely Accurate SPI Bus RTC with Integrated Crystal and SRAM

## AC ELECTRICAL CHARACTERISTICS

($V_{CC}$ = 2.0V to 5.5V, $T_A$ = -40°C to +85°C, unless otherwise noted.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| SCLK Clock Frequency | $f_{SCL}$ | 2.7V ≤ $V_{CC}$ ≤ 5.5V | | | 4 | MHz |
| | | 2.0V ≤ $V_{CC}$ < 2.7V | | | 2 | |
| Data to SCLK Setup | $t_{DC}$ | | 30 | | | ns |
| SCLK to Data Hold | $t_{CDH}$ | | 30 | | | ns |
| SCLK to $\overline{CS}$ Setup | $t_{CCS}$ | | 30 | | | ns |
| SCLK to Data Valid (Note 6) | $t_{CDD}$ | 2.7V ≤ $V_{CC}$ ≤ 5.5V | | | 80 | ns |
| | | 2.0V ≤ $V_{CC}$ < 2.7V | | | 160 | |
| SCLK Low Time | $t_{CL}$ | 2.7V ≤ $V_{CC}$ ≤ 5.5V | 110 | | | ns |
| | | 2.0V ≤ $V_{CC}$ < 2.7V | 220 | | | |
| SCLK High Time | $t_{CH}$ | 2.7V ≤ $V_{CC}$ ≤ 5.5V | 110 | | | ns |
| | | 2.0V ≤ $V_{CC}$ < 2.7V | 220 | | | |
| SCLK Rise and Fall | $t_R$, $t_F$ | | | | 200 | ns |
| $\overline{CS}$ to SCLK Setup | $t_{CC}$ | | 400 | | | ns |
| SCLK to $\overline{CS}$ Hold | $t_{CCH}$ | 2.7V ≤ $V_{CC}$ ≤ 5.5V | 100 | | | ns |
| | | 2.0V ≤ $V_{CC}$ < 2.7V | 200 | | | |
| $\overline{CS}$ Inactive Time | $t_{CWH}$ | | 400 | | | ns |
| $\overline{CS}$ to Output High Impedance | $t_{CDZ}$ | (Note 7) | | | 40 | ns |
| Pushbutton Debounce | $PB_{DB}$ | | | 250 | | ms |
| Reset Active Time | $t_{RST}$ | | | 250 | | ms |
| Oscillator Stop Flag (OSF) Delay | $t_{OSF}$ | (Note 8) | | 100 | | ms |
| Temperature Conversion Time | $t_{CONV}$ | | | 125 | 200 | ms |

## POWER-SWITCH CHARACTERISTICS

($T_A$ = -40°C to +85°C)

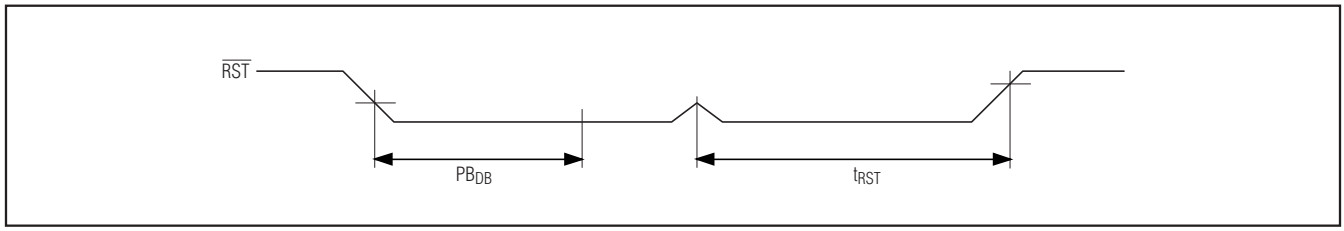
| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| $V_{CC}$ Fall Time; $V_{PF(MAX)}$ to $V_{PF(MIN)}$ | $t_{VCCF}$ | | 300 | | | µs |
| $V_{CC}$ Rise Time; $V_{PF(MIN)}$ to $V_{PF(MAX)}$ | $t_{VCCR}$ | | 0 | | | µs |
| Recovery at Power-Up | $t_{REC}$ | (Note 9) | | 125 | 300 | ms |

## CAPACITANCE

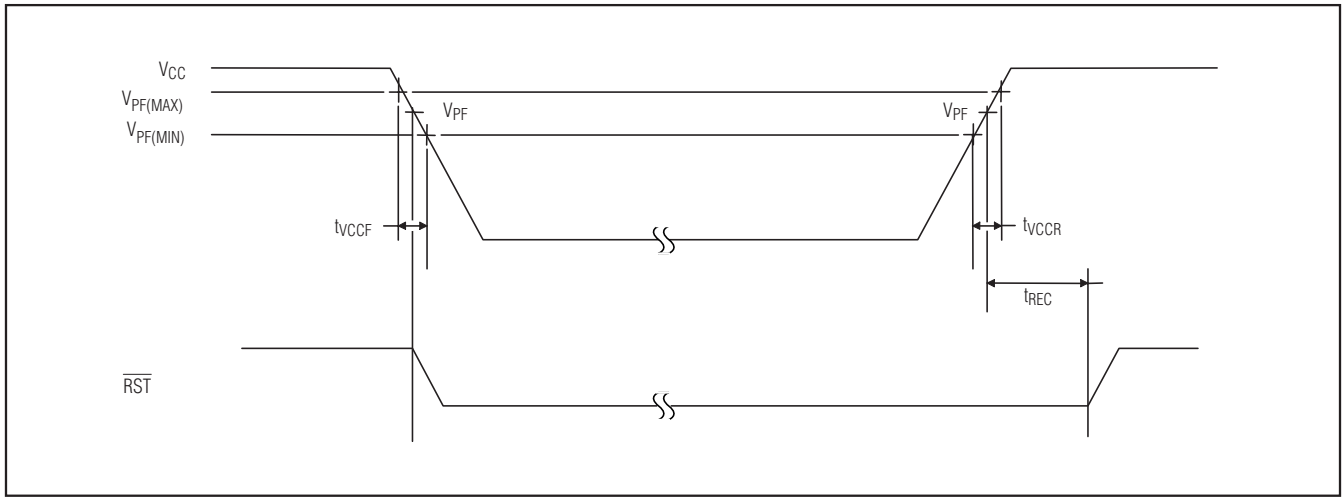
($T_A$ = +25°C)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Capacitance on All Input Pins | $C_{IN}$ | (Note 10) | | | 10 | pF |
| Capacitance on All Output Pins | $C_{IO}$ | Outputs high impedance (Note 10) | | | 10 | pF |

## Pushbutton Reset Timing




## Power-Switch Timing

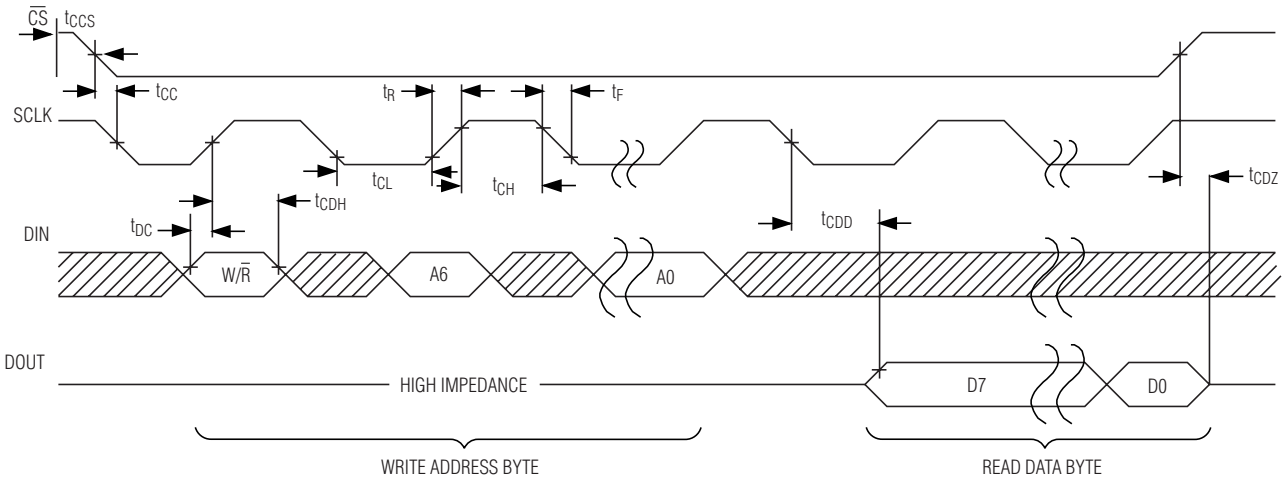



**WARNING: Negative undershoots below -0.3V while the part is in battery-backed mode may cause loss of data.**

**Note 1:** Limits at -40°C are guaranteed by design and not production tested.
**Note 2:** All voltages are referenced to ground.
**Note 3:** Measured at $V_{IH}$ = 0.8 x $V_{CC}$ or $V_{IL}$ = 0.2 x $V_{CC}$, 10ns rise/fall time, DOUT = no load.
**Note 4:** Current is the averaged input current, which includes the temperature conversion current. CRATE1 = CRATE0 = 0.
**Note 5:** The $\overline{RST}$ pin has an internal 50kΩ (nominal) pullup resistor to $V_{CC}$.
**Note 6:** Measured at $V_{OH}$ = 0.8 x $V_{CC}$ or $V_{OL}$ = 0.2 x $V_{CC}$. Measured from the 50% point of SCLK to the $V_{OH}$ minimum of DOUT.
**Note 7:** With 50pF load.
**Note 8:** The parameter $t_{OSF}$ is the period of time the oscillator must be stopped for the OSF flag to be set over the voltage range of 0V ≤ $V_{CC}$ ≤ $V_{CC(MAX)}$ and 2.3V ≤ $V_{BAT}$ ≤ $V_{BAT(MAX)}$.
**Note 9:** This delay only applies if the oscillator is enabled and running. If the $\overline{EOSC}$ bit is 1, $t_{REC}$ is bypassed and $\overline{RST}$ immediately goes high.
**Note 10:** Guaranteed by design and not production tested.

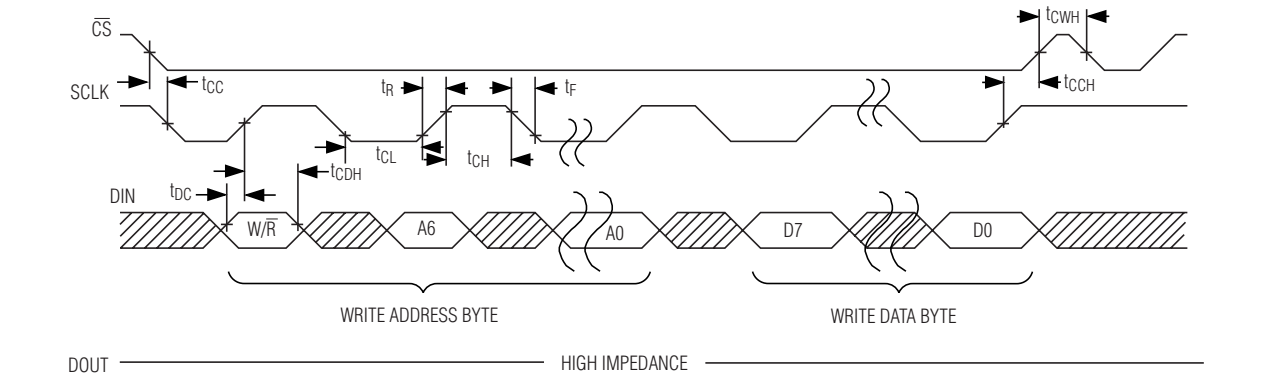
# Extremely Accurate SPI Bus RTC with Integrated Crystal and SRAM

## Timing Diagram—SPI Read Transfer




**NOTE:** SCLK CAN BE EITHER POLARITY, SHOWN FOR CPOL = 1.

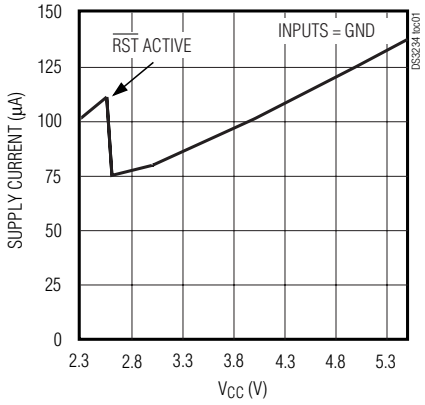
## Timing Diagram—SPI Write Transfer



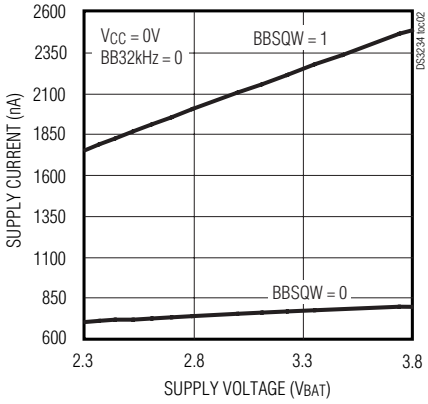
## Typical Operating Characteristics

($V_{CC}$ = +3.3V, $T_A$ = +25°C, unless otherwise noted.)

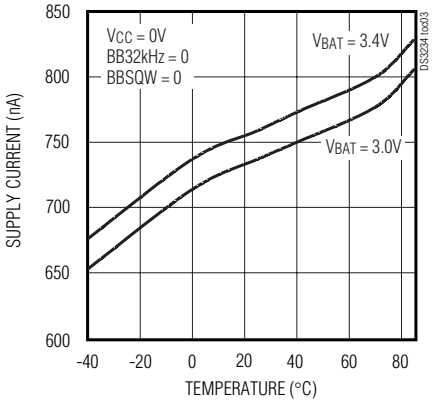
**STANDBY SUPPLY CURRENT vs. SUPPLY VOLTAGE**



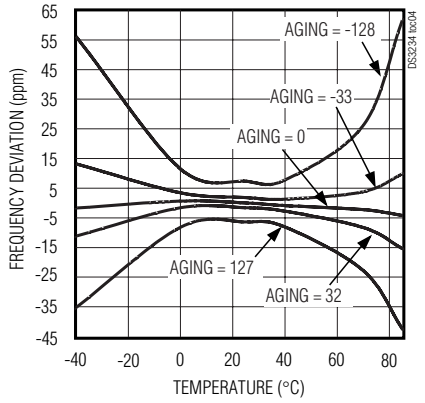

**BATTERY CURRENT vs. SUPPLY VOLTAGE**



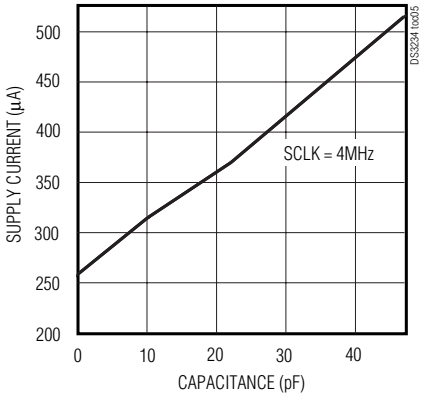

**BATTERY CURRENT vs. TEMPERATURE**



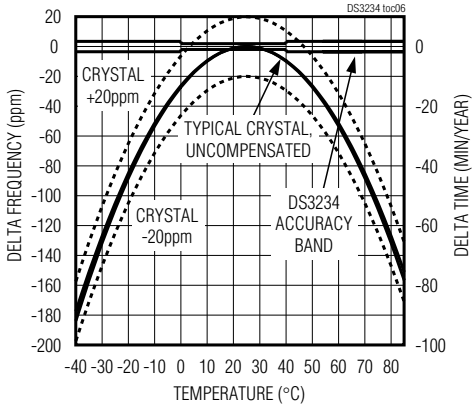

**FREQUENCY DEVIATION vs. TEMPERATURE vs. AGING VALUE**




**ICCA vs. DOUT LOAD**




**DELTA TIME AND FREQUENCY vs. TEMPERATURE**



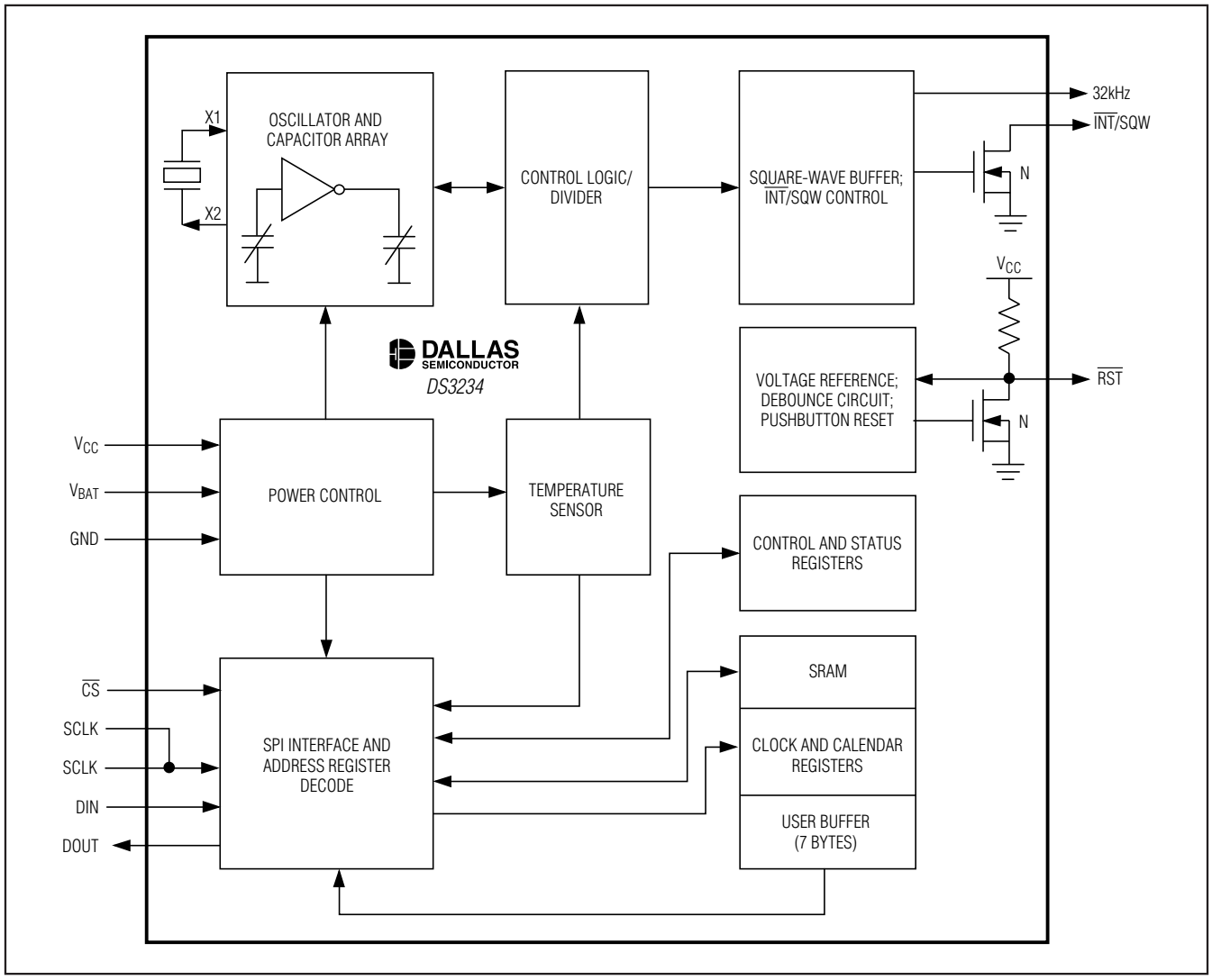
# Extremely Accurate SPI Bus RTC with Integrated Crystal and SRAM

## Pin Description

| PIN | NAME | FUNCTION |
|---|---|---|
| 1 | $\overline{CS}$ | Active-Low Chip Select Input. Used to select or deselect the device. |
| 2, 7–14 | N.C. | No Connection. Not connected internally. Must be connected to ground. |
| 3 | 32kHz | 32kHz Push-Pull Output. If disabled with either EN32kHz = 0 or BB32kHz = 0, the state of the 32kHz pin will be low. |
| 4 | $V_{CC}$ | DC Power Pin for Primary Power Supply. This pin should be decoupled using a 0.1µF to 1.0µF capacitor. |
| 5 | $\overline{INT}$/SQW | Active-Low Interrupt or Square-Wave Output. This open-drain pin requires an external pullup resistor. It can be left open if not used. This multifunction pin is determined by the state of the INTCN bit in the Control Register (0Eh). When INTCN is set to logic 0, this pin outputs a square wave and its frequency is determined by RS2 and RS1 bits. When INTCN is set to logic 1, then a match between the timekeeping registers and either of the alarm registers activates the $\overline{INT}$/SQW pin (if the alarm is enabled). Because the INTCN bit is set to logic 1 when power is first applied, the pin defaults to an interrupt output with alarms disabled. The pullup voltage can be up to 5.5V, regardless of the voltage on $V_{CC}$. If not used, this pin can be left floating. |
| 6 | $\overline{RST}$ | Active-Low Reset. This pin is an open-drain input/output. It indicates the status of $V_{CC}$ relative to the $V_{PF}$ specification. As $V_{CC}$ falls below $V_{PF}$, the $\overline{RST}$ pin is driven low. When $V_{CC}$ exceeds $V_{PF}$, for $t_{RST}$, the $\overline{RST}$ pin is driven high impedance. The active-low, open-drain output is combined with a debounced pushbutton input function. This pin can be activated by a pushbutton reset request. It has an internal 50kΩ nominal value pullup resistor to $V_{CC}$. No external pullup resistors should be connected. On first power-up, or if the crystal oscillator is disabled, $t_{RST}$ is bypassed and $\overline{RST}$ immediately goes high. |
| 15 | GND | Ground |
| 16 | $V_{BAT}$ | Backup Power-Supply Input. If $V_{BAT}$ is not used, connect to ground. Diodes placed in series between the $V_{BAT}$ pin and the battery can cause improper operation. UL recognized to ensure against reverse charging when used with a lithium battery. Go to www.maxim-ic.com/qa/info/ul. |
| 17 | DIN | SPI Data Input. Used to shift address and data into the device. |
| 18, 20 | SCLK | SPI Clock Input. Used to control timing of data into and out of the device. Either clock polarity can be used. The clock polarity is determined by the device based on the state of SCLK when $\overline{CS}$ goes low. Pins 18 and 20 are electrically connected together internally. |
| 19 | DOUT | SPI Data Output. Data is output on this pin when the device is in read mode; CMOS push-pull driver. |

# Extremely Accurate SPI Bus RTC with Integrated Crystal and SRAM

## Block Diagram




## Detailed Description

The DS3234 is a TCXO and RTC with integrated crystal and 256 bytes of SRAM. An integrated sensor periodically samples the temperature and adjusts the oscillator load to compensate for crystal drift caused by temperature variations. The DS3234 provides user-selectable sample rates. This allows the user to select a temperature sensor sample rate that allows for various temperature rates of change, while minimizing current consumption by temperature sensor sampling. The user should select a sample rate based upon the expected temperature rate of change, with faster sample rates for applications where the ambient temperature changes significantly over a short time. The TCXO provides a stable and accurate reference clock, and maintains the RTC to within ±2 minutes per year accuracy from -40°C to +85°C. The TCXO frequency output is available at the 32kHz pin. The RTC is a low-power clock/calendar with two programmable time-of-day alarms and a programmable square-wave output. The INT/SQW provides either an interrupt signal due to alarm conditions or a square-wave output. The clock/calendar provides seconds, minutes, hours, day,

# Extremely Accurate SPI Bus RTC with Integrated Crystal and SRAM

date, month, and year information. The date at the end of the month is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The clock operates in either the 24-hour or 12-hour format with AM/PM indicator. Access to the internal registers is possible through an SPI bus interface.

A temperature-compensated voltage reference and comparator circuit monitors the level of $V_{CC}$ to detect power failures and to automatically switch to the backup supply when necessary. When operating from the backup supply, access is inhibited to minimize supply current. Oscillator, time and date, and TCXO operations can continue while the backup supply powers the device. The $\overline{RST}$ pin provides an external pushbutton function and acts as an indicator of a power-fail event.

## Operation

The block diagram shows the main elements of the DS3234. The eight blocks can be grouped into four functional groups: TCXO, power control, pushbutton function, and RTC. Their operations are described separately in the following sections.

### 32kHz TCXO

The temperature sensor, oscillator, and control logic form the TCXO. The controller reads the output of the on-chip temperature sensor and uses a lookup table to determine the capacitance required, adds the aging correction in the AGE register, and then sets the capacitance selection registers. New values, including changes to the AGE register, are loaded only when a change in the temperature value occurs. The temperature is read on initial application of $V_{CC}$ and once every 64 seconds (default, see the description for CRATE1 and CRATE0 in the *Control/Status Register* section) afterwards.

### Power Control

The power control function is provided by a temperature-compensated voltage reference and a comparator circuit that monitors the $V_{CC}$ level. The device is fully accessible and data can be written and read when $V_{CC}$ is greater than $V_{PF}$. However, when $V_{CC}$ falls below both $V_{PF}$ and $V_{BAT}$, the internal clock registers are blocked from any access. If $V_{PF}$ is less than $V_{BAT}$, the device power is switched from $V_{CC}$ to $V_{BAT}$ when $V_{CC}$ drops below $V_{PF}$. If $V_{PF}$ is greater than $V_{BAT}$, the device power is switched from $V_{CC}$ to $V_{BAT}$ when $V_{CC}$ drops below $V_{BAT}$. After $V_{CC}$ returns above both $V_{PF}$ and $V_{BAT}$, read and write access is allowed after $\overline{RST}$ goes high (Table 1).

To preserve the battery, the first time $V_{BAT}$ is applied to the device, the oscillator does not start up until $V_{CC}$ crosses $V_{PF}$. After the first time $V_{CC}$ is ramped up, the oscillator starts up and the $V_{BAT}$ source powers the oscillator during power-down and keeps the oscillator running. When the DS3234 switches to $V_{BAT}$, the oscillator may be disabled by setting the $\overline{EOSC}$ bit.

**Table 1. Power Control**

| SUPPLY CONDITION | READ/WRITE ACCESS | ACTIVE SUPPLY | $\overline{RST}$ |
|---|---|---|---|
| $V_{CC} < V_{PF}$, $V_{CC} < V_{BAT}$ | No | $V_{BAT}$ | Active |
| $V_{CC} < V_{PF}$, $V_{CC} > V_{BAT}$ | Yes | $V_{CC}$ | Active |
| $V_{CC} > V_{PF}$, $V_{CC} < V_{BAT}$ | Yes | $V_{CC}$ | Inactive |
| $V_{CC} > V_{PF}$, $V_{CC} > V_{BAT}$ | Yes | $V_{CC}$ | Inactive |

## $V_{BAT}$ Operation

There are several modes of operation that affect the amount of $V_{BAT}$ current that is drawn. When the part is powered by $V_{BAT}$, timekeeping current ($I_{BATT}$), which includes the averaged temperature conversion current, $I_{BATTC}$, is drawn (refer to Application Note 3644: *Power Considerations for Accurate Real-Time Clocks* for details). Temperature conversion current, $I_{BATTC}$, is specified since the system must be able to support the periodic higher current pulse and still maintain a valid voltage level. Data retention current, $I_{BATTDR}$, is the current drawn by the part when the oscillator is stopped ($\overline{EOSC}$ = 1). This mode can be used to minimize battery requirements for times when maintaining time and date information is not necessary, e.g., while the end system is waiting to be shipped to a customer.

### Pushbutton Reset Function

The DS3234 provides for a pushbutton switch to be connected to the $\overline{RST}$ output pin. When the DS3234 is not in a reset cycle, it continuously monitors the $\overline{RST}$ signal for a low going edge. If an edge transition is detected, the DS3234 debounces the switch by pulling the $\overline{RST}$ low. After the internal timer has expired ($PB_{DB}$), the DS3234 continues to monitor the $\overline{RST}$ line. If the line is still low, the DS3234 continuously monitors the line looking for a rising edge. Upon detecting release, the DS3234 forces the $\overline{RST}$ pin low and holds it low for $t_{RST}$.

The same pin, $\overline{RST}$, is used to indicate a power-fail condition. When $V_{CC}$ is lower than $V_{PF}$, an internal power-fail signal is generated, which forces the $\overline{RST}$ pin low. When $V_{CC}$ returns to a level above $V_{PF}$, the $\overline{RST}$ pin is held low for $t_{REC}$ to allow the power supply to stabilize. If the $\overline{EOSC}$ bit is set to logic 1 (to disable the oscillator in battery-backup mode), $t_{REC}$ is bypassed and $\overline{RST}$ immediately goes high.

When $\overline{RST}$ is active due to a power-fail condition (see Table 1), SPI operations are inhibited while the TCXO and RTC continue to operate. When $\overline{RST}$ is active due to a pushbutton event, it does not affect the operation of the TCXO, SPI interface, or RTC functions.

### Real-Time Clock

With the clock source from the TCXO, the RTC provides seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The clock operates in either the 24-hour or 12-hour format with an $\overline{AM}$/PM indicator.

The clock provides two programmable time-of-day alarms and a programmable square-wave output. The $\overline{INT}$/SQW pin either generates an interrupt due to alarm condition or outputs a square-wave signal and the selection is controlled by the bit INTCN.

### SRAM

The DS3234 provides 256 bytes of general-purpose battery-backed read/write memory. The SRAM can be written or read whenever $V_{CC}$ is above either $V_{PF}$ or $V_{BAT}$.

## Address Map

Figure 1 shows the address map for the DS3234 timekeeping registers. During a multibyte access, when the address pointer reaches the end of the register space (13h read, 93h write), it wraps around to the beginning (00h read, 80h write). The DS3234 does not respond to a read or write to any reserved address, and the internal address pointer does not increment. Address pointer operation when accessing the 256-byte SRAM data is covered in the description of the SRAM address and data registers. On the falling edge of $\overline{CS}$, or during a multibyte access when the address pointer increments to location 00h, the current time is transferred to a second set of registers. The time information is read from these secondary registers, while the internal clock registers continue to increment normally. If the time and date registers are read using a multibyte read, this eliminates the need to reread the registers in case the main registers update during a read.

## SPI Interface

The DS3234 operates as a slave device on the SPI serial bus. Access is obtained by selecting the part by the $\overline{CS}$ pin and clocking data into/out of the part using the SCLK and DIN/DOUT pins. Multiple byte transfers are supported within one $\overline{CS}$ low period. The SPI on the DS3234 interface is accessible whenever $V_{CC}$ is above either $V_{BAT}$ or $V_{PF}$.

## Clock and Calendar

The time and calendar information is obtained by reading the appropriate register bytes. Figure 1 illustrates the RTC registers. The time and calendar data are set or initialized by writing the appropriate register bytes. The contents of the time and calendar registers are in binary-coded decimal (BCD) format. The DS3234 can be run in either 12-hour or 24-hour mode. Bit 6 of the hours register is defined as the 12- or 24-hour mode select bit. When high, 12-hour mode is selected. In 12-hour mode, bit 5 is the $\overline{AM}$/PM bit with logic-high being PM. In 24-hour mode, bit 5 is the second 10-hour bit (20–23 hours). The century bit (bit 7 of the month register) is toggled when the years register overflows from 99 to 00.

The day-of-week register increments at midnight. Values that correspond to the day of week are user-defined but must be sequential (i.e., if 1 equals Sunday, then 2 equals Monday, and so on). Illogical time and date entries result in undefined operation.

When reading or writing the time and date registers, secondary (user) buffers are used to prevent errors when the internal registers update. When reading the time and date registers, the user buffers are synchronized to the internal registers on the falling edge of $\overline{CS}$ or and when the register pointer rolls over to zero. The time information is read from these secondary registers, while the clock continues to run. This eliminates the need to reread the registers in case the main registers update during a read.

The countdown chain is reset whenever the seconds register is written. Write transfers occur when the last bit of a byte is clocked in. Once the countdown chain is reset, to avoid rollover issues the remaining time and date registers must be written within 1 second. The 1Hz square-wave output, if enabled, transitions high 500ms after the seconds data transfer.

# Extremely Accurate SPI Bus RTC with Integrated Crystal and SRAM

## Figure 1. Address Map for DS3234 Timekeeping Registers and SRAM

| ADDRESS READ/WRITE | | MSB BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | LSB BIT 0 | FUNCTION | RANGE |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 00h | 80h | 0 | 10 Seconds | | | Seconds | | | | Seconds | 00–59 |
| 01h | 81h | 0 | 10 Minutes | | | Minutes | | | | Minutes | 00–59 |
| 02h | 82h | 0 | 12/$\overline{24}$ | $\overline{AM}$/PM<br>10 hr | 10 hr | Hour | | | | Hours | 1-12 +$\overline{AM}$ /PM<br>00-23 |
| 03h | 83h | 0 | 0 | 0 | 0 | 0 | Day | | | Day | 1-7 |
| 04h | 84h | 0 | 0 | 10 Date | | Date | | | | Date | 01-31 |
| 05h | 85h | Century | 0 | 0 | 10 Mo | Month | | | | Month/<br>Century | 01-12 + Century |
| 06h | 86h | 10 Year | | | | Year | | | | Year | 00-99 |
| 07h | 87h | A1M1 | 10 Seconds | | | Seconds | | | | Alarm 1<br>Seconds | 00-59 |
| 08h | 88h | A1M2 | 10 Minutes | | | Minutes | | | | Alarm 1<br>Minutes | 00-59 |
| 09h | 89h | A1M3 | 12/$\overline{24}$ | $\overline{AM}$/PM<br>10 hr | 10 hr | Hour | | | | Alarm 1<br>Hours | 1-12 +$\overline{AM}$ /PM<br>00-23 |
| 0Ah | 8Ah | A1M4 | DY/$\overline{DT}$ | 0<br>10 Date | | Day<br>Date | | | | Alarm 1 Day<br>Alarm 1 Date | 1-7<br>01-31 |
| 0Bh | 8Bh | A2M2 | 10 Minutes | | | Minutes | | | | Alarm 2<br>Minutes | 00-59 |
| 0Ch | 8Ch | A2M3 | 12/$\overline{24}$ | $\overline{AM}$/PM<br>10 hr | 10 hr | Hour | | | | Alarm 2<br>Hours | 1-12 +$\overline{AM}$ /PM<br>00-23 |
| 0Dh | 8Dh | A2M4 | DY/$\overline{DT}$ | 0<br>10 Date | | Day<br>Date | | | | Alarm 2 Day<br>Alarm 2 Date | 1-7<br>01-31 |
| 0Eh | 8Eh | $\overline{EOSC}$ | BBSQW | CONV | RS2 | RS1 | INTCN | A2IE | A1IE | Control | — |
| 0Fh | 8Fh | OSF | BB32kHz | CRATE1 | CRATE0 | EN32kHz | BSY | A2F | A1F | Control/<br>Status | — |
| 10h | 90h | SIGN | DATA | DATA | DATA | DATA | DATA | DATA | DATA | Crystal Aging<br>Offset | — |
| 11h | 91h | SIGN | DATA | DATA | DATA | DATA | DATA | DATA | DATA | Temp MSB | Read Only |
| 12h | 92h | DATA | DATA | 0 | 0 | 0 | 0 | 0 | 0 | Temp LSB | Read Only |
| 13h | 93h | 0 | 0 | 0 | 0 | 0 | 0 | 0 | BB_TD | Disable<br>Temp<br>Conversions | — |
| 14h–17h | 94h–97h | — | — | — | — | — | — | — | — | Reserved | — |
| 18h | 98h | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | SRAM<br>Address | — |
| 19h | 99h | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | SRAM Data | — |

***Note:*** *Unless otherwise specified, the registers' state is not defined when power is first applied. Bits defined as 0 cannot be written to 1 and will always read 0.*

## Alarms

The DS3234 contains two time-of-day/date alarms. Alarm 1 can be set by writing to registers 07h to 0Ah. Alarm 2 can be set by writing to registers 0Bh to 0Dh. The alarms can be programmed (by the alarm enable and INTCN bits of the control register) to activate the $\overline{INT}$/SQW output on an alarm match condition. Bit 7 of each of the time-of-day/date alarm registers are mask bits (Table 2). When all the mask bits for each alarm are logic 0, an alarm only occurs when the values in the timekeeping registers match the corresponding values stored in the time-of-day/date alarm registers. The alarms can also be programmed to repeat every second, minute, hour, day, or date. Table 2 shows the possible settings. Configurations not listed in the table will result in illogical operations.

The DY/$\overline{DT}$ bits (bit 6 of the alarm day/date registers) control whether the alarm value stored in bits 0 to 5 of that register reflects the day of the week or the date of the month. If DY/$\overline{DT}$ is written to logic 0, the alarm will be the result of a match with date of the month. If DY/$\overline{DT}$ is written to logic 1, the alarm will be the result of a match with day of the week.

When the RTC register values match alarm register settings, the corresponding Alarm Flag 'A1F' or 'A2F' bit is set to logic 1. If the corresponding Alarm Interrupt Enable 'A1IE' or 'A2IE' is also set to logic 1 and the INTCN bit is set to logic 1, the alarm condition activates the $\overline{INT}$/SQW signal. The match is tested on the once-per-second update of the time and date registers.

### Table 2. Alarm Mask Bits

| DY/$\overline{DT}$ | ALARM 1 REGISTER MASK BITS (BIT 7) | | | | ALARM RATE |
|---|---|---|---|---|---|
| | A1M4 | A1M3 | A1M2 | A1M1 | |
| X | 1 | 1 | 1 | 1 | Alarm once per second |
| X | 1 | 1 | 1 | 0 | Alarm when seconds match |
| X | 1 | 1 | 0 | 0 | Alarm when minutes and seconds match |
| X | 1 | 0 | 0 | 0 | Alarm when hours, minutes, and seconds match |
| 0 | 0 | 0 | 0 | 0 | Alarm when date, hours, minutes, and seconds match |
| 1 | 0 | 0 | 0 | 0 | Alarm when day, hours, minutes, and seconds match |

| DY/$\overline{DT}$ | ALARM 2 REGISTER MASK BITS (BIT 7) | | | ALARM RATE |
|---|---|---|---|---|
| | A2M4 | A2M3 | A2M2 | |
| X | 1 | 1 | 1 | Alarm once per minute (00 seconds of every minute) |
| X | 1 | 1 | 0 | Alarm when minutes match |
| X | 1 | 0 | 0 | Alarm when hours and minutes match |
| 0 | 0 | 0 | 0 | Alarm when date, hours, and minutes match |
| 1 | 0 | 0 | 0 | Alarm when day, hours, and minutes match |

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## Control Register (0Eh/8Eh)

| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|---|
| **NAME:** | $\overline{EOSC}$ | BBSQW | CONV | RS2 | RS1 | INTCN | A2IE | A1IE |
| **POR*:** | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |

**POR is defined as the first application of power to the device, either $V_{BAT}$ or $V_{CC}$.*

## Special-Purpose Registers

The DS3234 has two additional registers (control and control/status) that control the real-time clock, alarms, and square-wave output.

### Control Register (0Eh/8Eh)

**Bit 7: Enable Oscillator ($\overline{EOSC}$).** When set to logic 0, the oscillator is started. When set to logic 1, the oscillator is stopped when the DS3234 switches to battery power. This bit is clear (logic 0) when power is first applied. When the DS3234 is powered by $V_{CC}$, the oscillator is always on regardless of the status of the $\overline{EOSC}$ bit. When $\overline{EOSC}$ is disabled, all register data is static.

**Bit 6: Battery-Backed Square-Wave Enable (BBSQW).** When set to logic 1, this bit enables the square-wave or interrupt output when $V_{CC}$ is absent and the DS3234 is being powered by the $V_{BAT}$ pin. When BBSQW is logic 0, the $\overline{INT}$/SQW pin goes high impedance when $V_{CC}$ falls below the power-fail trip point. This bit is disabled (logic 0) when power is first applied.

**Bit 5: Convert Temperature (CONV).** Setting this bit to 1 forces the temperature sensor to convert the temperature into digital code and execute the TCXO algorithm to update the capacitance array to the oscillator. This can only happen when a conversion is not already in progress. The user should check the status bit BSY before forcing the controller to start a new TCXO execution. A user-initiated temperature conversion does not affect the internal 64-second (default interval) update cycle. This bit is disabled (logic 0) when power is first applied.

A user-initiated temperature conversion does not affect the BSY bit for approximately 2ms. The CONV bit remains at a 1 from the time it is written until the conversion is finished, at which time both CONV and BSY go to 0. The CONV bit should be used when monitoring the status of a user-initiated conversion.

**Bits 4 and 3: Rate Select (RS2 and RS1).** These bits control the frequency of the square-wave output when the square wave has been enabled. The following table shows the square-wave frequencies that can be selected with the RS bits. These bits are both set to logic 1 (8.192kHz) when power is first applied.

**SQUARE-WAVE OUTPUT FREQUENCY**

| RS2 | RS1 | SQUARE-WAVE OUTPUT FREQUENCY |
|---|---|---|
| 0 | 0 | 1Hz |
| 0 | 1 | 1.024kHz |
| 1 | 0 | 4.096kHz |
| 1 | 1 | 8.192kHz |

**Bit 2: Interrupt Control (INTCN).** This bit controls the $\overline{INT}$/SQW signal. When the INTCN bit is set to logic 0, a square wave is output on the $\overline{INT}$/SQW pin. When the INTCN bit is set to logic 1, a match between the timekeeping registers and either of the alarm registers activates the $\overline{INT}$/SQW (if the alarm is also enabled). The corresponding alarm flag is always set regardless of the state of the INTCN bit. The INTCN bit is set to logic 1 when power is first applied.

**Bit 1: Alarm 2 Interrupt Enable (A2IE).** When set to logic 1, this bit permits the alarm 2 flag (A2F) bit in the status register to assert $\overline{INT}$/SQW (when INTCN = 1). When the A2IE bit is set to logic 0 or INTCN is set to logic 0, the A2F bit does not initiate an interrupt signal. The A2IE bit is disabled (logic 0) when power is first applied.

**Bit 0: Alarm 1 Interrupt Enable (A1IE).** When set to logic 1, this bit permits the alarm 1 flag (A1F) bit in the status register to assert $\overline{INT}$/SQW (when INTCN = 1). When the A1IE bit is set to logic 0 or INTCN is set to logic 0, the A1F bit does not initiate the $\overline{INT}$/SQW signal. The A1IE bit is disabled (logic 0) when power is first applied.

## Control/Status Register (0Fh/8Fh)

| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|---|
| NAME: | OSF | BB32kHz | CRATE1 | CRATE0 | EN32kHz | BSY | A2F | A1F |
| POR*: | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |

**POR is defined as the first application of power to the device, either $V_{BAT}$ or $V_{CC}$.*

### Control/Status Register (0Fh/8Fh)

**Bit 7: Oscillator Stop Flag (OSF).** A logic 1 in this bit indicates that the oscillator either is stopped or was stopped for some period and may be used to judge the validity of the timekeeping data. This bit is set to logic 1 any time that the oscillator stops. The following are examples of conditions that can cause the OSF bit to be set:

1) The first time power is applied.
2) The voltages present on both $V_{CC}$ and $V_{BAT}$ are insufficient to support oscillation.
3) The $\overline{EOSC}$ bit is turned off in battery-backed mode.
4) External influences on the crystal (i.e., noise, leakage, etc.).

This bit remains at logic 1 until written to logic 0.

**Bit 6: Battery-Backed 32kHz Output (BB32kHz).** This bit enables the 32kHz output when powered from $V_{BAT}$ (provided EN32kHz is enabled). If BB32kHz = 0, the 32kHz output is low when the part is powered by $V_{BAT}$. This bit is enabled (logic 1) when power is first applied.

**Bits 5 and 4: Conversion Rate (CRATE1 and CRATE0).** These two bits control the sample rate of the TCXO. The sample rate determines how often the temperature sensor makes a conversion and applies compensation to the oscillator. Decreasing the sample rate decreases the overall power consumption by decreasing the frequency at which the temperature sensor operates. However, significant temperature changes that occur between samples may not be completely compensated for, which reduce overall accuracy. These bits are set to logic 0 when power is first applied.

| CRATE1 | CRATE0 | SAMPLE RATE (seconds) |
|---|---|---|
| 0 | 0 | 64 |
| 0 | 1 | 128 |
| 1 | 0 | 256 |
| 1 | 1 | 512 |

**Bit 3: Enable 32kHz Output (EN32kHz).** This bit indicates the status of the 32kHz pin. When set to logic 1, the 32kHz pin is enabled and outputs a 32.768kHz square-wave signal. When set to logic 0, the 32kHz pin is low. The initial power-up state of this bit is logic 1, and a 32.768kHz square-wave signal appears at the 32kHz pin after a power source is applied to the DS3234. This bit is enabled (logic 1) when power is first applied.

**Bit 2: Busy (BSY).** This bit indicates the device is busy executing TCXO functions. It goes to logic 1 when the conversion signal to the temperature sensor is asserted and then is cleared when the conversion is complete.

**Bit 1: Alarm 2 Flag (A2F).** A logic 1 in the alarm 2 flag bit indicates that the time matched the alarm 2 registers. If the A2IE bit and INTCN bit are set to logic 1, the $\overline{INT}$/SQW pin is driven low while A2F is active. A2F is cleared when written to logic 0. This bit can only be written to logic 0. Attempting to write to logic 1 leaves the value unchanged.

**Bit 0: Alarm 1 Flag (A1F).** A logic 1 in the alarm 1 flag bit indicates that the time matched the alarm 1 registers. If the A1IE bit and the INTCN bit are set to logic 1, the $\overline{INT}$/SQW pin is driven low while A1F is active. A1F is cleared when written to logic 0. This bit can only be written to logic 0. Attempting to write to logic 1 leaves the value unchanged.

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### Aging Offset (10h/90h)

| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|---|
| NAME: | SIGN | DATA | DATA | DATA | DATA | DATA | DATA | DATA |
| POR*: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

### Temperature Register (MSB) (11h)

| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|---|
| NAME: | SIGN | DATA | DATA | DATA | DATA | DATA | DATA | DATA |
| POR*: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

### Temperature Register (LSB) (12h)

| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|---|
| NAME: | DATA | DATA | 0 | 0 | 0 | 0 | 0 | 0 |
| POR*: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**POR is defined as the first application of power to the device, either $V_{BAT}$ or $V_{CC}$.*

## Aging Offset Register (10h/90h)

The aging offset register takes a user-provided value to add to or subtract from the oscillator capacitor array. The data is encoded in two's complement, with bit 7 representing the SIGN bit. One LSB represents the smallest capacitor to be switched in or out of the capacitance array at the crystal pins. The aging offset register capacitance value is added or subtracted from the capacitance value that the device calculates for each temperature compensation. The offset register is added to the capacitance array during a normal temperature conversion, if the temperature changes from the previous conversion, or during a manual user conversion (setting the CONV bit). To see the effects of the aging register on the 32kHz output frequency immediately, a manual conversion should be performed after each aging offset register change.

Positive aging values add capacitance to the array, slowing the oscillator frequency. Negative values remove capacitance from the array, increasing the oscillator frequency.

The change in ppm per LSB is different at different temperatures. The frequency vs. temperature curve is shifted by the values used in this register. At +25°C, one LSB typically provides about 0.1ppm change in frequency. These bits are all set to logic 0 when power is first applied.

Use of the aging register is not needed to achieve the accuracy as defined in the EC tables, but could be used to help compensate for aging at a given temperature. See the *Typical Operating Characteristics* section for a graph showing the effect of the register on accuracy over temperature.

## Temperature Registers (11h–12h)

Temperature is represented as a 10-bit code with a resolution of 0.25°C and is accessible at location 11h and 12h. The temperature is encoded in two's complement format, with bit 7 in the MSB representing the SIGN bit. The upper 8 bits, the integer portion, are at location 11h and the lower 2 bits, the fractional portion, are in the upper nibble at location 12h. Example: 00011001 01b = +25.25°C. Upon power reset, the registers are set to a default temperature of 0°C and the controller starts a temperature conversion.

The temperature is read on initial application of $V_{CC}$ and once every 64 seconds afterwards. The temperature registers are updated after each user-initiated conversion and on every 64-second conversion. The temperature registers are read-only.

## Temperature Control (13h/93h)

| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|---|
| **NAME:** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | BB_TD |
| **POR*:** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**POR is defined as the first application of power to the device, either $V_{BAT}$ or $V_{CC}$.*

## SRAM Address (18h/98h)

| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|---|
| **NAME:** | A7 | A6 | A5 | A4 | A2 | A1 | A1 | A0 |

## SRAM Data (19h/99h)

| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|---|
| **NAME:** | D7 | D6 | D5 | D4 | D2 | D1 | D1 | D0 |

***Note:*** *These registers do not default to any specific value.*

### Temperature Control Register (13h/93h)

**Bit 0: Battery-Backed Temperature Conversion Disable (BB_TD).** The battery-backed tempconv disable bit prevents automatic temperature conversions when the device is powered by the $V_{BAT}$ supply. This reduces the battery current at the expense of frequency accuracy.

### SRAM Address Register (18h/98h)

The SRAM address register provides the 8-bit address of the 256-byte memory array. The desired memory address should be written to this register before the data register is accessed. The contents of this register are incremented automatically if the data register is accessed more than once during a single transfer. When the contents of the address register reach 0FFh, the next access causes the register to roll over to 00h.

### SRAM Data Register (19h/99h)

The SRAM data register provides the data to be written to or the data read from the 256-byte memory array. During a read cycle, the data in this register is that found in the memory location in the SRAM address register (18h/98h). During a write cycle, the data in this register is placed in the memory location in the SRAM address register (18h/98h). When the SRAM data register is read or written, the internal register pointer remains at 19h/99h and the SRAM address register increments after each byte that is read or written, allowing multibyte transfers.

### SPI Serial Data Bus

The DS3234 provides a 4-wire SPI serial data bus to communicate in systems with an SPI host controller. The DS3234 supports both single byte and multiple byte data transfers for maximum flexibility. The DIN and DOUT pins are the serial data input and output pins, respectively. The $\overline{CS}$ input is used to initiate and terminate a data transfer. The SCLK pin is used to synchronize data movement between the master (microcontroller) and the slave devices (see Table 3). The shift clock (SCLK), which is generated by the microcontroller, is active only during address and data transfer to any device on the SPI bus. Input data (DIN) is latched on the internal strobe edge and output data (DOUT) is shifted out on the shift edge (Figure 2). There is one clock for each bit transferred. Address and data bits are transferred in groups of eight.

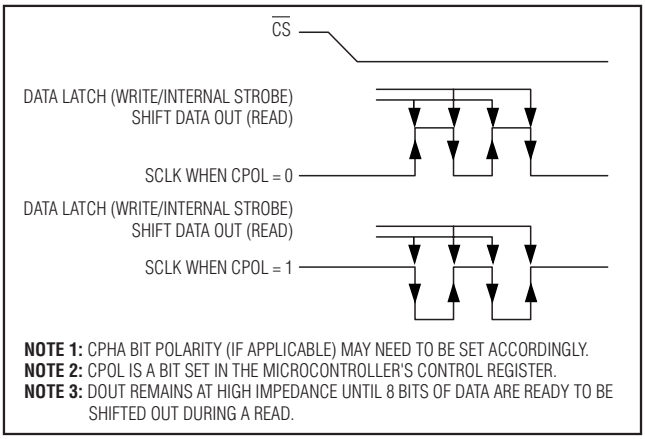



*Figure 2. Serial Clock as a Function of Microcontroller Clock-Polarity Bit*

# Extremely Accurate SPI Bus RTC with Integrated Crystal and SRAM

Address and data bytes are shifted MSB first into the serial data input (DIN) and out of the serial data output (DOUT). Any transfer requires the address of the byte to specify a write or read, followed by one or more bytes of data. Data is transferred out of the DOUT pin for a read operation and into the DIN for a write operation (Figures 3 and 4).

The address byte is always the first byte entered after $\overline{CS}$ is driven low. The most significant bit of this byte determines if a read or write takes place. If the MSB is 0, one or more read cycles occur. If the MSB is 1, one or more write cycles occur.

## Table 3. SPI Pin Function

| MODE | $\overline{CS}$ | SCLK | DIN | DOUT |
|---|---|---|---|---|
| Disable | H | Input Disabled | Input Disabled | High Impedance |
| Write | L | *CPOL = 1, SCLK Rising | Data Bit Latch | High Impedance |
| | | CPOL = 0, SCLK Falling | | |
| Read | L | CPOL = 1, SCLK Falling | X | Next Data Bit Shift** |
| | | CPOL = 0, SCLK Rising | | |
| Read Invalid Location | L | Don't Care | Don't Care | High Impedance |

**CPOL is the clock-polarity bit set in the control register of the host microprocessor.*

***DOUT remains at high impedance until 8 bits of data are ready to be shifted out during a read.*

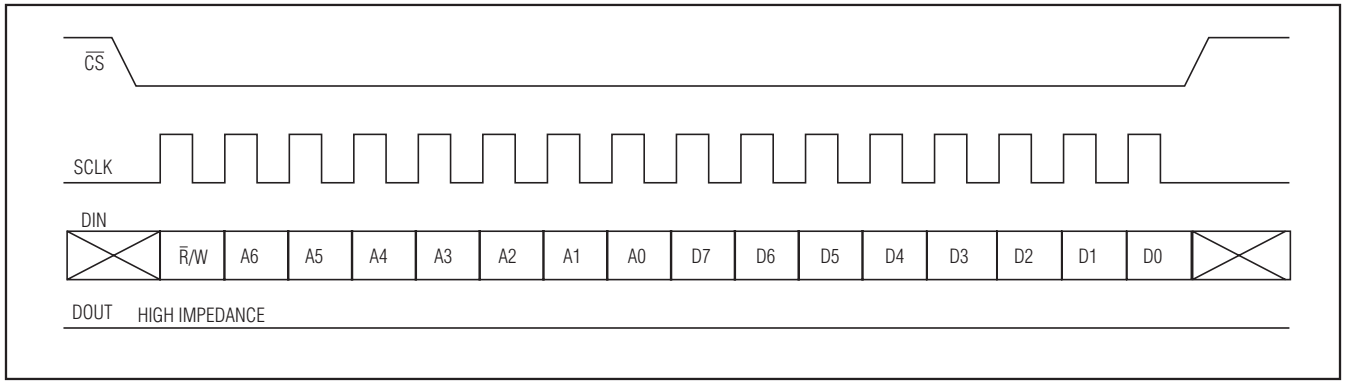



*Figure 3. SPI Single-Byte Write*

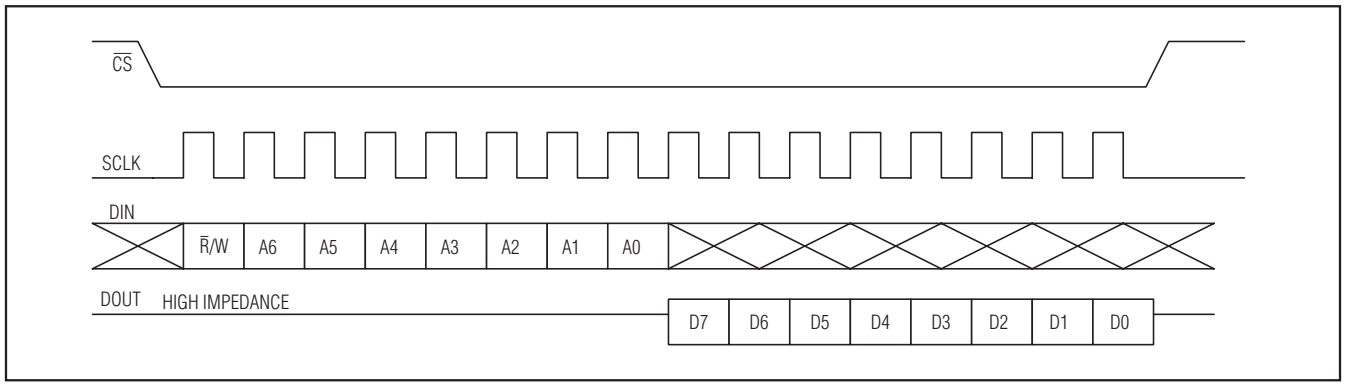



*Figure 4. SPI Single-Byte Read*

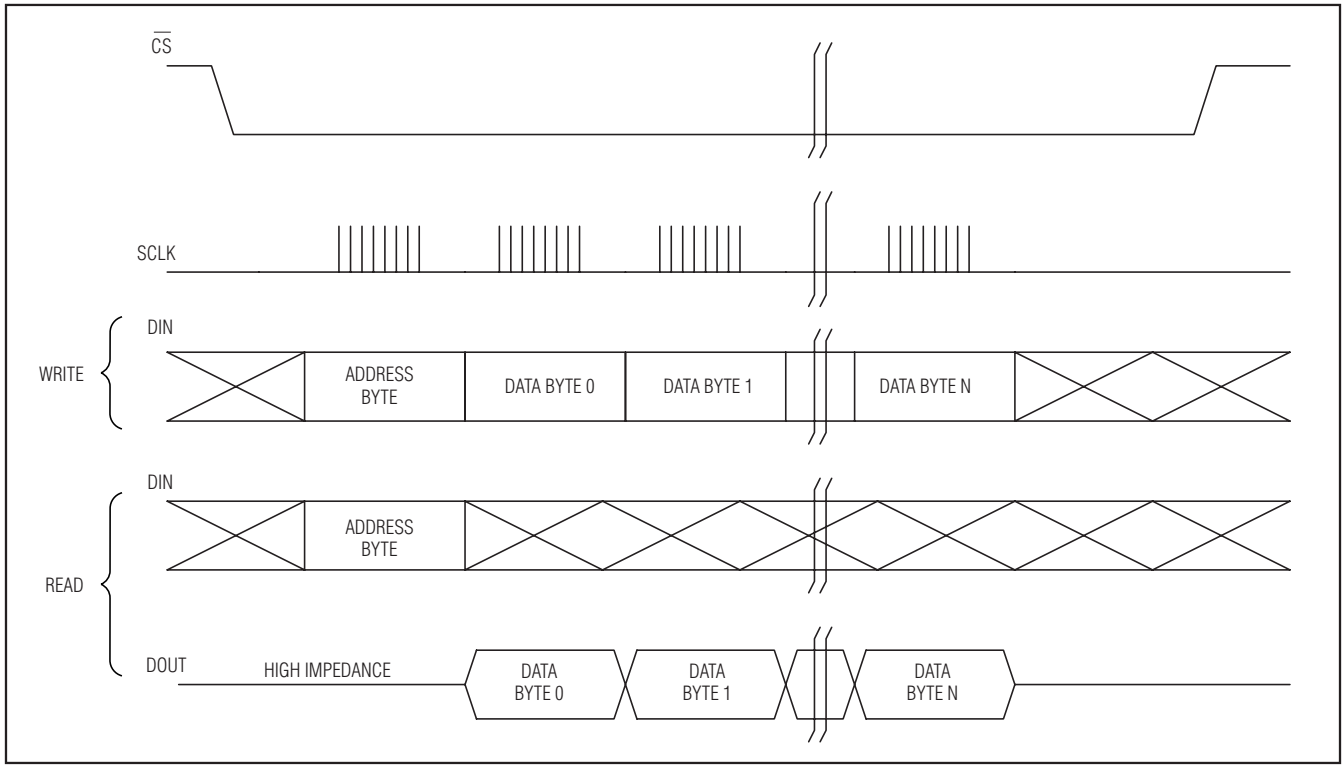



*Figure 5. SPI Multiple-Byte Burst Transfer*

Data transfers can occur one byte at a time or in multiple-byte burst mode. After $\overline{CS}$ is driven low, an address is written to the DS3234. After the address, one or more data bytes can be written or read. For a single-byte transfer, one byte is read or written and then $\overline{CS}$ is driven high. For a multiple-byte transfer, however, multiple bytes can be read or written after the address has been written (Figure 5). Each read or write cycle causes the RTC register address to automatically increment, which continues until the device is disabled. The address wraps to 00h after incrementing to 13h (during a read) and wraps to 80h after incrementing to 93h (during a write). An updated copy of the time is loaded into the user buffers upon the falling edge of $\overline{CS}$ and each time the address pointer increments from 13h to 00h. Because the internal and user copies of the time are only synchronized on these two events, an alarm condition can occur internally and activate the $\overline{INT}$/SQW pin independently of the user data.

If the SRAM is accessed by reading (address 19h) or writing (address 99h) the SRAM data register, the contents of the SRAM address register are automatically incremented after the first access, and all data cycles will use the SRAM data register.

## Handling, PC Board Layout, and Assembly

The DS3234 package contains a quartz tuning-fork crystal. Pick-and-place equipment can be used, but precautions should be taken to ensure that excessive shock and vibration are avoided. Ultrasonic cleaning should be avoided to prevent damage to the crystal.

Avoid running signal traces under the package, unless a ground plane is placed between the package and the signal line. All N.C. (no connect) pins must be connected to ground.

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## Chip Information

TRANSISTOR COUNT: 48,000
SUBSTRATE CONNECTED TO GROUND
PROCESS: CMOS

## Thermal Information

Theta-$J_A$: +55°C/W
Theta-$J_C$: +24°C/W

## Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

| PACKAGE TYPE | PACKAGE CODE | DOCUMENT NO. |
|---|---|---|
| 20 SO | — | **21-0042** |

# Extremely Accurate SPI Bus RTC with Integrated Crystal and SRAM

## Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|---|---|---|---|
| 0 | 2/06 | Initial release. | — |
| 1 | 7/07 | Clarified the behavior of $t_{REC}$ on initial power-up in the $\overline{RST}$ description of the *Pin Description*. | 8 |
| | | Corrected the POR for the BB32kHz bit from 0 to 1. | 15 |
| 2 | 10/08 | Updated the *Typical Operating Circuit*. | 1 |
| | | Removed the $V_{PU}$ parameter from the *Recommended DC Operating Conditions* table and added verbiage about the pullup to the *Pin Description* table for $\overline{INT}$/SQW. | 2, 8 |
| | | In the *Electrical Characteristics* table, added CRATE1 = CRATE0 = 0 to the $I_{BATT}$ parameter and changed the symbols for Timekeeping Battery Current, Temperature Conversion Current, and Data-Retention Current from $I_{BAT}$, $I_{TC}$, and $I_{BATTC}$ to $I_{BATT}$, $I_{BATTC}$, and $I_{BATTDR}$, respectively. | 3 |
| | | In the *AC Electrical Characteristics*, changed the $t_{CWH}$ specification from 400ns (max) to 400ns (min). | 4 |
| | | Added the Delta Time and Frequency vs. Temperature graph in the *Typical Operating Characteristics* section. | 7 |
| | | Updated the *Block Diagram*. | 9 |
| | | Added the *$V_{BAT}$ Operation* section, improved some sections of text for the *Pushbutton Reset Function, Aging Offset Register (10h/90h)*, and *Temperature Registers (11h–12h)* sections. | 10, 16 |
| | | Corrected the description of when the countdown chain is reset in the *Clock and Calendar* section. | 11 |

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