Short Form Data Sheet
April 2012

DS31400
8-Input, 14-Output, Dual DPLL Timing IC with Sub-ps Output Jitter

General Description

The DS31400 is a flexible, high-performance timing IC for diverse frequency conversion and frequency synthesis applications. On each of its eight input clocks and 14 output clocks, the device can accept or generate nearly any frequency between 2kHz and 750MHz. The device offers two independent DPLLs to serve two independent clock-generation paths.

The input clocks are divided down, fractionally scaled as needed, and continuously monitored for activity and frequency accuracy. The best input clock is selected, manually or automatically, as the reference clock for each of the two flexible, high-performance digital PLLs. Each DPLL locks to the selected reference and provides programmable bandwidth, very high-resolution holdover capability, and truly hitless switching between input clocks. The digital PLLs are followed by a clock synthesis subsystem that has seven fully programmable digital frequency synthesis blocks, three high-speed low-jitter APLLs, and 14 output clocks, each with its own 32-bit divider and phase adjustment. The APLLs provide fractional scaling and output jitter less than 1ps RMS.

For telecom systems, the device has all required features and functions to serve as a central timing function or as a line card timing IC. With a suitable oscillator the device meets the requirements of Stratum 2, 3E, 3, 4E, and 4; G.812 Types I to IV; G.813; and G.8262.

Applications

Frequency Conversion Applications in a Wide Variety of Equipment Types

Telecom Line Cards or Timing Cards with Any Mix of SONET/SDH, Synchronous Ethernet, and/or OTN Ports in WAN Equipment Including MSPPs, Ethernet Switches, Routers, DSLAMs, and Base Stations

Ordering Information

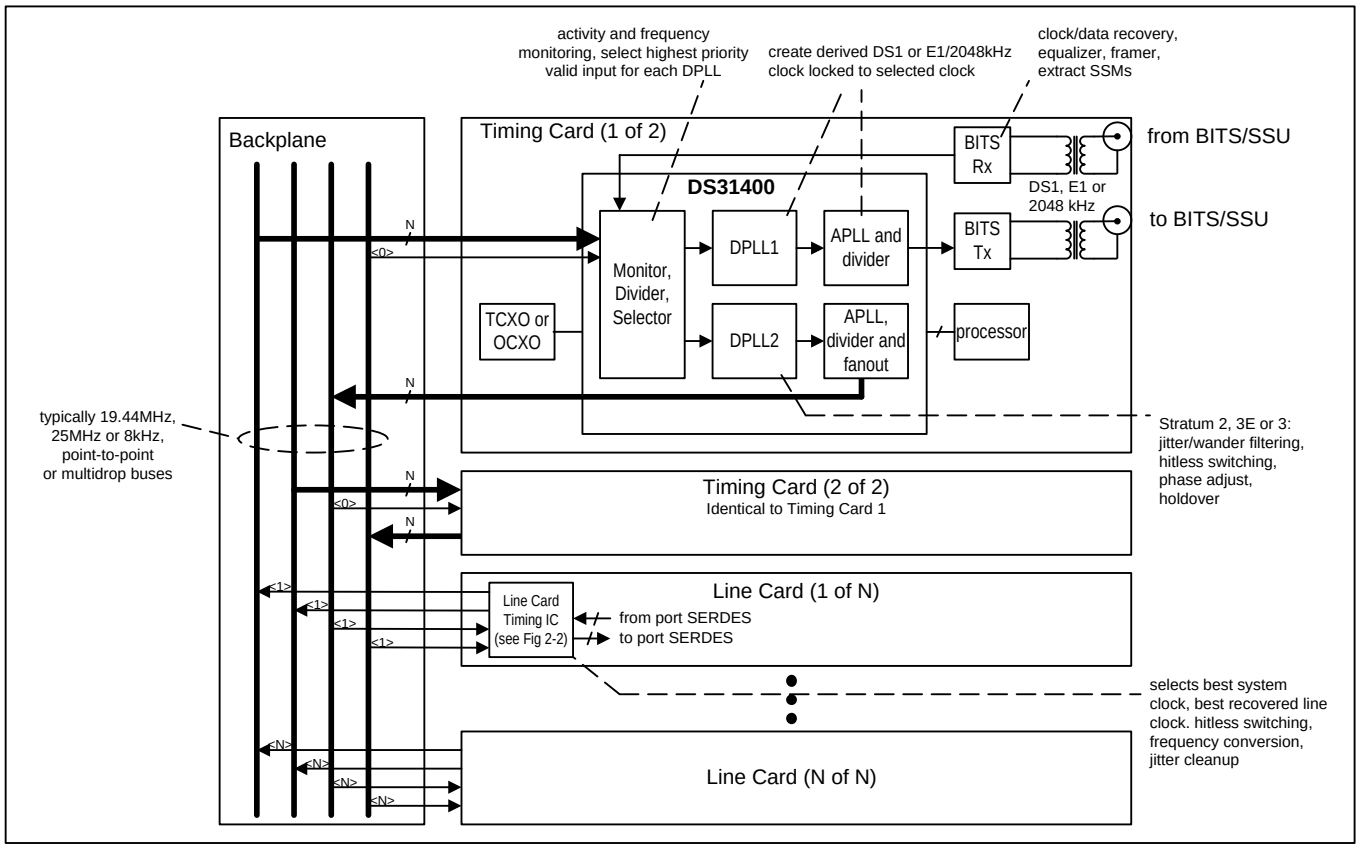
PART	TEMP RANGE	PIN-PACKAGE
DS31400GN	-40°C to +85°C	256 CSBGA
DS31400GN+	-40°C to +85°C	256 CSBGA

+Denotes a lead(Pb)-free/RoHS-compliant package.
SPI is a trademark of Motorola, Inc.

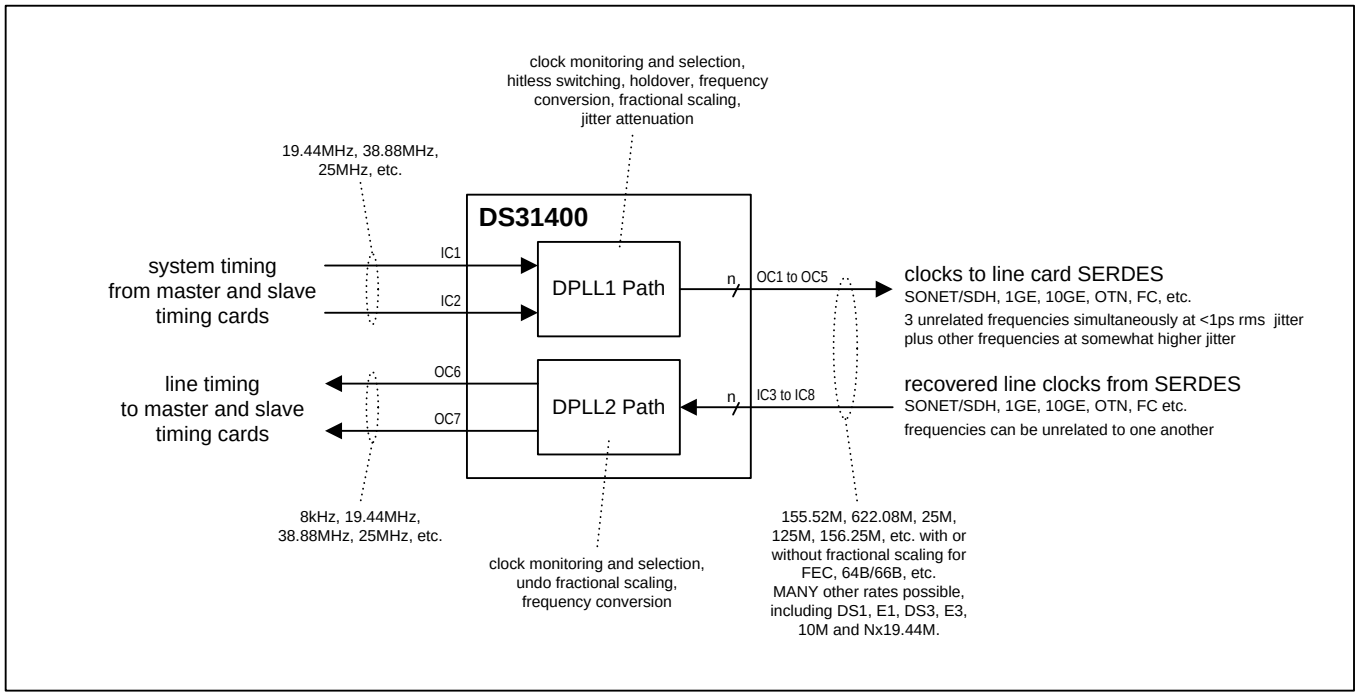
Features

- **Eight Input Clocks**
  - Differential or CMOS/TTL Format
  - Any Frequency from 2kHz to 750MHz
  - Fractional Scaling for 64B/66B and FEC Scaling (e.g., 64/66, 237/255, 238/255) or Any Other Downscaling Requirement
  - Continuous Input Clock Quality Monitoring
  - Automatic or Manual Clock Selection
  - Three 2/4/8kHz Frame Sync Inputs
- **Two High-Performance DPLLs**
  - Hitless Reference Switching on Loss of Input
  - Automatic or Manual Phase Build-Out
  - Holdover on Loss of All Inputs
  - Programmable Bandwidth, 0.5mHz to 400Hz
- **Seven Digital Frequency Synthesizers**
  - Each Can Slave to Either DPLL
  - Produce Any 2kHz Multiple Up to 77.76MHz
  - Per-DFS Clock Phase Adjust
- **Three Output APLLs**
  - Output Frequencies to 750MHz
  - High Resolution Fractional Scaling for FEC and 64B/66B (e.g., 255/237, 255/238, 66/64) or Any Other Scaling Requirement
  - Less than 1ps RMS Output Jitter
  - Simultaneously Produce Three Low-Jitter Rates from the Same Reference (e.g., 622.08MHz for SONET, 255/237 x 622.08MHz for OTU2, and 156.25MHz for 10GE)
- **14 Output Clocks in Seven Groups**
  - Nearly Any Frequency from < 1Hz to 750MHz
  - Each Group Slaves to a DFS Clock, Any APLL Clock, or Any Input Clock (Divided and Scaled)
  - Each Has a Differential Output (Three CML, Four LVDS/LVPECL) and Separate CMOS/TTL Output
  - 32-Bit Frequency Divider Per Output
  - Two Sync Pulse Outputs: 8kHz and 2kHz
- **General Features**
  - Suitable Line Card IC or Timing Card IC for Stratum 2/3E/3/4E/4, SMC, SEC/EEC, or SSU
  - Accepts and Produces Nearly Any Frequency fom 1Hz to 750MHz
  - Internal Compensation for Local Oscillator Frequency Error
  - SPI™ Processor Interface
  - 1.8V Operation with 3.3V I/O (5V Tolerant)
  - 17mm x 17mm CSGBA Package

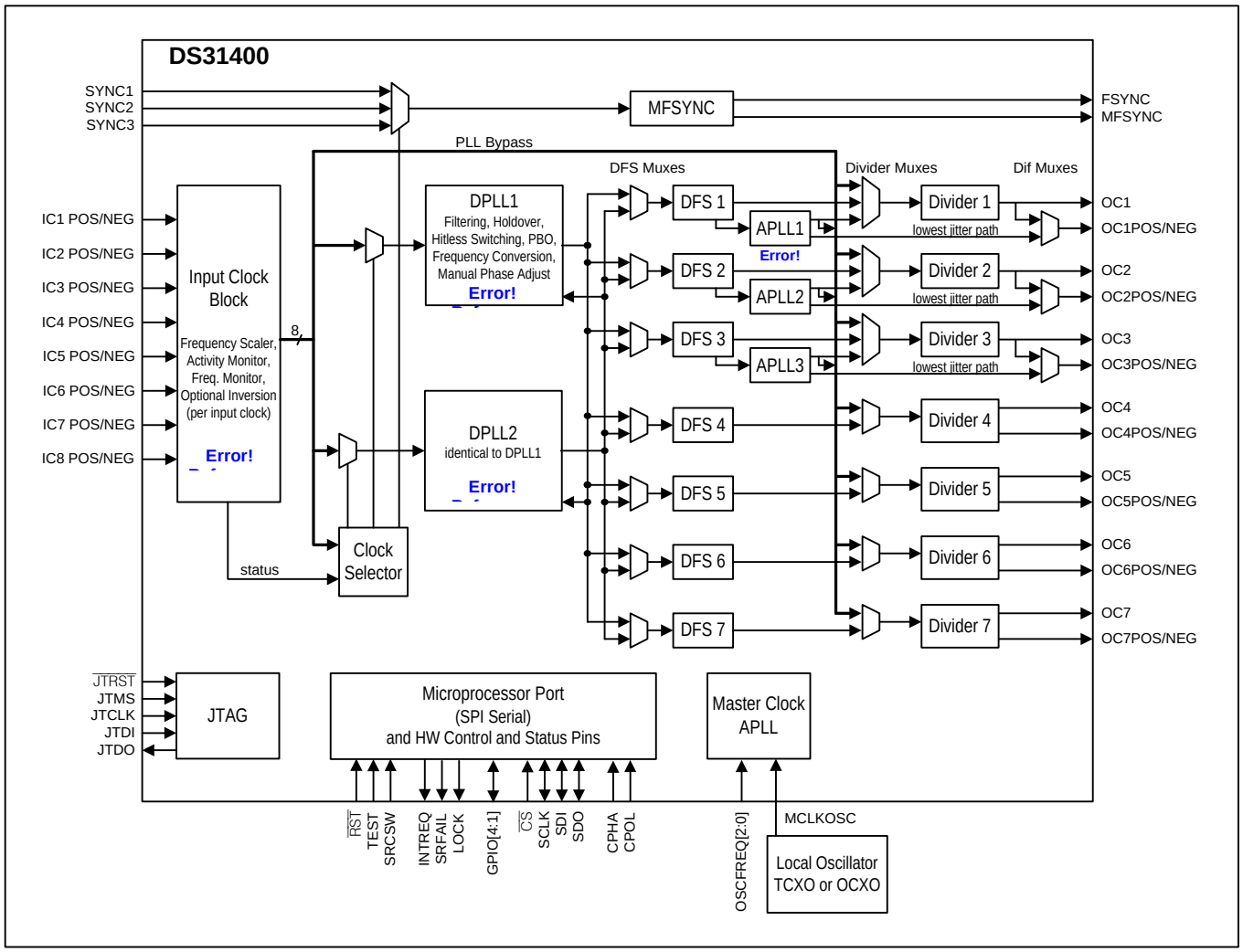
Application Example: Timing Card



Application Example: Line Card



Block Diagram



Detailed Features

Input Clock Features

- Eight input clocks, differential or CMOS/TTL signal format
- Input clocks can be any frequency from 2kHz up to 750MHz
- Supported telecom frequencies include PDH, SDH, Synchronous Ethernet, OTU-1, OTU-2, OTU-3
- Per-input fractional scaling (i.e., multiplying by N÷D where N is a 16-bit integer and D is a 32-bit integer and N<D) to undo 64B/66B and FEC scaling (e.g., 64/66, 238/255, 237/255, 236/255)
- Special mode allows locking to 1Hz input clocks
- All inputs constantly monitored by programmable activity monitors and frequency monitors
- Fast activity monitor can disqualify the selected reference after a few missing clock cycles
- Frequency measurement and frequency monitor thresholds with 0.2ppm resolution
- Three optional 2/4/8kHz frame-sync inputs

DPLL Features

- Very high-resolution DPLL architecture
- Sophisticated state machine automatically transitions between free-run, locked, and holdover states
- Revertive or nonrevertive reference selection algorithm
- Programmable bandwidth from 0.5mHz to 400Hz
- Separately configurable acquisition bandwidth and locked bandwidth
- Programmable damping factor to balance lock time with peaking: 1.2, 2.5, 5, 10 or 20
- Multiple phase detectors: phase/frequency and multicycle
- Phase/frequency locking (±360° capture) or nearest-edge phase locking (±180° capture)
- Multicycle phase detection and locking (up to ±8191UI) improves jitter tolerance and lock time
- Phase build-out in response to reference switching for true hitless switching
- Less than 1 ns output clock phase transient during phase build-out
- Output phase adjustment up to ±200ns in 6ps steps with respect to selected input reference
- High-resolution frequency and phase measurement
- Holdover frequency averaging over 1 second, 5.8 minute and 93.2 minute intervals
- Fast detection of input clock failure and transition to holdover mode
- Low-jitter frame sync (8kHz) and multiframe sync (2kHz) aligned with output clocks

Digital Frequency Synthesizer Features

- Seven independently programmable DFS blocks
- Each DFS can slave to either of the DPLLs
- Each DFS can synthesize any 2kHz multiple up to 77.76MHz
- Per-DFS phase adjust (1/256UI steps)
- Approximately 40ps RMS output jitter

Output APLL Features

- Simultaneously produce three high-frequency, low-jitter, rates from the same reference clock, e.g., 622.08MHz for SONET, 255/237 x 622.08MHz for OTU2, and156.25MHz for 10GE
- Standard telecom output frequencies include 622.08MHz, 155.52MHz and 19.44MHz for SONET/SDH and 156.25MHz, 125MHz and 25MHz for Synchronous Ethernet
- Very high-resolution fractional scaling (i.e., noninteger multiplication)
- Less than 1ps RMS output jitter

Output Clock Features

- Fourteen output clock signals in seven groups
- Output clock groups OC1 – OC3 have a very high-speed differential output (current-mode logic, ≤750MHz) and a separate CMOS/TTL output (≤125 MHz)
- Output clock groups OC4 – OC7 have a high-speed differential output (LVDS/LVPECL, ≤312.5MHz) and a separate CMOS/TTL ouptut (≤125 MHz)
- Supported telecom frequencies include PDH, SDH, Synchronous Ethernet, OTU-1, OTU-2, OTU-3
- Internal clock muxing allows each output group to slave to its associated DFS block, any of the APLLs, or any input clock (after being divided and scaled)
- Outputs sourced directly from APLLs have less than 1ps RMS output jitter
- Outputs sourced directly from DFS blocks have approximately 40ps RMS output jitter
- Optional 32-bit frequency divider per output
- 8kHz frame sync and 2kHz multiframe sync outputs have programmable polarity and pulse width and can be disciplined by a 2kHz or 8kHz frame sync input
- Per-output delay adjustment
- Per-output enable/disable
- All outputs disabled during reset

General Features

- SPI serial microprocessor interface
- Four general-purpose I/O pins
- Register set can be write-protected
- Operates from a 12.8MHz, 25.6MHz, 10.24MHz, 20.48MHz, 10MHz, 20MHz, 19.44MHz or 38.88MHz local oscillator
- On-chip watchdog circuit for the local oscillator
- Internal compensation for local oscillator frequency error



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