Rev: 072407

DS3104-SE
Line Card Timing IC with Synchronous Ethernet Support

General Description

The DS3104-SE is a low-cost, feature-rich timing IC for line cards with synchronous Gigabit Ethernet (GbE), 10-Gigabit Ethernet (10GbE), and Fast Ethernet ports. ITU-T recommendation G.8261 (formerly G.pactiming) specifies that network synchronization can be carried over packet links by synchronizing the bit clock of the physical layer as is currently done on SONET/SDH links. The DS3104-SE enables synchronization in Ethernet line cards in both the transmit and receive directions.

In the transmit direction, the device accepts traditional SONET/SDH system clocks such as 19.44MHz from redundant system timing cards and synthesizes frequency-locked xMII clock rates, such as the 125MHz GTX_CLK for GbE GMIIs. Each Ethernet PHY then synthesizes a transmit bit clock that is frequency-locked to the xMII clock, and thus to the system clock and network clock. In the receive direction, each PHY divides down the recovered bit clock to produce the receive xMII clock. The DS3104-SE accepts the xMII clock from any of several Ethernet ports and forwards a frequency-locked system clock, such as 19.44MHz, to the system timing cards. SONET/SDH ports are also supported.

Applications

Line Cards with Any Mix of Synchronous Ethernet and SONET/SDH Ports in WAN Equipment Including MSPPs, Ethernet Switches, Routers, DSLAMs, and Wireless Base Stations

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
DS3104GN	-40°C to +85°C	81 CSBGA (10mm)^2
DS3104GN+	-40°C to +85°C	81 CSBGA (10mm)^2

+Denotes a lead-free/RoHS-compliant package.

Features

- **Timing Card to Line Card Path**
  - Two Input Clocks from Master and Slave Timing Cards (LVDS/LVPECL or CMOS/TTL)
  - Optional Frame Sync Inputs and Outputs
  - Continuous Input Clock Quality Monitoring
  - Hitless Reference Switching, Automatic or Manual
  - Holdover on Loss of All Inputs
  - Programmable PLL Bandwidth, 0.1Hz to 400Hz
  - Frequency Conversion Between SONET/SDH Rates and Ethernet MII/GMII/XGMII Rates
  - Up to 7 Output Clocks: 3 CMOS/TTL (≤ 125MHz), 2 LVDS/LVPECL (≤ 312.50MHz), and 2 Dual CMOS/TTL and LVDS/LVPECL
- **Line Card to Timing Card Path**
  - Up to 8 Input Clocks: 4 CMOS/TTL (≤ 125MHz) and 4 LVDS/LVPECL/CMOS/TTL (≤ 156.25MHz)
  - Hitless Reference Switching, Automatic or Manual
  - Frequency Conversion Between Ethernet MII/GMII/XGMII and SONET/SDH Rates
  - Two Output Clocks to Master and Slave Timing Cards (CMOS/TTL or LVDS/LVPECL)
- **General**
  - **Suitable Line Card IC for Stratum 3/3E/4, SMC, SEC**
  - **Numerous Input Clock Frequencies Supported**
    Ethernet xMII: 2.5, 25, 125, 156.25MHz
    SONET/SDH: 6.48, N x 19.44, N x 51.84MHz
    PDH: N x DS1, N x E1, N x DS2, DS3, E3
    Frame Sync: 2kHz, 4kHz, 8kHz
    Custom: Any Multiple of 2kHz Up to 131.072MHz, Any Multiple of 8kHz Up to 155.52MHz
  - **Numerous Output Clock Frequencies Supported**
    Ethernet xMII: 2.5, 25, 125, 156.25, 312.5MHz
    SONET/SDH: 6.48, N x 19.44, N x 51.84MHz
    PDH: N x DS1, N x E1, N x DS2, DS3, E3
    Other: 10, 10.24, 13, 30.72MHz
    Frame Sync: 2kHz, 8kHz
    Custom Clock Rates: Any Multiple of 2kHz Up to 77.76MHz, Any Multiple of 8kHz Up to 311.04MHz
  - **Internal Compensation for Master Clock Oscillator**
  - **SPI™ Processor Interface**
  - **1.8V Operation with 2.5V/3.3V I/O (5V Tolerant)**

Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, go to: www.maxim-ic.com/errata. For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

Table of Contents

1. STANDARDS COMPLIANCE 6
2. APPLICATION EXAMPLE 7
3. BLOCK DIAGRAM 8
4. DETAILED DESCRIPTION 9
5. DETAILED FEATURES 11
5.1 INPUT CLOCK FEATURES 11
5.2 TIMING CARD TO LINE CARD DPLL FEATURES (T0 DPLL) 11
5.3 LINE CARD TO TIMING CARD DPLL FEATURES (T4 DPLL) 11
5.4 OUTPUT APLL FEATURES 12
5.5 OUTPUT CLOCK FEATURES 12
5.6 GENERAL FEATURES 12
6. PIN DESCRIPTIONS 13
7. FUNCTIONAL DESCRIPTION 17
7.1 OVERVIEW 17
7.2 DEVICE IDENTIFICATION AND PROTECTION 18
7.3 LOCAL OSCILLATOR AND MASTER CLOCK CONFIGURATION 18
7.4 INPUT CLOCK CONFIGURATION 19
7.4.1 Signal Format Configuration 19
7.4.2 Frequency Configuration 20
7.5 INPUT CLOCK MONITORING 21
7.5.1 Frequency Monitoring 21
7.5.2 Activity Monitoring 21
7.5.3 Selected Reference Activity Monitoring 21
7.6 INPUT CLOCK PRIORITY, SELECTION AND SWITCHING 22
7.6.1 Priority Configuration 22
7.6.2 Automatic Selection Algorithm 22
7.6.3 Forced Selection 23
7.6.4 Ultra-Fast Reference Switching 23
7.6.5 External Reference Switching Mode 24
7.6.6 Output Clock Phase Continuity During Reference Switching 24
7.7 DPLL ARCHITECTURE AND CONFIGURATION 25
7.7.1 T0 DPLL State Machine 26
7.7.2 T4 DPLL State Machine 29
7.7.3 Bandwidth 31
7.7.4 Damping Factor 31
7.7.5 Phase Detectors 31
7.7.6 Loss of Phase Lock Detection 32
7.7.7 Phase Build-Out 33
7.7.8 Input to Output (Manual) Phase Adjustment 33
7.7.9 Phase Recalibration 33
7.7.10 Frequency and Phase Measurement 34
7.7.11 Input Jitter Tolerance 35
7.7.12 Jitter and Wander Transfer 35
7.7.13 Output Jitter and Wander 36
7.8 OUTPUT CLOCK CONFIGURATION 37
7.8.1 Signal Format Configuration 37
7.8.2 Frequency Configuration 37
7.9 FRAME AND MULTIFRAME ALIGNMENT 45
7.9.1 Sampling 45

7.9.2 Resampling 45
7.9.3 Enable 45
7.9.4 Qualification 46
7.9.5 Output Clock Alignment 46
7.9.6 Frame Sync Monitor 46
7.9.7 SYNCn Pins 46
7.9.8 Other Configuration Options 47
7.10 MICROPROCESSOR INTERFACE 47
7.11 RESET LOGIC 51
7.12 POWER-SUPPLY CONSIDERATIONS 51
7.13 INITIALIZATION 51
8. REGISTER DESCRIPTIONS 52
8.1 STATUS BITS 52
8.2 CONFIGURATION FIELDS 52
8.3 MULTIREGISTER FIELDS 52
8.4 REGISTER DEFINITIONS 53
9. JTAG TEST ACCESS PORT AND BOUNDARY SCAN 116
9.1 JTAG DESCRIPTION 116
9.2 JTAG TAP CONTROLLER STATE MACHINE DESCRIPTION 117
9.3 JTAG INSTRUCTION REGISTER AND INSTRUCTIONS 119
9.4 JTAG TEST REGISTERS 120
10. ELECTRICAL CHARACTERISTICS 121
10.1 DC CHARACTERISTICS 121
10.2 INPUT CLOCK TIMING 125
10.3 OUTPUT CLOCK TIMING 125
10.4 SPI INTERFACE TIMING 126
10.5 JTAG INTERFACE TIMING 128
10.6 RESET PIN TIMING 129
11. PIN ASSIGNMENTS 130
12. PACKAGE INFORMATION 132
13. ACRONYMS AND ABBREVIATIONS 133
14. TRADEMARK ACKNOWLEDGEMENTS 134
15. DATA SHEET REVISION HISTORY 135

List of Figures

Figure 2-1. Typical Application Example 7
Figure 3-1. DS3104-SE Functional Diagram 8
Figure 7-1. DPLL Block Diagram 25
Figure 7-2. T0 DPLL State Transition Diagram 27
Figure 7-3. T4 DPLL State Transition Diagram 30
Figure 7-4. FSYNC 8kHz Options 44
Figure 7-5. SPI Clock Phase Options 49
Figure 7-6. SPI Bus Transactions 50
Figure 9-1. JTAG Block Diagram 116
Figure 9-2. JTAG TAP Controller State Machine 118
Figure 10-1. Recommended Termination for LVDS Pins 123
Figure 10-2. Recommended Termination for LVPECL Signals on LVDS Input Pins 123
Figure 10-3. Recommended Termination for LVPECL-Compatible Output Pins 124
Figure 10-4. SPI Interface Timing Diagram 127
Figure 10-5. JTAG Timing Diagram 128
Figure 10-6. Reset Pin Timing Diagram 129
Figure 11-1. Pin Assignment Diagram 131

List of Tables

Table 1-1. Applicable Telecom Standards 6
Table 6-1. Input Clock Pin Descriptions 13
Table 6-2. Output Clock Pin Descriptions 14
Table 6-3. Global Pin Descriptions 15
Table 6-4. SPI Bus Mode Pin Descriptions 15
Table 6-5. JTAG Interface Pin Descriptions 16
Table 6-6. Power-Supply Pin Descriptions 16
Table 7-1. Input Clock Capabilities 19
Table 7-2. Locking Frequency Modes 20
Table 7-3. Default Input Clock Priorities 22
Table 7-4. Damping Factors and Peak Jitter/Wander Gain 31
Table 7-5. T0 DPLL Adaptation for the T4 DPLL Phase Measurement Mode 35
Table 7-6. Output Clock Capabilities 37
Table 7-7. Digital1 Frequencies 39
Table 7-8. Digital2 Frequencies 39
Table 7-9. APLL Frequency to Output Frequencies (T0 APLL and T4 APLL) 40
Table 7-10. T0 APLL Frequency Configuration 40
Table 7-11. T0 APLL2 Frequency Configuration 40
Table 7-12. T4 APLL Frequency Configuration 41
Table 7-13. OC1–OC7 Output Frequency Selection 41
Table 7-14. Standard Frequencies for Programmable Outputs 42
Table 7-15. External Frame Sync Source 47
Table 8-1. Register Map 53
Table 9-1. JTAG Instruction Codes 119
Table 9-2. JTAG ID Code 120
Table 10-1. Recommended DC Operating Conditions 121
Table 10-2. DC Characteristics 121
Table 10-3. CMOS/TTL Pins 122
Table 10-4. LVDS/LVPECL Input Pins 122
Table 10-5. LVDS Output Pins 122
Table 10-6. LVPECL Level-Compatible Output Pins 123
Table 10-7. Input Clock Timing 125
Table 10-8. Input Clock to Output Clock Delay 125
Table 10-9. Output Clock Phase Alignment, Frame Sync Alignment Mode 125
Table 10-10. SPI Interface Timing 126
Table 10-11. JTAG Interface Timing 128
Table 10-12. Reset Pin Timing 129
Table 11-1. Pin Assignments Sorted by Signal Name 130
Table 12-1. CSBGA Package Thermal Properties, Natural Convection 132

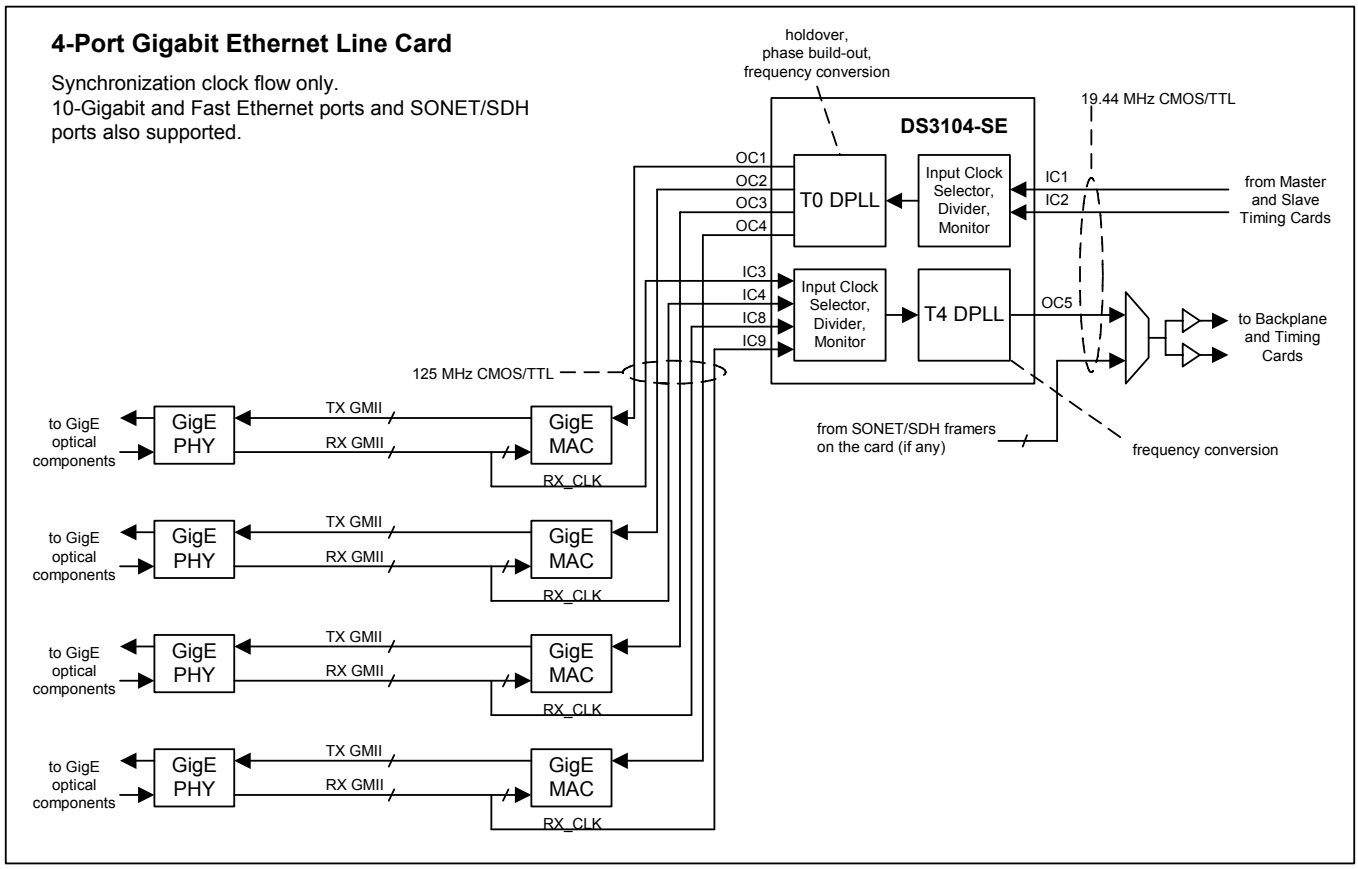
1. Standards Compliance

Table 1-1. Applicable Telecom Standards

SPECIFICATION	SPECIFICATION TITLE
ANSI	
T1.101	*Synchronization Interface Standard*, 1999
TIA/EIA-644-A	*Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits,* 2001
ETSI	
EN 300 417-6-1	*Transmission and Multiplexing (TM); Generic Requirements of Transport Functionality of Equipment; Part 6-1: Synchronization Layer Functions*, v1.1.3 (1999-05)
EN 300 462-3-1	*Transmission and Multiplexing (TM); Generic Requirements for Synchronization Networks; Part 3-1: The Control of Jitter and Wander within Synchronization Networks*, v1.1.1 (1998-05)
EN 300 462-5-1	*Transmission and Multiplexing (TM); Generic Requirements for Synchronization Networks; Part 5-1: Timing Characteristics of Slave Clocks Suitable for Operation in Synchronous Digital Hierarchy (SDH) Equipment*, v1.1.1 (1998-05)
IEEE	
IEEE 1149.1	*Standard Test Access Port and Boundary-Scan Architecture*, 1990
ITU-T	
G.783	*ITU G.783 Characteristics of Synchronous Digital Hierarchy (SDH) Equipment Functional Blocks* (10/2000 plus Amendment 1 06/2002 and Corrigendum 2 03/2003)
G.813	*Timing characteristics of SDH equipment slave clocks (SEC)* (03/2003)
G.823	*The Control of Jitter and Wander within Digital Networks which are Based on the 2048kbps Hierarchy* (03/2000)
G.824	*The Control of Jitter and Wander within Digital Networks which are Based on the 1544kbps Hierarchy* (03/2000)
G.825	*The Control of Jitter and Wander within Digital Networks which are Based on the Synchronous Digital Hierarchy (SDH)* (03/2000)
G.8261	*Timing and Synchronization Aspects in Packet Networks* (05/2006, prepublished)
G.8262	*Timing Characteristics of Synchronous Ethernet Equipment Slave Clock (EEC)* (06/2007, prepublished)
TELCORDIA	
GR-253-CORE	*SONET Transport Systems: Common Generic Criteria*, Issue 3, September 2000
GR-378-CORE	*Generic Requirements for Timing Signal Generators*, Issue 2, February 1999
GR-499-CORE	*Transport Systems Generic Requirements (TSGR) Common Requirements,* Issue 2, December 1998
GR-1244-CORE	*Clocks for the Synchronized Network: Common Generic Criteria,* Issue 2, December 2000

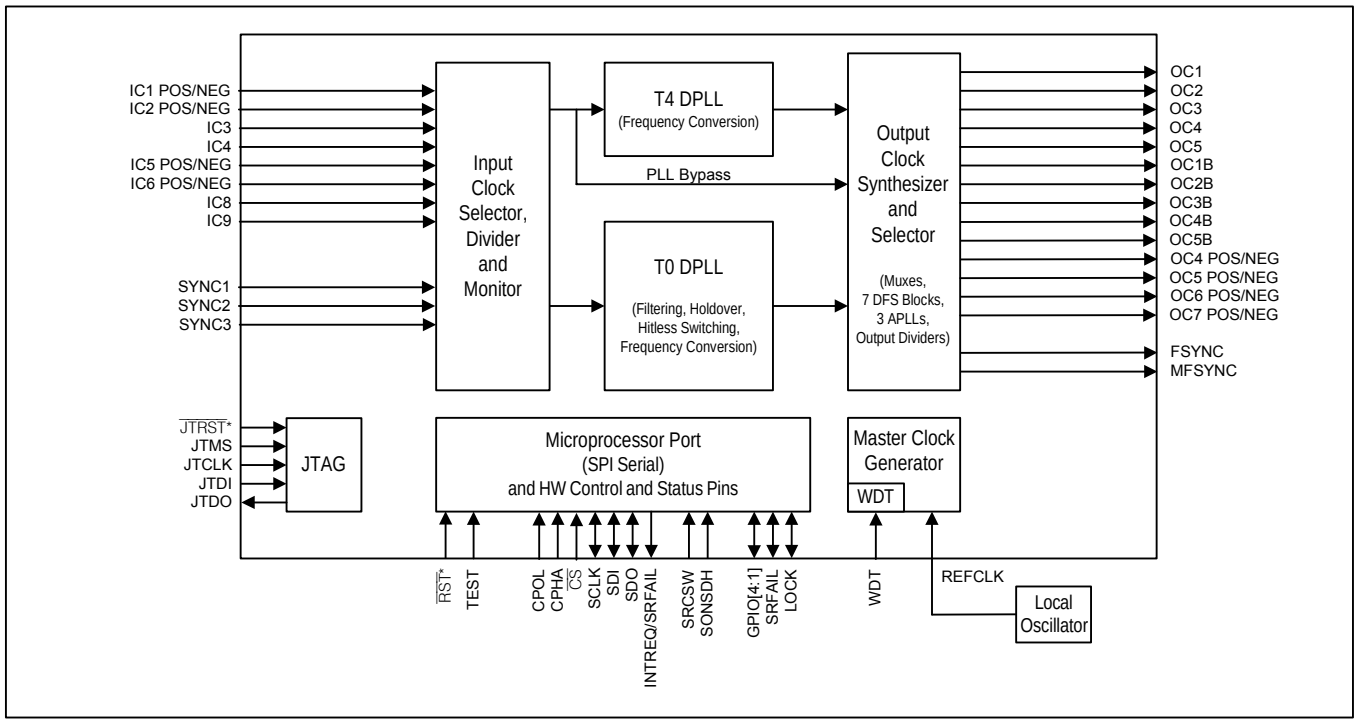
2. Application Example

Figure 2-1. Typical Application Example



3. Block Diagram

Figure 3-1. DS3104-SE Functional Diagram



4. Detailed Description

Figure 3-1 illustrates the blocks described in this section and how they relate to one another. Section 5 provides a detailed feature list.

The DS3104-SE is a complete line card timing IC for systems with SONET/SDH or Synchronous Ethernet ports. At the core of this device are two digital phase-locked loops (DPLLs) labeled T0 and T4[1]. DPLL technology makes uses of digital-signal processing (DSP) and digital-frequency synthesis (DFS) techniques to implement PLLs that are precise, flexible, and have consistent performance over voltage, temperature, and manufacturing process variations. The DS3104-SE's DPLLs are digitally configurable for input and output frequencies, loop bandwidth, damping factor, pull-in/hold-in range, and a variety of other factors. Both DPLLs can directly lock to many common telecom frequencies and also can lock at 8kHz to any multiple of 8kHz up to 156.25MHz. The DPLLs can also tolerate and filter significant amounts of jitter and wander.

In typical line card applications, the T0 DPLL takes reference clock signals from two redundant system timing cards, monitors both, selects one and uses that reference to produce a variety of clocks that are needed to time the outgoing traffic interfaces of the line card (SONET/SDH, Synchronous Ethernet, etc.). To perform this role in a variety of systems with diverse performance requirements, the T0 DPLL has a sophisticated feature set and is highly configurable. T0 can automatically transition among free-run, locked and holdover states all without software intervention. In free-run, T0 generates a stable, low-noise clock with the same frequency accuracy as the external oscillator connected to the REFCLK pin. With software calibration the DS3104-SE can even improve the accuracy to within ±0.02ppm. When at least one input reference clock has been validated, T0 transitions to the locked state in which its output clock accuracy is equal to the accuracy of the input reference. While in the locked state, T0 acquires an average frequency value to use as the holdover frequency. When its selected reference fails, T0 can very quickly detect the failure and enter the holdover state to avoid affecting its output clock. From holdover it can automatically switch to another input reference, again without affecting its output clock (hitless switching). Switching among input references can be either revertive or nonrevertive. When all input references are lost, T0 stays in holdover in which it generates a stable low-noise clock with initial frequency accuracy equal to its stored holdover value and drift performance determined by the quality of the external oscillator. T0 can also perform phase build-outs and fine-granularity output clock phase adjustments.

The T4 DPLL has a much less demanding role to play and therefore is much simpler than T0. Often T4 is used as a frequency converter to create a clock derived from one of the incoming traffic interfaces of the line card. This clock (often 19.44MHz, 38.88MHz, or 8kHz) is sent across the system backplane to the system's timing cards where a timing card IC creates a frequency-locked derived DS1- or E1-rate clock to be sent to a nearby BITS Timing Signal Generator (TSG, Telcordia terminology) or Synchronization Supply Unit (SSU, ITU-T terminology) or uses it as the system clock reference in a line-timed mode of operation. In other applications T4 is phase-locked to T0 and used as a frequency converter to produce additional output clock rates for use within the line card, such as NxDS1, NxE1, NxDS2, DS3, E3, 125MHz for Synchronous Gigabit Ethernet, or 156.25MHz for Synchronous 10G Ethernet. T4 can also be configured as a measuring tool to measure the frequency of an input reference or the phase difference between two input references.

At the front end of both the T0 and T4 DPLLs is the Input Clock Selector, Divider, and Monitor (ICSDM) block. This block continuously monitors as many as 8 different input clocks of various frequencies for activity and frequency accuracy. In addition, ICSDM maintains separate input clock priority tables for the T0 and T4 DPLLs and can automatically select and provide the highest priority valid clock to each DPLL without any software intervention. The ICSDM block can also divide the selected clock down to a lower rate as needed by the DPLL.

The Output Clock Synthesizer and Selector (OCSS) block shown in Figure 3-1 and in more detail in Figure 7-1 contains three output APLLs—T0 APLL, T0 APLL2 and T4 APLL—and their associated DFS engines and output divider logic plus several additional DFS engines. The APLL DFS blocks do frequency translation, creating clocks

[1] These names are adapted from output ports of the SETS function specified in ITU and ETSI standards such as ETSI EN 300 462-2-1. Although strictly speaking these names are appropriate only for timing card ICs such as the DS3100 that can serve as the SETS function, the names have been carried over to the DS3104-SE so that all of the products in Maxim's timing IC product line have consistent nomenclature.

of other frequencies that are phase/frequency locked to the output clock of the associated DPLL. The APLLs multiply the clock rates from the APLL DFS blocks and simultaneously attenuate jitter. Altogether the output blocks of the DS3104-SE can produce more than 90 different output frequencies including common SONET/SDH, PDH and Synchronous Ethernet rates plus 2kHz and 8kHz frame sync pulses.

The entire chip is clocked from the external oscillator connected to the REFCLK pin. Thus the free-run and holdover stability of the DS3104-SE is entirely a function of the stability of the external oscillator, the performance of which can be selected to match the application: XO or TCXO. The 12.8MHz clock from the external oscillator is multiplied by 16 by the Master Clock Generator block to create the 204.8MHz master clock used by the rest of the device. Since every block on the device depends on the master clock and therefore the local oscillator clock for proper operation, the master clock generator has a watchdog timer (WDT) function that can be used to signal a local microprocessor in the event of a local oscillator clock failure.

5. Detailed Features

5.1 Input Clock Features

- Eight input clocks: four CMOS/TTL (≤ 125MHz) and four LVDS/LVPECL/CMOS/TTL (≤ 156.25MHz)
- CMOS/TTL Input clocks accept any multiple of 2kHz up to 125MHz
- LVDS/LVPECL inputs accept any multiple of 2kHz up to 131.072MHz, any multiple of 8kHz up to 155.52MHz plus 156.25MHz
- All input clocks are constantly monitored by programmable activity monitors
- Fast activity monitor can disqualify the selected reference after two missing clock cycles
- Three optional 2/4/8kHz frame-sync inputs for frame-sync signals from master and slave timing cards and an optional backup timing source

5.2 Timing Card to Line Card DPLL Features (T0 DPLL)

- High-resolution DPLL plus two or three low-jitter output APLLs
- Sophisticated state machine automatically transitions between free-run, locked, and holdover states
- Revertive or nonrevertive reference selection algorithm
- Programmable bandwidth from 0.1Hz to 400Hz
- Separately configurable acquisition bandwidth and locked bandwidth
- Programmable damping factor to balance lock time with peaking: 1.2, 2.5, 5, 10 or 20
- Multiple phase detectors: phase/frequency, early/late, and multicycle
- Phase/frequency locking (±360° capture) or nearest-edge phase locking (±180° capture)
- Multicycle phase detection and locking (up to ±8191UI) improves jitter tolerance and lock time
- Phase build-out in response to reference switching
- Less than 5 ns output clock phase transient during phase build-out
- Output phase adjustment up to ±200ns in 6ps steps with respect to selected input reference
- High-resolution frequency and phase measurement
- Holdover frequency averaging over 1 second interval
- Fast detection of input clock failure and transition to holdover mode
- Low-jitter frame sync (8kHz) and multiframe sync (2kHz) aligned with output clocks

5.3 Line Card to Timing Card DPLL Features (T4 DPLL)

- High-resolution DPLL plus low-jitter output APLL
- Programmable bandwidth from 18Hz to 70Hz
- Programmable damping factor to balance lock time with peaking: 1.2, 2.5, 5, 10, or 20
- Multiple phase detectors: phase/frequency, early/late, and multicycle
- Phase/frequency locking (±360° capture) or nearest-edge phase locking (±180° capture)
- Multicycle phase detection and locking (up to ±8191UI) improves jitter tolerance and lock time
- 2kHz and 8kHz frame syncs with programmable polarity and pulse width
- Can operate independently or locked to T0 DPLL
- Phase detector can be used to measure phase difference between two input clocks
- Optional PLL bypass mode provides input clock monitoring, selection, and optional frequency division but bypasses the DPLL and APLL when they aren't needed (e.g., dividing an input clock to 8kHz)
- High-resolution frequency and phase measurement

5.4 Output APLL Features

- Three separate clock-multiplying, jitter attenuating APLLs can simultaneously produce SONET/SDH rates, Fast/Gigabit Ethernet rates and 10G Ethernet rates, all locked to a common reference clock
- The T0 APLL, always connected to the T0 DPLL, has frequency options suitable for Nx19.44MHz, NxDS1, NxE1, Nx25MHz and Nx62.5MHz
- The T4 APLL can be connected to either the T0 DPLL or the T4 DPLL and has frequency options suitable for Nx19.44MHz, NxDS1, NxE1, NxDS2, DS3, E3, Nx10MHz, Nx10.24MHz, Nx13MHz, Nx25MHz, and Nx62.5MHz
- The T0 APLL2, always connected to the T0 DPLL, produces 312.5MHz for 10G Synchronous Ethernet applications

5.5 Output Clock Features

- Seven output clocks: three CMOS/TTL (≤ 125MHz), two LVDS/LVPECL (≤ 312.50MHz), and two dual CMOS/TTL and LVDS/LVPECL
- Output clock rates include 2kHz, 8kHz, NxDS1, NxE1, DS2, DS3, E3, 6.48MHz, 19.44MHz, 38.88MHz, 51.84MHz, 77.76MHz, 155.52MHz, 311.04MHz, 2.5MHz, 25MHz, 125MHz, 156.25MHz, 312.50MHz, 10MHz, 10.24MHz, 13MHz, 30.72MHz and various multiples and submultiples of these rates
- Custom clock rates also available: any multiple of 2kHz up to 77.76MHz and any multiple of 8kHz up to 311.04MHz
- Three independent output APLLs support simultaneous generation of 155.52MHz for SONET/SDH, 125MHz for Gigabit Ethernet, and 156.25/312.5MHz for 10G Ethernet (plus various multiples/submultiples of each)
- All outputs have < 1ns peak-to-peak output jitter; outputs from APLLs have < 0.5ns peak-to-peak
- Each CMOS/TTL clock output has two leads, the standard output (e.g., OC1) with a 3.3V power supply, and the “B” output (e.g., OC1B) connected to the VDDIOB power supply for optional 2.5V output signal levels.
- 8kHz frame sync and 2kHz multiframe sync outputs have programmable polarity and pulse width and can be disciplined by a 2kHz or 8kHz sync input

5.6 General Features

- Operates from a single external 12.800MHz local oscillator (XO or TCXO)
- On-chip watchdog circuit for the local (REFCLK) oscillator
- SPI serial microprocessor interface
- Four general-purpose I/O pins
- Register set can be write-protected

6. Pin Descriptions

Table 6-1. Input Clock Pin Descriptions

PIN NAME[1]	TYPE[2]	PIN DESCRIPTION
REFCLK	I	**Reference Clock.** Connect to a 12.800MHz, high-accuracy, high-stability, low-noise local oscillator (XO or TCXO). See Section 7.3.
IC1POS, IC1NEG	I_{DIFF}	**Input Clock 1.** LVDS/LVPECL or CMOS/TTL. Programmable frequency (default 8kHz). *LVDS/LVPECL:* See Table 10-4, Figure 10-1 and Figure 10-2. *CMOS/TTL:* Bias IC1NEG to 1.4V and connect the single-ended signal to IC1POS.
IC2POS, IC2NEG	I_{DIFF}	**Input Clock 2.** LVDS/LVPECL or CMOS/TTL. Programmable frequency (default 8kHz). *LVDS/LVPECL:* See Table 10-4, Figure 10-1 and Figure 10-2. *CMOS/TTL:* Bias IC2NEG to 1.4V and connect the single-ended signal to IC2POS. This input can be associated with the SYNC3 pin.
IC3	I_{PD}	**Input Clock 3.** CMOS/TTL. Programmable frequency (default 8kHz). This input can be associated with the SYNC1 pin.
IC4	I_{PD}	**Input Clock 4.** CMOS/TTL. Programmable frequency (default 8kHz). This input can be associated with the SYNC2 pin.
IC5POS, IC5NEG	I_{DIFF}	**Input Clock 5.** LVDS/LVPECL or CMOS/TTL. Programmable frequency (default 19.44MHz). *LVDS/LVPECL:* See Table 10-4, Figure 10-1 and Figure 10-2. *CMOS/TTL:* Bias IC5NEG to 1.4V and connect the single-ended signal to IC5POS. This input can be associated with the SYNC1 pin.
IC6POS, IC6NEG	I_{DIFF}	**Input Clock 6.** LVDS/LVPECL or CMOS/TTL. Programmable frequency (default 19.44MHz). *LVDS/LVPECL:* See Table 10-4, Figure 10-1 and Figure 10-2. *CMOS/TTL:* Bias IC6NEG to 1.4V and connect the single-ended signal to IC6POS. This input can be associated with the SYNC2 pin.
IC8	I_{PD}	**Input Clock 8.** CMOS/TTL. Programmable input reference (default 19.44MHz).
IC9	I_{PD}	**Input Clock 9.** CMOS/TTL. Programmable frequency (default 19.44MHz). This input can be associated with the SYNC3 pin.
SYNC1	I_{PD}	**Frame Sync1 Input.** 2kHz, 4kHz, or 8kHz. FSCR3:SOURCE ! = 11XX This pin is the external frame sync input associated with any input pin using the FSCR3:SOURCE field. FSCR3:SOURCE = 11XX This pin is the external frame sync signal associated with IC3 or IC5 depending on which one is currently selected and the setting of FSCR1.SYNCSRC[1:0].
SYNC2	I_{PD}	**Frame Sync2 Input.** 2kHz, 4kHz, or 8kHz. FSCR3:SOURCE ! = 11XX This pin is not used for the EXTERNAL FRAME SYNC signal. FSCR3:SOURCE = 11XX This pin is the external frame sync signal associated with IC4 or IC6 depending on which one is currently selected and the setting of FSCR1.SYNCSRC[1:0].
SYNC3	I_{PU}	**Frame Sync3 Input.** 2kHz, 4kHz, or 8kHz. FSCR3:SOURCE ! = 11XX This pin is not used for the external frame sync signal. FSCR3:SOURCE = 11XX This pin is the external frame sync signal associated with IC9 or IC2 depending on which one is currently selected and the setting of FSCR1.SYNCSRC[1:0].

Table 6-2. Output Clock Pin Descriptions

PIN NAME[1]	TYPE[2]	PIN DESCRIPTION
OC1	O	**Output Clock 1.** CMOS/TTL. Programmable frequency (default 25MHz)
OC2	O	**Output Clock 2.** CMOS/TTL. Programmable frequency (default 62.5MHz).
OC3	O	**Output Clock 3.** CMOS/TTL. Programmable frequency (default 77.76MHz)
OC4	O	**Output Clock 4.** CMOS/TTL. Programmable frequency (default 125MHz)
OC5	O	**Output Clock 5.** CMOS/TTL. Programmable frequency (default 155.52MHz).
OC4POS, OC4NEG	O_{DIFF}	**Output Clock 4.** LVDS/LVPECL. These pins present the same clock as the OC4 pin but in differential signal format. The output mode is selected by MCR8.OC4SF[1:0]. See Table 10-5, Table 10-6, Figure 10-1, and Figure 10-3.
OC5POS, OC5NEG	O_{DIFF}	**Output Clock 5.** LVDS/LVPECL. These pins present the same clock as the OC5 pin but in differential signal format. The output mode is selected by MCR8.OC5SF[1:0]. See Table 10-5, Table 10-6, Figure 10-1, and Figure 10-3.
OC6POS, OC6NEG	O_{DIFF}	**Output Clock 6.** LVDS/LVPECL. Programmable frequency (default 156.25MHz LVDS). The output mode is selected by MCR8.OC6SF[1:0]. See Table 10-5, Table 10-6, Figure 10-1, and Figure 10-3.
OC7POS, OC7NEG	O_{DIFF}	**Output Clock 7.** LVDS/LVPECL. Programmable frequency (default 312.5MHz LVDS). The output mode is selected by MCR8.OC7SF[1:0]. See Table 10-5, Table 10-6, Figure 10-1, and Figure 10-3.
OC1B/ GPIO1	O_3	**Output Clock 1B/General-Purpose IO 1.** CMOS/TTL. (default CLK1B, disabled) This pin is programmable as an output clock pin or a GPIO pin using OCR6.OC1BEN. When programmed as a clock output pin (OC1BEN = 1) it presents the same clock as the OC1 pin. This pin is powered from the VDDIOB power supply pin.
OC2B/ GPIO2	O_3	**Output Clock 2B/General-Purpose IO 2.** CMOS/TTL. (default CLK2B, disabled) This pin is programmable as an output clock pin or a GPIO pin using OCR6.OC2BEN. When programmed as a clock output pin (OC2BEN = 1) it presents the same clock as the OC2 pin. This pin is powered from the VDDIOB power supply pin.
OC3B/ GPIO3	O_3	**Output Clock 3B/General-Purpose IO 3.** CMOS/TTL. (default CLK3B, disabled) This pin is programmable as an output clock pin or a GPIO pin using OCR6.OC3BEN. When programmed as a clock output pin (OC3BEN = 1) it presents the same clock as the OC3 pin. This pin is powered from the VDDIOB power supply pin.
OC4B	O_3	**Output Clock 4B.** CMOS/TTL (default off). When enabled (OCR6.OC4BEN = 1), this pin presents the same clock as the OC4 pin. This pin is powered from the VDDIOB power pin.
OC5B	O_3	**Output Clock 5B.** CMOS/TTL (default off) . When enabled (OCR6.OC5BEN = 1), this pin presents the same clock as the OC5 pin. This pin is powered from the VDDIOB power pin.
FSYNC	O_3	**FSYNC.** CMOS/TTL. 8kHz frame sync or clock (default 50% duty cycle clock, noninverted). The pulse polarity and width are selectable using FSCR1.8KINV and FSCR1.8KPUL.
MFSYNC	O_3	**MFSYNC.** CMOS/TTL. 2kHz frame sync or clock (default 50% duty cycle clock, noninverted). The pulse polarity and width are selectable using FSCR1.2KINV and FSCR1.2KPUL.

Table 6-3. Global Pin Descriptions

PIN NAME[1]	TYPE[2]	PIN DESCRIPTION
$\overline{RST}$	I_{PU}	**Reset (Active Low).** When this global asynchronous reset is pulled low, all internal circuitry is reset to default values. The device is held in reset as long as $\overline{RST}$ is low. $\overline{RST}$ should be held low for at least two REFCLK cycles after the external oscillator has stabilized and is providing valid clock signals.
SRCSW	I_{PD}	**Source Switching.** Fast source-switching control input. See Section 7.6.5. The value of this pin is latched into MCR10:EXTSW when $\overline{RST}$ goes high. After $\overline{RST}$ goes high this pin can be used to select between IC3/IC5 and IC4/IC6, if enabled.
TEST	I_{PD}	**Factory Test Mode Select.** Wire this pin to V_{SS} for normal operation.
WDT	I/O	**Watchdog Timer Pin.** Analog node for the REFCLK watchdog timer. Connect to a resistor (R) to V_{DDIO} and a capacitor (C) to ground. Suggested values are R = 20kΩ and C = 0.01µF. See Section 7.3.
SONSDH/ GPIO4	I/O_{PD}	**SONET/SDH Frequency Select Input or GPIO4 Pin.** When $\overline{RST}$ goes high the state of this pin sets the reset-default state of MCR3:SONSDH, MCR6:DIG1SS and MCR6:DIG2SS. After $\overline{RST}$ goes high this pin can be used as a general-purpose I/O pin. GPCR:GPIO4D configures this pin as an input or an output. GPCR:GPIO4O specifies the output value. GPSR:GPIO4 indicates the state of the pin. Reset latched values: 0 = SDH rates (N x 2.048MHz) 1 = SONET rates (N x 1.544MHz)
SRFAIL	O	**SRFAIL Status.** When MCR10:SRFPIN = 1, this pin follows the state of the SRFAIL latched status bit in the MSR2 register. This gives the system a very fast indication of the failure of the current reference. When MCR10:SRFPIN = 0, SRFAIL is disabled (low).
LOCK	O	**T0 DPLL LOCK Status.** When MCR1.LOCKPIN = 1, this pin indicates the lock state of the T0 DPLL. When MCR1.LOCKPIN = 0, LOCK is disabled (low). 0 = Not Locked 1 = Locked
INTREQ/LOS	O_3	**Interrupt Request/Loss of Signal.** Programmable (default: INTREQ). The INTCR:LOS bit determines whether the pin is indicates interrupt requests or loss of signal (i.e. loss of selected reference). **INTCR:LOS = 0: INTREQ mode** The behavior of this pin is configured in the INTCR register. Polarity can be active high or active low. Drive action can be push-pull or open drain. The pin can also be configured as a general-purpose output if the interrupt request function is not needed. **INTCR:LOS = 1: LOS mode** This pin indicates the real-time state of the selected reference activity monitor (see Section 7.5.3). This function is most useful when external switching mode (Section 7.6.5) is enabled (MCR10:EXTSW = 1).

Table 6-4. SPI Bus Mode Pin Descriptions

See Section 7.10 for functional description and Section 10.4 for timing specifications.

PIN NAME[1]	TYPE[2]	PIN DESCRIPTION
$\overline{CS}$	I_{PU}	**Chip Select.** This pin must be asserted (low) to read or write internal registers.
SCLK	I	**Serial Clock.** SCLK is always driven by the SPI bus master.
SDI	I	**Serial Data Input.** The SPI bus master transmits data to the device on this pin.
SDO	O	**Serial Data Output.** The device transmits data to the SPI bus master on this pin.
CPHA	I	**Clock Phase.** See Figure 7-5. 0 = Data is latched on the leading edge of the SCLK pulse. 1 = Data is latched on the trailing edge of the SCLK pulse.
CPOL	I_{PD}	**Clock Polarity.** See Figure 7-5. 0 = SCLK is normally low and pulses high during bus transactions. 1 = SCLK is normally high and pulses low during bus transactions.

Table 6-5. JTAG Interface Pin Descriptions

See Section 9 for functional description and Section 10.5 for timing specifications.

PIN NAME[1]	TYPE[2]	PIN DESCRIPTION
$\overline{\text{JTRST}}$	I_{PU}	**JTAG Test Reset (Active Low).** Asynchronously resets the test access port (TAP) controller. If not used, $\overline{\text{JTRST}}$ can be held low or high.
JTCLK	I	**JTAG Clock.** Shifts data into JTDI on the rising edge and out of JTDO on the falling edge. If not used, JTCLK can be held low or high.
JTDI	I_{PU}	**JTAG Test Data Input.** Test instructions and data are clocked in on this pin on the rising edge of JTCLK. If not used, JTDI can be held low or high.
JTDO	O_3	**JTAG Test Data Output.** Test instructions and data are clocked out on this pin on the falling edge of JTCLK. If not used, leave floating.
JTMS	I_{PU}	**JTAG Test Mode Select.** Sampled on the rising edge of JTCLK and is used to place the port into the various defined IEEE 1149.1 states. If not used connect to VDDIO or leave floating.

Table 6-6. Power-Supply Pin Descriptions

PIN NAME[1]	TYPE[2]	PIN DESCRIPTION
VDD	P	**Core Power Supply.** 1.8V ±10%.
VDDIO	P	**I/O Power Supply.** 3.3V ±5%.
VDDIOB	P	**Power for Pins OC1B through OC5B.** Voltage can be from 2.5V ±5% to 3.3V ±5%.
VSS	P	**Ground Reference**
VDD_OC45	P	**Power Supply for Differential Outputs OC4POS/NEG and OC5POS/NEG.** 1.8V ±10%.
VSS_OC45	P	**Return for Differential Outputs OC4POS/NEG and OC5POS/NEG**
VDD_OC67	P	**Power Supply for Differential Outputs OC6POS/NEG and OC7POS/NEG.** 1.8V ±10%.
VSS_OC67	P	**Return for LVDS Differential Outputs OC6POS/NEG and OC7POS/NEG**
AVDD_PLL1	P	**Power Supply for Master Clock Generator APLL.** 1.8V ±10%.
AVSS_PLL1	P	**Return for Master Clock Generator APLL**
AVDD_PLL2	P	**Power Supply for T0 APLL.** 1.8V ±10%.
AVSS_PLL2	P	**Return for T0 APLL**
AVDD_PLL3	P	**Power Supply for T4 APLL.** 1.8V ±10%.
AVSS_PLL3	P	**Return for T4 APLL**
AVDD_PLL4	P	**Power Supply for T0 APLL2.** 1.8V ±10%.
AVSS_PLL4	P	**Return for T0 APLL2**

Note 1: All pin names with an overbar (e.g., $\overline{\text{RST}}$) are active low.

Note 2: All pins, except power and analog pins, are CMOS/TTL unless otherwise specified in the pin description.

PIN TYPES

I = input pin
I_{DIFF} = input pin that is LVDS/LVPECL differential signal compatible
I_{PD} = input pin with internal 50kΩ pulldown
I_{PU} = input pin with internal 50kΩ pullup
I/O = input/output pin
IO_{PD} = input/output pin with internal 50kΩ pulldown
IO_{PU} = input/output pin with internal 50kΩ pullup
O = output pin
O_3 = output pin that can tri-stated (i.e., placed in a high-impedance state)
O_{DIFF} = output pin that is LVDS/LVPECL differential signal compatible
P = power-supply pin

Note 3: All digital pins, except OCn, are I/O pins in JTAG mode. OCn pins do not have JTAG functionality.

7. Functional Description

7.1 Overview

The DS3104-SE has eight input clocks pins and three frame-sync input pins. The device can output as many as nine different clock frequencies on 16 output clock pins. There are two separate DPLLs in the device: the high-performance T0 DPLL and the simpler the T4 DPLL. Both DPLLs can generate output clocks. See Figure 3-1.

Four of the input clock pins are single-ended and can accept clock signals from 2kHz to 125MHz. The other four are differential inputs that can accept clock signals up to 156.25MHz. The differential inputs can be configured to accept differential LVDS or LVPECL signals or single-ended CMOS/TTL signals.

Each input clock can be monitored continually for activity, and each can be marked unavailable or given a priority number. Separate input priority numbers are maintained for the T0 DPLL and the T4 DPLL. Except in special modes, the highest priority valid input is automatically selected as the reference for each path. SRFAIL is set or cleared based on activity and/or frequency of the selected input.

Both the T0 DPLL and the T4 DPLL can directly lock to many common telecom and datacom frequencies, including, but not limited to 8kHz, DS1, E1, 10MHz, 19.44MHz, and 38.88MHz as well as Ethernet frequencies including 25MHz, 62.5MHz, 125MHz and 156.25MHz. The DPLLs can also lock to multiples of the standard direct-lock frequencies including 8kHz.

The T0 DPLL is the high-performance path with all the features needed for synchronizing a line card to dual redundant system timing cards. The T4 DPLL is a simpler auxiliary path typically used to provide a clock derived from an incoming line rate to system timing cards. The T4 APLL can be connected to either the T4 DPLL or the T0 DPLL to provide more low-jitter output frequencies from the T0 DPLL. There is also a dedicated low-jitter APLL output that operates at 312.5MHz for 10G Ethernet applications.

Using the optional PLL bypass, the T4 selected reference, after any frequency division, can be directly output on any of the OC1 to OC7 output clock pins.

Both DPLLs have these features:

- Automatic reference selection based on input activity and priority
- Optional manual reference selection/forcing
- Adjustable PLL characteristics, including bandwidth, pull-in range, and damping factor
- Ability to lock to several common telecom and Ethernet frequencies plus multiples of any standard direct lock frequency.
- Frequency conversion between input and output using digital frequency synthesis
- Combined performance of a stable, consistent digital PLL and low-jitter analog output PLLs

The T0 DPLL has these additional features not available in the T4 DPLL:

- A full state machine for automatic transitions among free-run, locked, and holdover states
- Nonrevertive reference switching mode
- Phase build-out for reference switching (“hitless”)
- Output vs. input phase offset control
- 13 bandwidth selections from 0.1Hz to 400Hz (vs. six selections for the T4 DPLL)
- Noise rejection circuitry for low-frequency references
- Output phase alignment to input frame sync signal
- Instant digital one-second averaging and free-run holdover modes

The T4 DPLL has these additional features not available in the T0 DPLL:

- Three bandwidth selections limited to 18Hz to 70Hz
- Optional mode to measure the phase difference between two input clocks

Typically, the internal state machine controls the T0 DPLL, but manual control by system software is also available. The T4 DPLL has a simpler state machine that software cannot directly control. In either DPLL, however, software can override the DPLL logic using manual reference selection.

The output and feedback synthesizers are locked to either the T0 DPLL or the T4 DPLL. Most of the output signals that are locked to the same DPLL are always aligned to the falling edge at 2kHz.

The outputs of the T0 DPLL and the T4 DPLL can be connected to seven output DFS engines. See Figure 7-1. Three of these output DFS engines are associated with high-speed APLLs that multiply the DPLL clock rate and filter DPLL output jitter. The outputs of the APLLs are divided down to make a wide variety of possible frequencies available at the output clock pins. T0 APLL and T0 APLL2 are always locked to the T0 DPLL, while the T4 APLL can lock to either the T4 DPLL or the T0 DPLL. The output frequencies from the T0 DPLL can be synchronized to an input 2, 4, or 8kHz sync signal (SYNC1, SYNC2, or SYNC3 input pins).

The OC1 to OC7 output clocks can be configured for a variety of different frequencies that are frequency and phase locked to either the T0 DPLL or the T4 DPLL. The OC6 and OC7 outputs are LVDS/LVPECL, OC4 and OC5 are available in both LVDS/LVPECL and 3.3V CMOS, OC1 to OC3 are 3.3V CMOS. There are five outputs OC1B to OC5B that can be 3.3V or 2.5V CMOS outputs. Altogether more than 60 output frequencies are possible, ranging from 2kHz to 312.5MHz. The FSYNC output clock is always 8kHz, and the MFSYNC output clock is always 2kHz.

7.2 Device Identification and Protection

The 16-bit read-only ID field in the ID1 and ID2 registers is set to 0C20h = 3104 decimal. The device revision can be read from the REV register. Contact the factory to interpret this value and determine the latest revision. The register set can be protected from inadvertent writes using the PROT register.

7.3 Local Oscillator and Master Clock Configuration

The T0 DPLL, the T4 DPLL and the output DFS engines operate from a 204.8MHz master clock. The master clock is synthesized from a 12.800MHz clock originating from a local oscillator attached to the REFCLK pin. The stability of the T0 DPLL in free-run or holdover is equivalent to the stability of the local oscillator. Selection of an appropriate local oscillator is therefore of crucial importance if the telecom standards listed in Table 1-1 are to be met. Simple XOs can be used in less stringent cases, but TCXOs or even OCXOs may be required in the most demanding applications. Careful evaluation of the local oscillator component is necessary to ensure proper performance. Contact Maxim at telecom.support@dalsemi.com for recommended oscillators.

The stability of the local oscillator is very important, but its absolute frequency accuracy is less important because the DPLLs can compensate for frequency inaccuracies when synthesizing the 204.8MHz master clock from the local oscillator clock. The MCLKFREQ field in registers MCLK1 and MCLK2 specifies the frequency adjustment to be applied. The adjust can be from -771ppm to +514ppm in 0.0196229ppm (i.e., ~0.02ppm) steps.

The DS3104-SE has a watchdog circuit that causes an interrupt on the INTREQ pin when the local oscillator attached to the REFCLK pin is significantly off frequency. The watchdog interrupt is not maskable, but *is* subject to the INTCR register settings. When the watchdog circuit activates, reads of any and all registers in the device will return 00h to indicate the failure. In response to the activation of the INTREQ pin or during periodic polling, if system software ever reads 00h from the ID registers (which are hard-coded to 0C20h = 3104 decimal) then it can conclude that the local oscillator attached to that DS3104-SE has failed. For proper operation of the watchdog timer, connect the WDT pin to a 10kΩ resistor (R) to VDDIO and a 0.01μF capacitor (C) to VSS.

7.4 Input Clock Configuration

The DS3104-SE has eight input clocks, IC1 to IC6 and IC8 and IC9. Table 7-1 provides summary information about each clock, including signal format and available frequencies. The device tolerates a wide range of duty cycles on input clocks, out to a minimum high time or minimum low time of 3ns or 30% of the clock period, whichever is smaller.

7.4.1 Signal Format Configuration

Inputs with CMOS/TTL signal format accept both TTL and 3.3V CMOS levels. One key configuration bit that affects the available frequencies is the SONSDH bit in MCR3. When SONSDH = 1 (SONET mode), the 1.544MHz frequency is available. When SONSDH = 0 (SDH mode), the 2.048MHz frequency is available. During reset the default value of this bit is latched from the SONSDH pin.

Input clocks IC1, IC2, IC5, and IC6 can be configured to accept LVDS, LVPECL, or CMOS/TTL signals by using the proper set of external components. The recommended LVDS termination is shown in Figure 10-1 while the recommended LVPECL termination is shown in Figure 10-2. The electrical specifications for these inputs are listed in Table 10-4. To configure these differential inputs to accept single-ended CMOS/TTL signals, use a voltage-divider to bias the ICxNEG pin to approximately 1.4V and connect the single-ended signal to the ICxPOS pin. If a differential input is not used it should be configured left floating (one input is internally pulled high and the other internally pulled low). (See also MCR5:IC5SF and IC6SF.)

Table 7-1. Input Clock Capabilities

INPUT CLOCK	SIGNAL FORMATS	FREQUENCIES (MHz)	DEFAULT FREQUENCY
IC1	LVDS/LVPECL or CMOS/TTL	Up to 156.25 (2)	8kHz
IC2	LVDS/LVPECL or CMOS/TTL	Up to 156.25 (2)	8kHz
IC3	CMOS/TTL	Up to 125 (1)	8kHz
IC4	CMOS/TTL	Up to 125 (1)	8kHz
IC5	LVDS/LVPECL or CMOS/TTL	Up to 156.25 (2)	19.44MHz
IC6	LVDS/LVPECL or CMOS/TTL	Up to 156.25 (2)	19.44MHz
IC8	CMOS/TTL	Up to 125 (1)	19.44MHz
IC9	CMOS/TTL	Up to 125 (1)	19.44MHz

Note 1: Available frequencies for CMOS/TTL input clocks are: 2kHz, 4kHz, 8kHz, 1.544MHz (SONET mode), 2.048MHz (SDH mode), 6.312MHz, 6.48MHz, 19.44MHz, 25.0MHz, 25.92MHz, 38.88MHz, 51.84MHz, 62.5MHz, 77.76MHz, and any multiple of 2kHz up to 125MHz.

Note 2: Available frequencies for LVDS/LVPECL input clocks include all CMOS/TTL frequencies in Note 1 plus any multiple of 8kHz up to 155.52MHz and 156.25MHz.

7.4.2 Frequency Configuration

Input clock frequencies are configured in the FREQ field of the ICR registers. The DIVN and LOCK8K bits of these same registers specify the locking frequency mode, as shown in Table 7-2.

Table 7-2. Locking Frequency Modes

DIVN	LOCK8K	LOCKING FREQUENCY MODE
0	0	Direct Lock
0	1	LOCK8K
1	0	DIVN
1	1	Alternate Direct Lock

7.4.2.1 Direct Lock Mode

In direct lock mode, the DPLLs lock to the selected reference at the frequency specified in the corresponding ICR register. Direct lock mode can only be used for input clocks with these specific frequencies: 2kHz, 4kHz, 8kHz, 1.544MHz, 2.048MHz, 5MHz, 6.312MHz, 6.48MHz, 19.44MHz, 25.92MHz, 31.25MHz, 38.88MHz, 51.84MHz, 77.76MHz, and 155.52MHz. For the 155.52MHz case, the input clock is internally divided by two, and the DPLL direct-locks at 77.76MHz. The DIVN mode can be used to divide an input down to any of these frequencies except 155.52MHz.

MTIE figures may be marginally better in direct lock mode because the higher frequencies allow more frequent phase updates.

7.4.2.2 Alternate Direct Lock Mode

Alternate direct lock mode is the same as direct lock mode except an alternate list of direct lock frequencies is used (see the FREQ field definition in the ICR register description). The alternate frequencies are included to support clock rates found in Ethernet, CMTS, wireless, and GPS applications. The alternate frequencies are: 10MHz, 25MHz, 62.5MHz, 125MHz, and 156.25MHz. The frequencies 62.5MHz, 125MHz, and 156.25MHz are internally divided down to 31.25MHz, while 10MHz and 25MHz are internally divided down to 5MHz.

7.4.2.3 LOCK8K Mode

In LOCK8K mode, an internal divider is configured to divide the selected reference down to 8kHz. The DPLL locks to the 8kHz output of the divider. LOCK8K mode can only be used for input clocks with the standard direct lock frequencies: 8kHz, 1.544MHz, 2.048MHz, 5MHz, 6.312MHz, 6.48MHz, 19.44MHz, 25.0MHz, 25.92MHz, 31.25MHz, 38.88MHz, 51.84MHz, 62.5MHz, 77.76MHz, and 155.52MHz. LOCK8K mode is enabled for a particular input clock by setting the LOCK8K bit in the corresponding ICR register. LOCK8K mode cannot be used with 5MHz input clocks.

LOCK8K mode gives a greater tolerance to input jitter when the multicycle phase detector is disabled because it uses lower frequencies for phase comparisons. The clock edge to lock to on the selected reference can be configured using the 8KPOL bit in the TEST1 register. For 2kHz and 4kHz clocks the LOCK8K bit is ignored and direct-lock mode is used.

7.4.2.4 DIVN Mode

In DIVN mode, an internal divider is configured from the value stored in the DIVN registers. The DIVN value must be chosen so that when the selected reference is divided by DIVN+1, the resulting clock frequency is the same as the standard direct lock frequency selected in the FREQ field of the ICR register. The DPLL locks to the output of the divider. DIVN mode can only be used for input clocks whose frequency is less than or equal to 155.52MHz. The DIVN register field can range from 0 to 65,535 inclusive. The same DIVN+1 factor is used for all input clocks configured for DIVN mode. Note that although the DIVN divider is able to divide down clock rates as high as 155.52MHz, the CMOS/TTL inputs are only rated for a maximum clock rate of 125MHz.

7.5 Input Clock Monitoring

Each input clock is continuously monitored for activity. Activity monitoring is described in Sections 7.5.2 and 7.5.3. The valid/invalid state of each input clock is reported in the corresponding real-time status bit in registers VALSR1 or VALSR2. When the valid/invalid state of a clock changes, the corresponding latched status bit is set in registers MSR1 or MSR2, and an interrupt request occurs if the corresponding interrupt enable bit is set in registers IER1 or IER2. Input clocks marked invalid cannot be automatically selected as the reference for either DPLL. If the T4 DPLL does not have any valid input clocks available, the T4NOIN status bit is set to 1 in MSR3.

7.5.1 Frequency Monitoring

The DS3104-SE monitors the frequency of each input clock and invalidates any clock whose frequency is more than 10,000ppm away from nominal. The frequency range monitor can be disabled by clearing the MCR1.FREN bit. The frequency range measurement uses the internal 204.8MHz master clock as the frequency reference.

7.5.2 Activity Monitoring

Each input clock is monitored for activity and proper behavior using a leaky bucket accumulator. A leaky bucket accumulator is similar to an analog integrator: the output amplitude increases in the presence of input events and gradually decays in the absence of events. When events occur infrequently, the accumulator value decays fully between events and no alarm is declared. When events occur close enough together, the accumulator increments faster than it can decay and eventually reaches the alarm threshold. After an alarm has been declared, if events occur infrequently enough, the accumulator can decay faster than it is incremented and eventually reaches the alarm clear threshold. The leaky bucket events come from the frequency range and fast activity monitors.

The leaky bucket accumulator for each input clock can be assigned one of four configurations (0 through 3) in the BUCKET field of the ICR registers. Each leaky bucket configuration has programmable size, alarm declare threshold, alarm clear threshold, and decay rate, all of which are specified in the LBxy registers.

Activity monitoring is divided into 128ms intervals. The accumulator is incremented once for each 128ms interval in which the input clock is inactive for more than two cycles (more than four cycles for 155.52MHz, 156.25MHz, 125MHz, 62.5MHz, 25MHz and 10MHz input clocks). Thus the “fill” rate of the bucket is at most 1 unit per 128ms, or approximately 8 units/second. During each period of 1, 2, 4 or 8 intervals (programmable), the accumulator decrements if no irregularities occur. Thus the “leak” rate of the bucket is approximately 8, 4, 2, or 1 units/second. A leak is prevented when a fill event occurs in the same interval.

When the value of an accumulator reaches the alarm threshold (LBxU register), the corresponding ACT alarm bit is set to 1 in the ISR registers, and the clock is marked invalid in the VALSR registers. When the value of an accumulator reaches the alarm clear threshold (LBxL register), the activity alarm is cleared by clearing the clock’s ACT bit. The accumulator cannot increment past the size of the bucket specified in the LBxS register. The decay rate of the accumulator is specified in the LBxD register. The values stored in the leaky bucket configuration registers must have the following relationship at all times: LBxS ≥ LBxU > LBxL.

When the leaky bucket is empty, the minimum time to declare an activity alarm in seconds is LBxU / 8 (where the ‘x’ in ‘LBxU’ is the leaky bucket configuration number, 0 to 3). The minimum time to clear an activity alarm in seconds is 2^LBxD x (LBxS – LBxL) / 8. As an example, assume LBxU = 8, LBxL = 1, LBxS = 10, and LBxD = 0. The minimum time to declare an activity alarm would be 8 / 8 = 1 second. The minimum time to clear the activity alarm would be 2^0 x (10 – 1) / 8 = 1.125 seconds.

7.5.3 Selected Reference Activity Monitoring

The input clock that each DPLL is currently locked to is called the selected reference. The quality of a DPLL’s selected reference is exceedingly important, since missing cycles and other anomalies on the selected reference can cause unwanted jitter, wander or frequency offset on the output clocks. When anomalies occur on the selected reference they must be detected as soon as possible to give the DPLL opportunity to temporarily disconnect from the reference until the reference is available again. By design, the regular input clock activity monitor (Section

7.5.2) is too slow to be suitable for monitoring the selected reference. Instead, each DPLL has its own fast activity monitor that detects that the frequency is within range (approximately 10,000ppm) and detects inactivity within approximately two missing reference clock cycles (approximately four missing cycles for 156.25MHz, 155.52MHz, 125MHz, 62.5MHz, 25MHz, and 10MHz references).

When the T0 DPLL detects a no-activity event, it immediately enters mini-holdover mode to isolate itself from the selected reference and sets the SRFAIL bit in MSR2. The setting of the SRFAIL bit can cause an interrupt request if the corresponding enable bit is set in IER2. If MCR10:SRFPIN = 1, the SRFAIL output pin follows the state of the SRFAIL status bit. Optionally, a no-activity event can also cause an ultra-fast reference switch (see Section 7.6.4). When PHLIM1:NALOL = 0 (default), the T0 DPLL does not declare loss-of-lock during no-activity events. If the selected reference becomes available again before any alarms are declared by the activity monitor, then the T0 DPLL continues to track the selected reference using nearest-edge locking (±180°) to avoid cycle slips. When NALOL = 1, the T0 DPLL declares loss-of-lock during no-activity events. This causes the T0 DPLL state machine to transition to the loss-of-lock state, which sets the MSR2:STATE bit and causes an interrupt request if enabled. If the selected reference becomes available again before any alarms are declared by the activity monitor, then the T0 DPLL tracks the selected reference using phase/frequency locking (±360°) until phase lock is reestablished.

When the T4 DPLL detects a no-activity event, its behavior is similar to the T0 DPLL with respect to the PHLIM1:NALOL control bit. Unlike the T0 DPLL, however, the T4 DPLL does not set the SRFAIL status bit. If NALOL = 1, the T4 DPLL clears the OPSTATE:T4LOCK status bit, which sets MSR3:T4LOCK and causes an interrupt request if enabled.

7.6 Input Clock Priority, Selection and Switching

7.6.1 Priority Configuration

During normal operation, the selected reference for the T0 DPLL and the selected reference for the T4 DPLL are chosen automatically based on the priority rankings assigned to the input clocks in the input priority registers (IPR1 to IPR5). Each of these registers has priority fields for one or two input clocks. When T4T0 = 0 in the MCR11 register, the IPR registers specify the input clock priorities for the T0 DPLL. When T4T0 = 1, the IPR registers specify the input clock priorities for the T4 DPLL. The default input clock priorities, for both PLLs, are shown in Table 7-3.

Any unused input clock should be given the priority value 0, which disables the clock and marks it as unavailable for selection. Priority 1 is highest while priority 15 is lowest. The same priority can be given to two or more clocks.

Table 7-3. Default Input Clock Priorities

INPUT CLOCK	T0 DPLL DEFAULT PRIORITY	T4 DPLL DEFAULT PRIORITY
IC1	0 (off)	0 (off)
IC2	1	1
IC3	2	2
IC4	3	3
IC5	0 (off)	0 (off)
IC6	0 (off)	0 (off)
IC8	4	5
IC9	5	0 (off)

7.6.2 Automatic Selection Algorithm

The real-time valid/invalid state of each input clock is maintained in the VALSR1 and VALSR2 registers. The selected reference can be marked invalid for phase lock, frequency, or activity. Other input clocks can be invalidated for frequency or activity.

The reference selection algorithm for each DPLL chooses the highest-priority valid input clock to be the selected reference. To select the proper input clock based on these criteria, the selection algorithm maintains a priority table of valid inputs. The top three entries in this table and the selected reference are displayed in the PTAB1 and PTAB2 registers. When T4T0 = 0 in the MCR11 register, these registers indicate the highest priority input clocks for the T0 DPLL. When T4T0 = 1, they indicate the highest priority input clocks for the T4 DPLL.

If two or more input clocks are given the same priority number then those inputs are prioritized among themselves using a fixed circular list. If one equal-priority clock is the selected reference but becomes invalid then the next equal-priority clock in the list becomes the selected reference. If an equal-priority clock that is not the selected reference becomes invalid, it is simply skipped over in the circular list. The selection among equal-priority inputs is inherently nonrevertive, and revertive switching mode (see next paragraph) has no effect in the case where multiple equal-priority inputs have the highest priority.

An important input to the selection algorithm for the T0 DPLL is the REVERT bit in the MCR3 register. In revertive mode (REVERT = 1), if an input clock with a higher priority than the selected reference becomes valid, the higher priority reference immediately becomes the selected reference. In nonrevertive mode (REVERT = 0), the higher priority reference does not immediately become the selected reference but does become the highest priority reference in the priority table (REF1 field in the PTAB1 register). (The selection algorithm always switches to the highest-priority valid input when the selected reference goes invalid, regardless of the state of the REVERT bit.) For many applications, nonrevertive mode is preferred for the T0 DPLL because it minimizes disturbances on the output clocks due to reference switching. The T4 DPLL always operates in revertive mode.

In nonrevertive mode, planned switchover to a newly-valid higher priority input clock can be done manually under software control. The validation of the new higher priority clock sets the corresponding status bit in the MSR1 or MSR2 register, which can drive an interrupt request on the INTREQ pin if needed. System software can then respond to this change of state by briefly enabling revertive mode (toggling REVERT high then back low) to drive the switchover to the higher priority clock.

7.6.3 Forced Selection

The T0FORCE field in the MCR2 register and the T4FORCE field in the MCR4 register provide a way to force a specified input clock to be the selected reference for the T0 and T4 DPLLs, respectively. In both T0FORCE and T4FORCE, values of 0 and 15 specify normal operation with automatic reference selection. Values from 1 to 6 and 8 and 9 specify the input clock to be the forced selection; other values will cause no input to be selected. Internally, forcing is accomplished by giving the specified clock the highest priority (as specified in PTAB1:REF1). In revertive mode (MCR3:REVERT = 1) the forced clock automatically becomes the selected reference (as specified in PTAB1:SELREF) as well. In nonrevertive mode (T0 DPLL only) the forced clock only becomes the selected reference when the existing selected reference is invalidated or made unavailable for selection. In both revertive and nonrevertive modes when an input is forced to be the highest priority, the normal highest priority input (when no input is forced) is listed as the second-highest priority (PTAB2:REF2) and the normal second-highest priority input is listed as the third-highest priority (PTAB2:REF3).

When the T4 DPLL is used to measure the phase difference between the T0 DPLL selected reference and another reference input by setting the T0CR1:T4MT0 bit, the T4FORCE field in the MCR4 register can be used to select the other reference input.

7.6.4 Ultra-Fast Reference Switching

By default, disqualification of the selected reference and switchover to another reference occurs when the activity monitor's inactivity alarm threshold has been crossed, a process that takes on the order of hundreds of milliseconds or seconds. For the T0 DPLL, an option for extremely fast disqualification and switchover is also available. When ultra-fast switching is enabled (MCR10:UFSW = 1), if the fast activity monitor detects approximately two missing clock cycles it declares the reference failed by forcing the leaky bucket accumulator to its upper threshold (see Section 7.5.2) and initiates reference switching. This is in addition to setting the SRFAIL bit in MSR2 and optionally generating an interrupt request, as described in Section 7.5.3. When ultra-fast switching occurs, the T0 DPLL transitions to the prelocked 2 state, which allows switching to occur faster by bypassing the loss-of-lock state. The device should be in nonrevertive mode when ultra-fast switching is enabled. If the device is

in revertive mode, ultra-fast switching could cause excessive reference switching when the highest priority input is intermittent.

7.6.5 External Reference Switching Mode

In this mode the SRCSW input pin controls reference switching between two clock inputs. This mode is enabled by setting the EXTSW bit to 1 in the MCR10 register. In this mode, if the SRCSW pin is high, the T0 DPLL is forced to lock to input IC3 (if the priority of IC3 is nonzero in IPR2) or IC5 (if the priority of IC3 is zero) whether or not the selected input has a valid reference signal. If the SRCSW pin is low the T0 DPLL is forced to lock to input IC4 (if the priority of IC4 is nonzero in IPR2) or IC6 (if the priority of IC4 is zero) whether or not the selected input has a valid reference signal. During reset the default value of the EXTSW bit is latched from the SRCSW pin. If external reference switching mode is enabled during reset, the default frequency tolerance (DLIMIT registers) is configured to ±80ppm rather than the normal default of ±9.2ppm.

In external reference switching mode the device is simply a clock switch, and the T0 DPLL is forced to lock onto the selected reference whether it is valid or not. Unlike forced reference selection (Section 7.6.3) this mode controls the PTAB1:SELREF field directly and is, therefore, not affected by the state of the MCR3:REVERT bit. During external reference switching mode, only PTAB1:SELREF is affected; the REF1, REF2, and REF3 fields in the PTAB registers continue to indicate the highest, second-highest, and third-highest priority valid inputs chosen by the automatic selection logic. External reference switching mode only affects the T0 DPLL.

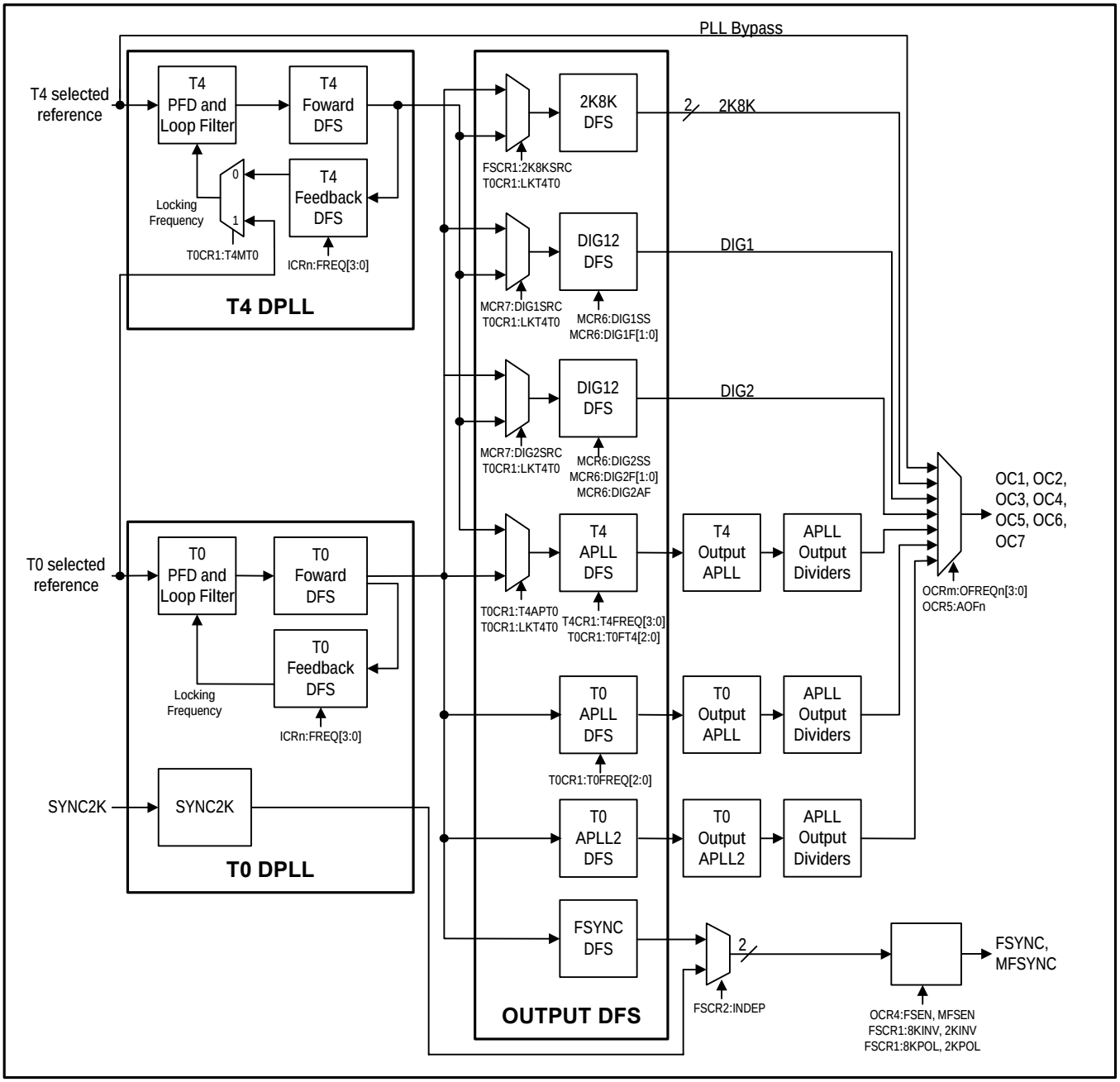
7.6.6 Output Clock Phase Continuity During Reference Switching

If phase build-out is enabled (PBOEN = 1 in MCR10) or the DPLL frequency limit (DLIMIT) is set to less than ±30ppm, the device always complies with the GR-1244-CORE requirement that the rate of phase change must be less than 81ns per 1.326ms during reference switching.

7.7 DPLL Architecture and Configuration

Both T0 and T4 are digital PLLs with separate analog PLLs (APLLs) as the output stage. This architecture combines the benefits of both PLL types. See Figure 7-1.

Figure 7-1. DPLL Block Diagram



Digital PLLs have two key benefits: (1) stable, repeatable performance that is insensitive to process variations, temperature, and voltage; and (2) flexible behavior that is easily programmed via configuration registers. DPLLs use digital frequency synthesis (DFS) to generate various clocks. In DFS a high-speed master clock (204.8MHz) is multiplied up from the 12.800MHz local oscillator clock applied to the REFCLK pin. This master clock is then digitally divided down to the desired output frequency. The DFS output clock has jitter of about 1ns pk-pk.

The analog PLLs filter the jitter from the DPLLs, reducing the 1ns pk-pk jitter to less than 0.5ns pk-pk and 60ps RMS, typical, measured broadband (10Hz to 1GHz).

The DPLLs in the device are configurable for many PLL parameters including bandwidth, damping factor, input frequency, pull-in/hold-in range, input-to-output phase offset, phase build-out, and more. No knowledge of loop equations or gain parameters is required to configure and operate the device. No external components are required for the DPLLs or the APLLs except the high-quality local oscillator connected to the REFCLK pin.

The T0 DPLL to T0 APLL path is the main path through the device. The T0 DPLL has a full free-run/locked/holdover state machine and full programmability. The T4 DPLL to T4 APLL path is a simpler frequency converter/synthesis path, lacking the low bandwidth settings, phase build-out, and phase adjustment controls found in the T0 DPLL.

7.7.1 T0 DPLL State Machine

The T0 DPLL has three main timing modes: locked, holdover and free-run. The control state machine for the T0 DPLL has states for each timing mode as well as three temporary states: prelocked, prelocked 2 and loss-of-lock. The state transition diagram is shown in Figure 7-2. Descriptions of each state are given in the paragraphs below. During normal operation the state machine controls state transitions. When necessary, however, the state can be forced using the T0STATE field of the MCR1 register.

Whenever the T0 DPLL changes state, the STATE bit in MSR2 is set, which can cause an interrupt request if enabled. The current T0 DPLL state can be read from the T0STATE field of the OPSTATE register.

7.7.1.1 Free-Run State

Free-run mode is the reset default state. In free-run all output clocks are derived from the 12.800 MHz local oscillator attached to the REFCLK pin. The frequency of each output clock is a specific multiple of the local oscillator. The frequency accuracy of each output clock is equal to the frequency accuracy of the master clock, which can be calibrated using the MCLKFREQ field in registers MCLK1 and MCLK2 (see Section 7.3). The state machine transitions from free-run to the prelocked state when at least one input clock is valid.

7.7.1.2 Prelocked State

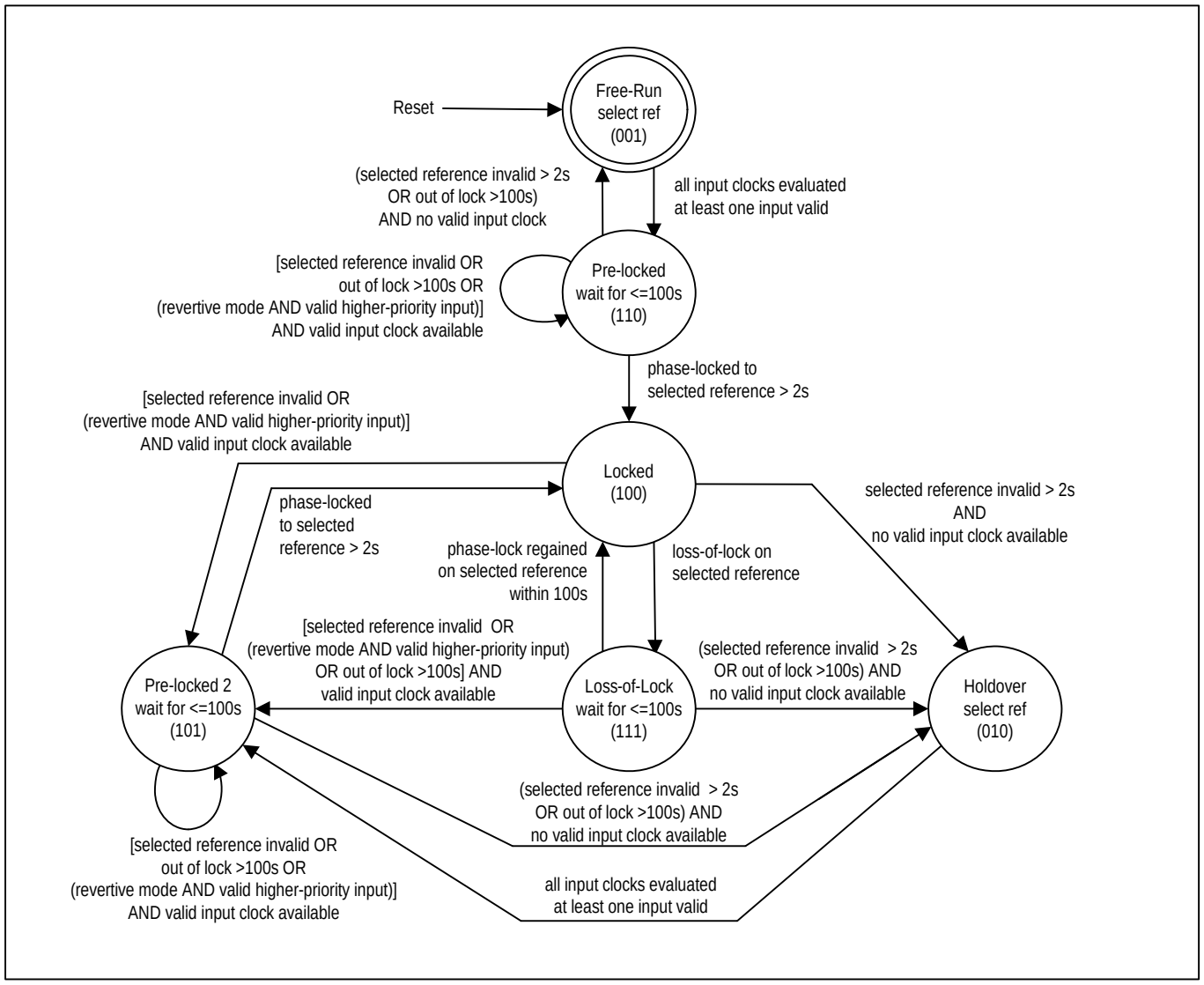
The prelocked state provides a 100-second period (default value of PHLKTO register) for the DPLL to lock to the selected reference. If phase lock (see Section 7.7.6) is achieved for 2 seconds during this period then the state machine transitions to locked mode.

If the DPLL fails to lock to the selected reference within the phase-lock timeout period specified by PHLKTO then a phase lock alarm is raised (corresponding LOCK bit set in the ISR register), invalidating the input (ICn bit goes low in VALSR registers). If another input clock is valid then the state machine re-enters the prelocked state and tries to lock to the alternate input clock. If no other input clocks are valid for two seconds, then the state machine transitions back to the free-run state.

In revertive mode (REVERT = 1 in MCR3), if a higher priority input clock becomes valid during the phase-lock timeout period then the state machine re-enters the prelocked state and tries to lock the higher priority input.

If a phase-lock timeout period longer than 100 seconds is required for locking, then the PHLKTO register must be configured accordingly.

Figure 7-2. T0 DPLL State Transition Diagram



Notes:

- An input clock is valid when it has no activity alarm and no phase lock alarm (see the VALSR registers and the ISR registers).
- All input clocks are continuously monitored for activity.
- Only the selected reference is monitored for loss of lock.
- Phase lock is declared internally when the DPLL has maintained phase lock continuously for approximately 1 to 2 seconds.
- To simply the diagram, the phase-lock timeout period is always shown as 100s, which is the default value of the PHLKTO register. Longer or shorter timeout periods can be specified as needed by writing the appropriate value to the PHLKTO register.
- When selected reference is invalid and the DPLL is not in free-run or holdover, the DPLL is in a temporary holdover state.

7.7.1.3 Locked State

The T0 DPLL state machine can reach the locked state from the prelocked, prelocked 2, or loss-of-lock states when the DPLL has locked to the selected reference for at least 2 seconds (see Section 7.7.6). In the locked state the output clocks track the phase and frequency of the selected reference.

If the MCR1.LOCKPIN bit is set, the LOCK pin is driven high when the T0 DPLL is in the locked state.

While in the locked state, if the selected reference is so impaired that an activity alarm is raised (corresponding ACT bit set in the ISR register), then the selected reference is invalidated (ICn bit goes low in VALSR registers), and the state machine immediately transitions to either the prelocked 2 state (if another valid input clock is available) or, after being invalid for 2 seconds, to the holdover state (if no other input clock is valid).

If loss-of-lock (see Section 7.7.6) is declared while in the locked state then the state machine transitions to the loss-of-lock state.

7.7.1.4 Loss-of-Lock State

When the loss-of-lock detectors (see Section 7.7.6) indicate loss of phase lock, the state machine immediately transitions from the locked state to the loss-of-lock state. In the loss-of-lock state the DPLL tries for 100 seconds (default value of PHLKTO register) to regain phase lock. If phase lock is regained during that period for more than 2 seconds, the state machine transitions back to the locked state.

If, during the phase-lock timeout period specified by PHLKTO, the selected reference is so impaired that an activity alarm is raised (corresponding ACT bit set in the ISR registers), then the selected reference is invalidated (ICn bit goes low in VALSR registers), and after being invalid for 2 seconds the state machine transitions to either the prelocked 2 state (if another valid input clock is available) or the holdover state (if no other input clock is valid).

If phase lock cannot be regained by the end of the phase-lock timeout period then a phase lock alarm is raised (corresponding LOCK bit set in the ISR registers), the selected reference is invalidated (ICn bit goes low in VALSR registers), and the state machine transitions to either the prelocked 2 state (if another valid input clock is available) or, after being invalid for 2 seconds, to the holdover state (if no other input clock is valid).

7.7.1.5 Prelocked 2 State

The prelocked and prelocked 2 states are similar. The prelocked 2 state provides a 100-second period (default value of PHLKTO register) for the DPLL to lock to the new selected reference. If phase lock (see Section 7.7.6) is achieved for more than 2 seconds during this period then the state machine transitions to locked mode.

If the DPLL fails to lock to the new selected reference within the phase-lock timeout period specified by PHLKTO then a phase lock alarm is raised (corresponding LOCK bit set in the ISR registers), invalidating the input (ICn bit goes low in VALSR registers). If another input clock is valid then the state machine re-enters the prelocked 2 state and tries to lock to the alternate input clock. If no other input clocks are valid for 2 seconds, the state machine transitions to the holdover state.

In revertive mode (REVERT = 1 in MCR3), if a higher priority input clock becomes valid during the phase-lock timeout period then the state machine re-enters the prelocked 2 state and tries to lock to the higher priority input.

If a phase-lock timeout period longer than 100 seconds is required for locking, then the PHLKTO register must be configured accordingly.

7.7.1.6 Holdover State

The device reaches the holdover state when it declares its selected reference invalid for 2 seconds and has no other valid input clocks available. During holdover the T0 DPLL is not phase locked to any input clock but instead generates its output frequency from stored frequency information acquired while it was in the locked state. When at least one input clock has been declared valid the state machine immediately transitions from holdover to the prelocked 2 state and tries to lock to the highest priority valid clock.

7.7.1.6.1 Automatic Holdover

For automatic holdover (FRUNHO = 0 in MCR3), the device can be further configured for instantaneous mode or averaged mode. In *instantaneous mode* (AVG = 0 in HOCR3), the holdover frequency is set to the DPLL's current frequency 50 to 100 ms before entry into holdover (i.e., the value of the FREQ field in the FREQ1, FREQ2 and FREQ3 registers when MCR11:T4T0 = 0). The FREQ field is the DPLL's integral path and therefore is an average frequency with a rate of change inversely proportional to the DPLL bandwidth. The DPLL's proportional path is not used in order to minimize the effect of recent phase disturbances on the holdover frequency.

In *averaged mode* (AVG = 1 in HOCR3 and FRUNHO = 1 in MCR3), the holdover frequency is set to an internally averaged value. During locked operation the frequency indicated in the FREQ field is internally averaged over a one-second period. The T0 DPLL indicates that it has acquired a valid holdover value by setting the HORDY status bit in VALSR2 (real-time status) and MSR4 (latched status). If the T0 DPLL must enter holdover before the one-second average is available, an instantaneous value 50ms to 100ms old from the integral path is used instead.

7.7.1.6.2 Free-Run Holdover

For free-run holdover (FRUNHO = 1 in MCR3), the output frequency accuracy is generated with the accuracy of the external oscillator frequency. The actual frequency is the frequency of the external oscillator plus the value of the MCLK offset specified in the MCLKFREQ field in registers MCLK1 and MCLK2 (see Section 7.3). When MCR3.FRUNHO is set the HOCR3:AVG bit is ignored.

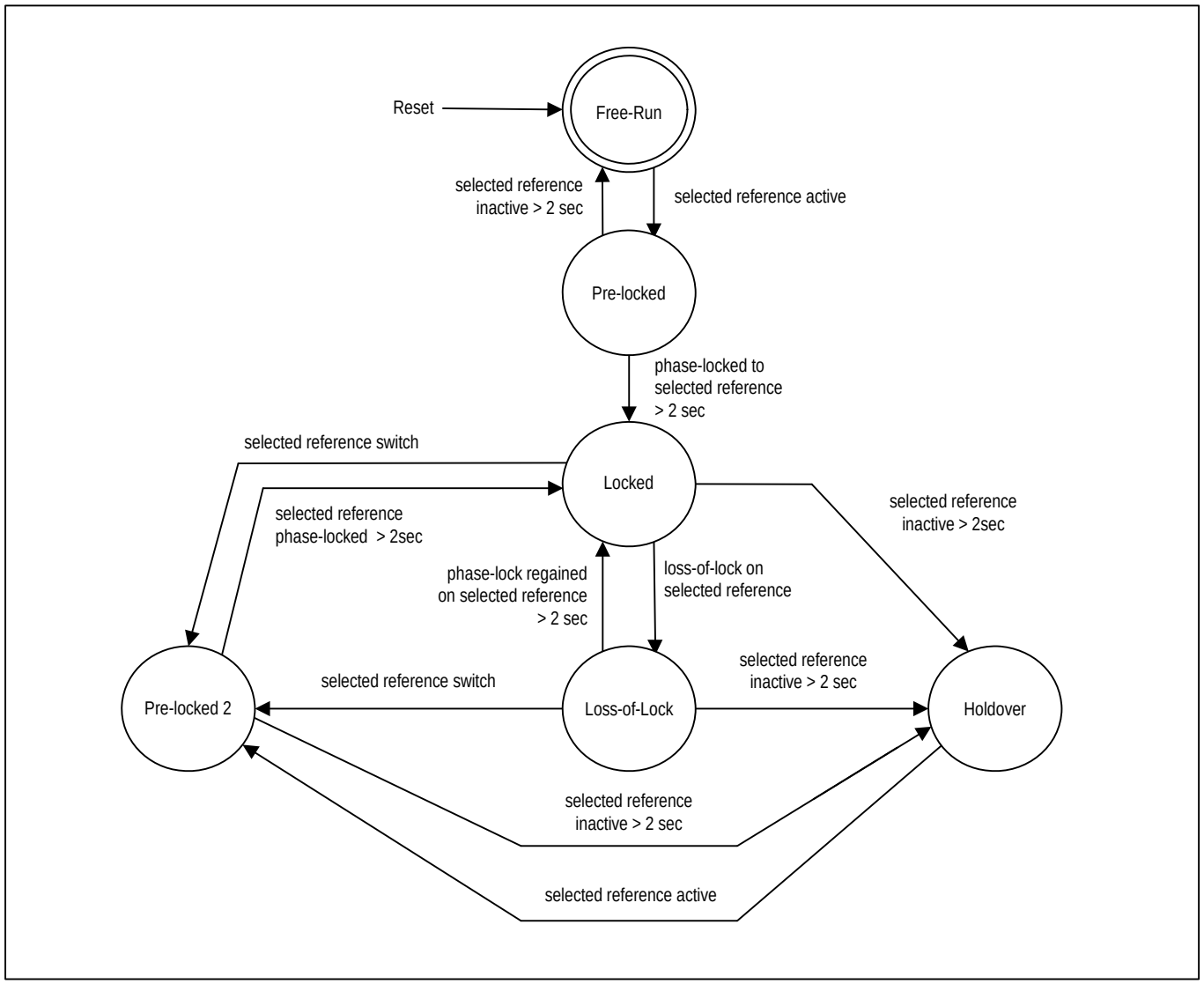
7.7.1.7 Mini-Holdover

When the selected reference fails, the fast activity monitor (Section 7.5.3) isolates the T0 DPLL from the reference within one or two clock cycles to avoid adverse effects on the DPLL frequency. When this fast isolation occurs, the DPLL enters a temporary mini-holdover mode, with a frequency equal to an instantaneous value 50ms to 100 ms old from the integral path of the loop filter. Mini-holdover lasts until the selected reference becomes active or the state machine enters the holdover state. If the free-run holdover mode is set (FRUNHO = 1 in MCR3), the mini-holdover frequency accuracy is exactly the same as the external oscillator accuracy plus the offset set by the MCLKFREQ field in registers MCLK1 and MCLK2 (see Section 7.3).

7.7.2 T4 DPLL State Machine

The T4 DPLL state machine is similar to the T0 DPLL, as shown in Figure 7-3. The T4 DPLL states are similar to the equivalent states of the T0 DPLL but the only state indicator is the T4LOCK bit in the OPSTATE register. Note that the T4 DPLL only operates in revertive switching mode. The full-holdover and mini-holdover modes are instantaneous (see the first paragraph of Section 7.7.1.6.1).

Figure 7-3. T4 DPLL State Transition Diagram



7.7.3 Bandwidth

The bandwidth of the T4 DPLL is configured in the T4BW register to be 18Hz to 70Hz.

The bandwidth of the T0 DPLL is configured in the T0ABW and T0LBW registers for various values from 0.1Hz to 400Hz. The AUTOBW bit in the MCR9 register controls automatic bandwidth selection. When AUTOBW = 1, the T0 DPLL uses the T0ABW bandwidth during acquisition (not phase locked) and the T0LBW bandwidth when phase locked. When AUTOBW = 0 the T0 DPLL uses the T0LBW bandwidth all the time, both during acquisition and when phase locked.

When LIMINT = 1 in the MCR9 register, the DPLL's integral path is limited (i.e., frozen) when the DPLL reaches minimum or maximum frequency. Setting LIMINT = 1 minimizes overshoot when the DPLL is pulling in.

7.7.4 Damping Factor

The damping factor for the T0 DPLL is configured in the DAMP field of the T0CR2 register, while the damping factor of the T4 DPLL is configured in the DAMP field of the T4CR2 register. The reset default damping factors for both DPLLs are chosen to give a maximum jitter/wander gain peak of approximately 0.1dB. Available settings are a function of DPLL bandwidth (configured in the T4BW, T0ABW, and T0LBW registers). See Table 7-4.

Table 7-4. Damping Factors and Peak Jitter/Wander Gain

BANDWIDTH (Hz)	DAMP[2:0] VALUE	DAMPING FACTOR	GAIN PEAK (dB)
0.1 to 4	1, 2, 3, 4, 5	5	0.1
8	1	2.5	0.2
	2, 3, 4, 5	5	0.1
18	1	1.2	0.4
	2	2.5	0.2
	3, 4, 5	5	0.1
35	1	1.2	0.4
	2	2.5	0.2
	3	5	0.1
	4, 5	10	0.06
70 to 400	1	1.2	0.4
	2	2.5	0.2
	3	5	0.1
	4	10	0.06
	5	20	0.03

7.7.5 Phase Detectors

Phase detectors are used to compare a PLL's feedback clock with its input clock. Several phase detectors are available in the T0 and T4 DPLLs:

- Phase/frequency detector (PFD)
- Early/late phase detector (PD2) for fine resolution
- Multicycle phase detector (MCPD) for large input jitter tolerance and/or faster lock times

These detectors can be used in combination to give fine phase resolution combined with large jitter tolerance. As with the rest of the DPLL logic, the phase detectors operate at input frequencies up to 77.76MHz. The multicycle phase detector detects and remembers phase differences of many cycles (up to 8191UI). When locking to 8kHz or lower, the normal phase/frequency detectors are always used.

The T0 DPLL phase detectors can be configured for normal phase/frequency locking (±360° capture) or nearest-edge phase locking (±180° capture). With nearest-edge detection the phase detectors are immune to occasional missing clock cycles. The DPLL automatically switches to nearest-edge locking when the multicycle phase detector is disabled and the other phase detectors determine that phase lock has been achieved. Setting D180 = 1 in the TEST1 register disables nearest-edge locking and forces the T0 DPLL to use phase/frequency locking. The T4 DPLL always has nearest edge locking enabled.

The early/late phase detector, also known as phase detector 2, is enabled and configured in the PD2* fields of registers T0CR2 and T0CR3 for the T0 DPLL and registers T4CR2 and T4CR3 for the T4 DPLL. The reset default settings of these registers are appropriate for all operating modes. Adjustments only affect small signal overshoot and bandwidth.

The multicycle phase detector is enabled by setting MCPDEN = 1 in the PHLIM2 register. The range of the MCPD—from ±1UI up to ±8191UI—is configured in the COARSELIM field of PHLIM2. The MCPD tracks phase position over many clock cycles, giving high jitter tolerance. Thus the use of the MCPD is an alternative to the use of LOCK8K mode for jitter tolerance. When a DPLL is direct locking to 8kHz, 4kHz, or 2kHz or in LOCK8K mode, the multicycle phase detector is automatically disabled.

When USEMCPD = 1 in PHLIM2, the MCPD is used in the DPLL loop, giving faster pull-in but more overshoot. In this mode the loop has similar behavior to LOCK8K mode. In both cases large phase differences contribute to the dynamics of the loop. When enabled by MCPDEN = 1, the MCPD tracks the phase position whether or not it is used in the DPLL loop.

When the input clock is divided before being sent to the phase detector, the divider output clock edge gets aligned to the feedback clock edge before the DPLL starts to lock to a new input clock signal or after the input clock signal has a temporary signal loss. This helps ensure locking to the nearest input clock edge which reduces output transients and decreases lock times.

7.7.6 Loss of Phase Lock Detection

Loss of phase lock can be triggered by any of the following in both the T0 and T4 DPLLs:

- The fine phase lock detector (measures phase between input and feedback clocks)
- The coarse phase lock detector (measures whole cycle slips)
- Hard frequency limit detector
- Inactivity detector

The fine phase lock detector is enabled by setting FLEN = 1 in the PHLIM1 register. The fine phase limit is configured in the FINELIM field of PHLIM1.

The coarse phase lock detector is enabled by setting CLEN = 1 in the PHLIM2 register. The coarse phase limit is configured in the COARSELIM field of PHLIM2. This coarse phase lock detector is part of the multicycle phase detector (MCPD) described in Section 7.7.5. The COARSELIM field sets both the MCPD range and the coarse phase limit, since the two are equivalent. If loss of phase lock should not be declared for multiple-UI input jitter then the fine phase lock detector should be disabled and the coarse phase lock detector should be used instead.

The hard frequency limit detector is enabled by setting FLLOL = 1 in the DLIMIT3 register. The hard limit for the T0 DPLL is configured in registers DLIMIT1 and DLIMIT2. The T4 DPLL hard limit is fixed at ±80ppm. When the DPLL frequency reaches the hard limit, loss-of-lock is declared. The DLIMIT3 register also has the SOFTLIM field to specify a soft frequency limit. Exceeding the soft frequency limit does not cause loss-of-lock to be declared. When the T0 DPLL frequency reaches the soft limit the T0SOFT status bit is set in the OPSTATE register. When the T4 DPLL frequency reaches the soft limit the T4SOFT status bit is set in OPSTATE. Both the SOFT and HARD alarm limits have hysteresis as required by GR-1244.

The inactivity detector is enabled by setting NALOL = 1 in the PHLIM1 register. When this detector is enabled the DPLL declares loss-of-lock after one or two missing clock cycles on the selected reference. See Section 7.5.3.

When the T0 DPLL declares loss of phase lock, the state machine immediately transitions to the loss-of-lock state, which sets the STATE bit in the MSR2 register and requests an interrupt if enabled.

When the T4 DPLL declares loss of phase lock, the T4LOCK bit is cleared in the OPSTATE register, which sets the T4LOCK bit in the MSR3 register and requests an interrupt if enabled.

7.7.7 Phase Build-Out

7.7.7.1 Automatic Phase Build-Out in Response to Reference Switching

When MCR10:PBOEN = 0, phase build-out is not performed during reference switching. The T0 DPLL always locks to the selected reference at zero degrees of phase. With PBO disabled, transitions from a failed reference to the next highest priority reference and transitions from holdover or free-run to locked mode cause phase transients on output clocks as the T0 DPLL jumps from its previous phase to the phase of the new selected reference.

When MCR10:PBOEN = 1, phase build-out is performed during reference switching (or exiting from holdover). With PBO enabled, if the selected reference fails and another valid reference is available then the device enters a temporary holdover state in which the phase difference between the new reference and the output is measured and fed into the DPLL loop to absorb the input phase difference. Similarly, during transitions from full-holdover, mini-holdover or free-run to locked mode, the phase difference between the new reference and the output is measured and fed into the DPLL loop to absorb the input phase difference. After a PBO event, regardless of the input phase difference, the output phase transient is less than or equal to 5ns.

Any time that PBO is enabled it can also be frozen at the current phase offset by setting MCR10:PBOFRZ = 1. When PBO is frozen the T0 DPLL ignores subsequent phase build-out events and maintains the current phase offset between inputs and outputs.

Disabling PBO while the T0 DPLL is not in the free-run or holdover states (locking or locked) will cause a phase change on the output clocks while the DPLL switches to tracking the selected reference with 0 degrees of phase error. The rate of phase change on the output clocks depends on the DPLL bandwidth. Enabling PBO (which includes un-freezing) while locking or locked also causes a PBO event.

7.7.7.2 PBO Phase Offset Adjustment

An uncertainty of up to 5ns is introduced each time a phase build-out event occurs. This uncertainty results in a phase hit on the output. Over a large number of phase build-out events the mean error should be zero. The PBOFF register specifies a small fixed offset for each phase build-out event to skew the average error toward zero and eliminate accumulation of phase shifts in one direction.

7.7.8 Input to Output (Manual) Phase Adjustment

When phase build-out is disabled (PBOEN = 0 in MCR10), the OFFSET registers can be used to adjust the phase of the T0 DPLL output clocks with respect to the selected reference when locked. Output phase offset can be adjusted over a ±200ns range in 6ps increments. This phase adjustment occurs in the feedback clock so that the output clocks are adjusted to compensate. The rate of change is therefore a function of DPLL bandwidth. Simply writing to the OFFSET registers with phase build-out disabled causes a change in the input to output phase, which can be considered to be a delay adjustment. Changing the OFFSET adjustment while in free-run or holdover state will not cause an output phase offset until it exits the state and enters one of the locking states.

7.7.9 Phase Recalibration

When a phase buildout occurs, either automatic or manual, the feedback frequency synthesizer does not get an internal alignment signal to keep it aligned with the output dividers, and therefore the phase difference between input and output may become incorrect. Setting the FSCR3:RECAL bit periodically causes a recalibration process to be executed which corrects any phase error that may have occurred.

During the recalibration process the device puts the DPLL into mini-holdover, internally ramps the phase offset to zero, resets all clock dividers, ramps the phase offset to the value stored in the OFFSET registers, and then switches the DPLL out of mini-holdover. If the OFFSET registers are written during the recalibration process, the process will ramp the phase offset to the new offset value.

7.7.10 Frequency and Phase Measurement

When the T4 DPLL is not needed to generate an output frequency locked to an input clock it can measure precise frequency by locking onto any input. It can also measure phase between the T0 selected reference and any input by setting the T0CR1.T4MT0 bit. The T4 APLL can still be used to clean up jitter on a synthesized clock from the T0 DPLL. When the T0CR1.T4MT0 bit is set the T4 DPLL goes to the free-run state.

Accurate measurement of frequency and phase can be accomplished using the DPLLs. The T0 DPLL is always monitoring its selected reference, but the T4 DPLL can be configured as a high-resolution phase monitor. The REFCLK signal accuracy after being adjusted with MCLKFREQ is used for the frequency reference. Software can then connect the T4 DPLL to various input clocks on a rotating basis to measure phase between the T0 DPLL input and another input. See the T4FORCE field of MCR4.

DPLL frequency measurements can be read from the FREQ field spanning registers FREQ1, FREQ2 and FREQ3. This field indicates the frequency of the selected reference for either the T0 DPLL or the T4 DPLL, depending on the setting of the T4T0 bit in MCR11. This frequency measurement has a resolution of 0.0003068ppm over a ±80ppm range. The value read from the FREQ field is the DPLL's integral path value, which is an averaged measurement with an averaging time inversely proportional to DPLL bandwidth.

DPLL phase measurements can be read from the PHASE field spanning registers PHASE1 and PHASE2. This field indicates the phase difference seen by the phase detector for either the T0 DPLL or the T4 DPLL, depending on the setting of the T4T0 bit in MCR11. This phase measurement has a resolution of approximately 0.703 degrees and is internally averaged with a -3dB attenuation point of approximately 100Hz. Thus for low DPLL bandwidths the PHASE field gives input phase wander in the frequency band from the DPLL corner frequency up to 100Hz. This information could be used by software to compute a crude MTIE measurement.

For the T0 DPLL the PHASE field always indicates the phase difference between the selected reference and the internal feedback clock. The T4 DPLL, however, can be configured to measure the phase difference between two input clocks. When T0CR1:T4MT0 = 1, the T4 DPLL locking capability is disabled and the T4 phase detector is configured to compare the T0 DPLL selected reference with the T4 DPLL selected reference. Any input clock can then be forced to be the T4 DPLL selected reference using the T4FORCE field of MCR4. This feature can be used, for example, to measure the phase difference between the T0 DPLL's selected reference and its next highest priority reference. Software could compute MTIE and TDEV with respect to the T0 DPLL selected reference for any or all of the other input clocks.

When comparing the phase of the T0 and T4 selected references by setting T0CR1:T4MT0 = 1, several details must be kept in mind. In this mode, the T4 path receives a copy of the T0 selected reference, either directly or through a divider to 8kHz. If the T4 selected reference is divided down to 8kHz using LOCK8K or DIVN modes (see Section 7.4.2), then the copy of the T0 selected reference is also divided down to 8kHz. If the T4 selected reference is configured for direct-lock mode, then the copy of the T0 selected reference is not divided down and must be the same frequency as the T4 selected reference. See Table 7-5 for more details. (While T0CR1:T4MT0 = 1, the T0 path continues to lock to the T0 selected reference in the manner specified in the corresponding ICR register.)

Table 7-5. T0 DPLL Adaptation for the T4 DPLL Phase Measurement Mode

LOCKING MODE FOR T4 SELECTED REFERENCE	LOCKING MODE FOR T0 SELECTED REFERENCE	LOCKING MODE FOR COPY OF T0 SELECTED REF	FREQUENCY OF THE T4 SELECTED REF FOR T4MT0 PHASE MEASUREMENT	FREQUENCY OF THE T0 SELECTED REF FOR T4MT0 PHASE MEASUREMENT
LOCK8K or DIVN(8K)	DIRECT	LOCK8K	8kHz	8kHz
LOCK8K or DIVN(8K)	LOCK8K	LOCK8K	8kHz	8kHz
LOCK8K or DIVN(8K)	DIVN (8K)	DIVN	8kHz	8kHz
LOCK8K or DIVN(8K)	DIVN (not 8K)	DIRECT	8kHz	8kHz
DIVN (not 8K)	Any	DIRECT	Same as the T4 forced ref input frequency	Same as the T0 selected ref input frequency(1)
DIRECT	Any	DIRECT	Same as the T4 forced ref input frequency	Same as the T0 selected ref input frequency(1)

Note 1: In this case the T0 select reference must be the same frequency as the T4 selected reference.

Note 2: If the T4 selected reference frequency is 8kHz and the T0 selected reference is a different frequency, the two references can be compared by configuring the T4 selected reference for 8kHz and LOCK8K mode. This forces the copy of the T0 selected reference to be divided down to 8kHz using either LOCK8K or DIVN mode.

Note 3: DIVN(8K) means that the FREQ field is set to 8kHz, DIVN(not 8K) means the FREQ field is not set to 8kHz.

7.7.11 Input Jitter Tolerance

The device is compliant with the jitter tolerance requirements of the standards listed in Table 1-1. When using the ±360°/±180° PFD, jitter can be tolerated up to the point of eye closure. Either LOCK8K mode (see Section 7.4.2.2) or the multicycle phase detector (see Section 7.7.5) should be used for high jitter tolerance.

7.7.12 Jitter and Wander Transfer

The transfer of jitter and wander from the selected reference to the output clocks has a programmable transfer function that is determined by the DPLL bandwidth. (See Section 7.7.3.) In the T0 DPLL, the 3dB corner frequency of the jitter transfer function can be set to any of 13 positions from 0.1Hz to 400Hz. In the T4 DPLL the 3dB corner frequency of the jitter transfer function can be set to various values from 18Hz to 70Hz.

During locked mode, the transfer of wander from the local oscillator clock (connected to the REFCLK pin) to the output clocks is not significant as long as the DPLL bandwidth is set high enough to allow the DPLL to quickly compensate for oscillator frequency changes. During free-run and holdover modes, local oscillator wander has a much more significant effect. See Section 7.3.

7.7.13 Output Jitter and Wander

Several factors contribute to jitter and wander on the output clocks, including:

- Jitter and wander amplitude on the selected reference (while in the locked state)
- The jitter/wander transfer characteristic of the device (while in the locked state)
- The jitter and wander on the local oscillator clock signal (especially wander while in the holdover state)

The DPLL in the device has programmable bandwidth (see Section 7.7.3). With respect to jitter and wander, the DPLL behaves as a low-pass filter with a programmable pole. The bandwidth of the DPLL is normally set low enough to strongly attenuate jitter. The wander and jitter attenuation depends on the DPLL bandwidth chosen.

Over time frequency changes in the local oscillator can cause a phase difference between the selected reference and the output clocks. This is especially true at lower frequency DPLL bandwidths because the DPLL's rate of change may be slower than the oscillator's rate of change. Oscillators with better stability will minimize this effect. In the most demanding applications an OCXO may be required rather than a TCXO.

7.8 Output Clock Configuration

A total of 18 output clock pins, OC1 to OC5, OC1B to OC5B, OC4POS/NEG to OC7POS/NEG and FSYNC and MFSYNC are available on the device. Output clocks OC1 to OC7 are individually configurable for a variety of frequencies derived from either the T0 DPLL or the T4 DPLL. OC1B to OC5B are powered from a dedicated IO power pin which can be set to any voltage from 2.2V to 3.3V. Output clocks FSYNC and MFSYNC serve as 8kHz frame sync and 2kHz multiframe sync outputs, respectively. Table 7-6 provides more detail on the capabilities of the output clock pins.

Table 7-6. Output Clock Capabilities

OUTPUT CLOCK	SIGNAL FORMAT	FREQUENCIES SUPPORTED
OC1	CMOS/TTL 3.3V powered	Frequency selection per Section 7.8.2.3 and Table 7-7 to Table 7-13.
OC2		
OC3		
OC4		
OC5		
OC1B	CMOS/TTL 2.5V or 3.3V powered	
OC2B		
OC3B		
OC4B		
OC5B		
OC4	LVDS/LVPECL	
OC5		
OC6		
OC7		
FSYNC	CMOS/TTL	8kHz frame sync with programmable pulse width and polarity.
MFSYNC		2kHz multiframe sync with programmable pulse width and polarity.

7.8.1 Signal Format Configuration

Output clocks OC4, OC5, OC6, and OC7 are LVDS-compatible, LVPECL level-compatible outputs. The type of output can be selected or the output can be disabled using the OCnSF configuration bits in the MCR8 register. The LVPECL level-compatible mode generates a differential signal that is large enough for most LVPECL receivers. Some LVPECL receivers have a limited common mode signal range which can be accommodated for by using an AC coupled signal. The LVDS electrical specifications are listed in Table 10-5, and the recommended LVDS termination is shown in Figure 10-1. The LVPECL level-compatible electrical specifications are listed in Table 10-6, and the recommended LVPECL receiver termination is shown in Figure 10-3. These differential outputs can be easily interfaced to LVDS, LVPECL and CML inputs on neighboring ICs using a few external passive components. See Maxim App Note HFAN-1.0 for details.

The other output clocks are CMOS/TTL signal format.

7.8.2 Frequency Configuration

The frequency of output clocks OC1 to OC7 is a function of the settings used to configure the components of the T0 and T4 PLL paths. These components are shown in the detailed block diagram of Figure 7-1.

The DS3104-SE uses digital frequency synthesis (DFS) to generate various clocks. In DFS a high-speed master clock (204.8MHz) is divided down to the desired output frequency by adding a number to an accumulator. The DFS output is a coding of the clock output phase which is used by a special circuit to determine where to put the edges of the output clock between the clock edges of the master clock. The edges of the output clock, however, are not ideally located in time resulting in jitter with an amplitude typically less than 1ns pk-pk.

7.8.2.1 T0 and T4 DPLL Details

See Figure 7-1. The T0 and T4 forward DFS blocks use the 204.8MHz master clock and DFS technology to synthesize internal clocks from which the output and feedback clocks are derived. The T4 DPLL only has a single DFS output clock signal for both the output clocks and the feedback clock, whereas there are two DFS output clock signals in the T0 DPLL, one for the output clocks and one for the feedback clock.

In the T0 DPLL the feedback clock signal output handles phase build-out or any phase offset configured in the OFFSET registers. Thus the T0 DPLL output clock signals and the feedback clock signal are frequency locked but may have a phase offset. The T0 and T4 feedback DFS blocks are always connected to the T0 forward DFS and the T4 forward DFS, respectively. The feedback DFS blocks synthesize the appropriate locking frequencies for use by the phase-frequency detectors (PFDs). See Section 7.4.2.

7.8.2.2 Output DFS and APLL Details

See Figure 7-1. The output clock frequencies are determined by two 2kHz/8kHz DFS blocks, two DIG12 DFS blocks, and three APLL DFS blocks. Four of the DFS blocks can be connected to either the T0 DPLL or the T4 DPLL, three are always connected to the T0 DPLL. The T0 APLL, the T0 APLL2 and the T4 APLL (and their output dividers) get their frequency references from three associated APLL DFS blocks. All of the output DFS blocks are connected to the T0 DPLL when MCR4:LKT4T0 = 1.

The 2K8K DFS and FSYNC DFS blocks generate both 2kHz and 8kHz signals which have about 1ns pk-pk jitter. The FSYNC (8kHz) and MFSYNC(2 kHz) signals come from the FSYNC DFS block, which is always connected to the T0 DPLL when not in independent mode (FSCR2:INDEP = 1). The 2kHz and 8kHz signals available on output clocks OC1 to OC7 come from the 2K8K DFS, which can be connected to either the T0 DPLL or the T4 DPLL depending on FSCR1:2K8KSRC and MCR4:LKT4T0.

The DIG1 DFS can generate an NxDS1 or NxE1 signal with about 1ns pk-pk jitter. The DIG2 DFS can generate an NxDS1, NxE1, 6.312MHz, 10MHz, or Nx19.44MHz clock with approximately 1ns pk-pk jitter. Each DIG12 DFS can be connected to either the T0 DPLL or the T4 DPLL using MCR7:DIG1SRC or MCR7:DIG2SRC and MCR4:LKT4T0. The frequency of the DIG1 clock is configured by the DIG1SS bit in MCR6 and the DIG1F[1:0] field in MCR7. The frequency of the DIG2 clock is configured by the DIG2AF and DIG2SS bits in MCR6 and the DIG2F[1:0] field in MCR7. DIG1 and DIG2 can be independently configured for any of the frequencies shown in Table 7-7 and Table 7-8, respectively.

The APLL DFS blocks and their associated output APLLs and output dividers can generate many different frequencies. The T0 APLL DFS and the T0 APLL2 DFS are always connected to the T0 DPLL. The T4 APLL DFS can be connected to either the T0 DPLL or the T4 DPLL depending on T0CR1:T4APT0 and MCR4:LKT4T0. The T0 APLL frequencies that can be generated are listed in Table 7-10. The T0 APLL2 frequency is always 312.500MHz. The T4 APLL frequencies that can be generated are listed in Table 7-12. The output frequencies that can be generated from the APLL circuits are listed in Table 7-9.

The T4 APLL is disabled and powered down when T4CR1:T4FREQ = 0000 and T0CR1:T4APT0 = 0. In this mode all outputs connected to the T4 APLL are driven low.

Together the T0 APLL, T0 APLL2 and T4 APLL can simultaneously generate SONET/SDH clock rates, Gigabit Ethernet clock rates (e.g., 125MHz) and 10G Ethernet clock rates (e.g., 156.25MHz), all locked to the same selected reference. This capability supports mixed SONET/SDH and Synchronous Ethernet line cards.

7.8.2.3 OC1 to OC7 Configuration

The following is a step-by-step procedure for configuring the frequencies of output clocks OC1 through OC7:

1) Determine whether the T4 APLL must be independent of the T0 DPLL or not. If the T4 APLL must be independent, set T4APT0 = 0 in register T0CR1. If the T4 APLL must be locked to the T0 DPLL then set T4APT0 = 1.
2) Use Table 7-9 to select a set of output frequencies for each APLL, T0 and T4. Each APLL can only generate one set of output frequencies. (In SONET/SDH equipment the T0 APLL is typically configured for a frequency of 311.04MHz to get 19.44MHz and/or 38.88MHz output clocks to distribute to system line cards.)
3) Determine from Table 7-9 the T0 and T4 APLL frequencies required for the frequency sets chosen in step 2.
4) Configure the T0FREQ field in register T0CR1 as shown in Table 7-10 for the T0 APLL frequency determined in step 3. Configure the T4FREQ field in register T4CR1 as shown in Table 7-12 for the T4 APLL frequency determined in step 3. If the T4 APLL is locked to the T0 DPLL, the T4APT0 and T0FT4 fields in T0CR1 must also be configured as shown in Table 7-12.
5) Using Table 7-9 and Table 7-13, configure the frequencies of output clocks OC1 through OC7 in the OFREQn fields of registers OCR1 through OCR4 and the AOFn bit in the OCR5 register.

Table 7-14 lists all standard frequencies for the output clocks and specifies how to configure the T0 APLL and/or the T4 APLL to obtain each frequency. Table 7-14 also indicates the expected jitter amplitude for each frequency.

Table 7-7. Digital1 Frequencies

DIG1F[1:0] SETTING IN MCR7	DIG1SS SETTING IN MCR6	FREQUENCY (MHz)	JITTER (pk-pk ns, typ)
00	0	2.048	< 1
01	0	4.096	< 1
10	0	8.192	< 1
11	0	16.384	< 1
00	1	1.544	< 1
01	1	3.088	< 1
10	1	6.176	< 1
11	1	12.352	< 1

Table 7-8. Digital2 Frequencies

DIG2AF SETTING IN MCR6	DIG2F[1:0] SETTING IN MCR7	DIG2SS SETTING IN MCR6	FREQUENCY (MHz)	JITTER (pk-pk ns, typ)
1	00	0	6.312	< 1
1	10	0	10.000	<1
1	00	1	19.440	< 1
1	01	1	38.880	< 1
0	00	0	2.048	< 1
0	01	0	4.096	< 1
0	10	0	8.192	< 1
0	11	0	16.384	< 1
0	00	1	1.544	< 1
0	01	1	3.088	< 1
0	10	1	6.176	< 1
0	11	1	12.352	< 1

Table 7-9. APLL Frequency to Output Frequencies (T0 APLL and T4 APLL)

APLL FREQUENCY	APLL / 2	APLL / 4	APLL / 5	APLL / 6	APLL / 8	APLL / 10	APLL / 12	APLL / 16	APLL / 20	APLL / 48	APLL / 64
312.500	**156.250**	—	**62.500**	—	—	31.250	—	—	—	—	—
311.040	**155.520**	**77.760**	62.208	**51.840**	**38.880**	31.104	25.920	**19.440**	15.552	**6.480**	4.860
274.944	**137.472**	68.376	—	45.824	**34.368**	—	22.912	17.184	—	5.728	4.296
250.000	**125.000**	**62.500**	50.000	—	31.250	**25.000**	—	—	12.500	—	—
178.944	89.472	**44.736**	—	29.824	22.368	—	14.912	11.184	—	3.728	2.796
160.000	80.000	40.000	32.00	—	20.000	16.000	—	**10.000**	8.000	—	2.500
148.224	74.112	37.056	—	24.704	18.528	—	12.352	9.264	—	**3.088**	2.316
131.072	65.536	**32.768**	—	—	**16.384**	—	—	**8.192**	—	—	**2.048**
122.880	61.440	**30.720**	24.576	20.48	15.360	12.288	**10.240**	7.680	6.144	2.560	1.920
104.000	52.000	26.000	20.800	—	**13.000**	10.400	—	6.500	5.200	—	—
100.992	50.496	25.248	—	16.832	12.624	—	8.416	**6.312**	—	2.104	1.578
98.816	49.408	24.704	—	—	12.352	—	—	**6.176**	—	—	**1.544**
98.304	49.152	24.576	—	**16.384**	12.288	—	**8.192**	6.144	—	**2.048**	1.536

Note: *All frequencies in MHz. Common telecom, datacom and synchronization frequencies are in* ***bold*** *type.*

Table 7-10. T0 APLL Frequency Configuration

T0 APLL FREQUENCY (MHz)	T0 APLL DFS FREQUENCY (MHz)	T0 APLL FREQUENCY MODE	T0FREQ[2:0] SETTING IN T0CR1	OUTPUT JITTER (pk-pk, ns, typ)
311.04	77.76	77.76MHz	000	< 0.5
311.04	77.76	77.76MHz	001	< 0.5
98.304	24.576	12 x E1	010	< 0.5
131.072	32.768	16 x E1	011	< 0.5
148.224	37.056	24 x DS1	100	< 0.5
98.816	24.704	16 x DS1	101	< 0.5
100.992	25.248	4 x 6312kHz	110	< 0.5
250.000	62.5	GbE ÷ 16	111	< 0.5

Table 7-11. T0 APLL2 Frequency Configuration

T0 APLL2 FREQUENCY (MHz)	T0 APLL2 DFS FREQUENCY(MHz)	OUTPUT JITTER (pk-pk, ns, typ)
312.500	62.500	<0.5

Table 7-12. T4 APLL Frequency Configuration

T4 APLL FREQUENCY (MHz)	T4 APLL DFS FREQUENCY (MHz)	T4 APLL FREQUENCY MODE	T4APT0 SETTING IN T0CR1	T4FREQ[3:0] SETTING IN T4CR1	T0FT4[2:0] SETTING IN T0CR1	OUTPUT JITTER (pk-pk, ns, typ)
Disabled	77.76	Squelched	0	0000	XXX	< 0.5
311.04	77.76	77.76MHz	0	0001	XXX	< 0.5
98.304	24.576	12 x E1	0	0010	XXX	< 0.5
131.072	32.768	16 x E1	0	0011	XXX	< 0.5
148.224	37.056	24 x DS1	0	0100	XXX	< 0.5
98.816	24.704	16 x DS1	0	0101	XXX	< 0.5
274.944	68.736	2 x E3	0	0110	XXX	< 0.5
178.944	44.736	DS3	0	0111	XXX	< 0.5
100.992	25.248	4 x 6312kHz	0	1000	XXX	< 0.5
250.000	62.500	GbE ÷ 16	0	1001	XXX	< 0.5
122.88	30.720	3 x 10.24	0	1010	XXX	< 0.5
160.000	40.000	4 x 10	0	1011	XXX	< 0.5
104.000	26.000	2 x 13	0	1100	XXX	< 0.5
98.304	24.576	T0 12 x E1	1	XXXX	000	< 0.5
250.000	62.500	T0 GbE ÷ 16	1	XXXX	001	< 0.5
131.072	32.768	T0 16 x E1	1	XXXX	010	< 0.5
148.224	37.056	T0 24 x DS1	1	XXXX	100	< 0.5
98.816	24.704	T0 16 x DS1	1	XXXX	110	< 0.5
100.992	25.248	T0 4 x 6312kHz	1	XXXX	111	< 0.5

Table 7-13. OC1–OC7 Output Frequency Selection

AOF BIT	OFREQ(1)	FREQUENCY						
		OC1	OC2	OC3	OC4	OC5	OC6	OC7
0	0000	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled
0	0001	2kHz	2kHz	2kHz	2kHz	2kHz	2kHz	2kHz
0	0010	8kHz	8kHz	8kHz	8kHz	8kHz	8kHz	8kHz
0	0011	Digital2	Digital2	Digital2	Digital2	Digital2	T0 / 2	Digital 2
0	0100	Digital1	Digital1	Digital1	Digital1	Digital1	Digital1	T0 / 2
0	0101	T0 / 48	T0 / 48	T0 / 48	T0 / 48	T0 / 48	T0 / 1	T0 / 48
0	0110	T0 / 16	T0 / 16	T0 / 16	T0 / 16	T0 / 16	T0 / 16	T0 / 16
0	0111	T0 / 12	T0 / 12	T0 / 12	T0 / 12	T0 / 12	T0 / 12	T0 / 12
0	1000	T0 / 8	T0 / 8	T0 / 8	T0 / 8	T0 / 8	T0 / 8	T0 / 8
0	1001	T0 / 6	T0 / 6	T0 / 6	T0 / 6	T0 / 6	T0 / 6	T0 / 6
0	1010	T0 / 4	T0 / 4	T0 / 4	T0 / 4	T0 / 4	T0 / 4	T0 / 4
0	1011	T4 / 64	T4 / 64	T4 / 64	T4 / 2	T4 / 2	T4 / 64	T4 / 64
0	1100	T4 / 48	T4 / 48	T4 / 48	T4 / 48	T4 / 48	T4 / 48	T4 / 48
0	1101	T4 / 16	T4 / 16	T4 / 16	T4 / 16	T4 / 16	T4 / 16	T4 / 16
0	1110	T4 / 8	T4 / 8	T4 / 8	T4 / 8	T4 / 8	T4 / 8	T4 / 8
0	1111	T4 / 4	T4 / 4	T4 / 4	T4 / 4	T4 / 4	T4 / 4	T4 / 4
1	0000	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled
1	0001	T0 / 64	T0 / 64	T0 / 64	T0 / 2	T0 / 2	T4 / 5	T4 / 5
1	0010	T4 / 20	T4 / 20	T4 / 20	T0 / 1	T0 / 1	T4 / 2	T4 / 2
1	0011	T4 / 12	T4 / 12	T4 / 12	T4 / 10	T4 / 10	T4 / 1	T4 / 1
1	0100	T4 / 10	T4 / 10	T4 / 10	T02 / 10	T02 / 10	T02 / 5	T02 / 5
1	0101	T02 / 10	T4 / 5	T4 / 5	T02 / 2	T02 / 2	T02 / 2	T02 / 2
1	0110	T02 / 5	T4 / 2	T4 / 2	T02 / 1	T02 / 1	T02 / 1	T02 / 1
1	0111	T4SELREF	T4SELREF	T4SELREF	T4SELREF	T4SELREF	T4SELREF	T4SELREF

Note 1: The value of the OFREQn field (in the OCR1 through OCR4 registers) corresponding to output clock OCn.

Note 2: T0 = T0 APLL. T02 = T0 APLL2. T4 = T4 APLL.

Table 7-14. Standard Frequencies for Programmable Outputs

FREQUENCY (MHz)		T0 APLL	T4 APLL		OFREQn	JITTER (TYP)	
		T0FREQ	T4FT0	T4FREQ		RMS (ps)	pk-pk (ns)
2kHz					2kHz	100	1.00
8kHz					8kHz	100	1.00
1.536	not OC4, OC5 from T4 APLL not OC4 to OC7 from T0 APLL	12 x E1	12 x E1	12 x E1	APLL/64	50	0.50
1.544	not OC6 from DIG2				DIG1,DIG2	100	1.00
1.544	not OC4, OC5 from T4 APLL not OC4 to OC7 from T0 APLL	16 x DS1	16 x DS1	16 x DS1	APLL/64	50	0.50
1.578	not OC4, OC5 from T4 APLL not OC4 to OC7 from T0 APLL	4 x 6.312	4 x 6.312	4 x 6.312	APLL/64	50	0.50
2.048	not OC6 from DIG2				DIG1,DIG2	100	1.00
2.048	not OC6 from T0 APLL	12 x E1	12 x E1	12 x E1	APLL/48	50	0.50
2.048	not OC4, OC5 from T4 APLL not OC4 to OC7 from T0 APLL	16 x E1	16 x E1	16 x E1	APLL/64	50	0.50
2.104	not OC6 from T0 APLL	4 x 6.312	4 x 6.312	4 x 6.312	APLL/48	50	0.50
2.316	not OC4, OC5 from T4 APLL not OC4 to OC7 from T0 APLL	24 x DS1	24 x DS1	24 x DS1	APLL/64	50	0.50
2.500	not OC4, OC5			4 x 10	APLL/64	50	0.50
2.560				3 x 10.24	APLL/48	50	0.50
2.796	not OC4, OC5			DS3	APLL/64	50	0.50
3.088	not OC6 from DIG2				DIG1,DIG2	100	1.00
3.088	not OC6 from T0 APLL	24 x DS1	24 x DS1	24 x DS1	APLL/48	50	0.50
3.728				DS3	APLL/48	50	0.50
4.096	not OC6 from DIG2				DIG1,DIG2	100	1.00
4.296	not OC4, OC5			2 x E3	APLL/64	50	0.50
4.860	not OC4, OC5 from T4 APLL not OC4 to OC7 from T0 APLL	77.76		77.76	APLL/64	50	0.50
5.200	OC1-OC3 only			2 x 13	APLL/20	50	0.50
5.728				2 x E3	APLL/48	50	0.50
6.144	OC1-OC3 only			3 x 10.24	APLL/20	50	0.50
6.144		12 x E1	12 x E1	12 x E1	APLL/16	50	0.50
6.176	not OC6 from DIG2				DIG1,DIG2	100	1.00
6.176		16 x DS1	16 x DS1	16 x DS1	APLL/16	50	0.50
6.312	not OC6				DIG2	100	1.00
6.312		4 x 6.312	4 x 6.312	4 x 6.312	APLL/16	50	0.50
6.480	not OC6 from T0 APLL	77.76		77.76	APLL/48	60	0.6
8.000	OC1-OC3 only			4 x 10	APLL/20	50	0.50
8.192	not OC6 from DIG2				DIG1,DIG2	100	1.00
8.192		12 x E1			APLL/12	50	0.50
8.192		16 x E1	16 x E1	16 x E1	APLL/16	50	0.50
8.416		4 x 6.312			APLL/12	50	0.50
9.264		24 x DS1	24 x DS1	24 x DS1	APLL/16	50	0.50
10.000	not OC6				DIG2	100	1.00
10.000				4 x 10	APLL/16	50	0.50
10.240	OC1-OC3 only			3 x 10.24	APLL/12	50	0.50
10.400	not OC6, OC7			3 x 10.24	APLL/10	50	0.50
11.184				DS3	APLL/16	50	0.50
12.288		12 x E1	12 x E1	12 x E1	APLL/8	50	0.50
12.288	not OC6, OC7			2 x 13	APLL/10	50	0.50
12.352		24 x DS1			APLL/12	50	0.50
12.352		16 x DS1	16 x DS1	16 x DS1	APLL/8	50	0.50
12.352	not OC6 from DIG2				DIG1,DIG2	100	1.00
12.500	OC1-OC3 only		GbE ÷ 16	GbE ÷ 16	APLL/20	50	0.50
12.624		4 x 6.312	4 x 6.312	4 x 6.312	APLL/8	50	0.50
13.000				2 x 13	APLL/8	50	0.50
15.360				3 x 10.24	APLL/8	50	0.50
15.552	OC1-OC3 only			77.76	APLL/20	50	0.50

FREQUENCY (MHz)		T0 APLL	T4 APLL		OFREQn	JITTER (TYP)	
		T0FREQ	T4FT0	T4FREQ		RMS (ps)	pk-pk (ns)
16.000	not OC6, OC7			4 x 10	APLL/10	50	0.50
16.384	not OC6 from DIG2				DIG1,DIG2	100	1.00
16.384		12 x E1			APLL/6	50	0.50
16.384		16 x E1	16 x E1	16 x E1	APLL/8	50	0.50
16.832		4 x 6.312			APLL/6	50	0.50
17.184				2 x E3	APLL/16	50	0.50
18.528		24 x DS1	24 x DS1	24 x DS1	APLL/8	50	0.50
19.440	not OC6				DIG2	100	1.00
19.440		77.76		77.76	APLL/16	50	0.50
20.000				4 x 10	APLL/8	50	0.50
20.800	OC2, OC3, OC6, OC7 only			2 x 13	APLL/5	50	0.50
22.368				DS3	APLL/8	50	0.50
24.576		12 x E1	12 x E1	12 x E1	APLL/4	50	0.50
24.576	OC2, OC3, OC6, OC7 only			3 x 10.24	APLL/5	50	0.50
24.704		24 x DS1			APLL/6	50	0.50
24.704		16 x DS1	16 x DS1	16 x DS1	APLL/4	50	0.50
25.000	not OC6, OC7		GbE ÷ 16	GbE ÷ 16	APLL/10	50	0.50
25.248		4 x 6.312	4 x 6.312	4 x 6.312	APLL/4	50	0.50
25.920		77.76			APLL/12	50	0.50
26.000				2 x 13	APLL/4	50	0.50
30.720				3 x 10.24	APLL/4	50	0.50
31.104	not OC6, OC7			77.76	APLL/10	50	0.50
31.250		GbE ÷ 16	GbE ÷ 16	GbE ÷ 16	APLL/8	50	0.50
31.250	OC1,OC4,OC5 from T0 APLL2				APLL/10	50	0.50
32.000	OC2, OC3, OC6, OC7 only			4 x 10	APLL/5	50	0.50
32.768		16 x E1	16 x E1	16 x E1	APLL/4	50	0.50
34.368				2 x E3	APLL/8	50	0.50
37.056		24 x DS1	24 x DS1	24 x DS1	APLL/4	50	0.50
38.880		77.76		77.76	APLL/8	50	0.50
40.000				4 x 10	APLL/4	50	0.50
44.736				DS3	APLL/4	50	0.50
49.152	not OC1-OC3 from T0 APLL not OC1, OC2 from T4 APLL	12 x E1	12 x E1	12 x E1	APLL/2	50	0.50
49.408	not OC1-OC3 from T0 APLL not OC1, OC2 from T4 APLL	16 x DS1	16 x DS1	16 x DS1	APLL/2	50	0.50
50.000	OC2, OC3, OC6, OC7 only		GbE ÷ 16	GbE ÷ 16	APLL/5	50	0.50
50.496	not OC1-OC3 from T0 APLL not OC1, OC2 from T4 APLL	4 x 6.312	4 x 6.312	4 x 6.312	APLL/2	50	0.50
51.840		77.76			APLL/6	60	0.6
52.000	not OC1, OC2			2 x 13	APLL/2	50	0.50
61.440	not OC1, OC2			3 x 10.24	APLL/2	50	0.50
62.208	OC2, OC3, OC6, OC7 only			77.76	APLL/5	50	0.50
62.500		GbE ÷ 16	GbE ÷ 16	GbE ÷ 16	APLL/4	50	0.50
62.500	OC1, OC6, OC7 from T0 APLL2				APLL/5	50	0.50
65.536	not OC1-OC3 from T0 APLL not OC1, OC2 from T4 APLL	16 x E1	16 x E1	16 x E1	APLL/2	50	0.50
68.736				2 x E3	APLL/4	50	0.50
74.112	not OC1-OC3 from T0 APLL not OC1, OC2 from T4 APLL	24 x DS1	24 x DS1	24 x DS1	APLL/2	50	0.50
77.76		77.76		77.76	APLL/4	50	0.50
80.000	not OC1, OC2			4 x 10	APLL/2	50	0.50
89.472	not OC1, OC2			DS3	APLL/2	50	0.50
98.304	not OC1-OC3 from T0 APLL OC6, OC7 only from T4 APLL	12 x E1	12 x E1	12 x E1	APLL/1	50	0.50
98.816	not OC1-OC3 from T0 APLL OC6, OC7 only from T4 APLL	16 x DS1	16 x DS1	16 x DS1	APLL/1	50	0.50
100.992	not OC1-OC3 from T0 APLL OC6, OC7 only from T4 APLL	4 x 6312 kHz	4 x 6312 kHz	4 x 6312 kHz	APLL/1	50	0.50
104.000	OC6, OC7 only			2 x 13	APLL/1	50	0.50

FREQUENCY (MHz)		T0 APLL	T4 APLL		OFREQn	JITTER (TYP)	
		T0FREQ	T4FT0	T4FREQ		RMS (ps)	pk-pk (ns)
122.880	OC6, OC7 only			3 x 10.24	APLL/1	50	0.50
125.000	not OC1-OC3 from T0 APLL not OC1, OC2 from T4 APLL	GbE ÷ 16	GbE ÷ 16	GbE ÷ 16	APLL/2	50	0.50
131.072	not OC1-OC3 from T0 APLL OC6, OC7 only from T4 APLL	16 x E1	16 x E1	16 x E1	APLL/1	50	0.50
137.472	OC6, OC7 only			2 x E3	APLL/2	50	0.50
148.224	not OC1-OC3 from T0 APLL OC6, OC7 only from T4 APLL	24 x DS1	24 x DS1	24 x DS1	APLL/1	50	0.50
155.520	not OC1-OC3 from T0 APLL not OC1, OC2 from T4 APLL	77.76		77.76	APLL/2	60	0.6
156.250	OC4-OC7 only from T0 APLL2				APLL/2	50	0.50
160.000	OC6, OC7 only			4 x 10	APLL/1	50	0.50
178.944	OC6, OC7 only			DS3	APLL/1	50	0.50
250.000	OC4-OC7 only	GbE ÷ 16			APLL/1	50	0.50
274.944	OC6, OC7 only						
311.040	OC4-OC7 only	77.76			APLL/1	50	0.50
312.500	OC4-OC7 only from T0 APLL2				APLL/2	50	0.50

7.8.2.4 FSYNC and MFSYNC Configuration

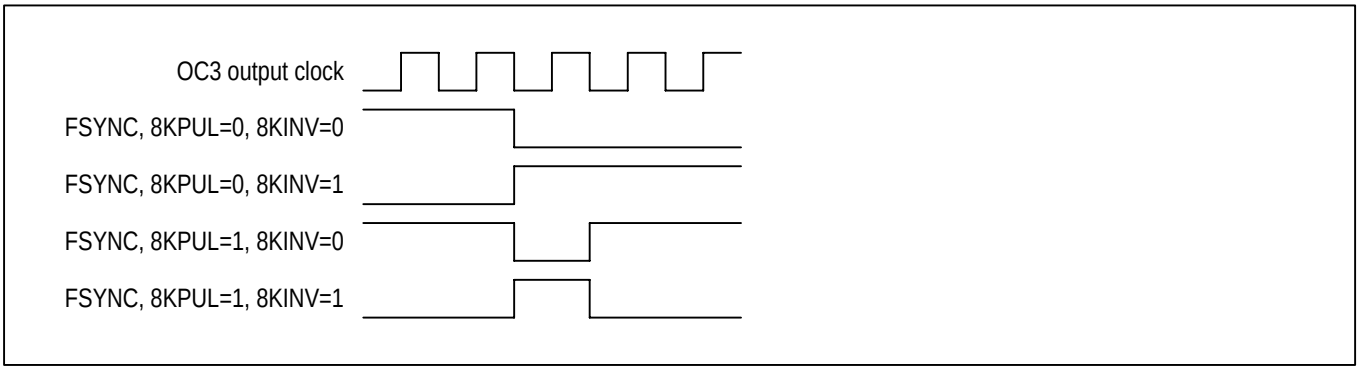
The FSYNC output is enabled by setting FSEN = 1 in the OCR4 register, while the MFSYNC output is enabled by setting MFSEN = 1 in OCR4. When disabled, these pins are driven low.

When 8KPUL = 0 in FSCR1, FSYNC is configured as an 8kHz clock with 50% duty cycle. When 8KPUL = 1, FSYNC is an 8kHz frame sync that pulses low once every 125µs with pulse width equal to one cycle of output clock OC3. When 8KINV = 1 in FSCR1, the clock or pulse polarity of FSYNC is inverted.

When 2KPUL = 0 in FSCR1, MFSYNC is configured as an 2kHz clock with 50% duty cycle. When 2KPUL = 1, MFSYNC is a 2kHz frame sync that pulses low once every 500µs with pulse width equal to one cycle of output clock OC3. When 2KINV = 1 in FSCR1, the clock or pulse polarity f MFSYNC is inverted.

If either 8KPUL = 1 or 2KPUL = 1, then output clock OC3 must be generated from the T0 DPLL and must be configured for a frequency of 1.544MHz or higher or the FSYNC/MFSYNC pulses may not be generated correctly. Figure 7-4 shows how the 8KPUL and 8KINV control bits affect the FSYNC output. The 2KPUL and 2KINV bits have an identical effect on MFSYNC.

Figure 7-4. FSYNC 8kHz Options



7.8.2.5 Custom Output Frequencies

In addition to the many standard frequencies available in the device, any of the seven output DFS blocks can be configured to generate a custom frequency. Possible custom frequencies include any multiple of 2kHz up to 77.76MHz and any multiple of 8kHz up to 311.04MHz. (An APLL must be used to achieve frequencies above 77.76MHz.) Any of the programmable output clocks can be configured to output the custom frequency or submultiples thereof. Contact the factory at telecom.support@dalsemi.com for help with custom frequencies.

7.9 Frame and Multiframe Alignment

In addition to receiving and locking to clocks such as 19.44MHz from system timing cards, the DS3104-SE can also receive and align its outputs to 2kHz multiframe sync or 8kHz frame sync signals from system timing cards. In this mode of operation, both a higher speed clock (such as 6.48MHz or 19.44MHz) and a frame (or multiframe) sync signal from each timing card are passed to the line cards. The higher speed clock from each timing card is connected to a regular input clock pin on the DS3104-SE, such as IC3 or IC4, while the frame sync signal is connected to a SYNCn input pin on the DS3104-SE, such as SYNC1 or SYNC2. The DS3104-SE locks to the higher speed clock from one of the timing cards and samples the frame sync signal on the associated SYNCn pin. The DS3104-SE then uses the SYNCn signal to falling-edge align some or all of the output clocks. Only the falling edge of the SYNCn signal has significance. A 4kHz or 8kHz clock can also be used on the SYNCn pins without any changes to the register configuration, but only output clocks of 8kHz and above are aligned in this case. Phase build-out should be disabled (PBOEN = 0 in MCR10) when using SYNCn signals.

When FSCR3.SOURCE! = 11XX, the frame sync signal can only come from the SYNC1 pin. When FSCR3.SOURCE = 11XX, the frame sync signal comes from one of SYNC1, SYNC2, or SYNC3. See Section 7.9.3.

7.9.1 Sampling

By default the SYNCn signal is first sampled on the rising edge of the selected reference. This gives the most margin, given that the SYNCn signal is falling-edge aligned with the selected reference since both come from the same timing card. The expected timing of the SYNCn signal with respect to the sampling clock can be adjusted from 0.5 cycles early to 1 cycle late using the FSCR2:PHASEn[1:0] field.

7.9.2 Resampling

The SYNCn signal is then resampled by an internal clock derived from the T0 DPLL. The resampling resolution is a function of the frequency of the selected reference and FSCR2:OCN. When OCN = 0, the resampling resolution is 6.48MHz, which gives the highest sampling margin and also aligns clocks at 6.48MHz and multiples thereof. When OCN = 1, if the selected reference is 19.44MHz the resampling resolution is 19.44MHz. If the selected reference is 38.88 MHz the resampling resolution is 38.88MHz. The selected reference must be either 19.44MHz or 38.88MHz.

7.9.3 Enable

The SYNCn signal is only allowed to align output clocks if the T0 DPLL is locked and the SYNCn signal is enabled and qualified.

When FSCR3:SOURCE[3:0]! = 11XX, external frame sync on the SYNC1 pin can be enabled automatically or manually. When MCR3:AEFSEN = 1, external frame sync is enabled automatically when EFSEN = 1 and the T0 DPLL is locked to the input clock specified by FSCR3:SOURCE[3:0]. When AEFSEN = 0, external frame sync is enabled manually when MCR3:EFSEN = 1 and disabled when EFSEN = 0. In manual mode when EFSEN = 1, FSCR3:SOURCE[3:0] is ignored and external frame sync is always enabled regardless of which input clock is the selected reference.

When FSCR3:SOURCE[3:0] = 11XX, external frame sync from the SYNCn pins can be enabled when EFSEN = 1 and the associated input clock becomes the selected reference. MCR3:AEFSEN can be used to automatically disable EFSEN when the selected reference changes. See Section 7.9.7.

7.9.4 Qualification

The SYNCn signal is qualified when it has consistent phase and correct frequency. Specifically, it is qualified when its significant edge has been found at exact 2kHz boundaries (when resampled as described above) for 64 cycles in a row. It is disqualified when one significant edge is not found at the 2kHz boundary. If there is no SYNCn signal or a bad SYNCn signal, and external frame sync is enabled, the SYNCn signal will never get qualified and the 2kHz output will simply free-run at its current 2kHz alignment.

7.9.5 Output Clock Alignment

When the T0 DPLL is locked, external frame sync is enabled and the SYNCn signal is qualified, the SYNCn signal can be used to falling-edge align the T0 DPLL derived output clocks. Output clocks FSYNC and MFSYNC share a 2kHz alignment generator, while the rest of the T0 DPLL derived output clocks share a second 2kHz alignment generator. When external frame sync is not enabled or the SYNCn signal is not qualified, these 2Hz alignment generators free-run with their existing 2kHz alignments. When external frame sync is enabled and the SYNCn signal is qualified, the FSYNC/MFSYNC 2kHz alignment generator is always synchronized by SYNCn, and therefore FSYNC and MFSYNC are always falling-edge aligned with SYNCn. When FSCR2:INDEP = 0, the T0 DPLL 2kHz alignment generator is also synchronized with the FSYNC/MFSYNC 2kHz alignment generator to falling-edge align all T0-derived output clocks with SYNCn. When INDEP = 1, the T0 DPLL 2-kHz alignment generator is not synchronized with the FSYNC/MFSYNC 2kHz alignment generator and continues to free-run with its existing 2kHz alignment. This avoids any disturbance on the T0 DPLL derived output clocks when SYNCn has a change of phase position.

7.9.6 Frame Sync Monitor

The frame sync monitor signal OPSTATE:FSMON operates in two modes, depending on the setting of the enable bit (MCR3:EFSEN).

When EFSEN = 1 (external frame sync enabled) the OPSTATE:FSMON bit is set when SYNCn is not qualified and cleared when SYNCn is qualified. If SYNCn is disqualified then both 2kHz alignment generators are immediately disconnected from SYNCn to avoid phase movement on the T0-derived outputs clocks. When OPSTATE:FSMON is set, the latched status bit MSR3:FSMON is also set, which can cause an interrupt if enabled in the IER3 register. If SYNCn immediately stabilizes at a new phase and proper frequency, then it is requalified after 64 2kHz cycles (nominally 32ms). Unless system software intervenes, after SYNCn is requalified the 2kHz alignment generators will synchronize with SYNCn's new phase alignment, causing a sudden phase movement on the output clocks. System software can avoid this sudden phase movement on the output clocks by responding to the FSMON interrupt within the 32ms window with appropriate action, which might include disabling external frame sync (MCR3:EFSEN = 0) to prevent the resynchronization of the 2kHz alignment generators with SYNCn, forcing the T0 DPLL into holdover (MCR1:T0STATE = 010) to avoid affecting the output clocks with any other phase hits, and possibly even disabling the master timing card and promoting the slave timing card to master since the 2kHz signal from the master should not have such phase movements.

When EFSEN = 0 (external frame sync disabled) OPSTATE:FSMON is set when the negative edge of the re-sampled SYNCn signal is outside of the window determined by FSCR3:MONLIM relative to the MFSYNC negative edge (or positive edge if MFSYNC is inverted) and clear when within the window. When OPSTATE:FSMON is set, the latched status bit MSR3:FSMON is also set, which can cause an interrupt if enabled in the IER3 register.

7.9.7 SYNCn Pins

The external frame sync signal can be automatically selected from one to three separate SYNC[1:3] pins depending on the setting of FSCR1:SYNCSRC[2:0] and which input clock is the T0 DPLL selected reference. If no associated input pin is selected as the T0 DPLL input reference, the internal SYNCn signal is inactive and will not be qualified. This function is enabled by setting FSCR3.SOURCE = 11XX.

Table 7-15. External Frame Sync Source

SYNCSRC[2:0]	SELECTED REFERENCE	EXTERNAL FRAME SYNC SOURCE
0XX	IC3 or IC5	SYNC1
	IC4 or IC6	SYNC2
	IC9 or IC2	SYNC3
1X0	IC3	SYNC1
	IC4	SYNC2
10X	IC9	SYNC3
1X1	IC5	SYNC1
	IC6	SYNC2
11X	IC2	SYNC3

There are three PHASEn[1:0] (n = 1, 2, 3) select fields in the FSCR2 register. PHASE1[1:0] is associated with SYNC1, PHASE2[1:0] is associated with SYNC2, and PHASE3[1:0] is associated with SYNC3. All three SYNCn inputs can have their timing adjusted to account for frame sync signal vs. clock signal delay differences in each path.

When this function is enabled with FSCR3.SOURCE = 11XX, MCR3.AEFSEN, and MCR3.EFSEN, the monitoring and qualification function described in Section 7.9.4 is only performed on the selected SYNCn input pin.

7.9.8 Other Configuration Options

FSYNC and MFSYNC are always produced from the T0 DPLL. Output clocks OC1 to OC7 can also be configured as 2kHz or 8kHz outputs, derived from either the T0 DPLL or the T4 DPLL (as specified by the 2K8KSRC bit in FSCR1). If needed, the T4 DPLL can be used as a separate DPLL for the frame sync path by configuring it for a 2kHz input and 2kHz and/or 8kHz frame sync outputs.

7.10 Microprocessor Interface

The device presents an SPI interface on the $\overline{CS}$, SCLK, SDI, and SDO pins. SPI is a widely used master/slave bus protocol that allows a master device and one or more slave devices to communicate over a serial bus. The DS3104-SE is always a slave device. Masters are typically microprocessors, ASICs or FPGAs. Data transfers are always initiated by the master device, which also generates the SCLK signal. The DS3104-SE receives serial data on the SDI pin and transmits serial data on the SDO pin. SDO is high impedance except when the DS3104-SE is transmitting data to the bus master.

Bit Order. When both bit 3 and bit 4 are low at device address 3FFFh, the register address and all data bytes are transmitted MSB first on both SDI and SDO. When either bit 3 or bit 4 is set to 1 at device address 3FFFh, the register address and all data bytes are transmitted LSB first on both SDI and SDO. The reset default setting and Motorola SPI convention is MSB first.

Clock Polarity and Phase. The CPOL pin defines the polarity of SCLK. When CPOL = 0, SCLK is normally low and pulses high during bus transactions. When CPOL = 1, SCLK is normally high and pulses low during bus transactions. The CPHA pin sets the phase (active edge) of SCLK. When CPHA = 0, data is latched in on SDI on the leading edge of the SCLK pulse and updated on SDO on the trailing edge. When CPHA = 1, data is latched in on SDI on the trailing edge of the SCLK pulse and updated on SDO on the following leading edge. SCLK does not have to toggle between access, i.e., when $\overline{CS}$ is high. See Figure 7-5.

Device Selection. Each SPI device has its own chip-select line. To select the DS3104-SE, pull its $\overline{CS}$ pin low.

Control Word. After $\overline{CS}$ is pulled low, the bus master transmits the control word during the first sixteen SCLK cycles. In MSB-first mode the control word has the form:

R/$\overline{W}$ A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0 BURST

where A[13:0] is the register address, R/$\overline{W}$ is the data direction bit (1 = read, 0 = write), and BURST is the burst bit (1 = burst access, 0 = single-byte access). In LSB-first mode the order of the 14 address bits is reversed. In the discussion that follows, a control word with R/$\overline{W}$ = 1 is a read control word, while a control word with R/$\overline{W}$ = 0 is a write control word.

Single-Byte Writes. See Figure 7-6. After $\overline{CS}$ goes low, the bus master transmits a write control word with BURST = 0 followed by the data byte to be written. The bus master then terminates the transaction by pulling $\overline{CS}$ high.

Single-Byte Reads. See Figure 7-6. After $\overline{CS}$ goes low, the bus master transmits a read control word with BURST = 0. The DS3104-SE then responds with the requested data byte. The bus master then terminates the transaction by pulling $\overline{CS}$ high.

Burst Writes. See Figure 7-6. After $\overline{CS}$ goes low, the bus master transmits a write control word with BURST = 1 followed by the first data byte to be written. The DS3104-SE receives the first data byte on SDI, writes it to the specified register, increments its internal address register, and prepares to receive the next data byte. If the master continues to transmit, the DS3104-SE continues to write the data received and increment its address counter. After the address counter reaches 3FFFh it rolls over to address 0000h and continues to increment.

Burst Reads. See Figure 7-6. After $\overline{CS}$ goes low, the bus master transmits a read control word with BURST = 1. The DS3104-SE then responds with the requested data byte on SDO, increments its address counter, and prefetches the next data byte. If the bus master continues to demand data, the DS3104-SE continues to provide the data on SDO, increment its address counter, and prefetch the following byte. After the address counter reaches 3FFFh it rolls over to address 0000h and continues to increment.

Early Termination of Bus Transactions. The bus master can terminate SPI bus transactions at any time by pulling $\overline{CS}$ high. In response to early terminations, the DS3104-SE resets its SPI interface logic and waits for the start of the next transaction. If a write transaction is terminated prior to the SCLK edge that latches the LSB of a data byte, the data byte is not written.

Design Option: Wiring SDI and SDO Together. Because communication between the bus master and the DS3104-SE is half-duplex, the SDI and SDO pins can be wired together externally to reduce wire count. To support this option, the bus master must not drive the SDI/SDO line when the DS3104-SE is transmitting.

AC Timing. See Table 10-10 and Figure 10-4 for AC timing specifications for the SPI interface.

Figure 7-5. SPI Clock Phase Options

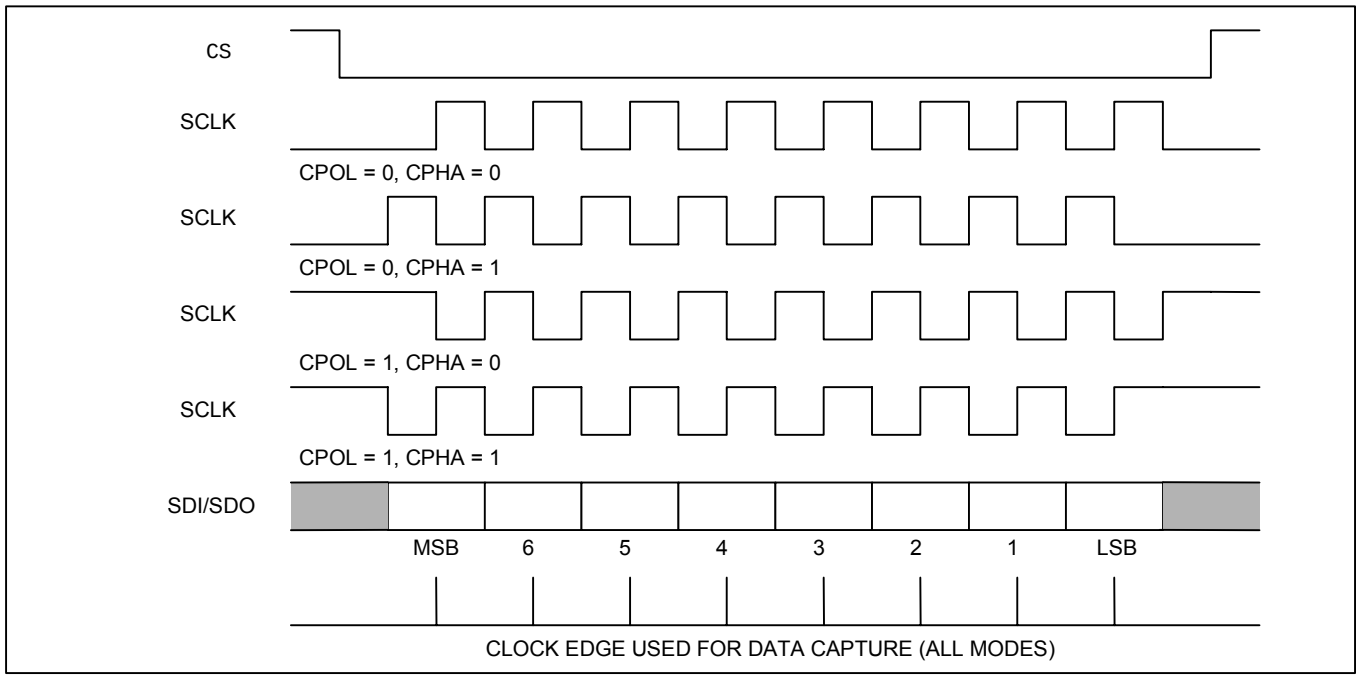
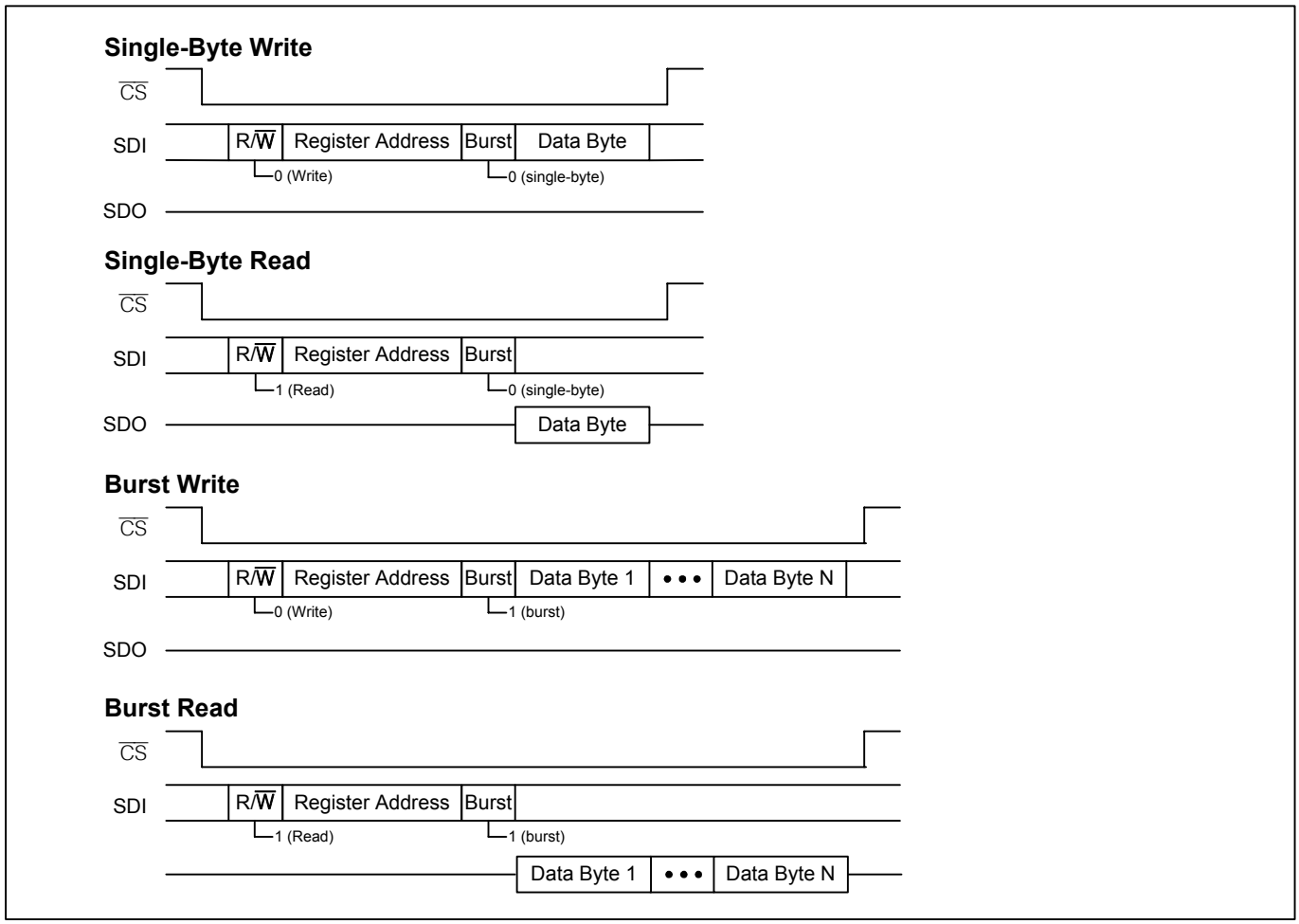


Figure 7-6. SPI Bus Transactions



7.11 Reset Logic

The device has three reset controls: the $\overline{RST}$ pin, the RST bit in MCR1, and the JTAG reset pin $\overline{JTRST}$. The $\overline{RST}$ pin asynchronously resets the entire device, except for the JTAG logic. When the $\overline{RST}$ pin is low all internal registers are reset to their default values, including those fields which latch their default values from, or based on, the states of configuration input pins when the $\overline{RST}$ goes high. **The $\overline{RST}$ pin must be asserted once after power-up while the external oscillator is stabilizing.**

The MCR1:RST bit resets the entire device (except for the microprocessor interface, the JTAG logic, and the RST bit itself), but when RST is active, the register fields with pin-programmed defaults do not latch their values from, or based on, the corresponding input pins. Instead these fields are reset to the default values that were latched when the $\overline{RST}$ pin was last active.

Maxim recommends holding $\overline{RST}$ low while the external oscillator starts up and stabilizes. An incorrect reset condition could result if $\overline{RST}$ is released before the oscillator has started up completely.

Important: System software must wait at least 100µs after reset ($\overline{RST}$ pin or RST bit) is deasserted before initializing the device as described in Section 7.13.

7.12 Power-Supply Considerations

Due to the dual-power-supply nature of the DS3104-SE, some I/Os have parasitic diodes between a 1.8V supply and a 3.3V supply. When ramping power supplies up or down, care must be taken to avoid forward-biasing these diodes because it could cause latchup. Two methods are available to prevent this. The first method is to place a Schottky diode external to the device between the 1.8V supply and the 3.3V supply to force the 3.3V supply to be less than one parasitic diode drop below the 1.8V supply. The second method is to ramp up the 3.3V supply first and then ramp up the 1.8V supply.

7.13 Initialization

After power-up or reset, a series of writes must be done to the DS3104-SE to tune it for optimal performance. This series of writes is called the initialization script. Each die revision of the DS3104-SE has a different initialization script. Download the latest initialization scripts from the DS3104-SE web page at www.maxim-ic.com/DS3104-SE, or email telecom.support@dalsemi.com.

8. Register Descriptions

The DS3104-SE has an overall address range from 000h to 1FFh. Table 8-1 in Section 8.4 shows the register map. In each register, bit 7 is the MSB and bit 0 is the LSB. Register addresses not listed and bits marked "—" are reserved and must be written with 0. Writing other values to these registers may put the device in a factory test mode resulting in undefined operation. Bits labeled "0" or "1" must be written with that value for proper operation. Register fields with underlined names are read-only fields; writes to these fields have no effect. All other fields are read-write. Register fields are described in detail in the register descriptions that follow Table 8-1.

8.1 Status Bits

The device has two types of status bits. Real-time status bits are read-only and indicate the state of a signal at the time it is read. Latched status bits are set when a signal changes state (low-to-high, high-to-low, or both, depending on the bit) and cleared when written with a logic 1 value. Writing a 0 has no effect. When set, some latched status bits can cause an interrupt request on the INTREQ pin if enabled to do so by corresponding interrupt enable bits. ISR#.LOCK# are special-case latched status bits because they cannot create an interrupt request on the INTREQ pin and a "write 0" is needed to clear them.

8.2 Configuration Fields

Configuration fields are read-write. During reset, each configuration field reverts to the default value shown in the register definition. Configuration register bits marked "—" are reserved and must be written with 0.

8.3 Multiregister Fields

Multiregister fields—such as FREQ[18:0] in registers FREQ1, FREQ2 and FREQ3—must be handled carefully to ensure that the bytes of the field remain consistent. A write access to a multiregister field is accomplished by writing all the registers of the field in any order, with no other accesses to the device in between. If the write sequence is interrupted by another access, none of the bytes are written and the MSR4:MRAA latched status bit is set to indicate the write was aborted. A read access from a multiregister field is accomplished by reading the registers of the field in any order, with no other accesses to the device in between. When one register of a multiregister field is read, the other register(s) in the field are frozen until after they are all read. If the read sequence is interrupted by another access, the registers of the multibyte field are unfrozen and the MSR4:MRAA bit is set to indicate the read was aborted. For best results, interrupt servicing should be disabled in the microprocessor before a multiregister access and then enabled again after the access is complete. The multiregister fields are:

FIELD	REGISTERS	ADDRESSES	TYPE
FREQ[18:0]	FREQ1, FREQ2, FREQ3	07, 0C, 0D	Read-Only
MCLKFREQ[15:0]	MCLK1, MCLK2	3C, 3D	Read/Write
HARDLIM[9:0]	DLIMIT1, DLIMIT2	41, 42	Read/Write
DIVN[15:0]	DIVN1, DIVN2	46, 47	Read/Write
OFFSET[15:0]	OFFSET1, OFFSET2	70, 71	Read/Write
PHASE[15:0]	PHASE1, PHASE2	77, 78	Read-Only

8.4 Register Definitions

Table 8-1. Register Map

Note: *Register names are hyperlinks to register definitions. Underlined fields are read-only.*

ADDR	REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
00h	ID1	ID[7:0]							
01	ID2	ID[15:8]							
02	REV	REV[7:0]							
03	TEST1	PALARM	D180	—	RA	0	8KPOL	0	0
05	MSR1	IC8	—	IC6	IC5	IC4	IC3	IC2	IC1
06	MSR2	STATE	SRFAIL	—	—	—	—	—	IC9
07	FREQ3	—	—	—	—	—	FREQ[18:16]		
08	MSR3	FSMON	T4LOCK	—	T4NOIN	—	—	—	—
09	OPSTATE	FSMON	T4LOCK	T0SOFT	T4SOFT	—	T0STATE[2:0]		
0A	PTAB1	REF1[3:0]				SELREF[3:0]			
0B	PTAB2	REF3[3:0]				REF2[3:0]			
0C	FREQ1	FREQ[7:0]							
0D	FREQ2	FREQ[15:8]							
0E	VALSR1	IC8	—	IC6	IC5	IC4	IC3	IC2	IC1
0F	VALSR2	—	HORDY	—	—	—	—	—	IC9
10	ISR1	—	—	ACT2	LOCK2	—	—	ACT1	LOCK1
11	ISR2	—	—	ACT4	LOCK4	—	—	ACT3	LOCK3
12	ISR3	—	—	ACT6	LOCK6	—	—	ACT5	LOCK5
13	ISR4	—	—	ACT8	LOCK8	—	—	—	—
14	ISR5	—	—	—	—	—	—	ACT9	LOCK9
17	MSR4	—	HORDY	MRAA	—	—	—	—	—
18	IPR1	PRI2[3:0]				PRI1[3:0]			
19	IPR2	PRI4[3:0]				PRI3[3:0]			
1A	IPR3	PRI6[3:0]				PRI5[3:0]			
1B	IPR4	PRI8[3:0]				—			
1C	IPR5	—				PRI9[3:0]			
20	ICR1	DIVN	LOCK8K	BUCKET[1:0]		FREQ[3:0]			
21	ICR2	DIVN	LOCK8K	BUCKET[1:0]		FREQ[3:0]			
22	ICR3	DIVN	LOCK8K	BUCKET[1:0]		FREQ[3:0]			
23	ICR4	DIVN	LOCK8K	BUCKET[1:0]		FREQ[3:0]			
24	ICR5	DIVN	LOCK8K	BUCKET[1:0]		FREQ[3:0]			
25	ICR6	DIVN	LOCK8K	BUCKET[1:0]		FREQ[3:0]			
27	ICR8	DIVN	LOCK8K	BUCKET[1:0]		FREQ[3:0]			
28	ICR9	DIVN	LOCK8K	BUCKET[1:0]		FREQ[3:0]			
30	VALCR1	IC8	—	IC6	IC5	IC4	IC3	IC2	IC1
31	VALCR2	—	—	—	—	—	—	—	IC9
32	MCR1	RST	—	FREN	LOCKPIN	—	T0STATE[2:0]		
33	MCR2	—	—	—	—	T0FORCE[3:0]			
34	MCR3	AEFSEN	LKATO	XOEDGE	MANHO	EFSEN	SONSDH	—	REVERT
35	MCR4	LKT4T0	—	—	—	T4FORCE[3:0]			
36	MCR5	RSV4	RSV3	RSV2	RSV1	IC2SF	IC1SF	IC6SF	IC5SF
37	OCR6	—	OC5EN	OC4EN	OC5BEN	OC4BEN	OC3BEN	OC2BEN	OC1BEN
38	MCR6	DIG2AF	DIG2SS	DIG1SS	—	—	—	—	—
39	MCR7	DIG2F[1:0]		DIG1F[1:0]		—	—	DIG2SRC	DIG1SRC

ADDR	REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3A	MCR8	OC5SF		OC4SF		OC7SF		OC6SF	
3B	MCR9	AUTOBW	—	—	—	LIMINT	—	—	—
3C	MCLK1	MCLKFREQ[7:0]							
3D	MCLK2	MCLKFREQ[15:8]							
40	HOCR3	AVG	—	—	—		—		
41	DLIMIT1	HARDLIM[7:0]							
42	DLIMIT2	—	—	—	—	—	—	HARDLIM[9:8]	
43	IER1	IC8	—	IC6	IC5	IC4	IC3	IC2	IC1
44	IER2	STATE	SRFAIL	—	—	—	—	—	IC9
45	IER3	FSMON	T4LOCK	—	T4NOIN	—	—	—	—
46	DIVN1	DIVN[7:0]							
47	DIVN2	DIVN[15:0]							
48	MCR10	—	SRFPIN	UFSW	EXTSW	PBOFRZ	PBOEN	—	—
4B	MCR11	—	—	—	T4T0	—	—	—	—
4D	DLIMIT3	FLLOL	SOFTLIM[6:0]						
4E	IER4	—	HORDY	—	—	—	—	—	—
4F	OCR5	—	AOF7	AOF6	AOF5	AOF4	AOF3	AOF2	AOF1
50	LB0U	LB0U[7:0]							
51	LB0L	LB0L[7:0]							
52	LB0S	LB0S[7:0]							
53	LB0D	—	—	—	—	—	—	LB0D[1:0]	
54	LB1U	LB1U[7:0]							
55	LB1L	LB1L[7:0]							
56	LB1S	LB1S[7:0]							
57	LB1D	—	—	—	—	—	—	LB1D[1:0]	
58	LB2U	LB2U[7:0]							
59	LB2L	LB2L[7:0]							
5A	LB2S	LB2S[7:0]							
5B	LB2D	—	—	—	—	—	—	LB2D[1:0]	
5C	LB3U	LB3U[7:0]							
5D	LB3L	LB3L[7:0]							
5E	LB3S	LB3S[7:0]							
5F	LB3D	—	—	—	—	—	—	LB3D[1:0]	
60	OCR1	OFREQ2[3:0]				OFREQ1[3:0]			
61	OCR2	OFREQ4[3:0]				OFREQ3[3:0]			
62	OCR3	OFREQ6[3:0]				OFREQ5[3:0]			
63	OCR4	MFSEN	FSEN	—	—	OFREQ7[3:0]			
64	T4CR1	—	—	—	—	T4FREQ[3:0]			
65	T0CR1	T4MT0	T4APT0	T0FT4[2:0]			T0FREQ[2:0]		
66	T4BW	—	—	—	—	—	—	T4BW[1:0]	
67	T0LBW	—	—	—	RSV1	T0LBW[3:0]			
69	T0ABW	—	—	—	RSV1	T0ABW[3:0]			
6A	T4CR2	—	PD2G8K[2:0]			—	DAMP[2:0]		
6B	T0CR2	—	PD2G8K[2:0]			—	DAMP[2:0]		
6C	T4CR3	PD2EN	—				PD2G[2:0]		
6D	T0CR3	PD2EN	—				PD2G[2:0]		
6E	GPCR	GPIO4D	GPIO3D	GPIO2D	GPIO1D	GPIO4O	GPIO3O	GPIO2O	GPIO1O
6F	GPSR	—	—	—	—	GPIO4	GPIO3	GPIO2	GPIO1
70	OFFSET1	OFFSET[7:0]							
71	OFFSET2	OFFSET[15:8]							

ADDR	REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
72	PBOFF	—	—	PBOFF[5:0]					
73	PHLIM1	FLEN	NALOL	1	—	—	FINELIM[2:0]		
74	PHLIM2	CLEN	MCPDEN	USEMCPD	—	COARSELIM[3:0]			
76	PHMON	NW	—	—	—	—			
77	PHASE1	PHASE[7:0]							
78	PHASE2	PHASE[15:8]							
79	PHLKTO	PHLKTOM[1:0]		PHLKTO[5:0]					
7A	FSCR1	2K8KSRC	SYNCSRC			8KINV	8KPUL	2KINV	2KPUL
7B	FSCR2	INDEP	OCN	PHASE3[1:0]		PHASE2[1:0]		PHASE1[1:0]	
7C	FSCR3	RECAL	MONLIM[2:0]			SOURCE[3:0]			
7D	INTCR	—	—	—	—	LOS	GPO	OD	POL
7E	PROT	PROT[7:0]							

Register Map Color Coding

	Device Identification and Protection
	Local Oscillator and Master Clock Configuration
	Input Clock Configuration
	Input Clock Monitoring
	Input Clock Selection
	DPLL Configuration
	DPLL State
	Output Clock Configuration
	Frame/Multiframe Sync Configuration

Register Name: **ID1**
Register Description: **Device Identification Register, LSB**
Register Address: **00h**

Bit #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	ID[7:0]							
Default	0	0	1	0	0	0	0	0

Bits 7 to 0: Device ID (ID[7:0]). ID[15:0] = 0C20h = 3104 decimal.

Register Name: **ID2**
Register Description: **Device Identification Register, MSB**
Register Address: **01h**

Bit #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	ID[15:8]							
Default	0	0	0	0	1	1	0	0

Bits 7 to 0: Device ID (ID[15:8]). See the ID1 register description.

Register Name: **REV**
Register Description: **Device Revision Register**
Register Address: **02h**

Bit #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	REV[7:0]							
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: Device Revision (REV[7:0]). Contact the factory to interpret this value and determine the latest revision.

Register Name: **TEST1**
Register Description: **Test Register 1 (Not Normally Used)**
Register Address: **03h**

Bit #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	PALARM	D180	—	RA	0	8KPOL	0	0
Default	0	0	0	1	0	1	0	0

Bit 7: Phase Alarm (PALARM). This real-time status bit indicates the state of the T0 DPLL phase lock detector. See Section 7.7.6. (**Note:** This is not the same as T0STATE = Locked.)

0 = T0 DPLL phase-lock parameters are met (FLEN, CLEN, NALOL, FLLOL)
1 = T0 DPLL loss of phase lock

Bit 6: Disable 180 (D180). When locking to a new reference, the T0 DPLL first tries nearest-edge locking (±180°) for the first two seconds. If unsuccessful it then tries full phase/frequency locking (±360°). Disabling the nearest-edge locking can reduce lock time by up to two seconds but may cause an unnecessary phase shift (up to 360°) when the new reference is close in frequency/phase to the old reference. See Section 7.7.5.

0 = normal operation: try nearest-edge locking then phase/frequency locking
1 = phase/frequency locking only

Bit 4: Resync Analog Dividers (RA). When this bit is set the analog output dividers are always synchronized to ensure that low-frequency outputs are in sync with the higher frequency clock from the DPLL.

0 = synchronized for the first two seconds after power-up
1 = always synchronized

Bits 3, 1, and 0: Leave set to zero (test control).

Bit 2: 8kHz Edge Polarity (8KPOL). Specifies the input clock edge to lock to on the selected reference when it is configured for LOCK8K mode. See Section 7.4.2.

0 = Falling edge
1 = Rising edge

Register Name: **MSR1**
Register Description: **Master Status Register 1**
Register Address: **05h**

Bit #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	IC8	—	IC6	IC5	IC4	IC3	IC2	IC1
Default	1	0	1	1	1	1	1	1

Bits 7 and 5 to 0: Input Clock Status Change (IC8 and IC[6:1]). Each of these latched status bits is set to 1 when the corresponding VALSR1 status bit changes state (set or cleared). Each bit is cleared when written with a 1 and not set again until the VALSR1 bit changes state again. When one of these latched status bits is set it can cause an interrupt request on the INTREQ pin if the corresponding interrupt enable bit is set in the IER1 register. See Section 7.5 for input clock validation/invalidation criteria.

Register Name: **MSR2**
Register Description: **Master Status Register 2**
Register Address: **06h**

Bit #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	STATE	SRFAIL	—	—	—	—	—	IC9
Default	0	0	0	0	0	0	0	1

Bit 7: T0 DPLL State Change (STATE). This latched status bit is set to 1 when the operating state of the T0 DPLL changes. STATE is cleared when written with a 1 and not set again until the operating state changes again. When STATE is set it can cause an interrupt request on the INTREQ pin if the STATE interrupt enable bit is set in the IER2 register. The current operating state can be read from the T0STATE field of the OPSTATE register. See Section 7.7.1.

Bit 6: Selected Reference Failed (SRFAIL). This latched status bit is set to 1 when the selected reference to the T0 DPLL fails, (i.e., no clock edges in two UI). SRFAIL is cleared when written with a 1. When SRFAIL is set it can cause an interrupt request on the INTREQ pin if the SRFAIL interrupt enable bit is set in the IER2 register. SRFAIL is not set in free-run mode or holdover mode. See Section 7.5.3.

Bit 0: Input Clock Status Change (IC9). This latched status bit is set to 1 when the corresponding VALSR status bit changes state (set or cleared). Each bit is cleared when written with a 1 and not set again until the VALSR2 bit changes state again. When this latched status bit is set it can cause an interrupt request on the INTREQ pin if the corresponding interrupt enable bit is set in the IER2 register. See Section 7.5 for input clock validation/invalidation criteria.

Register Name: **FREQ3**
Register Description: **Frequency Register 3**
Register Address: **07h**

Bit #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	—	—	—	—	FREQ[18:16]		
Default	0	0	0	0	0	0	0	0

Bits 2 to 0: Current DPLL Frequency (FREQ[18:16]). See the FREQ1 register description.

Register Name: **MSR3**
Register Description: **Master Status Register 3**
Register Address: **08h**

Bit #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	FSMON	T4LOCK	—	T4NOIN	—	—	—	—
Default	0	1	0	1	0	0	0	0

Bit 7: Frame Sync Input Monitor Alarm (FSMON). This latched status bit is set to 1 when OPSTATE:FSMON transitions from 0 to 1. FSMON is cleared when written with a 1. When FSMON is set it can cause an interrupt request on the INTREQ pin if the FSMON interrupt enable bit is set in the IER3 register. See Section 7.9.

Bit 6: T4 DPLL Lock Status Change (T4LOCK). This latched status bit is set to 1 when the lock status of the T4 DPLL (OPSTATE:T4LOCK) changes (becomes locked when previously unlocked or becomes unlocked when previously locked). T4LOCK is cleared when written with a 1 and not set again until the T4 lock status changes again. When T4LOCK is set it can cause an interrupt request on the INTREQ pin if the T4LOCK interrupt enable bit is set in the IER3 register. See Section 7.7.6.

Bit 4: T4 No Valid Inputs Alarm (T4NOIN). This latched status bit is set to 1 when the T4 DPLL has no valid inputs available. T4NOIN is cleared when written with a 1 unless the T4 DPLL still has no valid inputs available. When T4NOIN is set it can cause an interrupt request on the INTREQ pin if the T4NOIN interrupt enable bit is set in the IER3 register. See Section 7.5.

Register Name: **OPSTATE**
Register Description: **Operating State Register**
Register Address: **09h**

Bit #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	FSMON	T4LOCK	T0SOFT	T4SOFT	—	T0STATE[2:0]		
Default	1	0	0	0	0	0	0	1

Bit 7: Frame Sync Input Monitor Alarm (FSMON). This real-time status bit indicates the current status of the frame sync input monitor. See Section 7.9.6.

0 = no alarm
1 = alarm

Bit 6: T4 DPLL Lock Status (T4LOCK). This real-time status bit indicates the current phase lock status of the T4 DPLL. See Sections 7.5.3 and 7.7.6.

0 = not locked to selected reference
1 = locked to selected reference

Bit 5: T0 DPLL Frequency Soft Alarm (T0SOFT). This real-time status bit indicates whether or not the T0 DPLL is tracking its reference within the soft alarm limits specified in the SOFT[6:0] field of the DLIMIT3 register. See Section 7.7.6.

0 = No alarm; frequency is within the soft alarm limits
1 = Soft alarm; frequency is outside the soft alarm limits

Bit 4: T4 DPLL Frequency Soft Alarm (T4SOFT). This real-time status bit indicates whether or not the T4 DPLL is tracking its reference within the soft alarm limits specified in the SOFT[6:0] field of the DLIMIT3 register. See Section 7.7.6.

0 = No alarm; frequency is within the soft alarm limits
1 = Soft alarm; frequency is outside the soft alarm limits

Bits 2 to 0: T0 DPLL Operating State (T0STATE[2:0]). This real-time status field indicates the current state of the T0 DPLL state machine. Values not listed below correspond to invalid (unused) states. See Section 7.7.1.

001 = Free-run
010 = Holdover
100 = Locked
101 = Prelocked 2
110 = Prelocked
111 = Loss-of-lock

Register Name: **PTAB1**
Register Description: **Priority Table Register 1**
Register Address: **0Ah**

Bit #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	REF1[3:0]				SELREF[3:0]			
Default	0	0	0	0	0	0	0	0

Bits 7 to 4: Highest Priority Valid Reference (REF1[3:0]). This real-time status field indicates the highest-priority valid input reference. When T4T0 = 0 in the MCR11 register, this field indicates the highest priority reference for the T0 DPLL. When T4T0 = 1, it indicates the highest priority reference for the T4 DPLL. Note that an input reference cannot be indicated in this field if it has been marked invalid in the VALCR1 or VALCR2 register. When the T0 DPLL is in nonrevertive mode (REVERT = 0 in the MCR3 register) this field may not have the same value as the SELREF[3:0] field. See Section 7.6.2.

0000 = No valid input reference available
0001 = Input IC1
0010 = Input IC2
0011 = Input IC3
0100 = Input IC4
0101 = Input IC5
0110 = Input IC6
0111 = {unused value}
1000 = Input IC8
1001 = Input IC9
1010 to 1111 = {unused values}

Bits 3 to 0: Selected Reference (SELREF[3:0]). This real-time status field indicates the current selected reference. When T4T0 = 0 in the MCR11 register, this field indicates the selected reference for the T0 DPLL. When T4T0 = 1, it indicates the selected reference for the T4 DPLL. Note that an input clock cannot be indicated in this field if it has been marked invalid in the VALCR1 or VALCR2 register. When the T0 DPLL is in nonrevertive mode (REVERT = 0 in the MCR3 register) this field may not have the same value as the REF1[3:0] field. See Section 7.6.2.

0000 = No source currently selected
0001 = Input IC1
0010 = Input IC2
0011 = Input IC3
0100 = Input IC4
0101 = Input IC5
0110 = Input IC6
0111 = {unused value}
1000 = Input IC8
1001 = Input IC9
1010 to 1111 = {unused values}

Register Name: **PTAB2**
Register Description: **Priority Table Register 2**
Register Address: **0Bh**

Bit #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	REF3[3:0]				REF2[3:0]			
Default	0	0	0	0	0	0	0	0

Bits 7 to 4: Third Highest Priority Valid Reference (REF3[3:0]). This real-time status field indicates the third highest priority validated input reference. When T4T0 = 0 in the MCR11 register, this field indicates the third highest priority reference for the T0 DPLL. When T4T0 = 1, it indicates the third highest reference for the T4 DPLL. Note that an input reference cannot be indicated in this field if it has been marked invalid in the VALCR1 or VALCR2 register. See Section 7.6.2.

0000 = Less than three valid sources available
0001 = Input IC1
0010 = Input IC2
0011 = Input IC3
0100 = Input IC4
0101 = Input IC5
0110 = Input IC6
0111 = {unused value}
1000 = Input IC8
1001 = Input IC9
1010 to 1111 = {unused values}

Bits 3 to 0: Second Highest Priority Valid Reference (REF2[3:0]). This real-time status field indicates the second highest priority validated input reference. When T4T0 = 0 in the MCR11 register, this field indicates the second highest priority reference for the T0 DPLL. When T4T0 = 1, it indicates the second highest reference for the T4 DPLL. Note that an input reference cannot be indicated in this field if it has been marked invalid in the VALCR1 or VALCR2 register. See Section 7.6.2.

0000 = Less than two valid sources available
0001 = Input IC1
0010 = Input IC2
0011 = Input IC3
0100 = Input IC4
0101 = Input IC5
0110 = Input IC6
0111 = {unused value}
1000 = Input IC8
1001 = Input IC9
1010 to 1111 = {unused values}

Register Name: **FREQ1**
Register Description: **Frequency Register 1**
Register Address: **0Ch**

Bit #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	FREQ[7:0]							
Default	0	0	0	0	0	0	0	0

Note: *The FREQ1, FREQ2, and FREQ3 registers must be read consecutively. See Section 8.3.*

Bits 7 to 0: Current DPLL Frequency (FREQ[7:0]). The full 19-bit FREQ[18:0] field spans this register, FREQ2 and FREQ3. FREQ is a two's-complement signed integer that expresses the current frequency as an offset with respect to the master clock frequency (see Section 7.3). When T4T0 = 0 in the MCR11 register, FREQ indicates the current frequency offset of the T0 DPLL. When T4T0 = 1, FREQ indicates the current frequency offset of the T4 path. Because the value in this register field is derived from the DPLL integral path, it can be considered an average frequency with a rate of change inversely proportional to the DPLL bandwidth. If LIMINT = 1 in the MCR9 register, the value of FREQ freezes when the DPLL reaches its minimum or maximum frequency. The frequency offset in ppm is equal to FREQ[18:0] x 0.0003068. See Section 7.7.1.6.

Application Note: Frequency measurements are relative, i.e., they measure the frequency of the selected reference with respect to the local oscillator. As such, when a frequency difference exists, it is difficult to distinguish whether the selected reference is off frequency or the local oscillator is off frequency. In systems with timing card redundancy, the use of two timing cards, master and slave, can address this difficulty. Both master and slave have separate local oscillators, and each measures the selected reference. These two measurements provide the necessary information to distinguish which reference is off frequency, if we make the simple assumption that at most one reference has a significant frequency deviation at any given time (i.e., a single point of failure). If both master and slave indicate a significant frequency offset, then the selected reference must be off frequency. If the master indicates a frequency offset but the slave does not, then the master's local oscillator must be off frequency. Likewise, if the slave indicates a frequency offset but the master does not, then slave's local oscillator must be off frequency.

Register Name: **FREQ2**
Register Description: **Frequency Register 2**
Register Address: **0Dh**

Bit #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	FREQ[15:8]							
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: Current DPLL Frequency (FREQ[15:8]). See the FREQ1 register description.

Register Name: **VALSR1**
Register Description: **Input Clock Valid Status Register 1**
Register Address: **0Eh**

Bit #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	IC8	—	IC6	IC5	IC4	IC3	IC2	IC1
Default	0	0	0	0	0	0	0	0

Bits 7 and 5 to 0: Input Clock Valid Status (IC8 and IC[6:1]). Each of these real-time status bits is set to 1 when the corresponding input clock is valid. An input is valid if it has no active alarms (ACT = 0, LOCK = 0 in the corresponding ISR register). See also the MSR1 register and Section 7.5.

0 = Invalid
1 = Valid

Register Name: **VALSR2**
Register Description: **Input Clock Valid Status Register 2**
Register Address: **0Fh**

Bit #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	HORDY	—	—	—	—	—	IC9
Default	0	0	0	0	0	0	0	0

Bit 6: Holdover Frequency Ready (HORDY). This real-time status bit is set to 1 when the T0 DPLL has a holdover value that has been averaged over the one-second holdover averaging period. See the related latched status bit in MSR4 and Section 7.7.1.6.

Bit 0: Input Clock Valid Status (IC9). This bit has the same behavior as the bits in VALSR1 but for the IC9 clock.

Register Name: **ISR1**
Register Description: **Input Status Register 1**
Register Address: **10h**

Bit #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	—	ACT2	LOCK2	—	—	ACT1	LOCK1
Default	0	0	1	0	0	0	1	0

Bit 5: Activity Alarm for Input Clock 2 (ACT2). This real-time status bit is set to 1 when the leaky bucket accumulator for IC2 reaches the alarm threshold specified in the LBxU register (where 'x' in 'LBxU' is specified in the BUCKET field of ICR1). An activity alarm clears the IC2 status bit in the VALSR1 register, invalidating the IC2 clock. See Section 7.5.2.

Bit 4: Phase Lock Alarm for Input Clock 2 (LOCK2). This status bit is set to 1 if IC2 is the selected reference and the T0 DPLL cannot phase lock to IC2 within the duration specified in the PHLKTO register (default = 100 seconds). A phase lock alarm clears the IC2 status bit in VALSR1, invalidating the IC2 clock. If LKATO = 1 in MCR3 then LOCK2 is automatically cleared after a timeout period of 128 seconds. LOCK2 is a read/write bit. System software can clear LOCK4 by writing 0 to it, but writing 1 is ignored. See Section 7.7.1.

Bit 1: Activity Alarm for Input Clock 1 (ACT1). This bit has the same behavior as the ACT2 bit but for the IC1 input clock.

Bit 0: Phase Lock Alarm for Input Clock 1 (LOCK1). This bit has the same behavior as the LOCK2 bit but for the IC1 input clock.

Register Name: **ISR2**
Register Description: **Input Status Register 2**
Register Address: **11h**

Bit #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	—	ACT4	LOCK4	—	—	ACT3	LOCK3
Default	0	0	1	0	0	0	1	0

Bit 5: Activity Alarm for Input Clock 4 (ACT4). This real-time status bit is set to 1 when the leaky bucket accumulator for IC4 reaches the alarm threshold specified in the LBxU register (where 'x' in 'LBxU' is specified in the BUCKET field of ICR4). An activity alarm clears the IC4 status bit in the VALSR1 register, invalidating the IC4 clock. See Section 7.5.2.

Bit 4: Phase Lock Alarm for Input Clock 4 (LOCK4). This status bit is set to 1 if IC4 is the selected reference and the T0 DPLL cannot phase lock to IC4 within the duration specified in the PHLKTO register (default = 100 seconds). A phase lock alarm clears the IC4 status bit in VALSR1, invalidating the IC4 clock. If LKATO = 1 in MCR3 then LOCK4 is automatically cleared after a timeout period of 128 seconds. LOCK4 is a read/write bit. System software can clear LOCK4 by writing 0 to it, but writing 1 is ignored. See Section 7.7.1.

Bit 1: Activity Alarm for Input Clock 3 (ACT3). This bit has the same behavior as the ACT4 bit but for the IC3 input clock.

Bit 0: Phase Lock Alarm for Input Clock 3 (LOCK3). This bit has the same behavior as the LOCK4 bit but for the IC3 input clock.

Register Name: **ISR3**
Register Description: **Input Status Register 3**
Register Address: **12h**

Bit #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	—	ACT6	LOCK6	—	—	ACT5	LOCK5
Default	0	0	1	0	0	0	1	0

This register has the same behavior as the ISR1and ISR2 registers, but for input clocks IC5 and IC6.

Register Name: **ISR4**
Register Description: **Input Status Register 4**
Register Address: **13h**

Bit #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	—	ACT8	LOCK8	—	—	—	—
Default	0	0	1	0	0	0	0	0

This register has the same behavior as the ISR1and ISR2 registers, but for input clock IC8.

Register Name: **ISR5**
Register Description: **Input Status Register 5**
Register Address: **14h**

Bit #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	—	—	—	—	—	ACT9	LOCK9
Default	0	0	0	0	0	0	1	0

This register has the same behavior as the ISR1and ISR2 registers, but for input clock IC9.

Register Name: **MSR4**
Register Description: **Master Status Register 4**
Register Address: **17h**

Bit #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	HORDY	MRAA	—	—	—	—	—
Default	0	0	0	0	0	0	0	0

Bit 6: Holdover Frequency Ready (HORDY). This latched status bit is set to 1 when the T0 DPLL has a holdover value that has been averaged over the 1-second holdover averaging period. HORDY is cleared when written with a 1. When HORDY is set it can cause an interrupt request on the INTREQ pin if the HORDY interrupt enable bit is set in the IER4 register. See Section 7.7.1.6.

Bit 5: Multiregister Access Aborted (MRAA). This latched status bit is set to 1 when a multibyte access (read or write) is interrupted by another access to the device. MRAA is cleared when written with a 1. MRAA cannot cause an interrupt to occur. See Section 8.3.

Register Name: **IPR1**
Register Description: **Input Priority Register 1**
Register Address: **18h**

Bit #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	PRI2[3:0]				PRI1[3:0]			
Default (T0)	0	0	0	1	0	0	0	0
Default (T4)	0	0	0	1	0	0	0	0

Bits 7 to 4: Priority for Input Clock 2 (PRI2[3:0]). Priority 0001 is highest; priority 1111 is lowest. When MCR11:T4T0 = 0, PRI2 configures IC2's priority for the T0 DPLL. When T4T0 = 1, PRI2 configures IC2's priority for the T4 path. See Section 7.6.1.

0000 = IC2 unavailable for selection.
0001–1111= IC2 relative priority

Bits 3 to 0: Priority for Input Clock 1 (PRI1[3:0]). Priority 0001 is highest; priority 1111 is lowest. When MCR11:T4T0 = 0, PRI1 configures IC1's priority for the T0 DPLL. When T4T0 = 1, PRI1 configures IC1's priority for the T4 path. See Section 7.6.1.

0000 = IC1 unavailable for selection.
0001–1111= IC1 relative priority

Register Name: **IPR2**
Register Description: **Input Priority Register 2**
Register Address: **19h**

Bit #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	PRI4[3:0]				PRI3[3:0]			
Default (T0)	0	0	1	1	0	0	1	0
Default (T4)	0	0	1	1	0	0	1	0

Bits 7 to 4: Priority for Input Clock 4 (PRI4[3:0]). Priority 0001 is highest; priority 1111 is lowest. When MCR11:T4T0 = 0, PRI4 configures IC4's priority for the T0 DPLL. When T4T0 = 1, PRI4 configures IC4's priority for the T4 path. See Section 7.6.1.

0000 = IC4 unavailable for selection
0001–1111= IC4 relative priority

Bits 3 to 0: Priority for Input Clock 3 (PRI3[3:0]). Priority 0001 is highest; priority 1111 is lowest. When MCR11:T4T0 = 0, PRI3 configures IC3's priority for the T0 DPLL. When T4T0 = 1, PRI3 configures IC3's priority for the T4 path. See Section 7.6.1.

0000 = IC3 unavailable for selection
0001–1111= IC3 relative priority

Register Name: **IPR3**
Register Description: **Input Priority Register 3**
Register Address: **1Ah**

Bit #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	PRI6[3:0]				PRI5[3:0]			
Default (T0)	0	0	0	0	0	0	0	0
Default (T4)	0	0	0	0	0	0	0	0

These registers have the same behavior as IPR2 but for input clocks IC5 and IC6.

Register Name: **IPR4**
Register Description: **Input Priority Register 4**
Register Address: **1Bh**

Bit #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	PRI8[3:0]				—			
Default (T0)	0	1	0	0	0	0	0	0
Default (T4)	0	1	0	1	0	0	0	0

These registers have the same behavior as IPR2 but for input clock IC8.

Register Name: **IPR5**
Register Description: **Input Priority Register 5**
Register Address: **1Ch**

Bit #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—				PRI9[3:0]			
Default (T0)	0	0	0	0	0	1	0	1
Default (T4)	0	0	0	0	0	0	0	0

These registers have the same behavior as IPR2 but for input clock IC9.

Register Name: **ICR1, ICR2, ICR3, ICR4, ICR5, ICR6, ICR8, ICR9**
Register Description: **Input Configuration Register 1, 2, 3, 4, 5, 6, 8, 9**
Register Address: **20h, 21h, 22h, 23h, 24h, 25h, 27h, 28h**

Bit #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	DIVN	LOCK8K	BUCKET[1:0]		FREQ[3:0]			
Default	0	0	0	0	see below			

Note: *These registers are identical in function. ICRx is the control register for input clock ICx.*

Bit 7: DIVN Mode (DIVN). When DIVN is set to 1 and LOCK8K = 0, the input clock is divided down by a programmable predivider. The resulting output clock is then passed to the DPLL. All input clocks for which DIVN = 1 are divided by the factor specified in DIVN1 and DIVN2. When DIVN = 1 and LOCK8K = 0 in an ICR register, the FREQ field of that register must be set to the input frequency divided by the divide factor. When DIVN = 1 and LOCK8K = 1 in an ICR register, the FREQ field of that register is decoded as the alternate frequencies. See Sections 7.4.2.2 and 7.4.2.4.

0 = Disabled
1 = Enabled

Bit 6: LOCK8K Mode (LOCK8K). When LOCK8K is set to 1 and DIVN = 0, the input clock is divided down by a preset predivider. The resulting output clock, which is always 8kHz, is then passed to the DPLL. LOCK8K is ignored when DIVN = 0 and FREQ[3:0] = 1001 (2kHz) or 1010 (4kHz). In addition, LOCK8K mode cannot be used with 5MHz input clocks. When DIVN = 1 and LOCK8K = 1 in an ICR register, the FREQ field of that register is decoded as the alternate frequencies. See Sections 7.4.2.2 and 7.4.2.3

0 = Disabled
1 = Enabled

Bits 5 to 4: Leaky Bucket Configuration (BUCKET[1:0]). Each input clock has leaky bucket accumulator logic in its activity monitor. The LBxy registers at addresses 50h to 5Fh specify four different leaky bucket configurations. Any of the four configurations can be specified for the input clock. See Section 7.5.2.

00 = leaky bucket configuration 0
01 = leaky bucket configuration 1
10 = leaky bucket configuration 2
11 = leaky bucket configuration 3

Bits 3 to 0: Input Clock Frequency (FREQ[3:0]). When DIVN = 0 and LOCK8K = 0 (standard direct-lock mode), this field specifies the input clock's nominal frequency for direct-lock operation. When DIVN = 0 and LOCK8K = 1 (LOCK8K mode) this field specifies the input clock's nominal frequency for LOCK8K operation. When DIVN = 1 and LOCK8K = 0 (DIVN mode), this field specifies the frequency after the DIVN divider (i.e., input frequency divided by DIVN + 1). When DIVN = 1 and LOCK8K = 1 (alternate direct-lock frequencies), this field specifies the input clock's nominal frequency for direct-lock operation.

DIVN = 0 or LOCK8K = 0: (Standard direct-lock mode, LOCK8K mode, or DIVN mode)

0000 = 8kHz
0001 = 1544 or 2048kHz (as determined by SONSDH bit in the MCR3 register)
0010 = 6.48MHz
0011 = 19.44MHz
0100 = 25.92MHz
0101 = 38.88MHz
0110 = 51.84MHz
0111 = 77.76MHz
1000 = 155.52MHz (only valid for LVDS inputs)
1001 = 2kHz
1010 = 4kHz
1011 = 6312kHz
1100 = 5MHz
1101 = 31.25 MHz (not a multiple of 8 kHz and therefore not valid for LOCK8K mode)
1110 to 1111 = undefined

DIVN = 1 and LOCK8K = 1: (Alternate direct-lock frequency decode)

0000 = 10MHz (internally divided down to 5MHz)
0001 = 25MHz (internally divided down to 5MHz)
0010 = 62.5MHz (internally down to 31.25MHz)
0011 = 125MHz (internally down to 31.25MHz)
0100 = 156.25MHz (differential inputs only. internally divided down to 31.25MHz)
0101 to 1111 = undefined

FREQ[3:0] Default Values:

ICR1 – ICR4:0000b
ICR5 – ICR9:0011b

Register Name: **VALCR1**
Register Description: **Input Clock Valid Control Register 1**
Register Address: **30h**

Bit #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	IC8	—	IC6	IC5	IC4	IC3	IC2	IC1
Default	1	0	1	1	1	1	1	1

Bits 7 and 5 to 0: Input Clock Valid Control (IC8 and IC[6:1]). These control bits can be used to force input clocks to be considered invalid. If a clock is invalidated by one of these control bits it will not appear in the priority table in the PTAB1 and PTAB2 registers, even if the clock is otherwise valid. These bits are useful when system software needs to force clocks to be invalid in response to OAM commands. Note that setting a VALCR bit low has no effect on the corresponding bit in the VALSR registers. See Sections 7.6.2.

0 = Force invalid
1 = Don't force invalid; determine validity normally

Register Name: **VALCR2**
Register Description: **Input Clock Valid Control Register 2**
Register Address: **31h**

Bit #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	—	—	—	—	—	—	IC9
Default	0	0	0	0	0	0	0	1

Bit 0: Input Clock Valid Control (IC9). This bit has the same behavior as the bits in VALCR1 but for the IC9 input clock.

Register Name: **MCR1**
Register Description: **Master Configuration Register 1**
Register Address: **32h**

Bit #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	RST	—	FREN	LOCKPIN	—	T0STATE[2:0]		
Default	0	0	1	0	0	0	0	0

Bit 7: Device Reset (RST). When this bit is high the entire device is held in reset, and all register fields, except the RST bit itself, are reset to their default states. When RST is active, the register fields with pin-programmed defaults do not latch their values from the corresponding input pins. Instead these fields are reset to the default values that were latched from the pins when the RST pin was last active. See Section 7.11.

0 = Normal operation
1 = Reset

Bit 5: Frequency Range Detect Enable (FREN). When this bit is high the frequency of each input clock is measured and used to quickly declare the input inactive.

0 = Frequency Range Detect disabled
1 = Frequency Range Detect enabled

Bit 4: T0 DPLL LOCK Pin Enable (LOCKPIN). When this bit is high the LOCK pin indicates when the T0 DPLL state machine is in the LOCK state (OPSTATE.T0STATE = 100).

0 = LOCK pin is not driven
1 = LOCK pin is driven high when the T0 DPLL is in the Lock state

Bits 2 to 0: T0 DPLL State Control (T0STATE[2:0]). This field allows the T0 DPLL state machine to be forced to a specified state. The state machine will remain in the forced state, and therefore cannot react to alarms and other events, as long as T0STATE is not equal to 000. See Section 7.7.1.

000 = Automatic (normal state machine operation)
001 = Free-run
010 = Holdover
011 = {unused value}
100 = Locked
101 = Prelocked 2
110 = Prelocked
111 = Loss-of-lock

Register Name: **MCR2**
Register Description: **Master Configuration Register 2**
Register Address: **33h**

Bit #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	—	—	—	T0FORCE[3:0]			
Default	0	0	0	0	1	1	1	1

Bits 3 to 0: T0 DPLL Force Selected Reference (T0FORCE[3:0]). This field provides a way to force a specified input clock to be the selected reference for the T0 DPLL. Internally this is accomplished by forcing the clock to have the highest priority (as specified in PTAB1:REF1). In revertive mode (MCR3:REVERT = 1) the forced clock automatically becomes the selected reference (as specified in PTAB1:SELREF) as well. In nonrevertive mode the forced clock only becomes the selected reference when the existing selected reference is invalidated or made unavailable for selection.

When a reference is forced, the activity monitor for that input and the T0 DPLL's loss-of-lock timeout logic all continue to operate and affect the relevant ISR, VALSR and MSR register bits. However, when the reference is declared invalid the T0 DPLL is not allowed to switch to another input clock. The T0 DPLL continues to respond to the fast activity monitor, transitioning to mini-holdover in response to short-term events and to full holdover in response to longer events. See Section 7.6.3.

0000 = Automatic source selection (normal operation)
0001 = Force to IC1
0010 = Force to IC2
0011 = Force to IC3
0100 = Force to IC4
0101 = Force to IC5
0110 = Force to IC6
0111 = {unused value}
1000 = Force to IC8
1001 = Force to IC9
1010 to 1110 = {unused values}
1111 = Automatic source selection (normal operation)

Register Name: **MCR3**
Register Description: **Master Configuration Register 3**
Register Address: **34h**

Bit #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	AEFSEN	LKATO	XOEDGE	FRUNHO	EFSEN	SONSDH	—	REVERT
Default	1	1	0	0	1	see below	1	0

Bit 7: Auto External Frame Sync Enable (AEFSEN). This bit has two modes depending on the SOURCE field of FSCR3. See Section 7.9.

SOURCE! = 11XX:

0 = EFSEN bit (bit 3 below) enables and disables the external frame sync on the SYNCn pin
1 = The external frame sync is enabled when EFSEN = 1 and the T0 DPLL is locked to the input clock specified in the SOURCE field of FSCR3.

SOURCE = 11XX:

0 = External frame sync enabled according to EFSEN bit.
1 = When the selected reference changes the EFSEN bit clears and the external frame sync is disabled. (EFSEN bit must be set to enable it again.)

Bit 6: Phase Lock Alarm Timeout (LKATO). This bit controls how phase alarms on input clocks can be terminated. Phase alarms are indicated by the LOCK bits in ISR registers.

0 = Phase alarms on input clocks can only be cancelled by software.
1 = Phase alarms are automatically cancelled after a timeout period of 128 seconds.

Bit 5: Local Oscillator Edge (XOEDGE). This bit specifies the significant clock edge of the local oscillator clock signal on the REFCLK input pin. The faster edge should be selected for best jitter performance. See Section 7.3.

0 = Rising edge
1 = Falling edge

Bit 4: Free-Run Holdover (FRUNHO). When this bit is set to 1 the T0 DPLL holdover frequency is set to 0ppm so the output frequency accuracy is set by the external oscillator accuracy. This effects both mini-holdover and the holdover state.

0 = Digital holdover
1 = Free-run holdover, 0ppm

Bit 3: External Frame Sync Enable (EFSEN). When this bit is set to 1 the T0 DPLL looks for a frame sync pulse on the SYNCn pin(s). When FSCR3.SOURCE = 11XX the function of this bit can be modified according to the setting of the AEFSEN bit. See the AEFSEN bit description above for more information. See Section 7.9.

0 = Disable external frame sync; ignore SYNCn pin(s)
1 = Enable external frame sync on SYNCn pin(s)

Bit 2: SONET or SDH Frequencies (SONSDH). This bit specifies the clock rate for input clocks with FREQ = 0001 in the ICR registers (20h to 28h). During reset the default value of this bit is latched from the SONSDH pin. See Section 7.4.2.

0 = 2048kHz
1 = 1544kHz

Bit 0: Revertive Mode (REVERT). This bit configures the T0 DPLL for revertive or nonrevertive operation. (The T4 DPLL is always revertive). In revertive mode, if an input clock with a higher priority than the selected reference becomes valid, the higher priority reference immediately becomes the selected reference. In nonrevertive mode the higher priority reference does not immediately become the selected reference but does become the highest-priority reference in the priority table (REF1 field in the PTAB1 register). See Section 7.6.2.

Register Name: **MCR4**
Register Description: **Master Configuration Register 4**
Register Address: **35h**

Bit #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	LKT4T0	—	—	—	T4FORCE[3:0]			
Default	0	0	0	0	0	0	0	0

Bit 7: Lock T4 to T0 (LKT4T0). When this bit is set to 1 (and T0CR1:T4APT0 = 0) all output clocks are generated from the T0 DPLL, and the T4CR1:T4FREQ field selects the frequency of the T4 APLL. See Section 7.8.2.2. When LKT4T0 = 0, the T4 APLL can be locked to either the T4 DPLL or the T0 DPLL depending on the setting of T0CR1:T4APT0.

0 = T4 APLL can lock to either T4 or the T0 DPLL
1 = T4 APLL always locked to the T0 DPLL

Bits 3 to 0: T4 DPL Force Selected Reference (T4FORCE[3:0]). This field provides a way to force a specified input clock to be the selected reference for the T4 DPLL. Internally this is accomplished by forcing the clock to have the highest priority (as specified in PTAB1:REF1). Since the T4 DPLL always operates in revertive mode, the forced clock automatically becomes the selected reference (as specified in PTAB1:SELREF) as well.

When a reference is forced, the activity monitor for that input continues to operate and affect the relevant ISR, VALSR and MSR register bits. However, when the reference is declared invalid, the T4 DPLL is not allowed to switch to another input clock. See Section 7.6.3.

0000 = Automatic source selection (normal operation)
0001 = Force to IC1
0010 = Force to IC2
0011 = Force to IC3
0100 = Force to IC4
0101 = Force to IC5
0110 = Force to IC6
0111 = {unused value}
1000 = Force to IC8
1001 = Force to IC9
1010 to 1110 = {unused value}
1111 = Automatic source selection (normal operation)

Register Name: **MCR5**
Register Description: **Master Configuration Register 5**
Register Address: **36h**

Bit #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	RSV4	RSV3	RSV2	RSV1	IC2SF	IC1SF	IC6SF	IC5SF
Default	0	0	0	0	0	0	0	0

Bits 7 to 4: Reserved Bit 4 to 1 (RSV[4:1]). These bits are reserved for future use, and can be written to and read back.

Bit 3: Input Clock 2 Signal Format (IC2SF). For backward compatibility this bit can be written to and read back, but it does not affect the IC2POS/NEG inputs pins. See Section 7.4.1.

Bit 2: Input Clock 1 Signal Format (IC1SF). For backward compatibility this bit can be written to and read back, but it does not affect the IC1POS/NEG inputs pins. See Section 7.4.1.

Bit 1: Input Clock 6 Signal Format (IC6SF). For backward compatibility this bit can be written to and read back, but it does not affect the IC6POS/NEG inputs pins. See Section 7.4.1.

Bit 0: Input Clock 5 Signal Format (IC5SF). For backward compatibility this bit can be written to and read back, but it does not affect the IC5POS/NEG inputs pins. See Section 7.4.1.

Register Name: **OCR6**
Register Description: **Output Configuration Register 6**
Register Address: **37h**

Bit #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	OC5EN	OC4EN	OC5BEN	OC4BEN	OC3BEN	OC2BEN	OC1BEN
Default	0	1	1	0	0	0	0	0

Bit 6: OC5 Output Enable (OC5EN). Enables the OC5 output pin.

0 = Output clock pin disabled, drives low.
1 = Output clock pin controlled by OCR3.OFREQ5.

Bit 5: OC4 Output Enable (OC4EN). Enables the OC4 output pin.

0 = Output clock pin disabled, drives low.
1 = Output clock pin controlled by OCR2.OFREQ4.

Bit 4: OC5B Output Enable (OC5BEN). Enables the OC5B output pin.

0 = Output clock pin disabled, drives low.
1 = Output clock pin controlled by OCR3.OFREQ5.

Bit 3: OC4B Output Enable (OC4BEN). Enables the OC4B output pin.

0 = Output clock pin disabled, drives low.
1 = Output clock pin controlled by OCR2.OFREQ4.

Bit 2: OC3B Output Enable (OC3BEN). Selects GPIO3 or OC3B function for the OC3B/GPIO3pin.

0 = GPIO3 functionality .
1 = Output clock pin controlled by OCR2.OFREQ3.

Bit 1: OC2B Output Enable (OC2BEN). Selects GPIO2 or OC2B function for the OC2B/GPIO2pin.

0 = GPIO2 functionality .
1 = Output clock pin controlled by OCR1.OFREQ2.

Bit 0: OC1B Output Enable (OC1BEN). Selects GPIO1 or OC1B function for the OC1B/GPIO1pin.

0 = GPIO1 functionality .
1 = Output clock pin controlled by OCR1.OFREQ1.

Register Name: **MCR6**
Register Description: **Master Configuration Register 6**
Register Address: **38h**

Bit #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	DIG2AF	DIG2SS	DIG1SS	—	—	—	—	—
Default	0	see below	see below	1	1	1	1	1

Bit 7: Digital Alternate Frequency (DIG2AF). Selects alternative frequencies.

0 = Digital2 NxE1 or NxDS1 frequency specified by DIG2SS and MCR7:DIG2F.
1 = Digital2 6.312MHz, 10MHz, or Nx19.44MHz frequency specified by DIG2SS and MCR7:DIG2F.

Bit 6: Digital2 SONET or SDH Frequencies (DIG2SS). This bit specifies whether the clock rates generated by the Digital2 clock synthesizer are multiples of 1.544MHz (SONET-compatible) or multiples of 2.048MHz (SDH-compatible) or alternate frequencies. The specific multiple is set in the DIG2F field of the MCR7 register. When $\overline{RST}$ = 0 the default value of this bit is latched from the SONSDH pin.

DIG2AF = 0:
0 = Multiples of 2048kHz
1 = Multiples of 1544kHz
DIG2AF = 1:
6.312MHz, 10 MHz or Nx19.44MHz

Bit 5: Digital1 SONET or SDH Frequencies (DIG1SS). This bit specifies whether the clock rates generated by the Digital1 clock synthesizer are multiples of 1544kHz (SONET compatible) or multiples of 2048kHz (SDH compatible). The specific multiple is set in the DIG1F field of the MCR7 register. When $\overline{RST}$ = 0 the default value of this bit is latched from the SONSDH pin.

0 = Multiples of 2048kHz
1 = Multiples of 1544kHz

Register Name: **MCR7**
Register Description: **Master Configuration Register 7**
Register Address: **39h**

Bit #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	DIG2F[1:0]		DIG1F[1:0]		—	—	DIG2SRC	DIG1SRC
Default	0	0	0	0	1	0	0	0

Bits 7 to 6: Digital2 Frequency (DIG2F[1:0]). This field, MCR6:DIG2SS and MCR6:DIG2AF configure the frequency of the Digital2 clock synthesizer.

DIG2AF = 0		DIG2AF = 1	
DIG2SS = 1	DIG2SS = 0	DIG2SS = 1	DIG2SS = 0
00 = 1544kHz	00 = 2048kHz	00 = 19.44MHz	00 = 6.312MHz
01 = 3088kHz	01 = 4096kHz	01 = 38.88MHz	01 = undefined
10 = 6176kHz	10 = 8192kHz	10 = undefined	10 = 10MHz
11 = 1235 kHz	11 = 16384kHz	11 = undefined	11 = undefined

Bits 5 to 4: Digital1 Frequency (DIG1F[1:0]). This field and MCR6:DIG1SS configure the frequency of the Digital1 clock synthesizer.

DIG1SS = 1	DIG1SS = 0
00 = 1544kHz	00 = 2048kHz
01 = 3088kHz	01 = 4096kHz
10 = 6176kHz	10 = 8192kHz
11 = 12352kHz	11 = 16384kHz

Bit 1: Digital2 Source (DIG2SRC). This bit selects which DPLL the Digital 2 DFS is connected to. When MCR4:LKT4T0 = 1 it is always connected to the T0 DPLL.

0 = the T0 DPLL
1 = the T4 DPLL

Bit 0: Digital1 Source (DIG1SRC). This bit selects which DPLL the Digital 1 DFS is connected to. When MCR4:LKT4T0 = 1 it is always connected to the T0 DPLL.

0 = the T0 DPLL
1 = the T4 DPLL

Register Name: **MCR8**
Register Description: **Master Configuration Register 8**
Register Address: **3Ah**

Bit #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	OC5SF[1:0]		OC4SF[1:0]		OC7SF[1:0]		OC6SF[1:0]	
Default	0	0	0	0	0	0	0	0

Bits 7 to 6: Output Clock 5 Signal Format (OC5SF[1:0]). See Section 7.8.1.

00 = Output disabled (default)
01 = 3V LVPECL level compatible
10 = 3V LVDS compatible
11 = 3V LVDS compatible

Bits 5 to 4: Output Clock 4 Signal Format (OC4SF[1:0]). See Section 7.8.1.

00 = Output disabled (default)
01 = 3V LVPECL level compatible
10 = 3V LVDS compatible
11 = 3V LVDS compatible

Bits 3 to 2: Output Clock 7 Signal Format (OC7SF[1:0]). See Section 7.8.1.

00 = Output disabled (default)
01 = 3V LVPECL level compatible
10 = 3V LVDS compatible
11 = 3V LVDS compatible

Bits 1 to 0: Output Clock 6 Signal Format (OC6SF[1:0]). See Section 7.8.1.

00 = Output disabled (default)
01 = 3V LVPECL level compatible
10 = 3V LVDS compatible
11 = 3V LVDS compatible

Register Name: **MCR9**
Register Description: **Master Configuration Register 9**
Register Address: **3Bh**

Bit #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	AUTOBW	—	—	—	LIMINT	—	—	—
Default	1	1	1	1	1	0	1	1

Bit 7: Automatic Bandwidth Selection (AUTOBW). See Section 7.7.3.

0 = Always selects locked bandwidth from the T0LBW register
1 = Automatically selects either locked bandwidth (T0LBW register) or acquisition bandwidth (T0ABW register) as appropriate

Bit 3: Limit Integral Path (LIMINT). When this bit is set to 1, the T0 DPLL's integral path is limited (i.e., frozen) when the DPLL reaches minimum or maximum frequency, as set by the HARDLIM field in DLIMIT1 and DLIMIT2. When the integral path is frozen, the current DPLL frequency in registers FREQ1, FREQ2 and FREQ3 is also frozen. Setting LIMINT = 1 minimizes overshoot when the DPLL is pulling in. See Section 7.7.3.

0 = Do not freeze integral path at min/max frequency
1 = Freeze integral path at min/max frequency

Register Name: **MCLK1**
Register Description: **Master Clock Frequency Adjustment Register 1**
Register Address: **3Ch**

Bit #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	MCLKFREQ[7:0]							
Default	1	0	0	1	1	0	0	1

Note: *The MCLK1 and MCLK2 registers must be read consecutively and written consecutively. See Section 8.3.*

Bits 7 to 0: Master Clock Frequency Adjustment (MCLKFREQ[7:0]). The full 16-bit MCLKFREQ[15:0] field spans this register and MCLK2. MCLKFREQ is an unsigned integer that adjusts the frequency of the internal 204.8MHz master clock with respect to the frequency of the local oscillator clock on the REFCLK pin by up to +514ppm and -771ppm. The master clock adjustment has the effect of speeding up the master clock with a positive adjustment and slowing it down with a negative adjustment. For example, if the oscillator connected to REFCLK has an offset of +1ppm the adjustment should be -1ppm to correct the offset.

The formulas below translate adjustments to register values and vice versa. The default register value of 39,321 corresponds to 0ppm. See Section 7.3.

MCLKFREQ[15:0] = adjustment_in_ppm / 0.0196229 + 39,321

adjustment_in_ppm = (MCLKFREQ[15:0] – 39,321) x 0.0196229

Register Name: **MCLK2**
Register Description: **Master Clock Frequency Adjustment Register 2**
Register Address: **3Dh**

Bit #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	MLCKFREQ[15:8]							
Default	1	0	0	1	1	0	0	1

Bits 7 to 0: Master Clock Frequency Adjustment (MCLKFREQ[15:8]). See the MCLK1 register description.

Register Name: **HOCR3**
Register Description: **Holdover Configuration Register 3**
Register Address: **40h**

Bit #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	AVG	—	—	—		—		
Default	1	0	0	0	1	0	0	0

Note: *See Section 8.3 for important information about writing and reading this register.*

Bit 7: Averaging (AVG). When this bit is set to 1 the T0 DPLL uses the averaged frequency value during holdover mode. When FRUNHO = 1 in the MCR3 register, this bit is ignored. See Section 7.7.1.6.

0 = Not averaged frequency; holdover frequency is either free-run (FRUNHO = 1) or instantaneously frozen
1 = Averaged frequency over the last 1 second while locked to the input

Register Name: **DLIMIT1**
Register Description: **DPLL Frequency Limit Register 1**
Register Address: **41h**

Bit #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	HARDLIM[7:0]							
Default	0	1	1	1	0	1	1	0

The DLIMIT1 and DLIMIT2 registers must be read consecutively and written consecutively. See Section 8.3.

Bits 7 to 0: DPLL Hard Frequency Limit (HARDLIM[7:0]). The full 10-bit HARDLIM[9:0] field spans this register and DLIMIT2. HARDLIM is an unsigned integer that specifies the hard frequency limit or pull-in/hold-in range of the T0 DPLL. When frequency limit detection is enabled by setting FLLOL = 1 in the DLIMIT3 register, if the DPLL frequency exceeds the hard limit the DPLL declares loss-of-lock. The hard frequency limit in ppm is ±HARDLIM[9:0] x 0.0782. The default value is normally ±9.2ppm. If external reference switching mode is enabled during reset (see Section 7.6.5), the default value is configured to ±79.794ppm (3FFh). See Section 7.7.6.

Register Name: **DLIMIT2**
Register Description: **DPLL Frequency Limit Register 1**
Register Address: **42h**

Bit #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	—	—	—	—	—	HARDLIM[9:8]	
Default	0	0	0	0	0	0	0	0

Bits 1 to 0: DPLL Hard Frequency Limit (HARDLIM[9:8]). See the DLIMIT1 register description.

Register Name: **IER1**
Register Description: **Interrupt Enable Register 1**
Register Address: **43h**

Bit #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	IC8	—	IC6	IC5	IC4	IC3	IC2	IC1
Default	0	0	0	0	0	0	0	0

Bits 7 and 5 to 0: Interrupt Enable for Input Clock Status Change (IC8 and IC[6:1]). Each of these bits is an interrupt enable control for the corresponding bit in the MSR1 register.

0 = Mask the interrupt
1 = Enable the interrupt

Register Name: **IER2**
Register Description: **Interrupt Enable Register 2**
Register Address: **44h**

Bit #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	STATE	SRFAIL	—	—	—	—	—	IC9
Default	0	0	0	0	0	0	0	0

Bit 7: Interrupt Enable for T0 DPLL State Change (STATE). This bit is an interrupt enable for the STATE bit in the MSR2 register.

0 = Mask the interrupt
1 = Enable the interrupt

Bit 6: Interrupt Enable for Selected Reference Failed (SRFAIL). This bit is an interrupt enable for the SRFAIL bit in the MSR2 register.

0 = Mask the interrupt
1 = Enable the interrupt

Bit 0: Interrupt Enable for Input Clock Status Change (IC9). This bit is an interrupt enable control for the IC9 bit in the MSR2 register.

0 = Mask the interrupt
1 = Enable the interrupt

Register Name: **IER3**
Register Description: **Interrupt Enable Register 3**
Register Address: **45h**

Bit #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	FSMON	T4LOCK	—	T4NOIN	—	—	—	—
Default	0	0	0	0	0	0	0	0

Bit 7: Interrupt Enable for Frame Sync Input Monitor Alarm (FSMON). This bit is an interrupt enable for the FSMON bit in the MSR3 register.

0 = Mask the interrupt
1 = Enable the interrupt

Bit 6: Interrupt Enable for the T4 DPLL Lock Status Change (T4LOCK). This bit is an interrupt enable for the T4LOCK bit in the MSR3 register.

0 = Mask the interrupt
1 = Enable the interrupt

Bit 4: Interrupt Enable for T4 No Valid Inputs Alarm (T4NOIN). This bit is an interrupt enable for the T4NOIN bit in the MSR3 register.

0 = Mask the interrupt
1 = Enable the interrupt

Register Name: **DIVN1**
Register Description: **DIVN Register 1**
Register Address: **46h**

Bit #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	DIVN[7:0]							
Default	1	1	1	1	1	1	1	1

Note: *The DIVN1 and DIVN2 registers must be read consecutively and written consecutively. See Section 8.3.*

Bits 7 to 0: DIVN Factor (DIVN[7:0]). The full 16-bit DIVN[15:0] field spans this register and DIVN2. This field contains the integer value used to divide the frequency of input clocks that are configured for DIVN mode. The frequency is divided by DIVN[15:0] + 1. See Section 7.4.2.4.

Register Name: **DIVN2**
Register Description: **DIVN Register 2**
Register Address: **47h**

Bit #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	DIVN[15:8]							
Default	0	0	1	1	1	1	1	1

Bits 7 to 0: DIVN Factor (DIVN[15:8]). See the DIVN1 register description.

Register Name: **MCR10**
Register Description: **Master Configuration Register 10**
Register Address: **48h**

Bit #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	SRFPIN	UFSW	EXTSW	PBOFRZ	PBOEN	—	—
Default	1	0	0	see below	0	1	0	0

Bit 6: SRFAIL Pin Enable (SRFPIN). When this bit is set to 1, the SRFAIL pin is enabled. When enabled the SRFAIL pin follows the state of the SRFAIL status bit in the MSR2 register. This gives the system a very fast indication of the failure of the current reference. See Section 7.5.3.

0 = SRFAIL pin disabled (not driven)
1 = SRFAIL pin enabled

Bit 5: Ultra-Fast Switching Mode (UFSW). See Section 7.6.4.

0 = Disabled
1 = Enabled. The current reference source is disqualified after less than three missing clock cycles.

Bit 4: External Reference Switching Mode (EXTSW). This bit enables external reference switching mode. In this mode, if the SRCSW pin is high the T0 DPLL is forced to lock to input IC3 (if the priority of IC3 is nonzero) or IC5 (if the priority of IC3 is zero) whether or not the selected input has a valid reference signal. If the SRCSW pin is low the device is forced to lock to input IC4 (if the priority of IC4 is nonzero) or IC6 (if the priority of IC4 is zero) whether or not the selected input has a valid reference signal. During reset the default value of this bit is latched from the SRCSW pin. This mode only controls the T0 DPLL. The T4 DPLL is not affected. See Section 7.6.5.

0 = Normal operation
1 = External switching mode

Bit 3: Phase Build-Out Freeze (PBOFRZ). This bit freezes the current input-output phase relationship and does not allow further phase build-out events to occur. This bit affects phase build-out in response to reference switching (Section 7.7.7.1).

0 = Not frozen
1 = Frozen

Bit 2: Phase Build-Out Enable (PBOEN). When this bit is set to 1 a phase build-out event occurs every time the T0 DPLL changes to a new reference, including exiting the holdover and free-run states. When this bit is set to 0, the T0 DPLL locks to the new source with zero degrees of phase difference. See Section 7.7.7.

Register Name: **MCR11**
Register Description: **Master Configuration Register 11**
Register Address: **4Bh**

Bit #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	—	—	T4T0	—	—	—	—
Default	0	0	0	0	0	0	0	0

Bit 4: T4 or T0 Path Select (T4T0). This bit specifies which path is being accessed when reads or writes are made to the following registers: PTAB1, PTAB2, FREQ1, FREQ2, FREQ3, IPR1, IPR2, IPR3, IPR4, IPR5, PHASE1, and PHASE2.

0 = T0 path
1 = T4 path

Register Name: **DLIMIT3**
Register Description: **DPLL Frequency Limit Register 3**
Register Address: **4Dh**

Bit #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	FLLOL	SOFTLIM[6:0]						
Default	1	0	0	0	1	1	1	0

Bit 7: Frequency Limit Loss of Lock (FLLOL). When this bit is set to 1, the T0 DPLL and the T4 DPLL internally declare loss-of-lock when their hard limits are reached. The T0 DPLL hard frequency limit is set in the HARDLIM[9:0] field in the DLIMIT1 and DLIMIT2 registers. The T4 DPLL hard frequency limit is fixed at ±80ppm. See Section 7.7.6.

0 = DPLL declares loss-of-lock normally
1 = DPLL also declares loss-of-lock when the hard frequency limit is reached

Bits 6 to 0: DPLL Soft Frequency Limit (SOFTLIM[6:0]). This field is an unsigned integer that specifies the soft frequency limit for the T0 DPLL and the T4 DPLL. The soft limit is only used for monitoring; exceeding this limit does not cause loss-of-lock. The limit in ppm is ±SOFTLIM[6:0] x 0.628. The default value is ±8.79ppm. When the T0 DPLL frequency reaches the soft limit the T0SOFT status bit is set in the OPSTATE register. When the T4 DPLL frequency reaches the soft limit the T4SOFT status bit is set in OPSTATE. See Section 7.7.6.

Register Name: **IER4**
Register Description: **Interrupt Enable Register 4**
Register Address: **4Eh**

Bit #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	HORDY	—	—	—	—	—	—
Default	0	0	0	0	0	0	0	0

Bit 6: Interrupt Enable for Holdover Frequency Ready (HORDY). This bit is an interrupt enable for the HORDY bit in the MSR4 register.

0 = Mask the interrupt
1 = Enable the interrupt

Register Name: **OCR5**
Register Description: **Output Configuration Register 1**
Register Address: **4Fh**

Bit #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	AOF7	AOF6	AOF5	AOF4	AOF3	AOF2	AOF1
Default	0	0	0	0	0	0	0	0

Bit 6: Alternate Output Frequency Mode Select 7 (AOF7). This bit controls the decoding of the OCR4.OFREQ7 field for the OC7 pin.

0 = Standard decodes
1 = Alternate decodes

Bit 5: Alternate Output Frequency Mode Select 6 (AOF6). This bit controls the decoding of the OCR3.OFREQ6 field for the OC6 pin.

0 = Standard decodes
1 = Alternate decodes

Bit 4: Alternate Output Frequency Mode Select 5 (AOF5). This bit controls the decoding of the OCR3.OFREQ5 field for the OC5 pin.

0 = Standard decodes
1 = Alternate decodes

Bit 3: Alternate Output Frequency Mode Select 4 (AOF4). This bit controls the decoding of the OCR2.OFREQ4 field for the OC4 pin.

0 = Standard decodes
1 = Alternate decodes

Bit 2: Alternate Output Frequency Mode Select 3 (AOF3). This bit controls the decoding of the OCR2.OFREQ3 field for the OC3 pin.

0 = Standard decodes
1 = Alternate decodes

Bit 1: Alternate Output Frequency Mode Select 2 (AOF2). This bit controls the decoding of the OCR1.OFREQ2 field for the OC2 pin.

0 = Standard decodes
1 = Alternate decodes

Bit 0: Alternate Output Frequency Mode Select 1 (AOF1). This bit controls the decoding of the OCR1.OFREQ1 field for the OC1 pin.

0 = Standard decodes
1 = Alternate decodes

Register Name: **LB0U**
Register Description: **Leaky Bucket 0 Upper Threshold Register**
Register Address: **50h**

Bit #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	LB0U[7:0]							
Default	0	0	0	0	0	1	1	0

Bits 7 to 0: Leaky Bucket 0 Upper Threshold (LB0U[7:0]). When the leaky bucket accumulator is equal to the value stored in this field, the activity monitor declares an activity alarm by setting the input clock's ACT bit in the appropriate ISR register. Registers LB0U, LB0L, LB0S and LB0D together specify leaky bucket configuration 0. See Section 7.5.2.

Register Name: **LB0L**
Register Description: **Leaky Bucket 0 Lower Threshold Register**
Register Address: **51h**

Bit #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	LB0L[7:0]							
Default	0	0	0	0	0	1	0	0

Bits 7 to 0: Leaky Bucket 0 Lower Threshold (LB0L[7:0]). When the leaky bucket accumulator is equal to the value stored in this field, the activity monitoring logic clears the activity alarm (if previously declared) by clearing the input clock's ACT bit in the appropriate ISR register. Registers LB0U, LB0L, LB0S, and LB0D together specify leaky bucket configuration 0. See Section 7.5.2.

Register Name: **LB0S**
Register Description: **Leaky Bucket 0 Size Register**
Register Address: **52h**

Bit #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	LB0S[7:0]							
Default	0	0	0	0	1	0	0	0

Bits 7 to 0: Leaky Bucket 0 Size (LB0S[7:0]). This field specifies the maximum value of the leaky bucket. The accumulator cannot increment past this value. Registers LB0U, LB0L, LB0S, and LB0D together specify leaky bucket configuration 0. See Section 7.5.2.

Register Name: **LB0D**
Register Description: **Leaky Bucket 0 Decay Rate Register**
Register Address: **53h**

Bit #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	—	—	—	—	—	LB0D[1:0]	
Default	0	0	0	0	0	0	0	1

Bits 1 to 0: Leaky Bucket 0 Decay Rate (LB0D[1:0]). This field specifies the decay or "leak" rate of the leaky bucket accumulator. For each period of 1, 2, 4, or 8 128ms intervals in which no irregularities are detected on the input clock, the accumulator decrements by 1. Registers LB0U, LB0L, LB0S, and LB0D together specify leaky bucket configuration 0. See Section 7.5.2.

00 = decrement every 128ms (8 units/second)
01 = decrement every 256ms (4 units/second)
10 = decrement every 512ms (2 units/second)
11 = decrement every 1024ms (1 unit/second)

Register Name: **LB1U, LB2U, LB3U**
Register Description: **Leaky Bucket 1/2/3 Upper Threshold Register**
Register Address: **54h, 58h, 5Ch**

Bit #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	LBxU[7:0]							
Default	0	0	0	0	0	1	1	0

Bits 7 to 0: Leaky Bucket 'x' Upper Threshold (LBxU[7:0]). See the LB0U register description.

Registers LB1U, LB1L, LB1S, and LB1D together specify leaky bucket configuration 1.
Registers LB2U, LB2L, LB2S, and LB2D together specify leaky bucket configuration 2.
Registers LB3U, LB3L, LB3S, and LB3D together specify leaky bucket configuration 3.

Register Name: **LB1L, LB2L, LB3L**
Register Description: **Leaky Bucket 1/2/3 Lower Threshold Register**
Register Address: **55h, 59h, 5Dh**

Bit #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	LBxL[7:0]							
Default	0	0	0	0	0	1	0	0

Bits 7 to 0: Leaky Bucket 'x' Lower Threshold (LBxL[7:0]). See the LB0L register description.

Registers LB1U, LB1L, LB1S, and LB1D together specify leaky bucket configuration 1.
Registers LB2U, LB2L, LB2S, and LB2D together specify leaky bucket configuration 2.
Registers LB3U, LB3L, LB3S, and LB3D together specify leaky bucket configuration 3.

Register Name: **LB1S, LB2S, LB3S**
Register Description: **Leaky Bucket 1/2/3 Size Register**
Register Address: **56h, 5Ah, 5Eh**

Bit #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	LBxS[7:0]							
Default	0	0	0	0	1	0	0	0

Bits 7 to 0: Leaky Bucket 'x' Size (LBxS[7:0]). See the LB0S register description.

Registers LB1U, LB1L, LB1S, and LB1D together specify leaky bucket configuration 1.
Registers LB2U, LB2L, LB2S, and LB2D together specify leaky bucket configuration 2.
Registers LB3U, LB3L, LB3S, and LB3D together specify leaky bucket configuration 3.

Register Name: **LB1D, LB2D, LB3D**
Register Description: **Leaky Bucket 1/2/3 Decay Rate Register**
Register Address: **57h, 5Bh, 5Fh**

Bit #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	—	—	—	—	—	LBxD[1:0]	
Default	0	0	0	0	0	0	0	1

Bits 1 to 0: Leaky Bucket 'x' Decay Rate (LBxD[1:0]). See the LB0D register description.

Registers LB1U, LB1L, LB1S, and LB1D together configure leaky bucket algorithm 1.
Registers LB2U, LB2L, LB2S, and LB2D together configure leaky bucket algorithm 2.
Registers LB3U, LB3L, LB3S, and LB3D together configure leaky bucket algorithm 3.

Register Name: **OCR1**
Register Description: **Output Configuration Register 1**
Register Address: **60h**

Bit #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	OFREQ2[3:0]				OFREQ1[3:0]			
Default	0	0	0	0	0	0	0	0

Bits 7 to 4: Output Frequency of OC2 (OFREQ2[3:0]). This field specifies the frequency of output clock OC2. The frequencies of the T0 APLL and the T4 APLL are configured in the T0CR1 and T4CR1 registers. The Digital1 and Digital2 frequencies are configured in the MCR7 register. See Section 7.8.2.3. The decode of this field is controlled by the value of the OCR5.AOF2 bit.

AOF2 = 0: (standard decodes)

0000 = Output disabled (i.e., low)
0001 = 2kHz
0010 = 8kHz
0011 = Digital2 (see Table 7-8)
0100 = Digital1 (see Table 7-7)
0101 = T0 APLL frequency divided by 48
0110 = T0 APLL frequency divided by 16
0111 = T0 APLL frequency divided by 12
1000 = T0 APLL frequency divided by 8
1001 = T0 APLL frequency divided by 6
1010 = T0 APLL frequency divided by 4
1011 = T4 APLL frequency divided by 64
1100 = T4 APLL frequency divided by 48
1101 = T4 APLL frequency divided by 16
1110 = T4 APLL frequency divided by 8
1111 = T4 APLL frequency divided by 4

AOF2 = 1: (alternate decodes)

0000 = Output disabled (i.e., low)
0001 = T0 APLL frequency divided by 64
0010 = T4 APLL frequency divided by 20
0011 = T4 APLL frequency divided by 12
0100 = T4 APLL frequency divided by 10
0101 = T4 APLL frequency divided by 5
0110 = T4 APLL frequency divided by 2
0111 = T4 selected reference (after dividing)
1000 to 1111 = undefined

Bits 3 to 0: Output Frequency of OC1 (OFREQ1[3:0]). This field specifies the frequency of output clock OC1. The frequencies of the T0 APLL and T4 APLL are configured in the T0CR1 and T4CR1 registers. The Digital1 and Digital2 frequencies are configured in the MCR7 register. See Section 7.8.2.3. The decode of this field is controlled by the value of the OCR5.AOF1 bit.

AOF1 = 0: (standard decodes)

0000 = Output disabled (i.e., low)
0001 = 2kHz
0010 = 8kHz
0011 = Digital2 (see Table 7-8)
0100 = Digital1 (see Table 7-7)
0101 = T0 APLL frequency divided by 48
0110 = T0 APLL frequency divided by 16
0111 = T0 APLL frequency divided by 12
1000 = T0 APLL frequency divided by 8
1001 = T0 APLL frequency divided by 6
1010 = T0 APLL frequency divided by 4

1011 = T4 APLL frequency divided by 64
1100 = T4 APLL frequency divided by 48
1101 = T4 APLL frequency divided by 16
1110 = T4 APLL frequency divided by 8
1111 = T4 APLL frequency divided by 4

AOF1 = 1: (alternate decodes)

0000 = Output disabled (i.e., low)
0001 = T0 APLL frequency divided by 64
0010 = T4 APLL frequency divided by 20
0011 = T4 APLL frequency divided by 12
0100 = T4 APLL frequency divided by 10
0101 = T0 APLL2 frequency divided by 10
0110 = T0 APLL2 frequency divided by 5
0111 = T4 selected reference (after dividing)
1000 to 1111 = undefined

Register Name: **OCR2**
Register Description: **Output Configuration Register 2**
Register Address: **61h**

Bit #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	OFREQ4[3:0]				OFREQ3[3:0]			
Default	0	0	0	0	0	0	0	0

Bits 7 to 4: Output Frequency of OC4 (OFREQ4[3:0]). This field specifies the frequency of output clock OC4. The frequencies of the T0 APLL and T4 APLL are configured in the T0CR1 and T4CR1 registers. The Digital1 and Digital2 frequencies are configured in the MCR7 register. See Section 7.8.2.3. The decode of this field is controlled by the value of the OCR5.AOF4 bit.

AOF4 = 0: (standard decodes)

0000 = Output disabled (i.e., low)
0001 = 2kHz
0010 = 8kHz
0011 = Digital2 (see Table 7-8)
0100 = Digital1 (see Table 7-7)
0101 = T0 APLL frequency divided by 48
0110 = T0 APLL frequency divided by 16
0111 = T0 APLL frequency divided by 12
1000 = T0 APLL frequency divided by 8
1001 = T0 APLL frequency divided by 6
1010 = T0 APLL frequency divided by 4
1011 = T4 APLL frequency divided by 2
1100 = T4 APLL frequency divided by 48
1101 = T4 APLL frequency divided by 16
1110 = T4 APLL frequency divided by 8
1111 = T4 APLL frequency divided by 4

AOF4 = 1: (alternate decodes)

0000 = Output disabled (i.e., low)
0001 = T0 APLL frequency divided by 2
0010 = T0 APLL frequency
0011 = T4 APLL frequency divided by 10
0100 = T0 APLL2 frequency divided by 10
0101 = T0 APLL2 frequency divided by 2
0110 = T0 APLL2 frequency
0111 = T4 selected reference (after dividing)
1000 to 1111 = undefined

Bits 3 to 0: Output Frequency of OC3 (OFREQ3[3:0]). This field specifies the frequency of output clock OC3. The frequencies of the T0 APLL and T4 APLL are configured in the T0CR1 and T4CR1 registers. The Digital1 and Digital2 frequencies are configured in the MCR7 register. See Section 7.8.2.3.The decode of this field is controlled by the value of the OCR5.AOF3 bit.

AOF3 = 0: (standard decodes)

0000 = Output disabled (i.e., low)
0001 = 2kHz
0010 = 8kHz
0011 = Digital2 (see Table 7-8)
0100 = Digital1 (see Table 7-7)
0101 = T0 APLL frequency divided by 48
0110 = T0 APLL frequency divided by 16
0111 = T0 APLL frequency divided by 12
1000 = T0 APLL frequency divided by 8
1001 = T0 APLL frequency divided by 6
1010 = T0 APLL frequency divided by 4

1011 = T4 APLL frequency divided by 64
1100 = T4 APLL frequency divided by 48
1101 = T4 APLL frequency divided by 16
1110 = T4 APLL frequency divided by 8
1111 = T4 APLL frequency divided by 4

AOF3 = 1: (alternate decodes)

0000 = Output disabled (i.e., low)
0001 = T0 APLL frequency divided by 64
0010 = T4 APLL frequency divided by 20
0011 = T4 APLL frequency divided by 12
0100 = T4 APLL frequency divided by 10
0101 = T4 APLL frequency divided by 5
0110 = T4 APLL frequency divided by 2
0111 = T4 selected reference (after dividing)
1000 to 1111 = undefined

Register Name: **OCR3**
Register Description: **Output Configuration Register 3**
Register Address: **62h**

Bit #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	OFREQ6[3:0]				OFREQ5[3:0]			
Default	0	0	0	0	0	0	0	0

Bits 7 to 4: Output Frequency of OC6 (OFREQ6[3:0]). This field specifies the frequency of output clock output OC6. The frequencies of the T0 APLL and T4 APLL are configured in the T0CR1 and T4CR1 registers. The Digital1 and Digital2 frequencies are configured in the MCR7 register. See Section 7.8.2.3.The decode of this field is controlled by the value of the OCR5.AOF6 bit.

AOF6 = 0: (standard decodes)

0000 = Output disabled (i.e., low)
0001 = 2kHz
0010 = 8kHz
0011 = T0 APLL frequency divided by 2
0100 = Digital1 (see Table 7-7)
0101 = T0 APLL frequency
0110 = T0 APLL frequency divided by 16
0111 = T0 APLL frequency divided by 12
1000 = T0 APLL frequency divided by 8
1001 = T0 APLL frequency divided by 6
1010 = T0 APLL frequency divided by 4
1011 = T4 APLL frequency divided by 64
1100 = T4 APLL frequency divided by 48
1101 = T4 APLL frequency divided by 16
1110 = T4 APLL frequency divided by 8
1111 = T4 APLL frequency divided by 4

AOF6 = 1: (alternate decodes)

0000 = Output disabled (i.e., low)
0001 = T4 APLL frequency divided by 5
0010 = T4 APLL frequency divided by 2
0011 = T4 APLL frequency
0100 = T0 APLL2 frequency divided by 5
0101 = T0 APLL2 frequency divided by 2
0110 = T0 APLL2 frequency
0111 = T4 selected reference (after dividing)
1000 to 1111 = undefined

Bits 3 to 0: Output Frequency of OC5 (OFREQ5[3:0]). This field specifies the frequency of output clock OC5. The frequencies of the T0 APLL and T4 APLL are configured in the T0CR1 and T4CR1 registers. The Digital1 and Digital2 frequencies are configured in the MCR7 register. See Section 7.8.2.3. The decode of this field is controlled by the value of the OCR5.AOF5 bit.

AOF5 = 0: (standard decodes)

0000 = Output disabled (i.e., low)
0001 = 2 kHz
0010 = 8 kHz
0011 = Digital2 (see Table 7-8)
0100 = Digital1 (see Table 7-7)
0101 = T0 APLL frequency divided by 48
0110 = T0 APLL frequency divided by 16
0111 = T0 APLL frequency divided by 12
1000 = T0 APLL frequency divided by 8
1001 = T0 APLL frequency divided by 6
1010 = T0 APLL frequency divided by 4

1011 = T4 APLL frequency divided by 2
1100 = T4 APLL frequency divided by 48
1101 = T4 APLL frequency divided by 16
1110 = T4 APLL frequency divided by 8
1111 = T4 APLL frequency divided by 4

AOF5 = 1: (alternate decodes)

0000 = Output disabled (i.e., low)
0001 = T0 APLL frequency divided by 2
0010 = T0 APLL frequency
0011 = T4 APLL frequency divided by 10
0100 = T0 APLL2 frequency divided by 10
0101 = T0 APLL2 frequency divided by 2
0110 = T0 APLL2 frequency
0111 = T4 selected reference (after dividing)
1000 to 1111 = undefined

Register Name: **OCR4**
Register Description: **Output Configuration Register 4**
Register Address: **63h**

Bit #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	MFSEN	FSEN	—	—	OFREQ7[3:0]			
Default	1	1	0	0	0	0	0	0

Bit 7: MFSYNC Enable (MFSEN). This configuration bit enables the 2kHz output on the MFSYNC pin. See Section 7.8.2.4.

0 = Disabled, driven low
1 = Enabled, output is 2kHz

Bit 6: FSYNC Enable (FSEN). This configuration bit enables the 8kHz output on the FSYNC pin. See Section 7.8.2.4.

0 = Disabled, driven low
1 = Enabled, output is 8kHz

Bits 3 to 0: Output Frequency of OC7 (OFREQ7[3:0]). This field specifies the frequency of output clock output OC7. The frequencies of the T0 APLL and T4 APLL are configured in the T0CR1 and T4CR1 registers. The Digital1 and Digital2 frequencies are configured in the MCR7 register. See Section 7.8.2.3. The decode of this field is controlled by the value of the OCR5.AOF7 bit.

AOF7 = 0: (standard decodes)

0000 = Output disabled (i.e., low)
0001 = 2kHz
0010 = 8kHz
0011 = Digital2 (see Table 7-8)
0100 = T0 APLL frequency divided by 2
0101 = T0 APLL frequency divided by 48
0110 = T0 APLL frequency divided by 16
0111 = T0 APLL frequency divided by 12
1000 = T0 APLL frequency divided by 8
1001 = T0 APLL frequency divided by 6
1010 = T0 APLL frequency divided by 4
1011 = T4 APLL frequency divided by 64
1100 = T4 APLL frequency divided by 48
1101 = T4 APLL frequency divided by 16
1110 = T4 APLL frequency divided by 8
1111 = T4 APLL frequency divided by 4

AOF7 = 1: (alternate decodes)

0000 = Output disabled (i.e., low)
0001 = T4 APLL frequency divided by 5
0010 = T4 APLL frequency divided by 2
0011 = T4 APLL frequency
0100 = T0 APLL2 frequency divided by 5
0101 = T0 APLL2 frequency divided by 2
0110 = T0 APLL2 frequency
0111 = T4 selected reference (after dividing)
1000 to 1111 = undefined

Register Name: **T4CR1**
Register Description: **T4 DPLL Configuration Register 1**
Register Address: **64h**

Bit #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	—	—	—	T4FREQ[3:0]			
Default	0	0	0	0	0	1	0	1

Bits 3 to 0: T4 APLL Frequency (T4FREQ[3:0]). When T0CR1:T4APT0 = 0, the T4 APLL DFS is connected to the T4 DPLL, and this field configures the T4 APLL DFS frequency. The T4 APLL DFS frequency affects the frequency of the T4 APLL which in turn affects the available output frequencies on the output clock pins (see the OCR registers). See Section 7.8.2.

T4FREQ[3:0]	T4 APLL DFS FREQUENCY	T4 APLL FREQUENCY (4 x T4 APLL DFS)
0000	APLL output disabled	Disabled, output is low
0001	77.76MHz	311.04MHz (4 x 77.76MHz)
0010	24.576MHz (12 x E1)	98.304MHz (48 x E1)
0011	32.768MHz (16 x E1)	131.072MHz (64 x E1)
0100	37.056MHz (24 x DS1)	148.224MHz (96 x DS1)
0101	24.704MHz (16 x DS1)	98.816MHz (64 x DS1)
0110	68.736MHz (2 x E3)	274.944MHz (8 x E3)
0111	44.736MHz (DS3)	178.944MHz (4 x DS3)
1000	25.248MHz (4 x 6312kHz)	100.992MHz (16 x 6312kHz)
1001	62.500MHz (GbE ÷ 16)	250.000MHz (GbE ÷ 4)
1010	30.720MHz (3 x 10.24)	122.880MHz (12 x 10.24)
1011	40.000MHz (4 x 10MHz)	160.000MHz (16 x 10MHz)
1100	26.000MHz (2 x 13MHz)	104.000MHz (8 x 13MHz)
1101–1111	{unused values}	{unused values}

Register Name: **T0CR1**
Register Description: **T0 DPLL Configuration Register 1**
Register Address: **65h**

Bit #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	T4MT0	T4APT0	T0FT4[2:0]			T0FREQ[2:0]		
Default	0	1	0	0	1	0	0	1

Bit 7: T4 Measure T0 Phase (T4MT0). When this bit is set to 1 the T4 DPLL goes to the free-run mode, and the T4 phase detector is configured to measure the phase difference between the selected T0 DPLL input clock and the selected the T4 DPLL input clock. See Section 7.7.10.

0 = Normal operation for the T4 path
1 = Enable T4-measure-T0-phase mode

Bit 6: T4 APLL Source from T0 (T4APT0). When this bit is set to 0, the T4 APLL DFS is connected to the T4 DPLL, and T4CR1:T4FREQ configures the T4 APLL DFS frequency. The T4 APLL DFS frequency affects the frequency of the T4 APLL which in turn affects the available output frequencies on the output clock pins (see the OCR registers). When this bit is set to 1, the T4 APLL DFS is connected to the T0 DPLL rather than the T4 DPLL, and the frequency of the T4 APLL DFS is configured by the T0CR1:T0FT4[2:0] field below. See Section 7.8.2.

0 = T4 APLL locks to T4 DPLL
1 = T4 APLL locks to T0 DPLL

Bits 5 to 3: T0 Frequency to T4 APLL (T0FT4[2:0]). When the T4APT0 bit is set to 1, this field specifies the frequency of the T4 APLL DFS. This frequency can be different than the frequency specified by T0CR1:T0FREQ. See Section 7.8.2.

T0FT4	T4 APLL DFS FREQUENCY	T4 APLL FREQUENCY (4 x T4 APLL DFS)
000 =	24.576MHz (12 x E1)	98.304MHz (48 x E1)
001 =	62.500MHz (GbE ÷ 16)	250.000MHz (GbE ÷ 4)
010 =	32.768MHz (16 x E1)	131.072MHz (64 x E1)
011 =	{unused value}	{unused value}
100 =	37.056MHz (24 x DS1)	148.224MHz (96 x DS1)
101 =	{unused value}	{unused value}
110 =	24.704MHz (16 x DS1)	98.816MHz (64 x DS1)
111 =	25.248MHz (4 x 6312kHz)	100.992MHz (16 x 6312kHz)

Bits 2 to 0: T0 DPLL Output Frequency (T0FREQ[2:0]). This field configures the T0 APLL DFS frequency. The T0 APLL DFS frequency affects the frequency of the T0 APLL, which in turn affects the available output frequencies on the output clock pins (see the OCR registers). See Section 7.8.2.

T0FREQ	T0 APLL DFS FREQUENCY	T0 APLL FREQUENCY (4 x T0 APLL DFS)
000 =	77.76MHz	311.04MHz (4 x 77.76MHz)
001 =	77.76MHz	311.04MHz (4 x 77.76MHz)
010 =	24.576MHz (12 x E1)	98.304MHz (48 x E1)
011 =	32.768MHz (16 x E1)	131.072MHz (64 x E1)
100 =	37.056MHz (24 x DS1)	148.224MHz (96 x DS1)
101 =	24.704MHz (16 x DS1)	98.816MHz (64 x DS1)
110 =	25.248MHz (4 x 6312kHz)	100.992MHz (16 x 6312kHz)
111 =	62.500MHz (GbE ÷ 16)	250.000MHz (GbE ÷ 4)

Register Name: **T4BW**
Register Description: **T4 Bandwidth Register**
Register Address: **66h**

Bit #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	0	0	0	0	0	0	T4BW[1:0]	
Default	0	0	0	0	0	0	0	0

Bits 2 to 0: T4 DPLL Bandwidth (T4BW[2:0]). See Section 7.7.3.

000 = 18Hz
001 = 35Hz
010 = 70Hz
011 = {unused value, undefined}

Register Name: **T0LBW**
Register Description: **T0 DPLL Locked Bandwidth Register**
Register Address: **67h**

Bit #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	—	—	RSV1	T0LBW[3:0]			
Default	0	0	0	0	1	1	0	1

Bit 4: Reserved Bit 1 (RSV1). This bit is reserved for future use, it can be written to and read back.

Bits 3 to 0: T0 DPLL Locked Bandwidth (T0LBW[3:0]). This field configures the bandwidth of the T0 DPLL when locked to an input clock. When AUTOBW = 0 in the MCR9 register, the T0LBW bandwidth is used for acquisition and for locked operation. When AUTOBW = 1, T0ABW bandwidth is used for acquisition while T0LBW bandwidth is used for locked operation. See Section 7.7.3.

1000 = 0.1Hz
1001 = 0.3Hz
1010 = 0.6Hz
1011 = 1.2Hz
1100 = 2.5Hz
1101 = 4Hz (default)
1110 = 8Hz
1111 = 18Hz
0000 = 35Hz
0001 = 70Hz
0010 = {unused values, undefined}
0011 = 18Hz
0100 = 120Hz
0101 = 250Hz
0110 = 400Hz
0111 = 18Hz

Register Name: **T0ABW**
Register Description: **T0 DPLL Acquisition Bandwidth Register**
Register Address: **69h**

Bit #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	—	—	RSV1	T0ABW[3:0]			
Default	0	0	0	0	1	1	1	1

Bit 4: Reserved Bit 1 (RSV1). This bit is reserved for future use, it can be written to and read back.

Bits 3 to 0: T0 DPLL Acquisition Bandwidth (T0ABW[3:0]). This field configures the bandwidth of the T0 DPLL when acquiring lock. When AUTOBW = 0 in the MCR9 register, the T0LBW bandwidth is used for acquisition and for locked operation. When AUTOBW = 1, T0ABW bandwidth is used for acquisition while T0LBW bandwidth is used for locked operation. See Section 7.7.3.

1000 = 0.1Hz
1001 = 0.3Hz
1010 = 0.6Hz
1011 = 1.2Hz
1100 = 2.5Hz
1101 = 4Hz
1110 = 8Hz
1111 = 18Hz (default)
0000 = 35Hz
0001 = 70Hz
0010 = {unused values, undefined}
0011 = 18Hz
0100 = 120Hz
0101 = 250Hz
0110 = 400Hz
0111 = 18Hz

Register Name: **T4CR2**
Register Description: **T4 Configuration Register 2**
Register Address: **6Ah**

Bit #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	PD2G8K[2:0]			—	DAMP[2:0]		
Default	0	0	0	1	0	0	1	1

Bits 6 to 4: Phase Detector 2 Gain 8kHz (PD2GA8K[2:0]). This field specifies the gain of the T4 phase detector 2 with an input clock of 8kHz or less. This value is only used if automatic gain selection is enabled by setting PD2EN = 1 in the T4CR3 register. See Section 7.7.5.

Bits 2 to 0: Damping Factor (DAMP[2:0]). This field configures the damping factor of the T4 DPLL. Damping factor is a function of both DAMP[2:0] and the T4 DPLL bandwidth (T4BW register). The default value corresponds to a damping factor of 5. See Section 7.7.4.

	18Hz	35Hz	≥ 70Hz
001 =	1.2	1.2	1.2
010 =	2.5	2.5	2.5
011 =	5	5	5
100 =	5	10	10
101 =	5	10	20
000, 110, and 111 =	{unused values}		

The gain peak for each damping factor is shown below:

DAMPING FACTOR	GAIN PEAK (dB)
1.2	0.4
2.5	0.2
5.0	0.1
10	0.06
20	0.03

Register Name: **T0CR2**
Register Description: **T0 Configuration Register 2**
Register Address: **6Bh**

Bit #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	PD2G8K[2:0]			—	DAMP[2:0]		
Default	0	0	0	1	0	0	1	1

Bits 6 to 4: Phase Detector 2 Gain, 8kHz (PD2G8K[2:0]). This field specifies the gain of the T0 phase detector 2 with an input clock of 8kHz or less. This value is only used if automatic gain selection is enabled by setting PD2EN = 1 in the T0CR3 register. See Section 7.7.5.

Bits 2 to 0: Damping Factor (DAMP[2:0]). This field configures the damping factor of the T0 DPLL. Damping factor is a function of both DAMP[2:0] and the T0 DPLL bandwidth (T0ABW and T0LBW). The default value corresponds to a damping factor of 5. See Section 7.7.4.

	≤ 4Hz	8Hz	18Hz	35Hz	≥ 70Hz
001 =	5	2.5	1.2	1.2	1.2
010 =	5	5	2.5	2.5	2.5
011 =	5	5	5	5	5
100 =	5	5	5	10	10
101 =	5	5	5	10	20
000, 110, and 111 =	{unused values}				

The gain peak for each damping factor is shown below:

DAMPING FACTOR	GAIN PEAK (dB)
1.2	0.4
2.5	0.2
5.0	0.1
10	0.06
20	0.03

Register Name: **T4CR3**
Register Description: **T4 Configuration Register 3**
Register Address: **6Ch**

Bit #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	PD2EN	—				PD2G[2:0]		
Default	1	1	0	0	0	0	1	0

Bit 7: Phase Detector 2 Gain Enable (PD2EN). When this bit is set to 1, the T4 phase detector 2 is enabled and the gain is determined by the input locking frequency. If the frequency is greater than 8kHz, the gain is set by the PD2G field. If the frequency is less or equal to 8kHz, the gain is set by the PD2G8K field in the T4CR2 register. See Section 7.7.5.

0 = Disable
1 = Enable

Bits 2 to 0: Phase Detector 2 Gain (PD2G[2:0]). This field specifies the gain of the T4 phase detector 2 when the input frequency is greater than 8kHz. This value is only used if automatic gain selection is enabled by setting PD2EN = 1. See Section 7.7.5.

Register Name: **T0CR3**
Register Description: **T0 Configuration Register 3**
Register Address: **6Dh**

Bit #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	PD2EN	—				PD2G[2:0]		
Default	1	1	0	0	0	0	1	0

Bit 7: Phase Detector 2 Gain Enable (PD2EN). When this bit is set to 1, the T0 phase detector 2 is enabled and the gain is determined by the input locking frequency. If the frequency is greater than 8kHz, the gain is set by the PD2G field. If the frequency is less or equal to 8kHz, the gain is set by the PD2G8K field in the T0CR2 register. See Section 7.7.5.

0 = Disable
1 = Enable

Bits 2 to 0: Phase Detector 2 Gain (PD2G[2:0]). This field specifies the gain of the T0 phase detector 2 when the input frequency is greater than 8kHz. This value is only used if automatic gain selection is enabled by setting PD2EN = 1. See Section 7.7.5.

Register Name: **GPCR**
Register Description: **GPIO Configuration Register**
Register Address: **6Eh**

Bit #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	GPIO4D	GPIO3D	GPIO2D	GPIO1D	GPIO4O	GPIO3O	GPIO2O	GPIO1O
Default	0	0	0	0	0	0	0	0

Bit 7: GPIO4 Direction (GPIO4D). This bit configures the data direction for the GPIO4 pin. When GPIO4 is an input its current state can be read from GPSR:GPIO4. When GPIO4 is an output, its value is controlled by the GPIO4O configuration bit.

0 = Input
1 = Output

Bit 6: GPIO3 Direction (GPIO3D). This bit configures the data direction for the GPIO3 pin. When GPIO3 is an input its current state can be read from GPSR:GPIO3. When GPIO3 is an output, its value is controlled by the GPIO3O configuration bit.

0 = Input
1 = Output

Bit 5: GPIO2 Direction (GPIO2D). This bit configures the data direction for the GPIO2 pin. When GPIO2 is an input its current state can be read from GPSR:GPIO2. When GPIO2 is an output, its value is controlled by the GPIO2O configuration bit.

0 = Input
1 = Output

Bit 4: GPIO1 Direction (GPIO1D). This bit configures the data direction for the GPIO1 pin. When GPIO1 is an input its current state can be read from GPSR:GPIO1. When GPI13 is an output, its value is controlled by the GPIO1O configuration bit.

0 = Input
1 = Output

Bit 3: GPIO4 Output Value (GPIO4O). When GPIO4 is configured as an output (GPIO4D = 1) then this bit specifies the output value.

0 = Low
1 = High

Bit 2: GPIO3 Output Value (GPIO3O). When GPIO3 is configured as an output (GPIO3D = 1) then this bit specifies the output value.

0 = Low
1 = High

Bit 1: GPIO2 Output Value (GPIO2O). When GPIO2 is configured as an output (GPIO2D = 1) then this bit specifies the output value.

0 = Low
1 = High

Bit 0: GPIO1 Output Value (GPIO1O). When GPIO1 is configured as an output (GPIO1D = 1) then this bit specifies the output value.

0 = Low
1 = High

Register Name: **GPSR**
Register Description: **GPIO Status Register**
Register Address: **6Fh**

Bit #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	—	—	—	GPIO4	GPIO3	GPIO2	GPIO1
Default	0	0	0	0	0	0	0	0

Bit 3: GPIO4 State (GPIO4). This bit indicates the current state of the GPIO4 pin.

0 = low
1 = high

Bit 2: GPIO3 State (GPIO3). This bit indicates the current state of the GPIO3 pin.

0 = low
1 = high

Bit 2: GPIO2 State (GPIO2). This bit indicates the current state of the GPIO2 pin.

0 = low
1 = high

Bit 1: GPIO1 State (GPIO1). This bit indicates the current state of the GPIO1 pin.

0 = low
1 = high

Register Name: **OFFSET1**
Register Description: **Phase Offset Register 1**
Register Address: **70h**

Bit #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	OFFSET[7:0]							
Default	0	0	0	0	0	0	0	0

The OFFSET1 and OFFSET2 registers must be read consecutively and written consecutively. See Section 8.3.

Bits 7 to 0: Phase Offset (OFFSET[7:0]). The full 16-bit OFFSET[15:0] field spans this register and the OFFSET2 register. OFFSET is a two's-complement signed integer that specifies the desired phase offset between the output clocks and the selected input reference. The phase offset in picoseconds is equal to OFFSET[15:0] x actual_internal_clock_period / 2^{11}. If the internal clock is at its nominal frequency of 77.76MHz then the phase offset equation simplifies to OFFSET[15:0] x 6.279ps. If, however, the DPLL is locked to a reference whose frequency is +1ppm from ideal, for example, then the actual internal clock period is 1ppm shorter and the phase offset is 1ppm smaller. When the OFFSET field is written, the phase of the output clocks is automatically ramped to the new offset value to avoid loss of synchronization. To adjust the phase offset without changing the phase of the output clocks, use the recalibration process enabled by FSCR3:RECAL. The OFFSET field is ignored when phase build-out is enabled (PBOEN = 1 in the MCR10 register) and when the DPLL is not locked. See Section 7.7.8.

Register Name: **OFFSET2**
Register Description: **Phase Offset Register 2**
Register Address: **71h**

Bit #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	OFFSET[15:8]							
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: Phase Offset (OFFSET[15:8]). See the OFFSET1 register description.

Register Name: **PBOFF**
Register Description: **Phase Build-Out Offset Register**
Register Address: **72h**

Bit #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	—	PBOFF[5:0]					
Default	0	0	0	0	0	0	0	0

Bits 5 to 0: Phase Build-Out Offset Register (PBOFF[5:0]). An uncertainty of up to 5ns is introduced each time a phase build-out event occurs. This uncertainty results in a phase hit on the output. Over a large number of phase build-out events the mean error should be zero. The PBOFF field specifies a fixed offset for each phase build-out event to skew the average error toward zero. This field is a two's-complement signed integer. The offset in nanoseconds is PBOFF[5:0] x 0.101. Values greater than 1.4ns or less than -1.4ns can cause internal math errors and should not be used. See Section 7.7.7.2.

Register Name: **PHLIM1**
Register Description: **Phase Limit Register 1**
Register Address: **73h**

Bit #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	FLEN	NALOL	1	—	—	FINELIM[2:0]		
Default	1	0	1	0	0	0	1	0

Bit 7: Fine Phase Limit Enable (FLEN). This configuration bit enables the fine phase limit specified in the FINELIM[2:0] field. The fine limit must be disabled for multi-UI jitter tolerance (see PHLIM2 fields). This field controls both T0 and T4. See Section 7.7.6.

0 = Disabled
1 = Enabled

Bit 6: No-Activity Loss of Lock (NALOL). The T0 and the T4 DPLLs can detect that an input clock has no activity very quickly (within two clock cycles). When NALOL = 0, loss-of-lock is not declared when clock cycles are missing, and nearest edge locking (±180°) is used when the clock recovers. This gives tolerance to missing cycles. When NALOL = 1, loss-of-lock is indicated as soon as no activity is detected, and the device switches to phase/frequency locking (±360°). This field controls both T0 and T4. See Sections 7.5.3 and 7.7.6.

0 = No activity does not trigger loss-of-lock
1 = No activity does trigger loss-of-lock

Bit 5: Leave set to 1 (test control).

Bits 2 to 0: Fine Phase Limit (FINELIM[2:0]). This field specifies the fine phase limit window, outside of which loss-of-lock is declared. The FLEN bit enables this feature. The phase of the input clock has to be inside the fine limit window for two seconds before phase lock is declared. Loss-of-lock is declared immediately if the phase of the input clock is outside the phase limit window. The default value of 010 is appropriate for most situations. This field controls both T0 and T4. See Section 7.7.6.

000 = Always indicates loss of phase lock—do not use
001 = Small phase limit window, ±45 to ±90°
010 = Normal phase limit window, ±90 to ±180° (default)
100, 101, 110, 111 = Proportionately larger phase limit window

Register Name: **PHLIM2**
Register Description: **Phase Limit Register 2**
Register Address: **74h**

Bit #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	CLEN	MCPDEN	USEMCPD	—	COARSELIM[3:0]			
Default	1	0	0	0	0	1	0	1

Bit 7: Coarse Phase Limit Enable (CLEN). This configuration bit enables the coarse phase limit specified in the COARSELIM[3:0] field. This field controls both T0 and T4. See Section 7.7.6.

0 = Disabled
1 = Enabled

Bit 6: Multicycle Phase Detector Enable (MCPDEN). This configuration bit enables the multicycle phase detector and allows the DPLL to tolerate large-amplitude jitter and wander. The range of this phase detector is the same as the coarse phase limit specified in the COARSELIM[3:0] field. This field controls both T0 and T4. See Section 7.7.5.

0 = Disabled
1 = Enabled

Bit 5: Use Multicycle Phase Detector in the DPLL Algorithm (USEMCPD). This configuration bit enables the DPLL algorithm to use the multicycle phase detector so that a large phase measurement drives faster DPLL pull-in. When USEMCPD = 0, phase measurement is limited to ±360°, giving slower pull-in at higher frequencies but with less overshoot. When USEMCPD = 1, phase measurement is set as specified in the COARSELIM[3:0] field, giving faster pull-in. MCPDEN should be set to 1 when USEMCPD = 1. This field controls both T0 and T4. See Section 7.7.5.

0 = Disabled
1 = Enabled

Bits 3 to 0: Coarse Phase Limit (COARSELIM[3:0]). This field specifies the coarse phase limit and the tracking range of the multicycle phase detector. The CLEN bit enables this feature. If jitter tolerance greater than 0.5UI is required and the input clock is a high frequency signal then the DPLL can be configured to track phase errors over many UI using the multicycle phase detector. This field controls both T0 and T4. See Section 7.7.5 and 7.7.6.

0000 = ±1UI
0001 = ±3UI
0010 = ±7UI
0011 = ±15UI
0100 = ±31UI
0101 = ±63UI
0110 = ±127UI
0111 = ±255UI
1000 = ±511UI
1001 = ±1023UI
1010 = ±2047UI
1011 = ±4095UI
1100 to 1111 = ±8191UI

Register Name: **PHMON**
Register Description: **Phase Monitor Register**
Register Address: **76h**

Bit #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	NW	—	—	—	—			
Default	0	0	0	0	0	1	1	0

Bit 7: Low-Frequency Input Clock Noise Window (NW). For 2kHz, 4kHz, or 8kHz input clocks, this configuration bit enables a ±5% tolerance noise window centered around the expected clock edge location. Noise-induced edges outside this window are ignored, reducing the possibility of phase hits on the output clocks. This only applies to the T0 DPLL and should be enabled only when the T0 DPLL is locked to an input and the 180 phase detector is being used.

0 = All edges are recognized by the T0 DPLL
1 = Only edges within the ±5% tolerance window are recognized by the T0 DPLL

Register Name: **PHASE1**
Register Description: **Phase Register 1**
Register Address: **77h**

Bit #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	PHASE[7:0]							
Default	0	0	0	0	0	0	0	0

Note: *The PHASE1 and PHASE2 registers must be read consecutively. See Section 8.3.*

Bits 7 to 0: Current DPLL Phase (PHASE[7:0]). The full 16-bit PHASE[15:0] field spans this register and the PHASE2 register. PHASE is a two's-complement signed integer that indicates the current value of the phase detector. The value is the output of the phase averager. When T4T0 = 0 in the MCR11 register, PHASE indicates the current phase of the T0 DPLL. When T4T0 = 1, PHASE indicates the current phase of the T4 DPLL. The averaged phase difference in degrees is equal to PHASE x 0.707. See Section 7.7.10.

Register Name: **PHASE2**
Register Description: **Phase Register 2**
Register Address: **78h**

Bit #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	PHASE[15:8]							
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: Current DPLL Phase (PHASE[15:8]). See the PHASE1 register description.

Register Name: **PHLKTO**
Register Description: **Phase Lock Timeout Register**
Register Address: **79h**

Bit #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	PHLKTOM[1:0]		PHLKTO[5:0]					
Default	0	0	1	1	0	0	1	0

Bits 7 to 6: Phase Lock Timeout Multiplier (PHLKTOM[1:0]). This field is an unsigned integer that specifies the resolution of the phase lock timeout field PHLKTO[5:0].

00 = 2 seconds
01 = 4 seconds
10 = 8 seconds
11 = 16 seconds

Bits 5 to 0: Phase Lock Timeout (PHLKTO[5:0]). This field is an unsigned integer that, together with the PHLKTOM[1:0] field, specifies the length of time that the T0 DPLL attempts to lock to an input clock before declaring a phase lock alarm (by setting the corresponding LOCK bit in the ISR registers). The timeout period in seconds is PHLKTO[5:0] x 2^(PHLKTOM[1:0]+1). The state machine remains in the prelocked, prelocked 2, or phase-lost modes for the specified time before declaring a phase alarm on the selected input. See Section 7.7.1.

Register Name: **FSCR1**
Register Description: **Frame Sync Configuration Register 1**
Register Address: **7Ah**

Bit #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	2K8KSRC	SYNCSRC[2:0]			8KINV	8KPUL	2KINV	2KPUL
Default	0	0	0	0	0	0	0	0

Bit 7: 2kHz/8kHz Source (2K8KSRC). This configuration bit specifies the source for the 2kHz and 8kHz outputs available on clock outputs. When MCR4:LKT4T0 = 1 it is always connected to the T0 DPLL. See Section 7.8.2.3.

0 = T0 DPLL
1 = T4 DPLL

Bit 6 to 4: SYNC123 Source (SYNCSRC). This field determines whether the SYNC1, SYNC2, or SYNC3 pins are associated with the selected input clock or forced to be associated with a specific input clock. See Section 7.9.3.

0XX = SYNC[1:3] pins associated with T0 DPLL selected reference IC3 or IC5, IC4 or IC6, IC9, or IC2
1X0 = SYNC1 pin associated with IC3, SYNC2 pin associated with IC4
1X1 = SYNC1 pin associated with IC5, SYNC2 pin associated with IC6
10X = SYNC3 pin associated with IC9
11X = SYNC3 pin associated with IC2

Bit 3: 8kHz Invert (8KINV). When this bit is set to 1 the 8kHz signal on clock output FSYNC is inverted. See Section 7.8.2.4.

0 = FSYNC not inverted
1 = FSYNC inverted

Bit 2: 8kHz Pulse (8KPUL). When this bit is set to 1, the 8kHz signal on clock output FSYNC is pulsed rather than 50% duty cycle. In this mode output clock OC3 must be enabled, and the pulse width of FSYNC is equal to the clock period of OC3. See Section 7.8.2.4.

0 = FSYNC not pulsed; 50% duty cycle
1 = FSYNC pulsed, with pulse width equal to OC3 period

Bit 1: 2kHz Invert (2KINV). When this bit is set to 1 the 2kHz signal on clock output MFSYNC is inverted. See Section 7.8.2.4.

0 = MFSYNC not inverted
1 = MFSYNC inverted

Bit 0: 2kHz Pulse (2KPUL). When this bit is set to 1, the 2kHz signal on clock output MFSYNC is pulsed rather than 50% duty cycle. In this mode output clock OC3 must be enabled, and the pulse width of MFSYNC is equal to the clock period of OC3. See Section 7.8.2.4.

0 = MFSYNC not pulsed; 50% duty cycle
1 = MFSYNC pulsed, with pulse width equal to OC3 period

Register Name: **FSCR2**
Register Description: **Frame Sync Configuration Register 2**
Register Address: **7Bh**

Bit #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	INDEP	OCN	PHASE3[1:0]		PHASE2[1:0]		PHASE1[1:0]	
Default	0	0	0	0	0	0	0	0

Bit 7: Independent Frame Sync and Multiframe Sync (INDEP). When this bit is set to 0, the 8kHz frame sync on FSYNC and the 2kHz multiframe sync on MFSYNC are aligned with the other output clocks when synchronized with the SYNCn input. When this bit is 1, the frame sync and multiframe sync are independent of the other output clocks, and their edge position may change without disturbing the other output clocks. See Section 7.9.5.

0 = FSYNC and MFSYNC are aligned with other output clocks; all are synchronized by the SYNCn input
1 = FSYNC and MFSYNC are independent of the other clock outputs; only FSYNC and MFSYNC are synchronized by the SYNCn input

Bit 6: Sync OC-N Rates (OCN). See Section 7.9.2.

0 = SYNCn is sampled with a 6.48MHz resolution; the selected reference must be 6.48MHz
1 = If the selected reference is 19.44MHz, SYNCn is sampled at 19.44MHz and output alignment is to 19.44MHz. If the selected reference is 38.88MHz, SYNCn is sampled at 38.88MHz. The selected reference must be either 19.44MHz or 38.88MHz

Bits 5 to 4: External Sync Sampling Phase 3 (PHASE3[1:0]). This field adjusts the sampling of the SYNC3 input pin. Normally the falling edge of SYNC3 is aligned with the falling edge of the selected reference. All UI numbers listed below are UI of the sampling clock. See Section 7.9.1.

00 = Coincident
01 = 0.5UI early
10 = 1UI late
11 = 0.5UI late

Bits 3 to 2: External Sync Sampling Phase 2 (PHASE2[1:0]). This field adjusts the sampling of the SYNC2 input pin. Normally the falling edge of SYNC2 is aligned with the falling edge of the selected reference. All UI numbers listed below are UI of the sampling clock. See Section 7.9.1.

00 = Coincident
01 = 0.5UI early
10 = 1UI late
11 = 0.5UI late

Bits 1 to 0: External Sync Sampling Phase 1 (PHASE1[1:0]). This field adjusts the sampling of the SYNC1 input pin. Normally the falling edge of SYNC1 is aligned with the falling edge of the selected reference. All UI numbers listed below are UI of the sampling clock. See Section 7.9.1.

00 = Coincident
01 = 0.5UI early
10 = 1UI late
11 = 0.5UI late

Register Name: **FSCR3**
Register Description: **Frame Sync Configuration Register 3**
Register Address: **7Ch**

Bit #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	RECAL	MONLIM[2:0]			SOURCE[3:0]			
Default	0	0	1	0	1	0	1	1

Bit 7: Phase Offset Recalibration (RECAL). When set to 1 this configuration bit causes a recalibration of the phase offset between the output clocks and the selected reference. This process puts the DPLL into mini holdover, internally ramps the phase offset to zero, resets all clock dividers, ramps the phase offset to the value stored in the OFFSET registers, and then switches the DPLL out of mini holdover. Unlike simply writing the OFFSET registers, the RECAL process causes no change in the phase offset of the output clocks. RECAL is automatically reset to 0 when recalibration is complete. See Section 7.7.8.

0 = Normal operation
1 = Phase offset recalibration

Bits 6 to 4: Sync Monitor Limit (MONLIM[2:0]). This field configures the sync monitor limit. When the external frame sync input is misaligned with respect to the MFSYNC output by the specified number of resampling clock cycles then a frame sync monitor alarm is declared in the FSMON bit of the OPSTATE register. See Section 7.9.6.

000 = ± 1UI
001 = ± 2UI
010 = ± 3UI
011 = ± 4UI
100 = ± 5UI
101 = ± 6UI
110 = ± 7UI
111 = ± 8UI

Bits 3 to 0: Sync Reference Source (SOURCE[3:0]). There are two modes of external frame sync operation, a mode using a single input pin (SYNC1) and a mode using three input pins (SYNC1, SYNC2, and SYNC3).

When SOURCE = 11XX one of The SYNC1, SYNC2, and SYNC3 pins is selected as the external sync reference depending on which input clock is selected for T0. See Section 7.9.7.

When SOURCE! = 11XX and automatic external frame sync is enabled (AEFSEN = 1 in the MCR3 register), the external sync reference on the SYNC1 pin is enabled when the T0 DPLL is locked to the input clock specified by the SOURCE field. See Section 7.9.

0000 = {unused value, undefined}
0001 = IC1
0010 = IC2
0011 = IC3
0100 = IC4
0101 = IC5
0110 = IC6
0111 = {unused value, undefined}
1000 = IC8
1001 = IC9
1010 to 1011 = {unused value, undefined}
11XX = SYNC1, SYNC2, and SYNC3 enabled (see Section 7.9.7)

Register Name: **INTCR**
Register Description: **Interrupt Configuration Register**
Register Address: **7Dh**

Bit #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	—	—	—	LOS	GPO	OD	POL
Default	0	0	0	0	0	0	1	0

Bit 3: INTREQ Pin Mode (LOS). When GPO = 0 this bit selects the function of the INTREQ pin.

0 = The INTREQ/LOS pin indicates interrupt requests
1 = The INTREQ/LOS pin indicates the real-time state of the selected reference activity monitor (see Section 7.5.3). This function is most useful when external switching mode (Section 7.6.5) is enabled (MCR10:EXTSW = 1).

Bit 2: INTREQ Pin General-Purpose Output Enable (GPO). When set to 1 this bit configures the interrupt request pin to be a general-purpose output whose value is set by the POL bit.

0 = INTREQ is function determined by the LOS bit
1 = INTREQ is a general-purpose output

Bit 1: INTREQ Pin Open-Drain Enable (OD).

When GPO = 0:
0 = INTREQ is driven in both inactive and active states
1 = INTREQ is driven high or low in the active state but is high impedance in the inactive state
When GPO = 1:
0 = INTREQ is driven as specified by POL
1 = INTREQ is high impedance and POL has no effect

Bit 0: INTREQ Pin Polarity (POL).

When GPO = 0:
0 = INTREQ goes low to signal an interrupt request or LOS = 1 (active low)
1 = INTREQ goes high to signal interrupt request or LOS = 1 (active high)
When GPO = 1:
0 = INTREQ driven low
1 = INTREQ driven high

Register Name: **PROT**
Register Description: **Protection Register**
Register Address: **7Eh**

Bit #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	PROT[7:0]							
Default	1	0	0	0	0	1	0	1

Bits 7 to 0: Protection Control (PROT[7:0]). This field can be used to protect the rest of the register set from inadvertent writes. In protected mode writes to all other registers are ignored. In single unprotected mode, one register (other than PROT) can be written, but after that write the device reverts to protected mode (and the value of PROT is internally changed to 00h). In fully unprotected mode all register can be written without limitation. See Section 7.2.

1000 0101 = Fully unprotected mode
1000 0110 = Single unprotected mode
All other values = Protected mode

9. JTAG Test Access Port and Boundary Scan

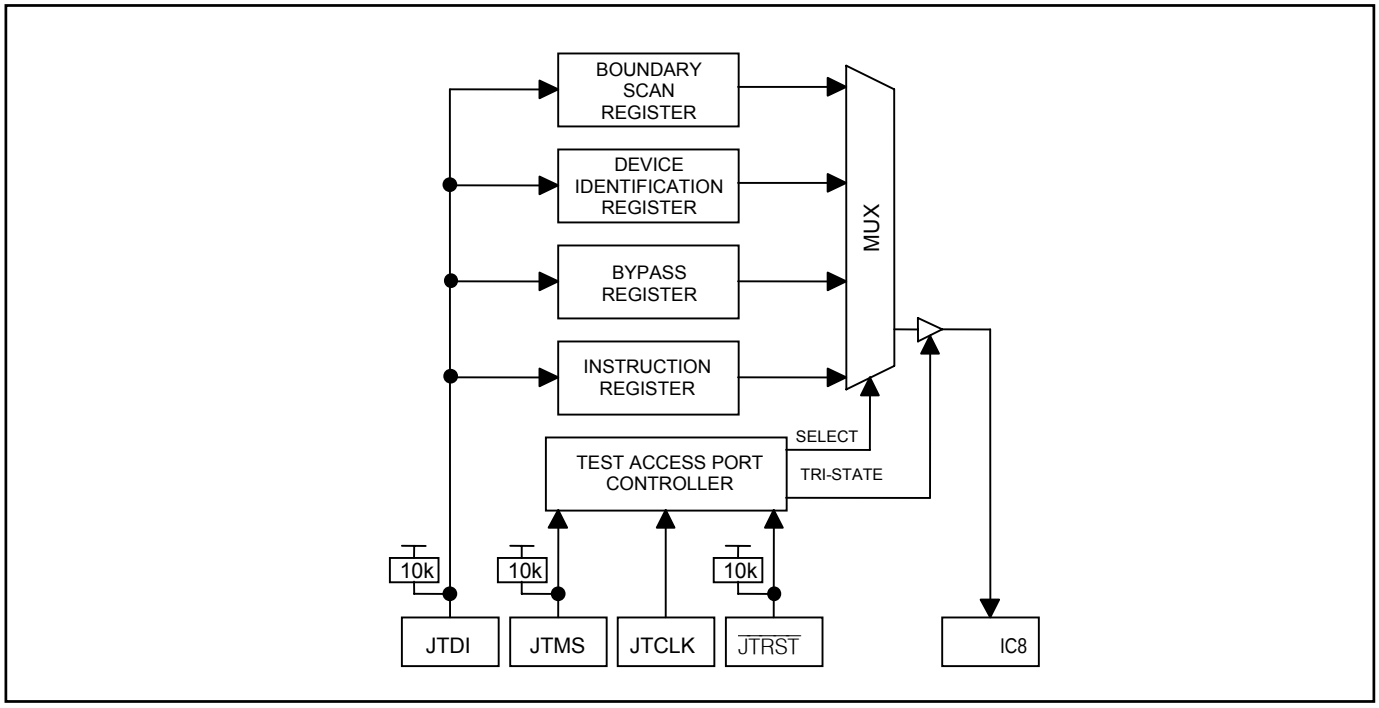
9.1 JTAG Description

The DS3104-SE supports the standard instruction codes SAMPLE/PRELOAD, BYPASS, and EXTEST. Optional public instructions included are HIGHZ, CLAMP, and IDCODE. Figure 9-1 shows a block diagram. The DS3104-SE contains the following items, which meet the requirements set by the IEEE 1149.1 Standard Test Access Port and Boundary Scan Architecture:

Test Access Port (TAP)	Bypass Register
TAP Controller	Boundary Scan Register
Instruction Register	Device Identification Register

The TAP has the necessary interface pins, namely JTCLK, $\overline{\text{JTRST}}$, JTDI, JTDO, and JTMS. Details on these pins can be found in Table 6-5. Details about the boundary scan architecture and the TAP can be found in IEEE 1149.1-1990, IEEE 1149.1a-1993, and IEEE 1149.1b-1994.

Figure 9-1. JTAG Block Diagram



9.2 JTAG TAP Controller State Machine Description

This section discusses the operation of the TAP controller state machine. The TAP controller is a finite state machine that responds to the logic level at JTMS on the rising edge of JTCLK. Each of the states denoted in Figure 9-2 is described in the following paragraphs.

Test-Logic-Reset. Upon device power-up, the TAP controller starts in the Test-Logic-Reset state. The instruction register contains the IDCODE instruction. All system logic on the device operates normally.

Run-Test-Idle. Run-Test-Idle is used between scan operations or during specific tests. The instruction register and all test registers remain idle.

Select-DR-Scan. All test registers retain their previous state. With JTMS low, a rising edge of JTCLK moves the controller into the Capture-DR state and initiates a scan sequence. JTMS high moves the controller to the Select-IR-SCAN state.

Capture-DR. Data can be parallel-loaded into the test register selected by the current instruction. If the instruction does not call for a parallel load or the selected test register does not allow parallel loads, the register remains at its current value. On the rising edge of JTCLK, the controller goes to the Shift-DR state if JTMS is low or to the Exit1-DR state if JTMS is high.

Shift-DR. The test register selected by the current instruction is connected between JTDI and JTDO and data is shifted one stage toward the serial output on each rising edge of JTCLK. If a test register selected by the current instruction is not placed in the serial path, it maintains its previous state.

Exit1-DR. While in this state, a rising edge on JTCLK with JTMS high puts the controller in the Update-DR state, which terminates the scanning process. A rising edge on JTCLK with JTMS low puts the controller in the Pause-DR state.

Pause-DR. Shifting of the test registers is halted while in this state. All test registers selected by the current instruction retain their previous state. The controller remains in this state while JTMS is low. A rising edge on JTCLK with JTMS high puts the controller in the Exit2-DR state.

Exit2-DR. While in this state, a rising edge on JTCLK with JTMS high puts the controller in the Update-DR state and terminates the scanning process. A rising edge on JTCLK with JTMS low puts the controller in the Shift-DR state.

Update-DR. A falling edge on JTCLK while in the Update-DR state latches the data from the shift register path of the test registers into the data output latches. This prevents changes at the parallel output because of changes in the shift register. A rising edge on JTCLK with JTMS low puts the controller in the Run-Test-Idle state. With JTMS high, the controller enters the Select-DR-Scan state.

Select-IR-Scan. All test registers retain their previous state. The instruction register remains unchanged during this state. With JTMS low, a rising edge on JTCLK moves the controller into the Capture-IR state and initiates a scan sequence for the instruction register. JTMS high during a rising edge on JTCLK puts the controller back into the Test-Logic-Reset state.

Capture-IR. The Capture-IR state is used to load the shift register in the instruction register with a fixed value. This value is loaded on the rising edge of JTCLK. If JTMS is high on the rising edge of JTCLK, the controller enters the Exit1-IR state. If JTMS is low on the rising edge of JTCLK, the controller enters the Shift-IR state.

Shift-IR. In this state, the instruction register's shift register is connected between JTDI and JTDO and shifts data one stage for every rising edge of JTCLK toward the serial output. The parallel register and the test registers remain at their previous states. A rising edge on JTCLK with JTMS high moves the controller to the Exit1-IR state. A rising edge on JTCLK with JTMS low keeps the controller in the Shift-IR state, while moving data one stage through the instruction shift register.

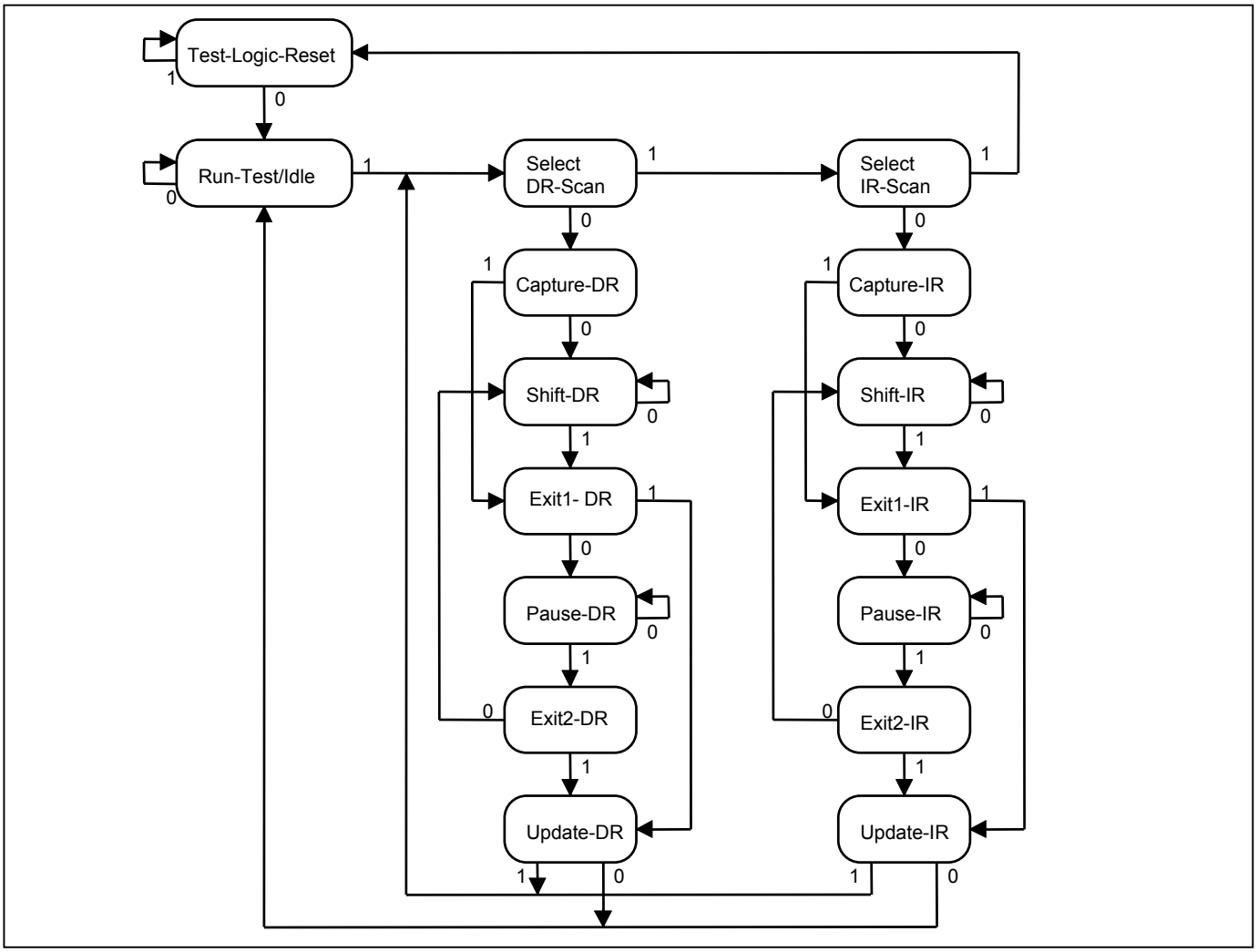
Exit1-IR. A rising edge on JTCLK with JTMS low puts the controller in the Pause-IR state. If JTMS is high on the rising edge of JTCLK, the controller enters the Update-IR state and terminates the scanning process.

Pause-IR. Shifting of the instruction register is halted temporarily. With JTMS high, a rising edge on JTCLK puts the controller in the Exit2-IR state. The controller remains in the Pause-IR state if JTMS is low during a rising edge on JTCLK.

Exit2-IR. A rising edge on JTCLK with JTMS high puts the controller in the Update-IR state. The controller loops back to the Shift-IR state if JTMS is low during a rising edge of JTCLK in this state.

Update-IR. The instruction shifted into the instruction shift register is latched into the parallel output on the falling edge of JTCLK as the controller enters this state. Once latched, this instruction becomes the current instruction. A rising edge on JTCLK with JTMS low puts the controller in the Run-Test-Idle state. With JTMS high, the controller enters the Select-DR-Scan state.

Figure 9-2. JTAG TAP Controller State Machine



9.3 JTAG Instruction Register and Instructions

The instruction register contains a shift register as well as a latched parallel output and is 3 bits in length. When the TAP controller enters the Shift-IR state, the instruction shift register is connected between JTDI and JTDO. While in the Shift-IR state, a rising edge on JTCLK with JTMS low shifts data one stage toward the serial output at JTDO. A rising edge on JTCLK in the Exit1-IR state or the Exit2-IR state with JTMS high moves the controller to the Update-IR state. The falling edge of that same JTCLK latches the data in the instruction shift register to the instruction parallel output. Table 9-1 shows the instructions supported by the DS3104-SE and their respective operational binary codes.

Table 9-1. JTAG Instruction Codes

INSTRUCTIONS	SELECTED REGISTER	INSTRUCTION CODES
SAMPLE/PRELOAD	Boundary Scan	010
BYPASS	Bypass	111
EXTEST	Boundary Scan	000
CLAMP	Bypass	011
HIGHZ	Bypass	100
IDCODE	Device Identification	001

SAMPLE/PRELOAD. SAMPLE/RELOAD is a mandatory instruction for the IEEE 1149.1 specification. This instruction supports two functions. First, the digital I/Os of the device can be sampled at the boundary scan register, using the Capture-DR state, without interfering with the device's normal operation. Second, data can be shifted into the boundary scan register through JTDI using the Shift-DR state.

EXTEST. EXTEST allows testing of the interconnections to the device. When the EXTEST instruction is latched in the instruction register, the following actions occur: (1) Once the EXTEST instruction is enabled through the Update-IR state, the parallel outputs of the digital output pins are driven. (2) The boundary scan register is connected between JTDI and JTDO. (3) The Capture-DR state samples all digital inputs into the boundary scan register.

BYPASS. When the BYPASS instruction is latched into the parallel instruction register, JTDI is connected to JTDO through the 1-bit bypass register. This allows data to pass from JTDI to JTDO without affecting the device's normal operation.

IDCODE. When the IDCODE instruction is latched into the parallel instruction register, the device identification register is selected. The device ID code is loaded into the device identification register on the rising edge of JTCLK, following entry into the Capture-DR state. Shift-DR can be used to shift the ID code out serially through JTDO. During Test-Logic-Reset, the ID code is forced into the instruction register's parallel output.

HIGHZ. All digital outputs are placed into a high-impedance state. The bypass register is connected between JTDI and JTDO.

CLAMP. All digital output pins output data from the boundary scan parallel output while connecting the bypass register between JTDI and JTDO. The outputs do not change during the CLAMP instruction.

9.4 JTAG Test Registers

IEEE 1149.1 requires a minimum of two test registers—the bypass register and the boundary scan register. An optional test register, the identification register, has been included in the device design. It is used with the IDCODE instruction and the Test-Logic-Reset state of the TAP controller.

Bypass Register. This is a single 1-bit shift register used with the BYPASS, CLAMP, and HIGHZ instructions to provide a short path between JTDI and JTDO.

Boundary Scan Register. This register contains a shift register path and a latched parallel output for control cells and digital I/O cells. BSDL files are available at www.maxim-ic.com/TechSupport/telecom/bsdl.htm.

Identification Register. This register contains a 32-bit shift register and a 32-bit latched parallel output. It is selected during the IDCODE instruction and when the TAP controller is in the Test-Logic-Reset state. The device identification code for the DS3104-SE is shown in Table 9-2.

Table 9-2. JTAG ID Code

DEVICE	REVISION	DEVICE CODE	MANUFACTURER CODE	REQUIRED
DS3104-SE	Consult factory	0000000010100010	00010100001	1

10. Electrical Characteristics

ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin with Respect to V_{SS} (except V_{DD})……..-0.3V to +5.5V
Supply Voltage Range (V_{DD}) with Respect to V_{SS}……..-0.3V to +1.98V
Supply Voltage Range (V_{DDIO}) with Respect to V_{SS}……-0.3V to +3.63V
Ambient Operating Temperature Range……-40°C to +85°C
Junction Operating Temperature Range……..-40°C to +125°C
Storage Temperature Range……..-55°C to +125°C
Soldering Temperature……See IPC/JEDEC J-STD-020 Specification

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to the absolute maximum rating conditions for extended periods may affect device. Ambient operating temperature range when device is mounted on a four-layer JEDEC test board with no airflow.

Note: The typical values listed in the tables of Section 10 are not production tested.

10.1 DC Characteristics

Table 10-1. Recommended DC Operating Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage, Core	VDD		1.62	1.8	1.98	V
Supply Voltage, I/O	VDDIO		3.135	3.3	3.465	V
Ambient Temperature Range	T_A		-40		+85	°C
Junction Temperature Range	T_J		-40		+125	°C

Table 10-2. DC Characteristics

(VDD = 1.8V ±10%; VDDIO = 3.3V ±5%, T_A = -40°C to +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current, Core	I_{DD}	(Notes 1, 2)		160	185	mA
Supply Current, I/O	I_{DDIO}	(Notes 1, 2)		29	45	mA
Supply Current from VDD_OC45 When Outputs OC4 and OC5 Enabled	I_{DDOC45}	(Note 3)		16		mA
Supply Current from VDD_OC67 When Outputs OC6 and OC7 Enabled	I_{DDOC67}	(Note 3)		16		mA
Input Capacitance	C_{IN}			5		pF
Output Capacitance	C_{OUT}			7		pF

Note 1: 12.800MHz clock applied to REFCLK and 19.44 MHz clock applied to one CMOS/TTL input clock pin. One 19.44MHz CMOS/TTL output clock pin driving 100pF load; all other inputs at VDDIO or grounded; all other outputs disabled and open.

Note 2: TYP current measured at VDD = 1.8V and VDDIO = 3.3V, MAX current measured at VDD = 1.98V and VDDIO = 3.465V.

Note 3: 19.44MHz output clock frequency, driving the load shown in Figure 10-1.

Table 10-3. CMOS/TTL Pins

(VDD = 1.8V ±10%; VDDIO = 3.3V ±5%, T_A = -40°C to +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2.0		5.5	V
Input Low Voltage	V_{IL}		-0.3		+0.8	V
Input Leakage	I_{IL}	(Note 1)	-10		+10	µA
Input Leakage, Pins with Internal Pullup Resistor (50kΩ typ)	I_{ILPU}	(Note 1)	-85		+10	µA
Input Leakage, Pins with Internal Pulldown Resistor (50kΩ typ)	I_{ILPD}	(Note 1)	-10		+85	µA
Output Leakage (when High Impedance)	I_{LO}	(Note 1)	-10		+10	µA
Output High Voltage (I_O = -4.0mA)	V_{OH}		2.4		VDDIO	V
Output High Voltage (I_O = -4.0mA)	V_{OH}	(Note 2)	2.0		VDDIOB	V
Output Low Voltage (I_O = +4.0mA)	V_{OL}		0		0.4	V

Note 1: 0V < V_{IN} < VDDIO for all other digital inputs.

Note 2: For OC1B through OC5B when VDDIOB = 2.5V.

Table 10-4. LVDS/LVPECL Input Pins

(VDD = 1.8V ±10%; VDDIO = 3.3V ±5%, T_A = -40°C to +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Tolerance	V_{TOL}	(Note 1)	0		VDDIO	V
Input Voltage Range	V_{IN}	V_{ID} = 100mV	0		2.4	V
Input Differential Voltage	V_{ID}		0.1		1.4	V
Input Differential Logic Threshold	V_{IDTH}		-100		+100	mV

Note 1: The device can tolerate this range of voltages w.r.t. VSS on its ICxPOS and ICxNEG pins without being damaged. Proper operation of the differential input circuitry is only guaranteed when the other specifications in this table are met.

Table 10-5. LVDS Output Pins

(VDD = 1.8V ±10%; VDDIO = 3.3V ±5%, T_A = -40°C to +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OHLVDS}	(Note 1)			1.6	V
Output Low Voltage	V_{OLLVDS}	(Note 1)	0.9			V
Differential Output Voltage	V_{ODLVDS}		247	350	454	mV
Output Offset (Common Mode) Voltage	V_{OSLVDS}	25°C (Note 1)	1.125	1.25	1.375	V
Difference in Magnitude of Output Differential Voltage for Complementary States	$V_{DOSLVDS}$				25	mV

Note 1: With 100Ω load across the differential outputs.

Note 2: The differential outputs can easily be interfaced to LVDS, LVPECL, and CML inputs on neighboring ICs using a few external passive components. See Maxim App Note HFAN-1.0 for details.

Table 10-6. LVPECL Level-Compatible Output Pins

(VDD = 1.8V ±10%; VDDIO = 3.3V ±5%, T_A = -40°C to +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Differential Output Voltage	V_{ODPECL}		595	700	930	mV
Output Offset (Common Mode) Voltage	V_{OSPECL}	25°C (Note 1)		0.8		V
Difference in Magnitude of Output Differential Voltage for Complementary States	$V_{DOSPECL}$				50	mV

Note 1: With 100Ω load across the differential outputs.

Note 2: The differential outputs can easily be interfaced to LVDS, LVPECL, and CML inputs on neighboring ICs using a few external passive components. See Maxim App Note HFAN-1.0 for details.

Figure 10-1. Recommended Termination for LVDS Pins

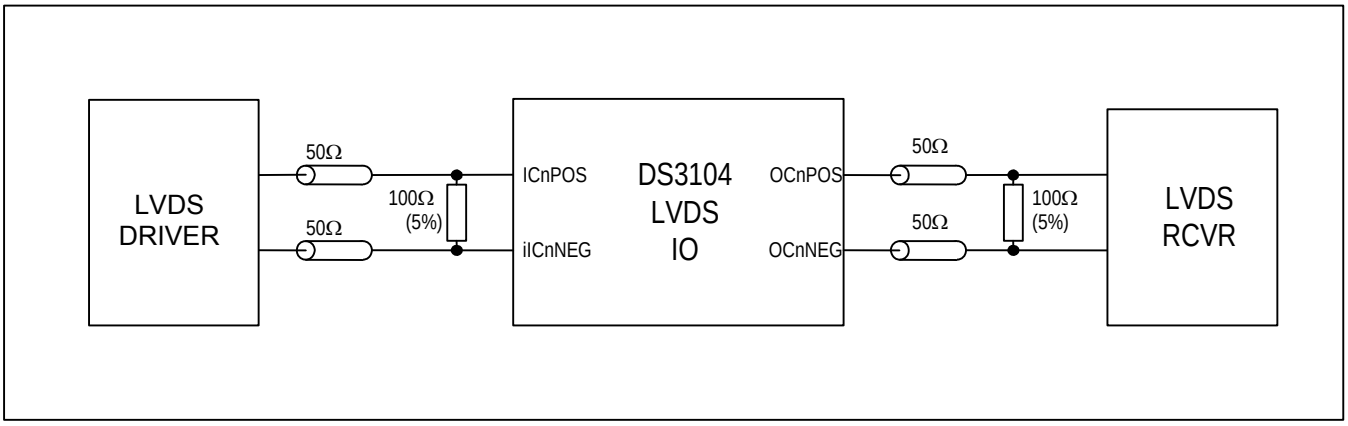


Figure 10-2. Recommended Termination for LVPECL Signals on LVDS Input Pins

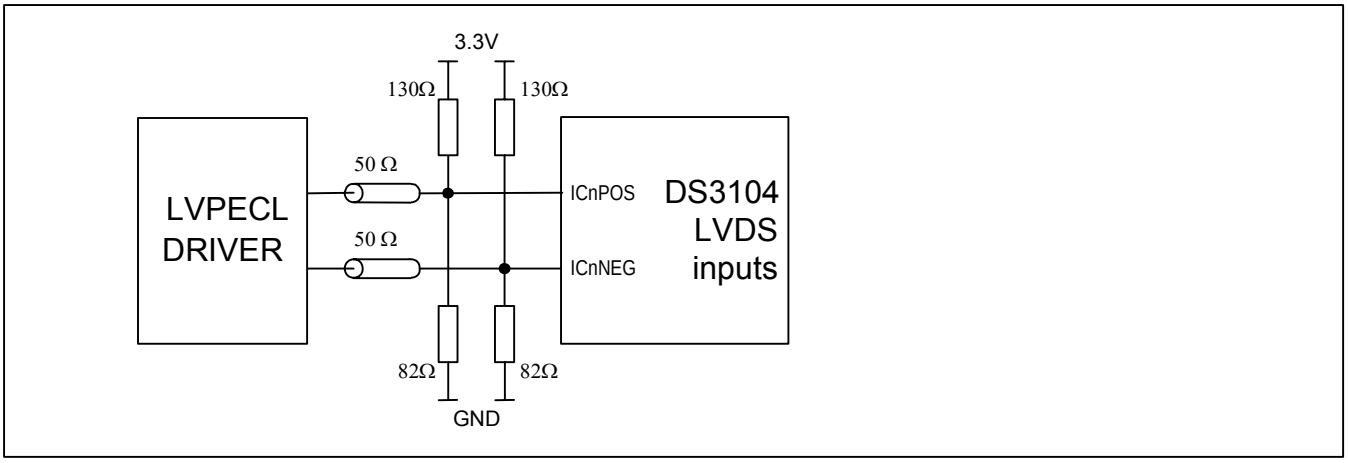
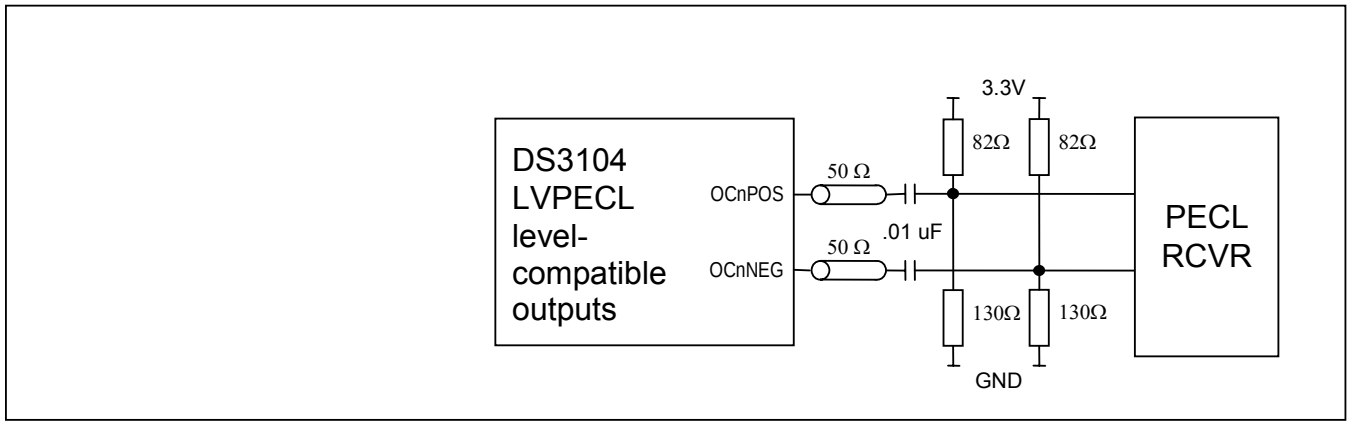


Figure 10-3. Recommended Termination for LVPECL-Compatible Output Pins



10.2 Input Clock Timing

Table 10-7. Input Clock Timing

(VDD = 1.8V ±10%; VDDIO = 3.3V ±5%, T_A = -40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX
Input Clock Period, CMOS/TTL Input Pins	t_{CYC}	8ns (125MHz)		500µs (2kHz)
Input Clock Period, LVDS/LVPECL Input Pins	t_{CYC}	6.4ns (156.25MHz)		500µs (2kHz)
Input Clock High, Low Time	t_H, t_L	3ns or 30% of t_{CYC}, whichever is smaller		

10.3 Output Clock Timing

Table 10-8. Input Clock to Output Clock Delay

INPUT FREQUENCY	OUTPUT FREQUENCY	DELAY, INPUT CLOCK EDGE TO OUTPUT CLOCK EDGE (ns)
8kHz	8kHz	0.0 ± 1.5
6.48MHz	6.48MHz	0.0 ± 1.5
19.44MHz	19.44MHz	0.0 ± 1.5
25.92MHz	25.92MHz	0.0 ± 1.5
38.88MHz	38.88MHz	0.0 ± 1.5
51.84MHz	51.84MHz	0.0 ± 1.5
77.76MHz	77.76MHz	0.0 ± 1.5
155.52MHz	155.52MHz	0.0 ± 1.5

Table 10-9. Output Clock Phase Alignment, Frame Sync Alignment Mode

OUTPUT FREQUENCY	DELAY, MFSYNC FALLING EDGE TO OUTPUT CLOCK FALLING EDGE (ns)
8kHz (FSYNC)	0.0 ± 0.5
2kHz	0.0 ± 0.5
8kHz	0.0 ± 0.5
1.544MHz	0.0 ± 1.25
2.048MHz	0.0 ± 1.25
44.736MHz	-2.0 ± 1.25
34.368MHz	-2.0 ± 1.25
6.48MHz	-2.0 ± 1.25
19.44MHz	-2.0 ± 1.25
25.92MHz	-2.0 ± 1.25
38.88MHz	-2.0 ± 1.25
51.84MHz	-2.0 ± 1.25
77.76MHz	-2.0 ± 1.25
155.52MHz	-2.0 ± 1.25
311.04MHz	-2.0 ± 1.25ns

See Section 7.9 for details on frame sync alignment and the SYNC[1:3] pins.

10.4 SPI Interface Timing

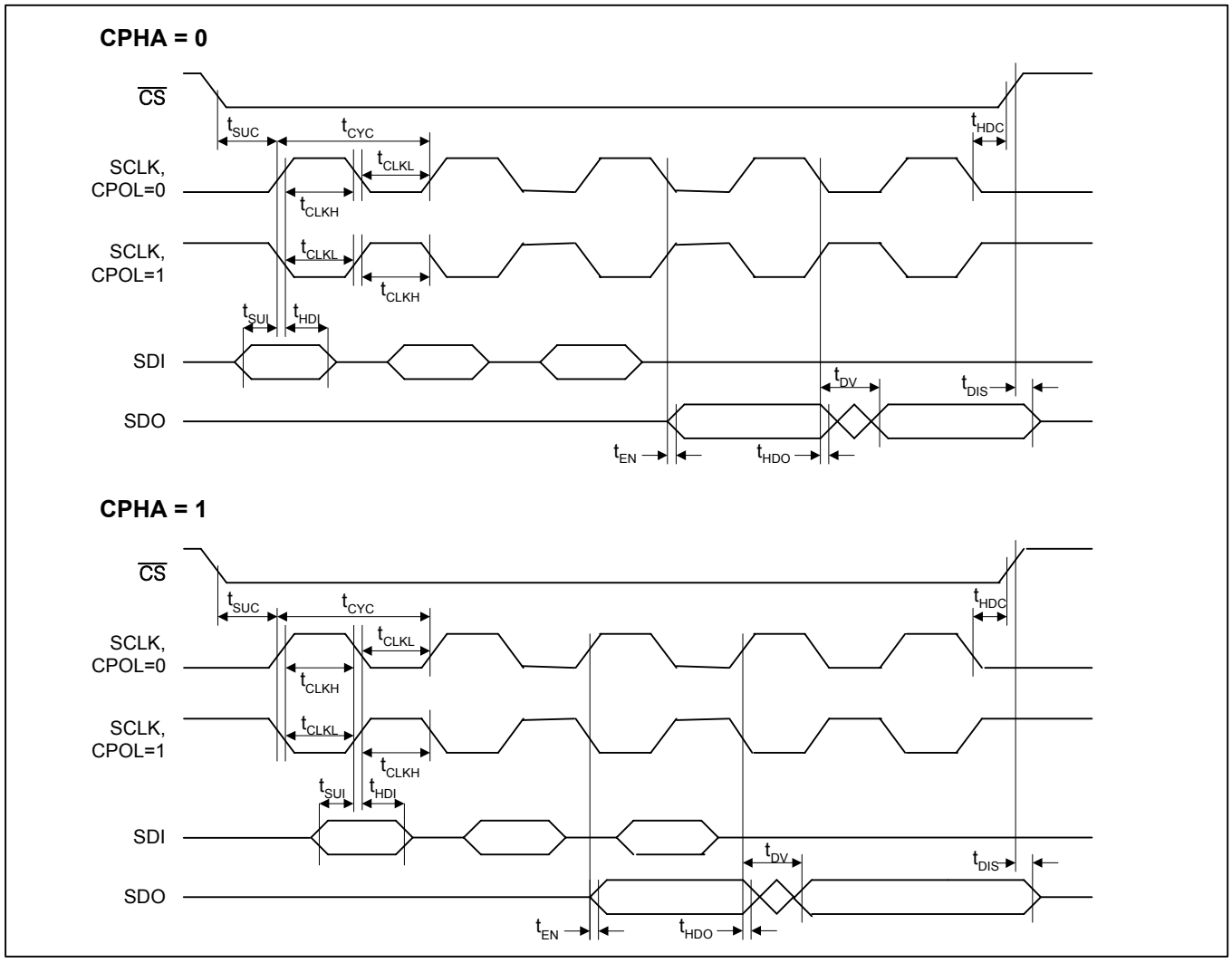
Table 10-10. SPI Interface Timing

(VDD = 1.8V ±10%; VDDIO = 3.3V ±5%, T_A = -40°C to +85°C) (See Figure 10-4.)

PARAMETER (Note 1)	SYMBOL	MIN	TYP	MAX	UNITS
SCLK Frequency	f_{BUS}			6	MHz
SCLK Cycle Time	t_{CYC}	100			ns
$\overline{CS}$ Setup to First SCLK Edge	t_{SUC}	15			ns
$\overline{CS}$ Hold Time After Last SCLK Edge	t_{HDC}	15			ns
SCLK High Time	t_{CLKH}	50			ns
SCLK Low Time	t_{CLKL}	50			ns
SDI Data Setup Time	t_{SUI}	5			ns
SDI Data Hold Time	t_{HDI}	15			ns
SDO Enable Time (High-Impedance to Output Active)	t_{EN}	0			ns
SDO Disable Time (Output Active to High-Impedance)	t_{DIS}			25	ns
SDO Data Valid Time	t_{DV}			50	ns
SDO Data Hold Time After Update SCLK Edge	t_{HDO}	5			ns

Note 1: All timing is specified with 100pF load on all SPI pins.

Figure 10-4. SPI Interface Timing Diagram



10.5 JTAG Interface Timing

Table 10-11. JTAG Interface Timing

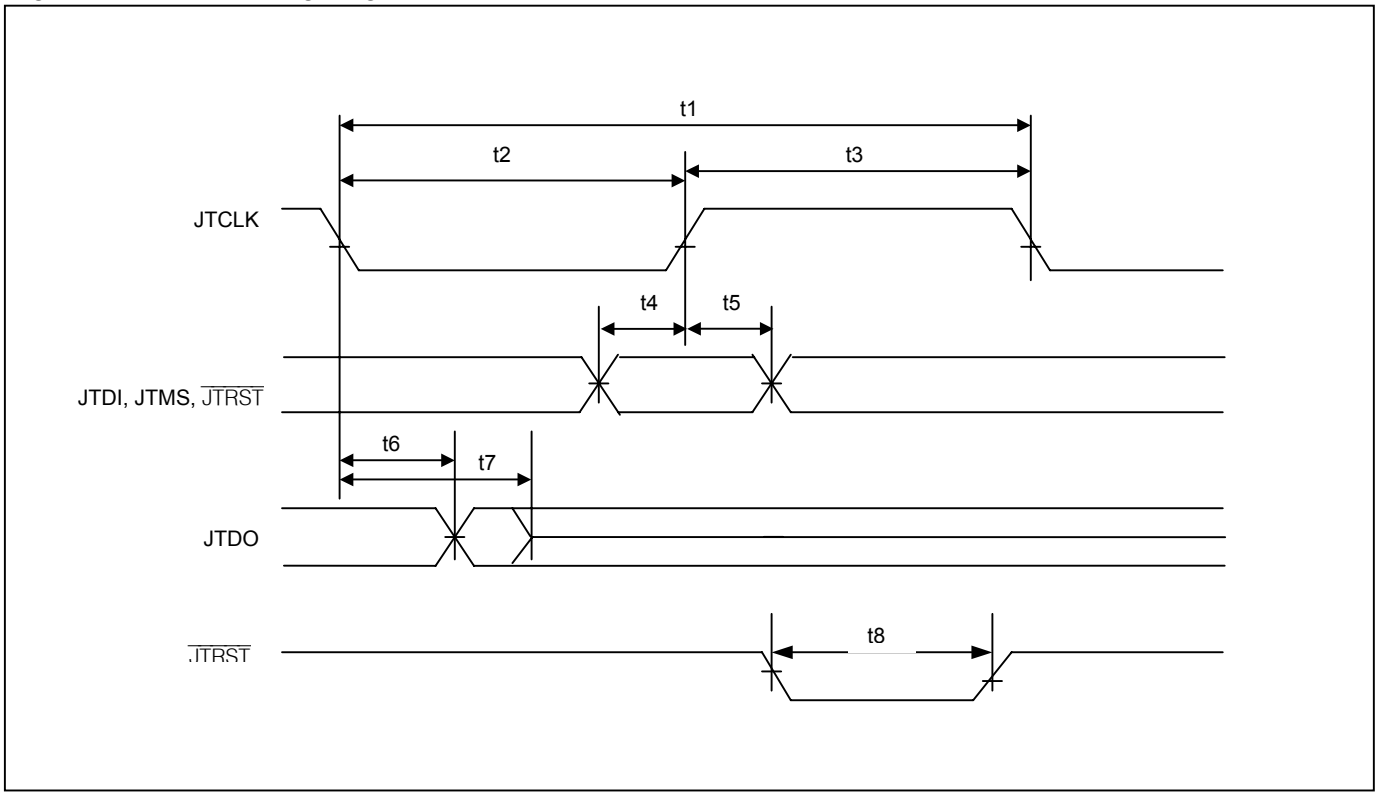
(VDD = 1.8V ±10%; VDDIO = 3.3V ±5%, T_A = -40°C to +85°C.) (See Figure 10-5.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
JTCLK Clock Period	t1		1000		ns
JTCLK Clock High/Low Time (Note 1)	t2/t3	50	500		ns
JTCLK to JTDI, JTMS Setup Time	t4	50			ns
JTCLK to JTDI, JTMS Hold Time	t5	50			ns
JTCLK to JTDO Delay	t6	2		50	ns
JTCLK to JTDO High-Impedance Delay (Note 2)	t7	2		50	ns
$\overline{\text{JTRST}}$ Width Low Time	t8	100			ns

Note 1: Clock can be stopped high or low.

Note 2: Not tested during production test.

Figure 10-5. JTAG Timing Diagram



10.6 Reset Pin Timing

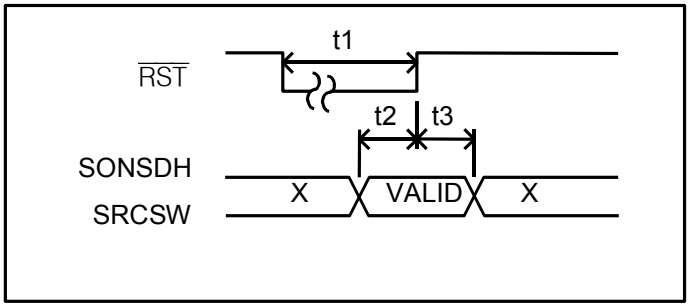
Table 10-12. Reset Pin Timing

(VDD = 1.8V ±10%; VDDIO = 3.3V ±5%, T_A = -40°C to +85°C) (See Figure 10-6.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
$\overline{RST}$ Low Time (Note 1)	t1	1000			ns
SONSDH, SRCSW Setup Time to $\overline{RST}$	t2	0			ns
SONSDH, SRCSW Hold Time from $\overline{RST}$	t3	50			ns

Note 1: $\overline{RST}$ should be held low while the REFCLK oscillator stabilizes. It is recommended to force $\overline{RST}$ low during power-up. The 1000ns minimum time applies if the $\overline{RST}$ pulse is applied any time after the device has powered up and the oscillator has stabilized.

Figure 10-6. Reset Pin Timing Diagram



11. Pin Assignments

Table 11-1 below lists pin assignments sorted in alphabetical order by pin name. Figure 11-1 shows pin assignments arranged by pin number.

Table 11-1. Pin Assignments Sorted by Signal Name

PIN NAME	PIN NUMBER
AVDD_PLL1	B2
AVDD_PLL2	C2
AVDD_PLL3	F2
AVDD_PLL4	F3
AVSS_PLL1	A1
AVSS_PLL2	C3
AVSS_PLL3	F1
AVSS_PLL4	G2
CPHA	E7
CPOL	D7
$\overline{CS}$	D9
FSYNC	H1
IC1NEG	J5
IC1POS	H5
IC2NEG	J7
IC2POS	H7
IC3	J8
IC4	J9
IC5NEG	J4
IC5POS	H4
IC6NEG	J6
IC6POS	H6
IC8	F9
IC9	G9
INTREQ/LOS	B1
JTCLK	A9
JTDI	A8
JTDO	C8
JTMS	E9
$\overline{JTRST}$	F8
LOCK	G7
MFSYNC	J1
OC1	B8
OC1B/GPIO1	B4
OC2	A7
OC2B/GPIO2	A5

PIN NAME	PIN NUMBER
OC3	B7
OC3B/GPIO3	B5
OC4	A3
OC4B	A6
OC4NEG	D1
OC4POS	D2
OC5	A4
OC5B	B6
OC5NEG	E1
OC5POS	E2
OC6NEG	J2
OC6POS	H2
OC7NEG	J3
OC7POS	H3
REFCLK	C1
$\overline{RST}$	B9
SCLK	C9
SDI	E8
SDO	C7
SONSDH/GPIO4	B3
SRCSW	G1
SRFAIL	F7
SYNC1	H8
SYNC2	H9
SYNC3	G8
TEST	A2
VDD	C5, E6, G6
VDD_OC45	E3
VDD_OC67	G5
VDDIO	C4, D6, F6, G3
VDDIOB	C6
VSS	D4, D5, E4, E5, F4, F5
VSS_OC45	D3
VSS_OC67	G4
WDT	D8

Figure 11-1. Pin Assignment Diagram

	1	2	3	4	5	6	7	8	9
A	AVSS_PLL1	TEST	OC4	OC5	OC2B/ GPIO2	OC4B	OC2	JTDI	JTCLK
B	INTREQ/ LOS	AVDD_PLL1	SONSDH/ GPIO4	OC1B/ GPIO1	OC3B/ GPIO3	OC5B	OC3	OC1	$\overline{\text{RST}}$
C	REFCLK	AVDD_PLL2	AVSS_PLL2	VDDIO	VDD	VDDIOB	SDO	JTDO	SCLK
D	OC4NEG	OC4POS	VSS_OC45	VSS	VSS	VDDIO	CPOL	WDT	$\overline{\text{CS}}$
E	OC5NEG	OC5POS	VDD_OC45	VSS	VSS	VDD	CPHA	SDI	JTMS
F	AVSS_PLL3	AVDD_PLL3	AVDD_PLL4	VSS	VSS	VDDIO	SRFAIL	$\overline{\text{JTRST}}$	IC8
G	SRCSW	AVSS_PLL4	VDDIO	VSS_OC67	VDD_OC67	VDD	LOCK	SYNC3	IC9
H	FSYNC	OC6POS	OC7POS	IC5POS	IC1POS	IC6POS	IC2POS	SYNC1	SYNC2
J	MFSYNC	OC6NEG	OC7NEG	IC5NEG	IC1NEG	IC6NEG	IC2NEG	IC3	IC4

- High-Speed Analog
- Low-Speed Analog
- High-Speed Digital
- Low-Speed Digital
- V_{DDIO} 3.3V
- V_{DDIOB} 3.3V or 2.5V
- V_{DD} 1.8V
- Analog V_{DD} 1.8V
- V_{SS}
- Analog V_{SS}
- N.C. = No Connection. Lead is not connected to anything inside the device.

12. Package Information

The latest package outline drawing for the 10mm x 10mm, 81-lead CSBGA package is **56-G6009-001** and can be found on the Maxim website at www.maxim-ic.com/DallasPackInfo.

Table 12-1. CSBGA Package Thermal Properties, Natural Convection

PARAMETER	MIN	TYP	MAX
Ambient Temperature (Note 1)	-40°C		+85°C
Junction Temperature	-40°C		+125°C
Theta-JA (θ_{JA}) (Note 2)		33.8°C/W	
Theta-JB (θ_{JB})		18.2°C/W	
Theta-JC (θ_{JC})		9.0°C/W	
Psi-JB		17.8°C/W	
Psi-JT		0.22°C/W	

Note 1: The package is mounted on a four-layer JEDEC standard test board with no airflow and dissipating maximum power.

Note 2: Theta-JA (θ_{JA}) is the junction to ambient thermal resistance, when the package is mounted on a four-layer JEDEC standard test board with no airflow and dissipating maximum power.

13. Acronyms and Abbreviations

AIS	alarm indication signal
AMI	alternate mark inversion
APLL	analog phase locked loop
BITS	building integrated timing supply
BPV	bipolar violation
DFS	digital frequency synthesis
DPLL	digital phase locked loop
ESF	extended superframe
EXZ	excessive zeros
GbE	gigabit ethernet
I/O	input/output
LOS	loss of signal
LVDS	low-voltage differential signal
LVPECL	low-voltage positive emitter-coupled logic
MTIE	maximum time interval error
OCXO	oven controlled crystal oscillator
OOF	out of frame alignment
PBO	phase build-out
PFD	phase/frequency detector
PLL	phase locked loop
ppb	parts per billion
ppm	parts per million
pk-pk	peak-to-peak
RMS	root-mean-square
RAI	remote alarm indication
RO	read-only
R/W	read/write
SDH	synchronous digital hierarchy
SEC	SDH equipment clock
SETS	synchronous equipment timing source
SF	superframe
SONET	synchronous optical network
SSM	synchronization status message
SSU	synchronization supply unit
STM	synchronous transport module
TDEV	time deviation
TCXO	temperature-compensated crystal oscillator
UI	unit interval
UI_{P-P}	unit interval, peak to peak
XO	crystal oscillator

14. Trademark Acknowledgements

SPI is a trademark of Motorola, Inc.

Motorola is a registered trademark of Motorola, Inc.

Telcordia is a registered trademark of Telcordia Technologies, Inc.

15. Data Sheet Revision History

REVISION DATE	DESCRIPTION
060507	Initial data sheet release.
070507	(Page 1) Corrected typo in Features bullet, Programmable PLL Bandwidth, from 1Hz to 0.1Hz (0.1Hz to 400Hz).
071807	(Page 6) Added reference to G.8262 to Table 1-1. (Page 14). In the OC3B pin description in Table 6-2, corrected typo by changing OC2BEN to OC3BEN. (Page 15) In Table 6-3, changed pin name INTREQ/SRFAIL to INTREQ/LOS and changed the pin description to clarify its non-INTREQ function. (Page 16) In Table 6-6, corrected AVDD_PLL4 and AVSS_PLL4 descriptions to say they are the power supply for T0 APLL2 rather than T0 APLL. (Page 52) In Section 7.11, emphasized the need for $\overline{\text{RST}}$ pin assertion and added requirement to least 100µs after reset is deasserted before initializing the device. (Page 58) In the MSR2:SRFAIL bit description, deleted references to the INTREQ/SRFAIL pin and to INTCR:SRFAIL. (Page 75) In the MCR4 register description header, corrected typo by renaming bit 6 from “T4DIGFB” to “—“. (Page 107) Deleted reference to nonexistent PMPBEN bit in the OFFSET1 register. (Page 115) Changed INTCR:SRFAIL to LOS and changed its bit description to clarify function. Updated references to this bit in other INTCR bit descriptions. (Page 130) In Table 11-1, changed INTREQ to INTREQ/LOS. (Page 131) In Figure 11-1, changed INTREQ to INTREQ/LOS.

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