*Data Sheet*
*April 2012*

# DS3102
# Stratum 2/3E/3 Timing Card IC with Synchronous Ethernet Support

## General Description

The DS3102 is a low-cost, feature-rich timing IC for telecom timing cards. With 8 input clocks, the device directly accepts both line timing from a large number of line cards and external timing from external DS1/E1 BITS transceivers. The DS3102 continually monitors all input clocks and performs automatic hitless reference switching if the primary reference fails. The T0 DPLL complies with the Stratum 2, 3E, 3, 4E and 4 requirements of GR-1244, GR-253, G.812 Types I – IV, G.813 and G.8262. The highly programmable DS3102 support numerous input and output frequencies including rates required for SONET/SDH, Synchronous Ethernet (1G, 10G, and 100Mbps), wireless base stations, and CMTS systems. PLL bandwidths from 0.5mHz to 400Hz are supported, and a wide variety of PLL characteristics and device features can be configured to meet the needs of many different applications. Two DS3102 devices can be configured in a master/slave arrangement for timing card equipment protection.

The DS3102 register set is backward compatible with Semtech's ACS8522 timing card IC. The DS3102 has a different package and pin arrangement than the ACS8522.

## Applications

SONET/SDH Equipment Clocks (SECs)
Synchronous Ethernet Equipment Clocks (EECs)
Timing Card IC in WAN Equipment Including MSPPs, Ethernet Switches, Routers, DSLAMs, and Wireless Base Stations

## Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE |
|---|---|---|
| DS3102GN | -40°C to +85°C | 81 CSBGA (10mm)$^2$ |
| DS3102GN+ | -40°C to +85°C | 81 CSBGA (10mm)$^2$ |

*+Denotes a lead(Pb)-free/RoHS-compliant package.*

## Features

- **Synchronization for Stratum 2, 3E, 3, 4E and 4 plus SMC, SEC and EEC**
  - **Meets Requirements of GR-1244 Stratum 2 – 4, GR-253, G.812 Types I – IV, G.813, and G.8262**
  - **Stratum 2, 3E or 3 Holdover Accuracy with Suitable External Oscillator**
  - **Programmable Bandwidth: 0.5mHz to 400Hz**
  - **Hitless Reference Switching on Loss of Input**
  - **Automatic or Manual Phase Build-Out**
  - **Frequency Conversion Among SONET/SDH, PDH, Ethernet, Wireless, and CMTS Rates**
- **8 Input Clocks**
  - **Four CMOS/TTL Inputs (≤ 125MHz)**
  - **Four LVDS/LVPECL/CMOS/TTL Inputs (≤ 156.25MHz)**
  - **Three Optional Frame-Sync Inputs (CMOS/TTL)**
  - **Continuous Input Clock Quality Monitoring**
  - **Numerous Input Clock Frequencies Supported:**
    SONET/SDH: 6.48, N x 19.44, N x 51.84MHz
    Ethernet xMII: 2.5, 25, 125, 156.25MHz
    PDH: N x DS1, N x E1, N x DS2, DS3, E3
    Frame Sync: 2kHz, 4kHz, 8kHz
    Custom: Any Multiple of 2kHz Up to 131.072MHz, Any Multiple of 8kHz Up to 155.52MHz
- **7 Output Clocks**
  - **Three CMOS/TTL Outputs (≤ 125MHz)**
  - **Two LVDS/LVPECL Outputs (≤ 312.50MHz)**
  - **Two Dual CMOS/TTL and LVDS/LVPECL Outputs**
  - **Five CMOS Outputs Have Additional Output Pins That Can Be Powered at 2.5V or 3.3V**
  - **Numerous Output Clock Frequencies Supported:**
    SONET/SDH: 6.48, N x 19.44, N x 51.84MHz
    Ethernet xMII: 2.5, 25, 125, 156.25, 312.5MHz
    PDH: N x DS1, N x E1, N x DS2, DS3, E3
    Other: 10, 10.24, 13, 30.72MHz
    Frame Sync: 2kHz, 8kHz
    Custom Clock Rates: Any Multiple of 2kHz Up to 77.76MHz, Any Multiple of 8kHz Up to 311.04MHz, Any Multiple of 10kHz Up to 388.79MHz
- **General**
  - **Internal Compensation for Master Clock Oscillator**
  - **SPI™ Processor Interface**
  - **1.8V Operation with 3.3V I/O (5V Tolerant)**
  - **Industrial Temperature Range**

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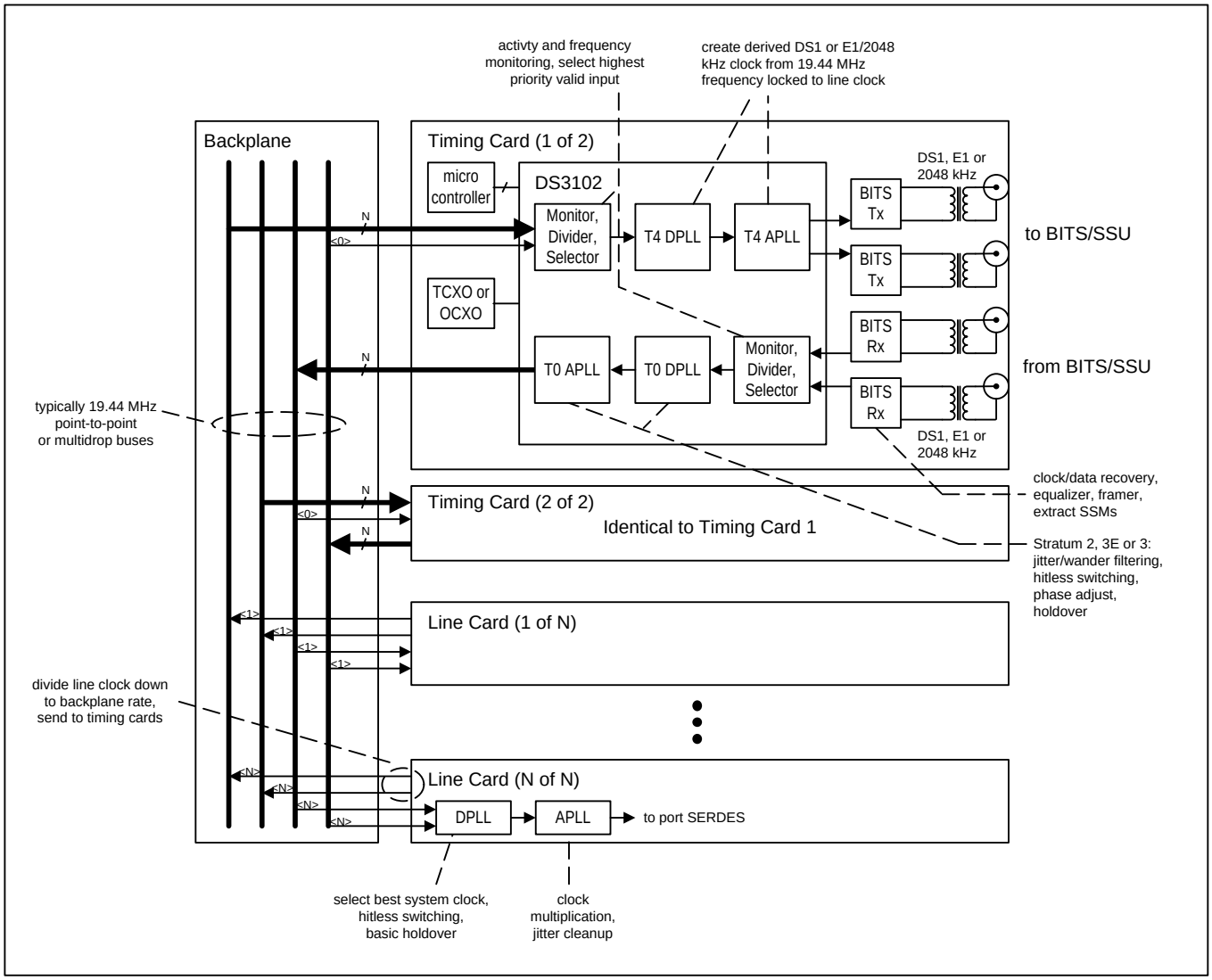
# 1. Standards Compliance

## Table 1-1. Applicable Telecom Standards

| SPECIFICATION | SPECIFICATION TITLE |
|---|---|
| **ANSI** | |
| T1.101 | *Synchronization Interface Standard*, 1999 |
| TIA/EIA-644-A | *Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits,* 2001 |
| **ETSI** | |
| EN 300 417-6-1 | *Transmission and Multiplexing (TM); Generic requirements of transport functionality of equipment; Part 6-1: Synchronization layer functions*, v1.1.3 (1999-05) |
| EN 300 462-3-1 | *Transmission and Multiplexing (TM); Generic requirements for synchronization networks; Part 3-1: The control of jitter and wander within synchronization networks*, v1.1.1 (1998-05) |
| EN 300 462-5-1 | *Transmission and Multiplexing (TM); Generic requirements for synchronization networks; Part 5-1: Timing characteristics of slave clocks suitable for operation in Synchronous Digital Hierarchy (SDH) Equipment*, v1.1.2 (1998-05) |
| **IEEE** | |
| IEEE 1149.1 | *Standard Test Access Port and Boundary-Scan Architecture*, 1990 |
| **ITU-T** | |
| G.781 | *Synchronization layer functions* (06/1999) |
| G.783 | *Characteristics of synchronous digital hierarchy (SDH) equipment functional blocks* (10/2000 plus Amendment 1 06/2002 and Corrigendum 2 03/2003) |
| G.812 | *Timing requirements of slave clocks suitable for use as node clocks in synchronization networks* (06/1998) |
| G.813 | *Timing characteristics of SDH equipment slave clocks (SEC)* (03/2003) |
| G.823 | *The control of jitter and wander within digital networks which are based on the 2048 kbit/s hierarchy* (03/2000) |
| G.824 | *The control of jitter and wander within digital networks which are based on the 1544 kbit/s hierarchy* (03/2000) |
| G.825 | *The control of jitter and wander within digital networks which are based on the synchronous digital hierarchy (SDH)* (03/2000) |
| G.8261 | *Timing and synchronization aspects in packet networks* (05/2006, prepublished) |
| G.8262 | *Timing characteristics of synchronous Ethernet equipment slave clock (EEC)* (08/2007) |
| **TELCORDIA** | |
| GR-253-CORE | *SONET Transport Systems: Common Generic Criteria*, Issue 3, September 2000 |
| GR-378-CORE | *Generic Requirements for Timing Signal Generators*, Issue 2, February 1999 |
| GR-1244-CORE | *Clocks for the Synchronized Network: Common Generic Criteria,* Issue 2, December 2000 |

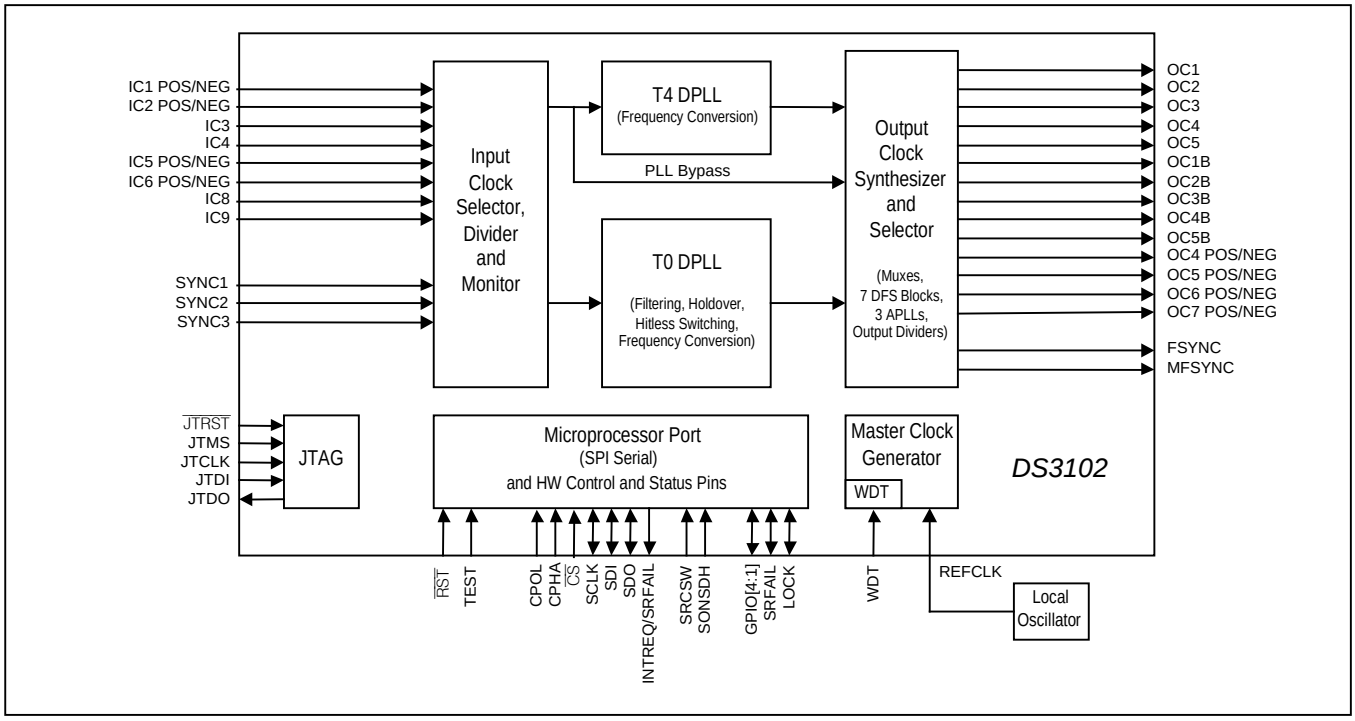
# 2. Application Example

*Figure 2-1. Typical Application Example*



# 3. Block Diagram

*Figure 3-1. Block Diagram*




See Figure 7-1 for a detailed view of the T0 and T4 DPLLs and the Output Clock Synthesizer and Selector block.

# 4. Detailed Description

Figure 3-1 illustrates the blocks described in this section and how they relate to one another. Section 5 provides a detailed feature list.

The DS3102 is a highly integrated timing card IC for systems with SONET/SDH or Synchronous Ethernet ports. At the core of this device are two digital phase-locked loops (DPLLs) labeled T0 and T4[1]. DPLL technology makes use of digital-signal processing (DSP) and digital-frequency synthesis (DFS) techniques to implement PLLs that are precise, flexible, and have consistent performance over voltage, temperature, and manufacturing process variations. The DS3102's DPLLs are digitally configurable for input and output frequencies, loop bandwidth, damping factor, pull-in/hold-in range, and a variety of other factors. Both DPLLs can directly lock to many common telecom frequencies and also can lock at 8kHz to any multiple of 8kHz up to 156.25MHz. The DPLLs can also tolerate and filter significant amounts of jitter and wander.

The T0 DPLL is responsible for generating the system clocks used to time the outgoing traffic interfaces of the system (SONET/SDH, Synchronous Ethernet, etc.). To perform this role in a variety of systems with diverse performance requirements, the T0 DPLL has a sophisticated feature set and is highly configurable. T0 can automatically transition among free-run, locked, and holdover states without software intervention. In free-run, T0 generates a stable, low-noise clock with the same frequency accuracy as the external oscillator connected to the REFCLK pin. With software calibration the DS3102 can even improve the accuracy to within ±0.02ppm. When an input reference has been validated, T0 transitions to the locked state in which its output clock accuracy is equal to the accuracy of the input reference. While in the locked state, T0 acquires a high-accuracy long-term average frequency value to use as the holdover frequency. When its selected reference fails, T0 can very quickly detect the failure and enter the holdover state to avoid affecting its output clock. From holdover it can automatically switch to the next highest priority input reference, again without affecting its output clock (hitless switching). Switching among input references can be either revertive or nonrevertive. When all input references are lost, T0 stays in holdover, in which it generates a stable low-noise clock with initial frequency accuracy equal to its stored holdover value and drift performance determined by the quality of the external oscillator. With a suitable local oscillator the T0 DPLL provides holdover performance suitable for all applications up to and including Stratum 2. T0 can also perform phase build-outs and fine-granularity output clock phase adjustments.

The T4 DPLL has a much less demanding role to play and therefore is much simpler than T0. Often T4 is used as a frequency converter to create a derived DS1- or E1-rate clock (frequency locked to an incoming SONET/SDH port) to be sent to a nearby BITS Timing Signal Generator (TSG, Telcordia terminology) or Synchronization Supply Unit (SSU, ITU-T terminology). In other applications T4 is phase-locked to T0 and used as a frequency converter to produce additional output clock rates for use within the system, such as N x DS1, N x E1, N x DS2, DS3, E3, 125MHz for Synchronous Gigabit Ethernet, or 156.25MHz for Synchronous 10G Ethernet. T4 can also be configured as a measuring tool to measure the frequency of an input reference or the phase difference between two input references.

At the front end of both the T0 and T4 DPLLs is the Input Clock Selector, Divider, and Monitor (ICSDM) block. This block continuously monitors as many as 8 different input clocks of various frequencies for activity and frequency accuracy. In addition, ICSDM maintains separate input clock priority tables for the T0 and T4 DPLLs, and can automatically select and provide the highest priority valid clock to each DPLL without any software intervention. The ICSDM block can also divide the selected clock down to a lower rate as needed by the DPLL.

The Output Clock Synthesizer and Selector (OCSS) block shown in Figure 3-1 and in more detail in Figure 7-1 contains three output APLLs—T0 APLL, T0 APLL2, and T4 APLL—and their associated DFS engines and output divider logic plus several additional DFS engines. The APLL DFS blocks perform frequency translation, creating clocks of other frequencies that are phase/frequency locked to the output clock of the associated DPLL. The APLLs multiply the clock rates from the APLL DFS blocks and simultaneously attenuate jitter. Altogether the output blocks of the DS3102 can produce more than 90 different output frequencies including common SONET/SDH, PDH and Synchronous Ethernet rates plus 2kHz and 8kHz frame-sync pulses.

[1] These names are adapted from output ports of the SETS function specified in ITU-T and ETSI standards such as ETSI EN 300 462-2-1.

The entire chip is clocked from the external oscillator connected to the REFCLK pin. Thus, the free-run and holdover stability of the DS3102-based timing card is entirely a function of the stability of the external oscillator, the performance of which can be selected to match the application: TCXO, OCXO, double-oven OCXO, etc. The 12.8MHz clock from the external oscillator is multiplied by 16 by the Master Clock Generator block to create the 204.8MHz master clock used by the rest of the device. Since every block on the device depends on the master clock and therefore the local oscillator clock for proper operation, the master clock generator has a watchdog timer (WDT) function that can be used to signal a local microprocessor in the event of a local oscillator clock failure.

The DS3102 also has several features to support master/slave timing card redundancy and protection. Two DS3102 devices on redundant cards can be configured to maintain the same priority tables, choose the same input references, and generate output clocks and frame syncs with the same frequency and phase.

# 5. Detailed Features

## 5.1 Input Clock Features

- Eight input clocks: four CMOS/TTL (≤ 125MHz) and four LVDS/LVPECL/CMOS/TTL (≤ 156.25MHz)
- CMOS/TTL input clocks accept any multiple of 2kHz up to 125MHz
- LVDS/LVPECL inputs accept any multiple of 2kHz up to 131.072MHz, any multiple of 8kHz up to 155.52MHz plus 156.25MHz
- All input clocks are constantly monitored by programmable frequency monitors and activity monitors
- Fast activity monitor can disqualify the selected reference after two missing clock cycles
- Three optional 2/4/8kHz frame-sync inputs

## 5.2 T0 DPLL Features

- High-resolution DPLL plus two or three low-jitter output APLLs
- Sophisticated state machine automatically transitions between free-run, locked, and holdover states
- Revertive or nonrevertive reference selection algorithm
- Programmable bandwidth from 0.5mHz to 400Hz
- Separately configurable acquisition bandwidth and locked bandwidth
- Programmable damping factor to balance lock time with peaking: 1.2, 2.5, 5, 10, or 20
- Multiple phase detectors: phase/frequency, early/late, and multicycle
- Phase/frequency locking (±360° capture) or nearest edge phase locking (±180° capture)
- Multicycle phase detection and locking (up to ±8191UI) improves jitter tolerance and lock time
- Phase build-out in response to reference switching
- Less than 5 ns output clock phase transient during phase build-out
- Output phase adjustment up to ±200ns in 6ps steps with respect to selected input reference
- High-resolution frequency and phase measurement
- Holdover frequency averaging over 8- or 110-minute intervals
- Fast detection of input clock failure and transition to holdover mode
- Low-jitter frame sync (8kHz) and multiframe sync (2kHz) aligned with output clocks

## 5.3 T4 DPLL Features

- High-resolution DPLL plus low-jitter output APLL
- Programmable bandwidth from 18Hz to 70Hz
- Programmable damping factor to balance lock time with peaking: 1.2, 2.5, 5, 10, or 20
- Multiple phase detectors: phase/frequency, early/late, and multicycle
- Phase/frequency locking (±360° capture) or nearest edge phase locking (±180° capture)
- Multicycle phase detection and locking (up to ±8191UI) improves jitter tolerance and lock time
- 2kHz and 8kHz frame syncs with programmable polarity and pulse width
- Can operate independently or locked to T0 DPLL
- Phase detector can be used to measure phase difference between two input clocks
- Optional PLL bypass mode provides input clock monitoring, selection, and optional frequency division but bypasses the DPLL and APLL when they are not needed (e.g., dividing an input clock to 8kHz)
- High-resolution frequency and phase measurement

## 5.4 Output APLL Features

- Three separate clock multiplying, jitter attenuating APLLs can simultaneously produce SONET/SDH rates, Fast/Gigabit Ethernet rates, and 10G Ethernet rates, all locked to a common reference clock
- The T0 APLL, always connected to the T0 DPLL, has frequency options suitable for N x 19.44MHz, N x DS1, N x E1, N x 25MHz, and N x 62.5MHz
- The T4 APLL can be connected to either the T0 DPLL or the T4 DPLL and has frequency options suitable for N x 19.44MHz, N x DS1, N x E1, N x DS2, DS3, E3, N x 10MHz, N x 10.24MHz, N x 13MHz, N x 25MHz, and N x 62.5MHz
- The T0 APLL2, always connected to the T0 DPLL, produces 312.5MHz for 10G Synchronous Ethernet applications

## 5.5 Output Clock Features

- Seven output clocks: three CMOS/TTL (≤ 125MHz), two LVDS/LVPECL (≤ 312.50MHz), and two dual CMOS/TTL and LVDS/LVPECL
- Output clock rates include 2kHz, 8kHz, N x DS1, N x E1, DS2, DS3, E3, 6.48MHz, 19.44MHz, 38.88MHz, 51.84MHz, 77.76MHz, 155.52MHz, 311.04MHz, 2.5MHz, 25MHz, 125MHz, 156.25MHz, 312.50MHz, 10MHz, 10.24MHz, 13MHz, 30.72MHz, and various multiples and submultiples of these rates
- Custom clock rates also available: any multiple of 2kHz up to 77.76MHz, any multiple of 8kHz up to 311.04MHz, and any multiple of 10kHz up to 388.79MHz
- Three independent output APLLs support simultaneous generation of 155.52MHz for SONET/SDH, 125MHz for Gigabit Ethernet, and 156.25/312.5MHz for 10G Ethernet (plus various multiples/submultiples of each)
- All outputs have < 1ns peak-to-peak output jitter; outputs from APLLs have < 0.5ns peak-to-peak
- Each CMOS/TTL clock output has two leads, the standard output (e.g., OC1) with a 3.3V power supply, and the “B” output (e.g., OC1B) connected to the $V_{DDIOB}$ power supply for optional 2.5V output signal levels.
- 8kHz frame sync and 2kHz multiframe sync outputs have programmable polarity and pulse width and can be disciplined by a 2kHz or 8kHz sync input

## 5.6 Redundancy Features

- Devices on redundant timing cards can be configured for master/slave operation
- Clocks and frame syncs can be cross-wired between devices to ensure that slave always tracks master
- Input clock priority tables can easily be kept synchronized between master and slave

## 5.7 General Features

- Operates from a single external 12.800MHz local oscillator (XO, TCXO, or OCXO)
- On-chip watchdog circuit for the local (REFCLK) oscillator
- SPI serial microprocessor interface
- Four general-purpose I/O pins
- Register set can be write protected

# 6. Pin Descriptions

## Table 6-1. Input Clock Pin Descriptions

| PIN NAME[1] | TYPE[2] | PIN DESCRIPTION |
|---|---|---|
| REFCLK | I | **Reference Clock.** Connect to a 12.800MHz, high-accuracy, high-stability, low-noise local oscillator (TCXO, OCXO, or XO). See Section 7.3. |
| IC1POS, IC1NEG | $I_{DIFF}$ | **Input Clock 1.** LVDS/LVPECL or CMOS/TTL. Programmable frequency (default 8kHz).<br>*LVDS/LVPECL:* See Table 10-4, Figure 10-1, and Figure 10-2.<br>*CMOS/TTL:* Bias IC1NEG to 1.4V and connect the single-ended signal to IC1POS. |
| IC2POS, IC2NEG | $I_{DIFF}$ | **Input Clock 2.** LVDS/LVPECL or CMOS/TTL. Programmable frequency (default 8kHz).<br>*LVDS/LVPECL:* See Table 10-4, Figure 10-1, and Figure 10-2.<br>*CMOS/TTL:* Bias IC2NEG to 1.4V and connect the single-ended signal to IC2POS.<br>This input can be associated with the SYNC3 pin. |
| IC3 | $I_{PD}$ | **Input Clock 3.** CMOS/TTL. Programmable frequency (default 8kHz). This input can be associated with the SYNC1 pin. |
| IC4 | $I_{PD}$ | **Input Clock 4.** CMOS/TTL. Programmable frequency (default 8kHz). This input can be associated with the SYNC2 pin. |
| IC5POS, IC5NEG | $I_{DIFF}$ | **Input Clock 5.** LVDS/LVPECL or CMOS/TTL. Programmable frequency (default 19.44MHz).<br>*LVDS/LVPECL:* See Table 10-4, Figure 10-1, and Figure 10-2.<br>*CMOS/TTL:* Bias IC5NEG to 1.4V and connect the single-ended signal to IC5POS.<br>This input can be associated with the SYNC1 pin. |
| IC6POS, IC6NEG | $I_{DIFF}$ | **Input Clock 6.** LVDS/LVPECL or CMOS/TTL. Programmable frequency (default 19.44MHz).<br>*LVDS/LVPECL:* See Table 10-4, Figure 10-1, and Figure 10-2.<br>*CMOS/TTL:* Bias IC6NEG to 1.4V and connect the single-ended signal to IC6POS.<br>This input can be associated with the SYNC2 pin. |
| IC8 | $I_{PD}$ | **Input Clock 8.** CMOS/TTL. Programmable input reference (default 19.44MHz). |
| IC9 | $I_{PD}$ | **Input Clock 9.** CMOS/TTL. Programmable frequency (default 19.44MHz). This input can be associated with the SYNC3 pin. |
| SYNC1 | $I_{PD}$ | **Frame-Sync 1 Input.** 2kHz, 4kHz, or 8kHz.<br>FSCR3:SOURCE ! = 11XX. This pin is the external frame-sync input associated with any input pin using the FSCR3:SOURCE field.<br>FSCR3:SOURCE = 11XX. This pin is the external frame-sync signal associated with IC3 or IC5, depending on which one is currently selected and the setting of FSCR1.SYNCSRC[1:0]. |
| SYNC2 | $I_{PD}$ | **Frame-Sync 2 Input.** 2kHz, 4kHz, or 8kHz.<br>FSCR3:SOURCE ! = 11XX. This pin is not used for the external frame-sync signal.<br>FSCR3:SOURCE = 11XX. This pin is the external frame-sync signal associated with IC4 or IC6, depending on which one is currently selected and the setting of FSCR1.SYNCSRC[1:0]. |
| SYNC3 | $I_{PU}$ | **Frame-Sync 3 Input.** 2kHz, 4kHz, or 8kHz.<br>FSCR3:SOURCE ! = 11XX. This pin is not used for the external frame-sync signal.<br>FSCR3:SOURCE = 11XX. This pin is the external frame-sync signal associated with IC9 or IC2, depending on which one is currently selected and the setting of FSCR1.SYNCSRC[1:0]. |

## Table 6-2. Output Clock Pin Descriptions

| PIN NAME[1] | TYPE[2] | PIN DESCRIPTION |
|---|---|---|
| OC1 | O | **Output Clock 1.** CMOS/TTL. Programmable frequency (default 6.48MHz). |
| OC2 | O | **Output Clock 2.** CMOS/TTL. Programmable frequency (default 38.88MHz). |
| OC3 | O | **Output Clock 3.** CMOS/TTL. Programmable frequency (default 19.44MHz). |
| OC4 | O | **Output Clock 4.** CMOS/TTL. Programmable frequency (default 38.88MHz). |
| OC5 | O | **Output Clock 5.** CMOS/TTL. Programmable frequency (default 1.544MHz or 2.048MHz depending on the value SONSDH pin at power-up or reset). |
| OC4POS, OC4NEG | $O_{DIFF}$ | **Output Clock 4.** LVDS/LVPECL. These pins present the same clock as the OC4 pin but in differential signal format. The output mode is selected by MCR8.OC4SF[1:0]. See Table 10-5, Table 10-6, Figure 10-1, and Figure 10-3. |
| OC5POS, OC5NEG | $O_{DIFF}$ | **Output Clock 5.** LVDS/LVPECL. These pins present the same clock as the OC5 pin but in differential signal format. The output mode is selected by MCR8.OC5SF[1:0]. See Table 10-5, Table 10-6, Figure 10-1, and Figure 10-3. |
| OC6POS, OC6NEG | $O_{DIFF}$ | **Output Clock 6.** LVDS/LVPECL. Programmable frequency (default 38.88MHz LVDS). The output mode is selected by MCR8.OC6SF[1:0]. See Table 10-5, Table 10-6, Figure 10-1, and Figure 10-3. |
| OC7POS, OC7NEG | $O_{DIFF}$ | **Output Clock 7.** LVDS/LVPECL. Programmable frequency (default 19.44MHz LVDS). The output mode is selected by MCR8.OC7SF[1:0]. See Table 10-5, Table 10-6, Figure 10-1, and Figure 10-3. |
| OC1B/ GPIO1 | $O_3$ | **Output Clock 1B/General-Purpose I/O 1.** CMOS/TTL (default CLK1B, disabled). This pin is programmable as an output clock pin or a GPIO pin using OCR6.OC1BEN. When programmed as a clock output pin (OC1BEN = 1) it presents the same clock as the OC1 pin. This pin is powered from the $V_{DDIOB}$ power-supply pin. |
| OC2B/ GPIO2 | $O_3$ | **Output Clock 2B/General-Purpose I/O 2.** CMOS/TTL (default CLK2B, disabled). This pin is programmable as an output clock pin or a GPIO pin using OCR6.OC2BEN. When programmed as a clock output pin (OC2BEN = 1) it presents the same clock as the OC2 pin. This pin is powered from the $V_{DDIOB}$ power-supply pin. |
| OC3B/ GPIO3 | $O_3$ | **Output Clock 3B/General-Purpose I/O 3.** CMOS/TTL (default CLK3B, disabled). This pin is programmable as an output clock pin or a GPIO pin using OCR6.OC3BEN. When programmed as a clock output pin (OC3BEN = 1) it presents the same clock as the OC3 pin. This pin is powered from the $V_{DDIOB}$ power-supply pin. |
| OC4B | $O_3$ | **Output Clock 4B.** CMOS/TTL (default off). When enabled (OCR6.OC4BEN = 1), this pin presents the same clock as the OC4 pin. This pin is powered from the $V_{DDIOB}$ power-supply pin. |
| OC5B | $O_3$ | **Output Clock 5B.** CMOS/TTL (default off) . When enabled (OCR6.OC5BEN = 1), this pin presents the same clock as the OC5 pin. This pin is powered from the $V_{DDIOB}$ power-supply pin. |
| FSYNC | $O_3$ | **FSYNC.** CMOS/TTL. 8kHz frame sync or clock (default 50% duty cycle clock, noninverted). The pulse polarity and width are selectable using FSCR1.8KINV and FSCR1.8KPUL. |
| MFSYNC | $O_3$ | **MFSYNC.** CMOS/TTL. 2kHz frame sync or clock (default 50% duty cycle clock, noninverted). The pulse polarity and width are selectable using FSCR1.2KINV and FSCR1.2KPUL. |

## Table 6-3. Global Pin Descriptions

| PIN NAME[1] | TYPE[2] | PIN DESCRIPTION |
|---|---|---|
| $\overline{RST}$ | $I_{PU}$ | **Reset (Active Low).** When this global asynchronous reset is pulled low, all internal circuitry is reset to default values. The device is held in reset as long as $\overline{RST}$ is low. $\overline{RST}$ should be held low for at least two REFCLK cycles after the external oscillator has stabilized and is providing valid clock signals. |
| SRCSW | $I_{PD}$ | **Source Switching.** Fast source-switching control input. See Section 7.6.5. The value of this pin is latched into MCR10:EXTSW when $\overline{RST}$ goes high. After $\overline{RST}$ goes high this pin can be used to select between IC3/IC5 and IC4/IC6, if enabled. |
| TEST | $I_{PD}$ | **Factory Test Mode Select.** Wire this pin to $V_{SS}$ for normal operation. |
| WDT | I/O | **Watchdog Timer Pin.** Analog node for the REFCLK watchdog timer. Connect to a resistor (R) to $V_{DDIO}$ and a capacitor (C) to ground. Suggested values are R = 10kΩ and C = 0.01µF. See Section 7.3. |
| SONSDH/ GPIO4 | $I/O_{PD}$ | **SONET/SDH Frequency Select Input/General-Purpose I/O 4.** When $\overline{RST}$ goes high the state of this pin sets the reset-default state of MCR3:SONSDH, MCR6:DIG1SS, and MCR6:DIG2SS. After $\overline{RST}$ goes high this pin can be used as a general-purpose I/O pin. GPCR:GPIO4D configures this pin as an input or an output. GPCR:GPIO4O specifies the output value. GPSR:GPIO4 indicates the state of the pin.<br><br>Reset latched values:<br>0 = SDH rates (N x 2.048MHz)<br>1 = SONET rates (N x 1.544MHz) |
| SRFAIL | O | **SRFAIL Status.** When MCR10:SRFPIN = 1, this pin follows the state of the SRFAIL latched status bit in the MSR2 register. This gives the system a very fast indication of the failure of the current reference. When MCR10:SRFPIN = 0, SRFAIL is disabled (high impedance). |
| LOCK | O | **T0 DPLL LOCK Status.** When MCR1.LOCKPIN = 1, this pin indicates the lock state of the T0 DPLL. When MCR1.LOCKPIN = 0, LOCK is disabled (low).<br>0 = Not locked<br>1 = Locked |
| INTREQ/ LOS | $O_3$ | **Interrupt Request/Loss of Signal.** Programmable (default: INTREQ). The INTCR:LOS bit determines whether the pin indicates interrupt requests or loss of signal (i.e., loss of selected reference).<br><br>**INTCR:LOS = 0: INTREQ Mode.** The behavior of this pin is configured in the INTCR register. Polarity can be active high or active low. Drive action can be push-pull or open drain. The pin can also be configured as a general-purpose output if the interrupt request function is not needed.<br>**INTCR:LOS = 1: LOS Mode.** This pin indicates the real-time state of the selected reference activity monitor (see Section 7.5.3). This function is most useful when external switching mode (Section 7.6.5) is enabled (MCR10:EXTSW = 1). |

## Table 6-4. SPI Bus Mode Pin Descriptions

See Section 7.10 for functional description and Section 10.4 for timing specifications.

| PIN NAME[1] | TYPE[2] | PIN DESCRIPTION |
|---|---|---|
| $\overline{CS}$ | $I_{PU}$ | **Chip Select.** This pin must be asserted (low) to read or write internal registers. |
| SCLK | I | **Serial Clock.** SCLK is always driven by the SPI bus master. |
| SDI | I | **Serial Data Input.** The SPI bus master transmits data to the device on this pin. |
| SDO | O | **Serial Data Output.** The device transmits data to the SPI bus master on this pin. |
| CPHA | I | **Clock Phase.** See Figure 7-5.<br>0 = Data is latched on the leading edge of the SCLK pulse.<br>1 = Data is latched on the trailing edge of the SCLK pulse. |
| CPOL | $I_{PD}$ | **Clock Polarity.** See Figure 7-5.<br>0 = SCLK is normally low and pulses high during bus transactions.<br>1 = SCLK is normally high and pulses low during bus transactions. |

## Table 6-5. JTAG Interface Pin Descriptions

See Section 9 for functional description and Section 10.5 for timing specifications.

| PIN NAME[1] | TYPE[2] | PIN DESCRIPTION |
|---|---|---|
| $\overline{\text{JTRST}}$ | $I_{PU}$ | **JTAG Test Reset (Active Low).** Asynchronously resets the test access port (TAP) controller. If not used, $\overline{\text{JTRST}}$ can be held low or high. |
| JTCLK | I | **JTAG Clock.** Shifts data into JTDI on the rising edge and out of JTDO on the falling edge. If not used, JTCLK can be held low or high. |
| JTDI | $I_{PU}$ | **JTAG Test Data Input.** Test instructions and data are clocked in on this pin on the rising edge of JTCLK. If not used, JTDI can be held low or high. |
| JTDO | $O_3$ | **JTAG Test Data Output.** Test instructions and data are clocked out on this pin on the falling edge of JTCLK. If not used, leave unconnected. |
| JTMS | $I_{PU}$ | **JTAG Test Mode Select.** Sampled on the rising edge of JTCLK and is used to place the port into the various defined IEEE 1149.1 states. If not used connect to $V_{DDIO}$ or leave unconnected. |

## Table 6-6. Power-Supply Pin Descriptions

| PIN NAME[1] | TYPE[2] | PIN DESCRIPTION |
|---|---|---|
| $V_{DD}$ | P | **Core Power Supply.** 1.8V ±10%. |
| $V_{DDIO}$ | P | **I/O Power Supply.** 3.3V ±5%. |
| $V_{DDIOB}$ | P | **Power for Pins OC1B to OC5B.** Voltage can be from 2.5V ±5% to 3.3V ±5%. |
| $V_{SS}$ | P | **Ground Reference** |
| VDD_OC45 | P | **Power Supply for Differential Outputs OC4POS/NEG and OC5POS/NEG.** 1.8V ±10%. |
| VSS_OC45 | P | **Return for Differential Outputs OC4POS/NEG and OC5POS/NEG** |
| VDD_OC67 | P | **Power Supply for Differential Outputs OC6POS/NEG and OC7POS/NEG.** 1.8V ±10%. |
| VSS_OC67 | P | **Return for LVDS Differential Outputs OC6POS/NEG and OC7POS/NEG** |
| AVDD_PLL1 | P | **Power Supply for Master Clock Generator APLL.** 1.8V ±10%. |
| AVSS_PLL1 | P | **Return for Master Clock Generator APLL** |
| AVDD_PLL2 | P | **Power Supply for T0 APLL.** 1.8V ±10%. |
| AVSS_PLL2 | P | **Return for T0 APLL** |
| AVDD_PLL3 | P | **Power Supply for T4 APLL.** 1.8V ±10%. |
| AVSS_PLL3 | P | **Return for T4 APLL** |
| AVDD_PLL4 | P | **Power Supply for T0 APLL2.** 1.8V ±10%. |
| AVSS_PLL4 | P | **Return for T0 APLL2** |

**Note 1:** All pin names with an overbar (e.g., $\overline{\text{RST}}$) are active low.

**Note 2:** All pins, except power and analog pins, are CMOS/TTL, unless otherwise specified in the pin description.

**PIN TYPES**
I = input pin
$I_{DIFF}$ = input pin that is LVDS/LVPECL differential signal compatible
$I_{PD}$ = input pin with internal 50kΩ pulldown
$I_{PU}$ = input pin with internal 50kΩ pullup
I/O = input/output pin
$IO_{PD}$ = input/output pin with internal 50kΩ pulldown
$IO_{PU}$ = input/output pin with internal 50kΩ pullup
O = output pin
$O_3$ = output pin that can placed in a high-impedance state
$O_{DIFF}$ = output pin that is LVDS/LVPECL differential signal compatible
P = power-supply pin

**Note 3:** All digital pins, except OCn, are I/O pins in JTAG mode. OCn pins do not have JTAG functionality.

# 7. Functional Description

## 7.1 Overview

The DS3102 has eight input clocks pins and three frame-sync input pins. The device can output as many as nine different clock frequencies on 16 output clock pins. There are two separate DPLLs in the device: the high-performance T0 DPLL and the simpler the T4 DPLL. Both DPLLs can generate output clocks. See Figure 3-1.

Four of the input clock pins are single-ended and can accept clock signals from 2kHz to 125MHz. The other four are differential inputs that can accept clock signals up to 156.25MHz. The differential inputs can be configured to accept differential LVDS or LVPECL signals or single-ended CMOS/TTL signals.

Each input clock can be monitored continually for activity and/or frequency. Frequency can be compared to both a hard limit and a soft limit. Inputs outside the hard limit are declared invalid, while inputs inside the hard limit but outside the soft limit are merely flagged. Each input can be marked unavailable or given a priority number. Separate input priority numbers are maintained for the T0 DPLL and the T4 DPLL. Except in special modes, the highest priority valid input is automatically selected as the reference for each path. SRFAIL is set or cleared based on activity and/or frequency of the selected input.

Both the T0 DPLL and the T4 DPLL can directly lock to many common telecom and datacom frequencies, including, but not limited to, 8kHz, DS1, E1, 10MHz, 19.44MHz, and 38.88MHz as well as Ethernet frequencies including 25MHz, 62.5MHz, 125MHz, and 156.25MHz. The DPLLs can also lock to multiples of the standard direct-lock frequencies including 8kHz.

The T0 DPLL is the high-performance path with all the features needed for line timing synchronization. The T4 DPLL is a simpler auxiliary path typically used to provide derived DS1s, E1s, or other synchronization signals to an external BITS/SSU. The T4 APLL can be connected to either the T4 DPLL or the T0 DPLL to provide extra low-jitter output frequencies from the T0 DPLL. There is also a dedicated low-jitter APLL output that operates at 312.5MHz for 10G Ethernet applications.

Using the optional PLL bypass, the T4 selected reference, after any frequency division, can be directly output on any of the OC1 to OC7 output clock pins.

Both DPLLs have these features:

- Automatic reference selection based on input activity, quality, and priority
- Optional manual reference selection/forcing
- Configurable quality thresholds for each input
- Adjustable PLL characteristics, including bandwidth, pull-in range, and damping factor
- Ability to lock to several common telecom and Ethernet frequencies plus multiples of any standard direct lock frequency.
- Frequency conversion between input and output using digital frequency synthesis
- Combined performance of a stable, consistent digital PLL and low-jitter analog output PLLs

The T0 DPLL has these additional features not available in the T4 DPLL:

- A full state machine for automatic transitions among free-run, locked, and holdover states
- Nonrevertive reference switching mode
- Phase build-out for reference switching (“hitless”) and for phase hits on the selected reference
- Output vs. input phase offset control
- 21 bandwidth selections from 0.5mHz to 400Hz (vs. three selections for the T4 DPLL)
- Noise rejection circuitry for low-frequency references
- Output phase alignment to input frame-sync signal
- Several frequency averaging methods for acquiring the holdover frequency

The T4 DPLL has these additional features not available in the T0 DPLL:

- Three bandwidth selections limited to 18Hz to 70Hz
- Optional mode to measure the phase difference between two input clocks

Typically, the internal state machine controls the T0 DPLL, but manual control by system software is also available. The T4 DPLL has a simpler state machine that software cannot directly control. In either DPLL, however, software can override the DPLL logic using manual reference selection.

The output and feedback synthesizers are locked to either the T0 DPLL or the T4 DPLL. Most of the output signals that are locked to the same DPLL are always aligned to the falling edge at 2kHz.

The outputs of the T0 DPLL and the T4 DPLL can be connected to seven output DFS engines. See Figure 7-1. Three of these output DFS engines are associated with high-speed APLLs that multiply the DPLL clock rate and filter DPLL output jitter. The outputs of the APLLs are divided down to make a wide variety of possible frequencies available at the output clock pins. T0 APLL and T0 APLL2 are always locked to the T0 DPLL, while the T4 APLL can lock to either the T4 DPLL or the T0 DPLL. The output frequencies from the T0 DPLL can be synchronized to an input 2, 4, or 8kHz sync signal (SYNC1, SYNC2, or SYNC3 input pins). This synchronization to a low-frequency input enables, among other things, two redundant timing cards to maintain output frame-sync alignment with one another.

The OC1 to OC7 output clocks can be configured for a variety of different frequencies that are frequency and phase-locked to either the T0 DPLL or the T4 DPLL. The OC6 and OC7 outputs are LVDS/LVPECL; OC4 and OC5 are available in both LVDS/LVPECL and 3.3V CMOS; and OC1 to OC3 are 3.3V CMOS. There are five outputs OC1B to OC5B that can be 3.3V or 2.5V CMOS outputs. Altogether more than 60 output frequencies are possible, ranging from 2kHz to 312.5MHz. The FSYNC output clock is always 8kHz, and the MFSYNC output clock is always 2kHz.

## 7.2 Device Identification and Protection

The 16-bit read-only ID field in the ID1 and ID2 registers is set to 0C1Eh = 3102 decimal. The device revision can be read from the REV register. Contact the factory to interpret this value and determine the latest revision. The register set can be protected from inadvertent writes using the PROT register.

## 7.3 Local Oscillator and Master Clock Configuration

The T0 DPLL, the T4 DPLL, and the output DFS engines operate from a 204.8MHz master clock. The master clock is synthesized from a 12.800MHz clock originating from a local oscillator attached to the REFCLK pin. The stability of the T0 DPLL in free-run or holdover is equivalent to the stability of the local oscillator. Selection of an appropriate local oscillator is therefore of crucial importance if the telecom standards listed in Table 1-1 are to be met. Simple XOs or TCXOs can be used in less stringent cases, but OCXOs may be required in the most demanding applications. Even OCXOs may need to be shielded to avoid slow frequency changes due to ambient temperature fluctuations and drift. Careful evaluation of the local oscillator component is necessary to ensure proper performance. Contact Microsemi timing products technical support for recommended oscillators. For reference, the Telcordia GR-1244-CORE stability requirements for Stratum 2, Stratum 3E and Stratum 3 are listed in Table 7-1.

### Table 7-1. GR-1244 Stratum 2/3E/3 Stability Requirements

| PARAMETER | STRATUM 2 | STRATUM 3E | STRATUM 3 |
|---|---|---|---|
| Temperature | n/a | $\pm 10 \times 10^{-9}$ | $\pm 280 \times 10^{-9}$ |
| Drift (nontemp) | $\pm 1 \times 10^{-10}$/day | $\pm 1.16 \times 10^{-14}$/sec ($\pm 1 \times 10^{-9}$/day) | $\pm 4.63 \times 10^{-13}$/sec ($\pm 40 \times 10^{-9}$/day) |

***Note:*** *Refer to GR-1244-CORE for additional details.*

The stability of the local oscillator is very important, but its absolute frequency accuracy is less important because the DPLLs can compensate for frequency inaccuracies when synthesizing the 204.8MHz master clock from the local oscillator clock. The MCLKFREQ field in registers MCLK1 and MCLK2 specifies the frequency adjustment to be applied. The adjust can be from -771ppm to +514ppm in 0.0196229ppm (i.e., ~0.02ppm) steps.

The DS3102 has a watchdog circuit that causes an interrupt on the INTREQ pin when the local oscillator attached to the REFCLK pin is significantly off frequency. The watchdog interrupt is not maskable, but *is* subject to the INTCR register settings. When the watchdog circuit activates, reads of any and all registers in the device will return

00h to indicate the failure. In response to the activation of the INTREQ pin or during periodic polling, if system software ever reads 00h from the ID registers (which are hard-coded to 0C1Eh = 3102 decimal), it can conclude that the local oscillator attached to that DS3102 has failed. For proper operation of the watchdog timer, connect the WDT pin to a 10kΩ resistor (R) to $V_{DDIO}$ and a 0.01µF capacitor (C) to $V_{SS}$.

## 7.4 Input Clock Configuration

The DS3102 has eight input clocks: IC1 to IC6, IC8, and IC9. Table 7-2 provides summary information about each clock, including signal format and available frequencies. The device tolerates a wide range of duty cycles on input clocks, out to a minimum high time or minimum low time of 3ns or 30% of the clock period, whichever is smaller.

### 7.4.1 Signal Format Configuration

Inputs with CMOS/TTL signal format accept both TTL and 3.3V CMOS levels. One key configuration bit that affects the available frequencies is the SONSDH bit in MCR3. When SONSDH = 1 (SONET mode), the 1.544MHz frequency is available. When SONSDH = 0 (SDH mode), the 2.048MHz frequency is available. During reset the default value of this bit is latched from the SONSDH pin.

Input clocks IC1, IC2, IC5, and IC6 can be configured to accept LVDS, LVPECL, or CMOS/TTL signals by using the proper set of external components. The recommended LVDS termination is shown in Figure 10-1 while the recommended LVPECL termination is shown in Figure 10-2. The electrical specifications for these inputs are listed in Table 10-4. To configure these differential inputs to accept single-ended CMOS/TTL signals, use a voltage-divider to bias the ICxNEG pin to approximately 1.4V and connect the single-ended signal to the ICxPOS pin. If a differential input is not used it should be configured left unconnected (one input is internally pulled high and the other internally pulled low). (See also MCR5:IC5SF and IC6SF.)

**Table 7-2. Input Clock Capabilities**

| INPUT CLOCK | SIGNAL FORMATS | FREQUENCIES (MHz) | DEFAULT FREQUENCY |
|---|---|---|---|
| IC1 | LVDS/LVPECL or CMOS/TTL | Up to 156.25 (2) | 8kHz |
| IC2 | LVDS/LVPECL or CMOS/TTL | Up to 156.25 (2) | 8kHz |
| IC3 | CMOS/TTL | Up to 125 (1) | 8kHz |
| IC4 | CMOS/TTL | Up to 125 (1) | 8kHz |
| IC5 | LVDS/LVPECL or CMOS/TTL | Up to 156.25 (2) | 19.44MHz |
| IC6 | LVDS/LVPECL or CMOS/TTL | Up to 156.25 (2) | 19.44MHz |
| IC8 | CMOS/TTL | Up to 125 (1) | 19.44MHz |
| IC9 | CMOS/TTL | Up to 125 (1) | 19.44MHz |

**Note 1:** Available frequencies for CMOS/TTL input clocks are: 2kHz, 4kHz, 8kHz, 1.544MHz (SONET mode), 2.048MHz (SDH mode), 6.312MHz, 6.48MHz, 19.44MHz, 25.0MHz, 25.92MHz, 38.88MHz, 51.84MHz, 62.5MHz, 77.76MHz, and any multiple of 2kHz up to 125MHz.

**Note 2:** Available frequencies for LVDS/LVPECL input clocks include all CMOS/TTL frequencies in Note 1 plus any multiple of 8kHz up to 155.52MHz and 156.25MHz.

### 7.4.2 Frequency Configuration

Input clock frequencies are configured in the FREQ field of the ICR registers. The DIVN and LOCK8K bits of these same registers specify the locking frequency mode, as shown in Table 7-3.

## Table 7-3. Locking Frequency Modes

| DIVN | LOCK8K | LOCKING FREQUENCY MODE |
|---|---|---|
| 0 | 0 | Direct Lock |
| 0 | 1 | LOCK8K |
| 1 | 0 | DIVN |
| 1 | 1 | Alternate Direct Lock |

#### 7.4.2.1 Direct Lock Mode

In direct lock mode, the DPLLs lock to the selected reference at the frequency specified in the corresponding ICR register. Direct lock mode can only be used for input clocks with these specific frequencies: 2kHz, 4kHz, 8kHz, 1.544MHz, 2.048MHz, 5MHz, 6.312MHz, 6.48MHz, 19.44MHz, 25.92MHz, 31.25MHz, 38.88MHz, 51.84MHz, 77.76MHz, and 155.52MHz. For the 155.52MHz case, the input clock is internally divided by two, and the DPLL direct-locks at 77.76MHz. The DIVN mode can be used to divide an input down to any of these frequencies except 155.52MHz.

MTIE figures may be marginally better in direct lock mode because the higher frequencies allow more frequent phase updates.

#### 7.4.2.2 Alternate Direct Lock Mode

Alternate direct lock mode is the same as direct lock mode except an alternate list of direct lock frequencies is used (see the FREQ field definition in the ICR register description). The alternate frequencies are included to support clock rates found in Ethernet, CMTS, wireless, and GPS applications. The alternate frequencies are: 10MHz, 25MHz, 62.5MHz, 125MHz, and 156.25MHz. The frequencies 62.5MHz, 125MHz, and 156.25MHz are internally divided down to 31.25MHz, while 10MHz and 25MHz are internally divided down to 5MHz.

#### 7.4.2.3 LOCK8K Mode

In LOCK8K mode, an internal divider is configured to divide the selected reference down to 8kHz. The DPLL locks to the 8kHz output of the divider. LOCK8K mode can only be used for input clocks with the standard direct lock frequencies: 8kHz, 1.544MHz, 2.048MHz, 5MHz, 6.312MHz, 6.48MHz, 19.44MHz, 25.0MHz, 25.92MHz, 31.25MHz, 38.88MHz, 51.84MHz, 62.5MHz, 77.76MHz, and 155.52MHz. LOCK8K mode is enabled for a particular input clock by setting the LOCK8K bit in the corresponding ICR register.

LOCK8K mode gives a greater tolerance to input jitter when the multicycle phase detector is disabled because it uses lower frequencies for phase comparisons. The clock edge to lock to on the selected reference can be configured using the 8KPOL bit in the TEST1 register. For 2kHz and 4kHz clocks the LOCK8K bit is ignored and direct-lock mode is used.

#### 7.4.2.4 DIVN Mode

In DIVN mode, an internal divider is configured from the value stored in the DIVN registers. The DIVN value must be chosen so that when the selected reference is divided by DIVN + 1, the resulting clock frequency is the same as the standard direct lock frequency selected in the FREQ field of the ICR register. The DPLL locks to the output of the divider. DIVN mode can only be used for input clocks whose frequency is less than or equal to 155.52MHz. The DIVN register field can range from 0 to 65,535 inclusive. The same DIVN + 1 factor is used for all input clocks configured for DIVN mode. Note that although the DIVN divider is able to divide down clock rates as high as 155.52MHz, the CMOS/TTL inputs are only rated for a maximum clock rate of 125MHz.

## 7.5 Input Clock Monitoring

Each input clock is continuously monitored for frequency accuracy and activity. Frequency monitoring is desribed in Section 7.5.1, while activity monitoring is described in Sections 7.5.2 and 7.5.3. Any input clock that has a frequency out-of-band alarm or activity alarm is automatically declared invalid. The valid/invalid state of each input clock is reported in the corresponding real-time status bit in registers VALSR1 or VALSR2. When the valid/invalid state of a clock changes, the corresponding latched status bit is set in registers MSR1 or MSR2, and an interrupt request occurs if the corresponding interrupt enable bit is set in registers IER1 or IER2. Input clocks marked invalid cannot be automatically selected as the reference for either DPLL. If the T4 DPLL does not have any valid input clocks available, the T4NOIN status bit is set to 1 in MSR3.

### 7.5.1 Frequency Monitoring

The DS3102 monitors the frequency of each input clock and invalidates any clock whose frequency is outside specified limits. Two different monitors are available: the course frequency range monitor and the high-resolution frequency monitor. The course frequency range monitor can quickly (less than 2ms) determine whether the input clock frequency is within approximately 10,000ppm of the target frequency. When the frequency range monitor is enabled by setting MCR1:FREN = 1, input clocks with frequency outside the 10,000ppm limit are very quickly disqualified.

The high-resolution frequency monitor has two frequency limits that can be specified: a soft limit and a hard limit. For all input clocks except the T0 DPLL's selected reference, these limits are specified in the ILIMIT register. For the T0 DPLL's selected reference, the limits are specified in the SRLIMIT register. When the frequency of an input clock is greater than or equal to the soft limit, the corresponding SOFT alarm bit is set to 1 in the ISR registers. The soft limit is only for monitoring; triggering it does not invalidate the clock. When the frequency of an input clock is greater than or equal to the hard limit, the corresponding HARD alarm bit is set to 1 in the ISR registers, and the clock is marked invalid in the VALSR registers. Monitoring according to the hard and soft limits is enabled/disabled using the HARDEN and SOFTEN bits in the MCR10 register. Both the ILIMIT and SRLIMIT registers have a default soft limit of ±11.43ppm and a default hard limit of ±15.24ppm. Limits can be set from ±3.81ppm to ±60.96ppm in 3.81ppm steps. Frequency monitoring is only done on an input clock when the clock does not have an activity alarm.

Frequency measurements can be done with respect to the internal 204.8MHz master clock or the T0 DPLL internal frequency, as specified by the FMONCLK bit in MCR10. Measured frequency can be read from any frequency monitor by specifying the input clock in the FMEASIN field of MCR11 and reading the frequency from the FMEAS register.

### 7.5.2 Activity Monitoring

Each input clock is monitored for activity and proper behavior using a leaky bucket accumulator. A leaky bucket accumulator is similar to an analog integrator: the output amplitude increases in the presence of input events and gradually decays in the absence of events. When events occur infrequently, the accumulator value decays fully between events and no alarm is declared. When events occur close enough together, the accumulator increments faster than it can decay and eventually reaches the alarm threshold. After an alarm has been declared, if events occur infrequently enough, the accumulator can decay faster than it is incremented and eventually reaches the alarm clear threshold. The leaky bucket events come from the frequency range and fast activity monitors.

The leaky bucket accumulator for each input clock can be assigned one of four configurations (0 to 3) in the BUCKET field of the ICR registers. Each leaky bucket configuration has programmable size, alarm declare threshold, alarm clear threshold, and decay rate, all of which are specified in the LBxy registers.

Activity monitoring is divided into 128ms intervals. The accumulator is incremented once for each 128ms interval in which the input clock is inactive for more than two cycles (more than four cycles for 155.52MHz, 156.25MHz, 125MHz, 62.5MHz, 25MHz, and 10MHz input clocks). Thus the "fill" rate of the bucket is at most 1 unit per 128ms, or approximately 8 units/second. During each period of 1, 2, 4, or 8 intervals (programmable), the accumulator

decrements if no irregularities occur. Thus the “leak” rate of the bucket is approximately 8, 4, 2, or 1 units/second. A leak is prevented when a fill event occurs in the same interval.

When the value of an accumulator reaches the alarm threshold (LBxU register), the corresponding ACT alarm bit is set to 1 in the ISR registers, and the clock is marked invalid in the VALSR registers. When the value of an accumulator reaches the alarm clear threshold (LBxL register), the activity alarm is cleared by clearing the clock’s ACT bit. The accumulator cannot increment past the size of the bucket specified in the LBxS register. The decay rate of the accumulator is specified in the LBxD register. The values stored in the leaky bucket configuration registers must have the following relationship at all times: LBxS ≥ LBxU > LBxL.

When the leaky bucket is empty, the minimum time to declare an activity alarm in seconds is LBxU / 8 (where the x in LBxU is the leaky bucket configuration number 0 to 3). The minimum time to clear an activity alarm in seconds is 2^LBxD * (LBxS – LBxL) / 8. For example, assume LBxU = 8, LBxL = 1, LBxS = 10, and LBxD = 0. The minimum time to declare an activity alarm would be 8 / 8 = 1 second. The minimum time to clear the activity alarm would be 2^0 * (10 – 1) / 8 = 1.125 seconds.

### *7.5.3 Selected Reference Activity Monitoring*

The input clock that each DPLL is currently locked to is called the selected reference. The quality of a DPLL’s selected reference is exceedingly important, since missing cycles and other anomalies on the selected reference can cause unwanted jitter, wander, or frequency offset on the output clocks. When anomalies occur on the selected reference they must be detected as soon as possible to give the DPLL opportunity to temporarily disconnect from the reference until the reference is available again. By design, the regular input clock activity monitor (Section 7.5.2) is too slow to be suitable for monitoring the selected reference. Instead, each DPLL has its own fast activity monitor that detects that the frequency is within range (approximately 10,000ppm) and detects inactivity within approximately two missing reference clock cycles (approximately four missing cycles for 156.25MHz, 155.52MHz, 125MHz, 62.5MHz, 25MHz, and 10MHz references).

When the T0 DPLL detects a no-activity event, it immediately enters mini-holdover mode to isolate itself from the selected reference and sets the SRFAIL latched status bit in MSR2. The setting of the SRFAIL bit can cause an interrupt request if the corresponding enable bit is set in IER2. If MCR10:SRFPIN = 1, the SRFAIL output pin follows the state of the SRFAIL status bit. Optionally, a no-activity event can also cause an ultra-fast reference switch (see Section 7.6.4). When PHLIM1:NALOL = 0 (default), the T0 DPLL does not declare loss-of-lock during no-activity events. If the selected reference becomes available again before any alarms are declared by the activity monitor, the T0 DPLL continues to track the selected reference using nearest edge locking (±180°) to avoid cycle slips. When NALOL = 1, the T0 DPLL declares loss-of-lock during no-activity events. This causes the T0 DPLL state machine to transition to the loss-of-lock state, which sets the MSR2:STATE bit and causes an interrupt request if enabled. If the selected reference becomes available again before any alarms are declared by the activity monitor, the T0 DPLL tracks the selected reference using phase/frequency locking (±360°) until phase lock is reestablished.

When the T4 DPLL detects a no-activity event, its behavior is similar to the T0 DPLL with respect to the PHLIM1:NALOL control bit. Unlike the T0 DPLL, however, the T4 DPLL does not set the SRFAIL status bit. If NALOL = 1, the T4 DPLL clears the OPSTATE:T4LOCK status bit, which sets MSR3:T4LOCK and causes an interrupt request if enabled.

## 7.6 Input Clock Priority, Selection, and Switching

### 7.6.1 Priority Configuration

During normal operation, the selected reference for the T0 DPLL and the selected reference for the T4 DPLL are chosen automatically based on the priority rankings assigned to the input clocks in the input priority registers (IPR1 to IPR5). Each of these registers has priority fields for one or two input clocks. When T4T0 = 0 in the MCR11 register, the IPR registers specify the input clock priorities for the T0 DPLL. When T4T0 = 1, the IPR registers specify the input clock priorities for the T4 DPLL. The default input clock priorities, for both PLLs, are shown in Table 7-4.

Any unused input clock should be given the priority value 0, which disables the clock and marks it as unavailable for selection. Priority 1 is highest while priority 15 is lowest. The same priority can be given to two or more clocks.

**Table 7-4. Default Input Clock Priorities**

| INPUT CLOCK | T0 DPLL DEFAULT PRIORITY | T4 DPLL DEFAULT PRIORITY |
|---|---|---|
| IC1 | 0 (off) | 0 (off) |
| IC2 | 1 | 1 |
| IC3 | 2 | 2 |
| IC4 | 3 | 3 |
| IC5 | 0 (off) | 0 (off) |
| IC6 | 0 (off) | 0 (off) |
| IC8 | 4 | 5 |
| IC9 | 5 | 0 (off) |

### 7.6.2 Automatic Selection Algorithm

The real-time valid/invalid state of each input clock is maintained in the VALSR1 and VALSR2 registers. The selected reference can be marked invalid for phase lock, frequency, or activity. Other input clocks can be invalidated for frequency or activity.

The reference selection algorithm for each DPLL chooses the highest priority valid input clock to be the selected reference. To select the proper input clock based on these criteria, the selection algorithm maintains a priority table of valid inputs. The top three entries in this table and the selected reference are displayed in the PTAB1 and PTAB2 registers. When T4T0 = 0 in the MCR11 register, these registers indicate the highest priority input clocks for the T0 DPLL. When T4T0 = 1, they indicate the highest priority input clocks for the T4 DPLL.

If two or more input clocks are given the same priority number, those inputs are prioritized among themselves using a fixed circular list. If one equal-priority clock is the selected reference but becomes invalid, the next equal-priority clock in the list becomes the selected reference. If an equal-priority clock that is not the selected reference becomes invalid, it is simply skipped over in the circular list. The selection among equal-priority inputs is inherently nonrevertive, and revertive switching mode (see next paragraph) has no effect in the case where multiple equal-priority inputs have the highest priority.

An important input to the selection algorithm for the T0 DPLL is the REVERT bit in the MCR3 register. In revertive mode (REVERT = 1), if an input clock with a higher priority than the selected reference becomes valid, the higher priority reference immediately becomes the selected reference. In nonrevertive mode (REVERT = 0), the higher priority reference does not immediately become the selected reference but does become the highest priority reference in the priority table (REF1 field in the PTAB1 register). (The selection algorithm always switches to the highest priority valid input when the selected reference goes invalid, regardless of the state of the REVERT bit.) For many applications, nonrevertive mode is preferred for the T0 DPLL because it minimizes disturbances on the output clocks due to reference switching. The T4 DPLL always operates in revertive mode.

In nonrevertive mode, planned switchover to a newly valid higher priority input clock can be done manually under software control. The validation of the new higher priority clock sets the corresponding status bit in the MSR1 or MSR2 register, which can drive an interrupt request on the INTREQ pin if needed. System software can then respond to this change of state by briefly enabling revertive mode (toggling REVERT high then back low) to drive the switchover to the higher priority clock.

In most systems redundant timing cards are required, with one functioning as the master and the other as the slave. In such systems the priority tables of the master and slave must match. The register set makes it easy for the slave's priority table to track the master's table. At system start-up, the same priorities must be assigned to the input clocks, for both DPLLs, in the master and slave devices. During operation, if an input clock becomes valid or invalid in one device (master or slave), the change is flagged in that device's MSR1 or MSR2 register, which can drive an interrupt request on the INTREQ pin if needed. The real-time valid/invalid state of the input clocks can then be read from that device's VALSR1 and VALSR2 registers. Once the nature of the state change is understood, the control bits of the other device's VALCR1 and VALCR2 registers can be manipulated to mark clocks invalid in the other device as well.

### *7.6.3 Forced Selection*

The T0FORCE field in the MCR2 register and the T4FORCE field in the MCR4 register provide a way to force a specified input clock to be the selected reference for the T0 and T4 DPLLs, respectively. In both T0FORCE and T4FORCE, values of 0 and 15 specify normal operation with automatic reference selection. Values from 1 to 6 and 8 and 9 specify the input clock to be the forced selection; other values will cause no input to be selected. Internally, forcing is accomplished by giving the specified clock the highest priority (as specified in PTAB1:REF1). In revertive mode (MCR3:REVERT = 1) the forced clock automatically becomes the selected reference (as specified in PTAB1:SELREF) as well. In nonrevertive mode (T0 DPLL only) the forced clock only becomes the selected reference when the existing selected reference is invalidated or made unavailable for selection. In both revertive and nonrevertive modes when an input is forced to be the highest priority, the normal highest priority input (when no input is forced) is listed as the second-highest priority (PTAB2:REF2) and the normal second-highest priority input is listed as the third-highest priority (PTAB2:REF3).

When the T4 DPLL is used to measure the phase difference between the T0 DPLL selected reference and another reference input by setting the T0CR1:T4MT0 bit, the T4FORCE field in the MCR4 register can be used to select the other reference input.

### *7.6.4 Ultra-Fast Reference Switching*

By default, disqualification of the selected reference and switchover to another reference occurs when the activity monitor's inactivity alarm threshold has been crossed, a process that takes on the order of hundreds of milliseconds or seconds. For the T0 DPLL, an option for extremely fast disqualification and switchover is also available. When ultra-fast switching is enabled (MCR10:UFSW = 1), if the fast activity monitor detects approximately two missing clock cycles, it declares the reference failed by forcing the leaky bucket accumulator to its upper threshold (see Section 7.5.2) and initiates reference switching. This is in addition to setting the SRFAIL latched status bit in MSR2 and optionally generating an interrupt request, as described in Section 7.5.3. When ultra-fast switching occurs, the T0 DPLL transitions to the prelocked 2 state, which allows switching to occur faster by bypassing the loss-of-lock state. The device should be in nonrevertive mode when ultra-fast switching is enabled. If the device is in revertive mode, ultra-fast switching could cause excessive reference switching when the highest priority input is intermittent.

### *7.6.5 External Reference Switching Mode*

In this mode the SRCSW input pin controls reference switching between two clock inputs. This mode is enabled by setting the EXTSW bit to 1 in the MCR10 register. In this mode, if the SRCSW pin is high, the T0 DPLL is forced to lock to input IC3 (if the priority of IC3 is nonzero in IPR2) or IC5 (if the priority of IC3 is zero) whether or not the selected input has a valid reference signal. If the SRCSW pin is low, the T0 DPLL is forced to lock to input IC4 (if the priority of IC4 is nonzero in IPR2) or IC6 (if the priority of IC4 is zero) whether or not the selected input has a valid reference signal. During reset the default value of the EXTSW bit is latched from the SRCSW pin. If external reference switching mode is enabled during reset, the default frequency tolerance (DLIMIT registers) is configured to ±80ppm rather than the normal default of ±9.2ppm.

In external reference switching mode the device is simply a clock switch, and the T0 DPLL is forced to lock onto the selected reference whether it is valid. Unlike forced reference selection (Section 7.6.3) this mode controls the PTAB1:SELREF field directly and is, therefore, not affected by the state of the MCR3:REVERT bit. During external reference switching mode, only PTAB1:SELREF is affected; the REF1, REF2, and REF3 fields in the PTAB registers continue to indicate the highest, second-highest, and third-highest priority valid inputs chosen by the automatic selection logic. External reference switching mode only affects the T0 DPLL.

### *7.6.6 Output Clock Phase Continuity During Reference Switching*

If phase build-out is enabled (PBOEN = 1 in MCR10) or the DPLL frequency limit (DLIMIT) is set to less than ±30ppm, the device always complies with the GR-1244-CORE requirement that the rate of phase change must be less than 81ns per 1.326ms during reference switching.

### *7.6.7 Frequency Monitoring Hysteresis Required by Telcordia GR-1244-CORE*

For stratum 3 and stratum 3E applications, taking all Telcordia GR-1244-CORE requirements together, the DS3102 must accept input clocks with frequency offsets of less than ±9.2ppm and must reject input clocks with frequency offsets of more than ±12.0ppm. In between 9.2ppm and 12.0ppm the actual accept and reject thresholds must be separated by at least 0.46ppm.

To realize GR-1244-CORE compliant thresholds for stratum 3 and stratum 3E, the appropriate settings are ILIMIT.HARD=2, DLIMIT1,2.HARDLIM=0x99, SRLIMIT.HARD=3.

An accept threshold greater than 9.2ppm is provided by the ILIMIT.HARD value. Setting ILIMIT.HARD=2 gives a value of 11.43ppm according to the register description, but the actual threshold is halfway between the values given in the register description. Therefore ILIMIT.HARD=2 is halfway between 7.62ppm and 11.43ppm. This gives an accept threshold of 9.53ppm.

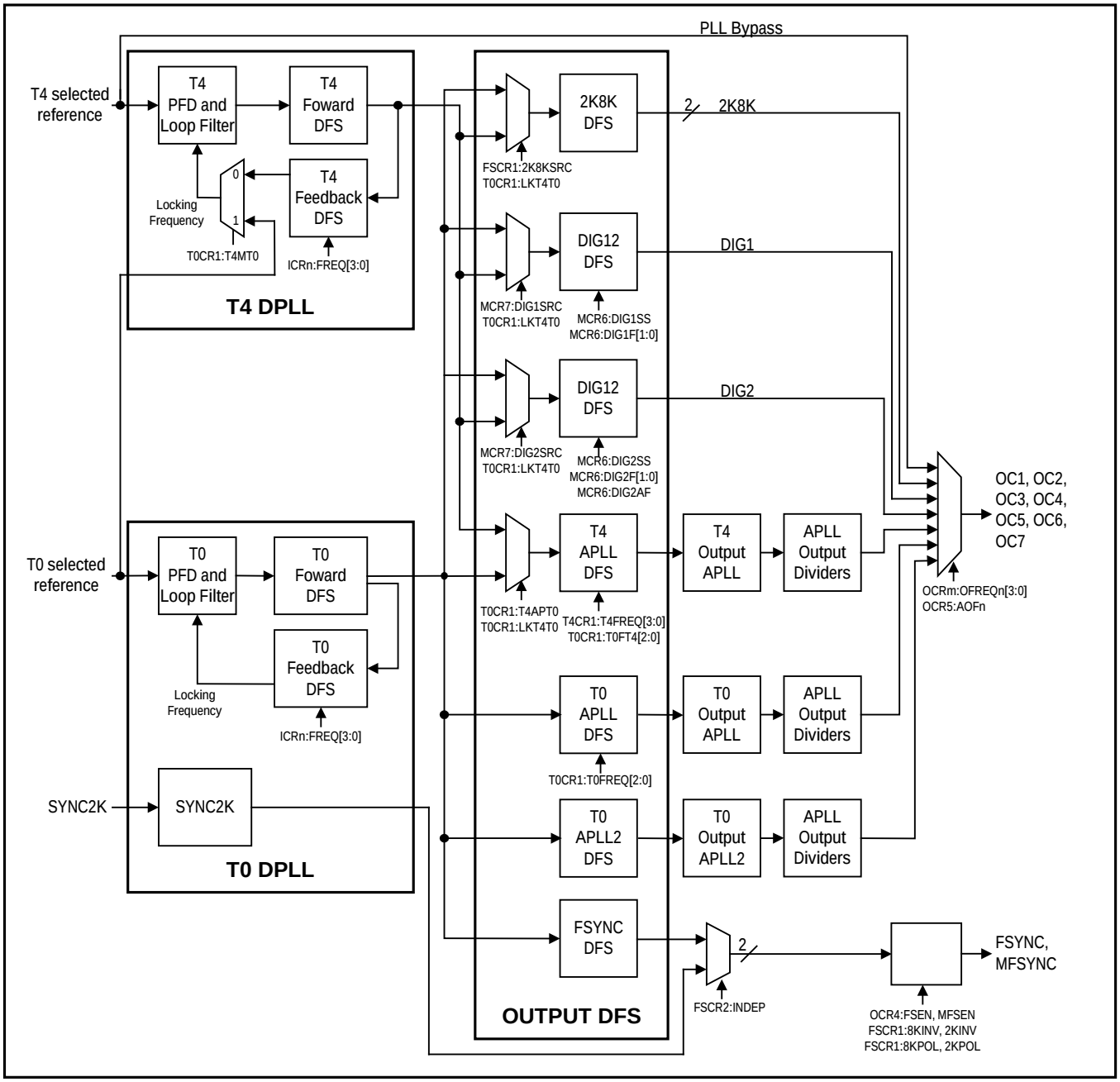
A reject threshold less than 12.0ppm is provided by the DLIMIT1,2.HARDLIM value. If the frequency of the selected reference exceeds this limit the DPLL does not track it and goes out of lock. After a loss-of-lock timeout (specified by PHLKTO) the DPLL rejects the input.

Finally, the SRLIMIT.HARD=3 value provides a backup reject threshold in case the selected reference frequency goes off frequency too rapidly. As with ILIMIT.HARD, the actual threshold is halfway between the values given in the register description. Therefore SRLIMIT.HARD=3 is halfway between 11.43ppm and 15.24ppm. This gives a backup reject threshold of 13.34ppm.

## 7.7 DPLL Architecture and Configuration

Both T0 and T4 are digital PLLs with separate analog PLLs (APLLs) as the output stage. This architecture combines the benefits of both PLL types. See Figure 7-1.

*Figure 7-1. DPLL Block Diagram*



Digital PLLs have two key benefits: (1) stable, repeatable performance that is insensitive to process variations, temperature, and voltage; and (2) flexible behavior that is easily programmed through the configuration registers. DPLLs use digital frequency synthesis (DFS) to generate various clocks. In DFS a high-speed master clock (204.8MHz) is multiplied up from the 12.800MHz local oscillator clock applied to the REFCLK pin. This master clock is then digitally divided down to the desired output frequency. The DFS output clock has jitter of about 1ns pk-pk.

The analog PLLs filter the jitter from the DPLLs, reducing the 1ns pk-pk jitter to less than 0.5ns pk-pk and 60ps RMS, typical, measured broadband (10Hz to 1GHz).

The DPLLs in the device are configurable for many PLL parameters including bandwidth, damping factor, input frequency, pull-in/hold-in range, input-to-output phase offset, phase build-out, and more. No knowledge of loop equations or gain parameters is required to configure and operate the device. No external components are required for the DPLLs or the APLLs except the high-quality local oscillator connected to the REFCLK pin.

The T0 DPLL to T0 APLL path is the main path through the device. The T0 DPLL has a full free-run/locked/holdover state machine and full programmability. The T4 DPLL to T4 APLL path is a simpler frequency converter/synthesis path, lacking the low bandwidth settings, phase build-out, and phase adjustment controls found in the T0 DPLL.

### *7.7.1 T0 DPLL State Machine*

The T0 DPLL has three main timing modes: locked, holdover, and free-run. The control state machine for the T0 DPLL has states for each timing mode as well as three temporary states: prelocked, prelocked 2, and loss-of-lock. The state transition diagram is shown in Figure 7-2. Descriptions of each state are given in the paragraphs below. During normal operation the state machine controls state transitions. When necessary, however, the state can be forced using the T0STATE field of the MCR1 register.

Whenever the T0 DPLL changes state, the STATE bit in MSR2 is set, which can cause an interrupt request if enabled. The current T0 DPLL state can be read from the T0STATE field of the OPSTATE register.

#### *7.7.1.1 Free-Run State*

Free-run mode is the reset default state. In free-run all output clocks are derived from the 12.800MHz local oscillator attached to the REFCLK pin. The frequency of each output clock is a specific multiple of the local oscillator. The frequency accuracy of each output clock is equal to the frequency accuracy of the master clock, which can be calibrated using the MCLKFREQ field in registers MCLK1 and MCLK2 (see Section 7.3). The state machine transitions from free-run to the prelocked state when at least one input clock is valid.

#### *7.7.1.2 Prelocked State*

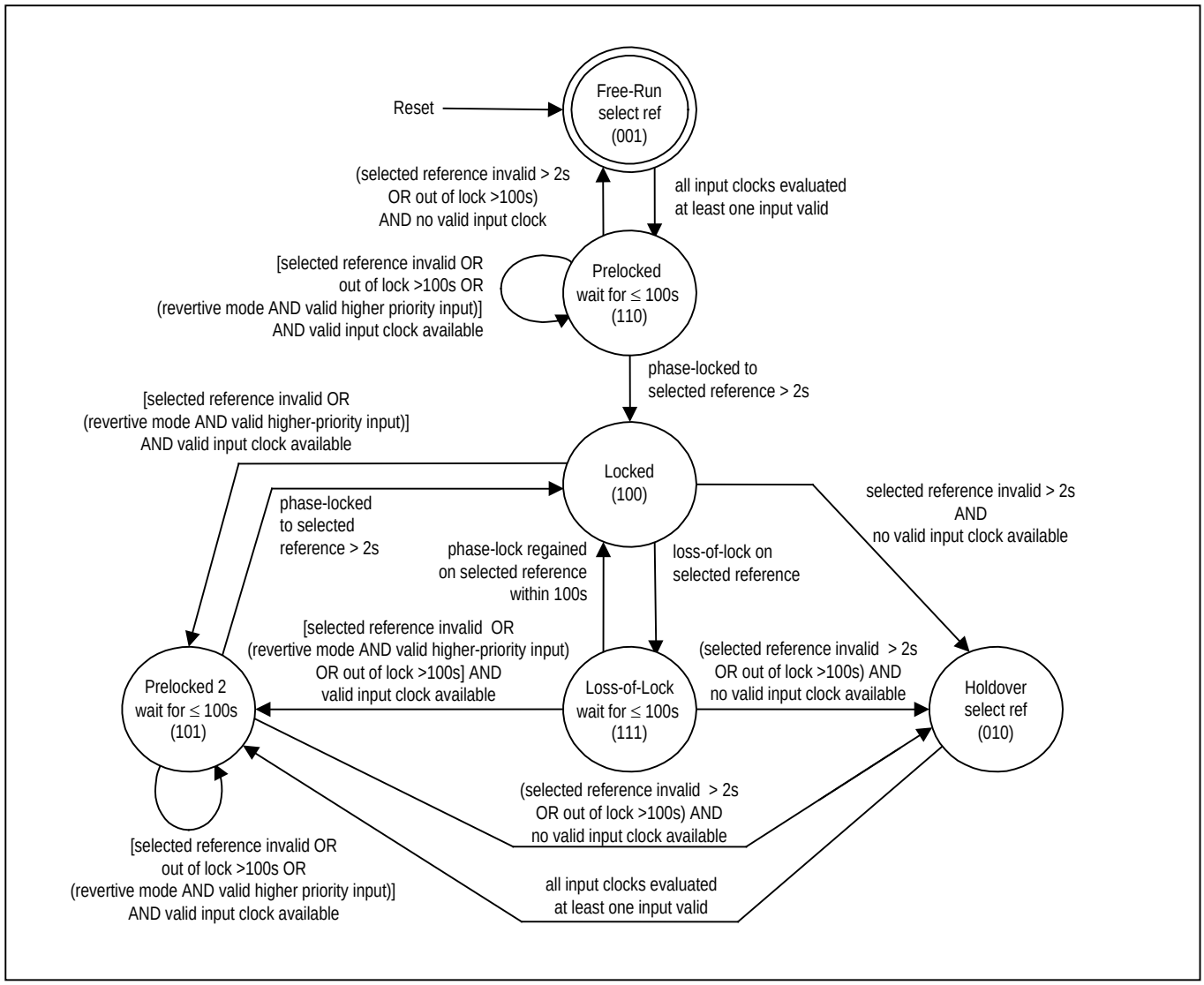
The prelocked state provides a 100-second period (default value of PHLKTO register) for the DPLL to lock to the selected reference. If phase lock (see Section 7.7.6) is achieved for 2 seconds during this period, the state machine transitions to locked mode.

If the DPLL fails to lock to the selected reference within the phase-lock timeout period specified by PHLKTO, a phase-lock alarm is raised (corresponding LOCK bit set in the ISR register), invalidating the input (ICn bit goes low in VALSR registers). If another input clock is valid, the state machine re-enters the prelocked state and tries to lock to the alternate input clock. If no other input clocks are valid for two seconds, the state machine transitions back to the free-run state.

In revertive mode (REVERT = 1 in MCR3), if a higher priority input clock becomes valid during the phase-lock timeout period, the state machine re-enters the prelocked state and tries to lock the higher priority input.

If a phase-lock timeout period longer than 100 seconds is required for locking (such as 700 seconds for Stratum 3E or 1000 seconds for Stratum 2 applications), the PHLKTO register must be configured accordingly.

*Figure 7-2. T0 DPLL State Transition Diagram*




**Note 1:** An input clock is valid when it has no activity alarm, no hard frequency limit alarm, and no phase-lock alarm (see the VALSR registers and the ISR registers).

**Note 2:** All input clocks are continuously monitored for activity and frequency.

**Note 3:** Only the selected reference is monitored for loss-of-lock.

**Note 4:** Phase lock is declared internally when the DPLL has maintained phase lock continuously for approximately 1 to 2 seconds.

**Note 5:** To simply the diagram, the phase-lock timeout period is always shown as 100s, which is the default value of the PHLKTO register. Longer or shorter timeout periods can be specified as needed by writing the appropriate value to the PHLKTO register.

**Note 6:** When selected reference is invalid and the DPLL is not in free-run or holdover, the DPLL is in a temporary holdover state.

#### 7.7.1.3 Locked State

The T0 DPLL state machine can reach the locked state from the prelocked, prelocked 2, or loss-of-lock states when the DPLL has locked to the selected reference for at least 2 seconds (see Section 7.7.6). In the locked state the output clocks track the phase and frequency of the selected reference.

If the MCR1.LOCKPIN bit is set, the LOCK pin is driven high when the T0 DPLL is in the locked state.

While in the locked state, if the selected reference is so impaired that an activity alarm or a hard frequency limit alarm is raised (corresponding ACT bit set in the ISR register), the selected reference is invalidated (ICn bit goes low in VALSR registers), and the state machine immediately transitions to either the prelocked 2 state (if another valid input clock is available) or, after being invalid for 2 seconds, to the holdover state (if no other input clock is valid).

If loss-of-lock (see Section 7.7.6) is declared while in the locked state, the state machine transitions to the loss-of-lock state.

#### 7.7.1.4 Loss-of-Lock State

When the loss-of-lock detectors (see Section 7.7.6) indicate loss-of-lock, the state machine immediately transitions from the locked state to the loss-of-lock state. In the loss-of-lock state the DPLL tries for 100 seconds (default value of PHLKTO register) to regain phase lock. If phase lock is regained during that period for more than 2 seconds, the state machine transitions back to the locked state.

If during the phase-lock timeout period specified by PHLKTO the selected reference is so impaired that an activity alarm or a hard frequency limit alarm is raised (corresponding ACT bit or HARD bit set in the ISR registers), the selected reference is invalidated (ICn bit goes low in VALSR registers), and after being invalid for 2 seconds the state machine transitions to either the prelocked 2 state (if another valid input clock is available) or the holdover state (if no other input clock is valid).

If phase lock cannot be regained by the end of the phase-lock timeout period, a phase-lock alarm is raised (corresponding LOCK bit set in the ISR registers), the selected reference is invalidated (ICn bit goes low in VALSR registers), and the state machine transitions to either the prelocked 2 state (if another valid input clock is available) or, after being invalid for 2 seconds, to the holdover state (if no other input clock is valid).

#### 7.7.1.5 Prelocked 2 State

The prelocked and prelocked 2 states are similar. The prelocked 2 state provides a 100-second period (default value of PHLKTO register) for the DPLL to lock to the new selected reference. If phase lock (see Section 7.7.6) is achieved for more than 2 seconds during this period, the state machine transitions to locked mode.

If the DPLL fails to lock to the new selected reference within the phase-lock timeout period specified by PHLKTO, a phase-lock alarm is raised (corresponding LOCK bit set in the ISR registers), invalidating the input (ICn bit goes low in VALSR registers). If another input clock is valid, the state machine re-enters the prelocked 2 state and tries to lock to the alternate input clock. If no other input clocks are valid for 2 seconds, the state machine transitions to the holdover state.

In revertive mode (REVERT = 1 in MCR3), if a higher priority input clock becomes valid during the phase-lock timeout period, the state machine re-enters the prelocked 2 state and tries to lock to the higher priority input.

If a phase-lock timeout period longer than 100 seconds is required for locking (such as 700 seconds for Stratum 3E or 1000 seconds for Stratum 2 applications), the PHLKTO register must be configured accordingly.

#### 7.7.1.6 Holdover State

The device reaches the holdover state when it declares its selected reference invalid for 2 seconds and has no other valid input clocks available. During holdover the T0 DPLL is not phase-locked to any input clock but instead generates its output frequency from stored frequency information, which is typically the averaged frequency of the

DPLL when it was in the locked state. The device can be configured for manual or automatic holdover as described in the following subsections. When at least one input clock has been declared valid, the state machine immediately transitions from holdover to the prelocked 2 state and tries to lock to the highest priority valid clock.

#### *7.7.1.6.1 Automatic Holdover*

For automatic holdover (FRUNHO = 0 in MCR3), the device can be further configured for instantaneous mode or averaged mode. In *instantaneous mode* (AVG = 0 in HOCR3), the holdover frequency is set to the DPLL's current frequency 50ms to 100ms before entry into holdover (i.e., the value of the FREQ field in the FREQ1, FREQ2, and FREQ3 registers when MCR11:T4T0 = 0). The FREQ field is the DPLL's integral path and, therefore, is an average frequency with a rate of change inversely proportional to the DPLL bandwidth. The DPLL's proportional path is not used in order to minimize the effect of recent phase disturbances on the holdover frequency.

In *averaged mode* (AVG = 1 in HOCR3 and MANHO = 0 in MCR3), the holdover frequency is set to an internally averaged value. During locked operation the frequency indicated in the FREQ field is internally averaged. The FAST bit in HOCR3 determines the period of this averaging. When FAST = 1, the frequency is averaged for a period of approximately 8 minutes. When FAST = 0 (slow), the frequency is averaged for a period of approximately 110 minutes. The T0 DPLL indicates that it has acquired valid holdover values by setting the FHORDY and SHORDY status bits in VALSR2 (real-time status) and MSR4 (latched status). If FAST = 0 and the T0 DPLL must enter holdover before the 110-minute average is available, the 8-minute average is used, if available. Otherwise, the instantaneous value from the integral path is used. If FAST = 1 and the T0 DPLL must enter holdover before the 8-minute average is available, an instantaneous value of 50ms to 100ms old from the integral path is used instead.

#### *7.7.1.6.2 Manual Holdover*

For *manual holdover* (MANHO = 1 in MCR3), the holdover frequency is set by the HOFREQ field in the HOCR1, HOCR2, and HOCR3 registers. The HOFREQ field has the same size and format as the current frequency field (FREQ[18:0] in the FREQ1, FREQ2, and FREQ3 registers). If desired, software can, during locked operation, read the current frequency from FREQ, filter or average it over time, and write the resulting holdover frequency to HOFREQ. The FREQ field is derived from the DPLL's integral path, and thus can be considered an average frequency with a rate of change inversely proportional to the DPLL bandwidth.

To combine internal averaging with additional software filtering, the HOFREQ field can be configured to read out the internally averaged frequency when RDAVG = 1 in the HOCR3 register. This averaged value can be read from HOFREQ regardless of the current holdover mode. The FAST bit in HOCR3 specifies whether the value read is from the fast averager or the slow averager.

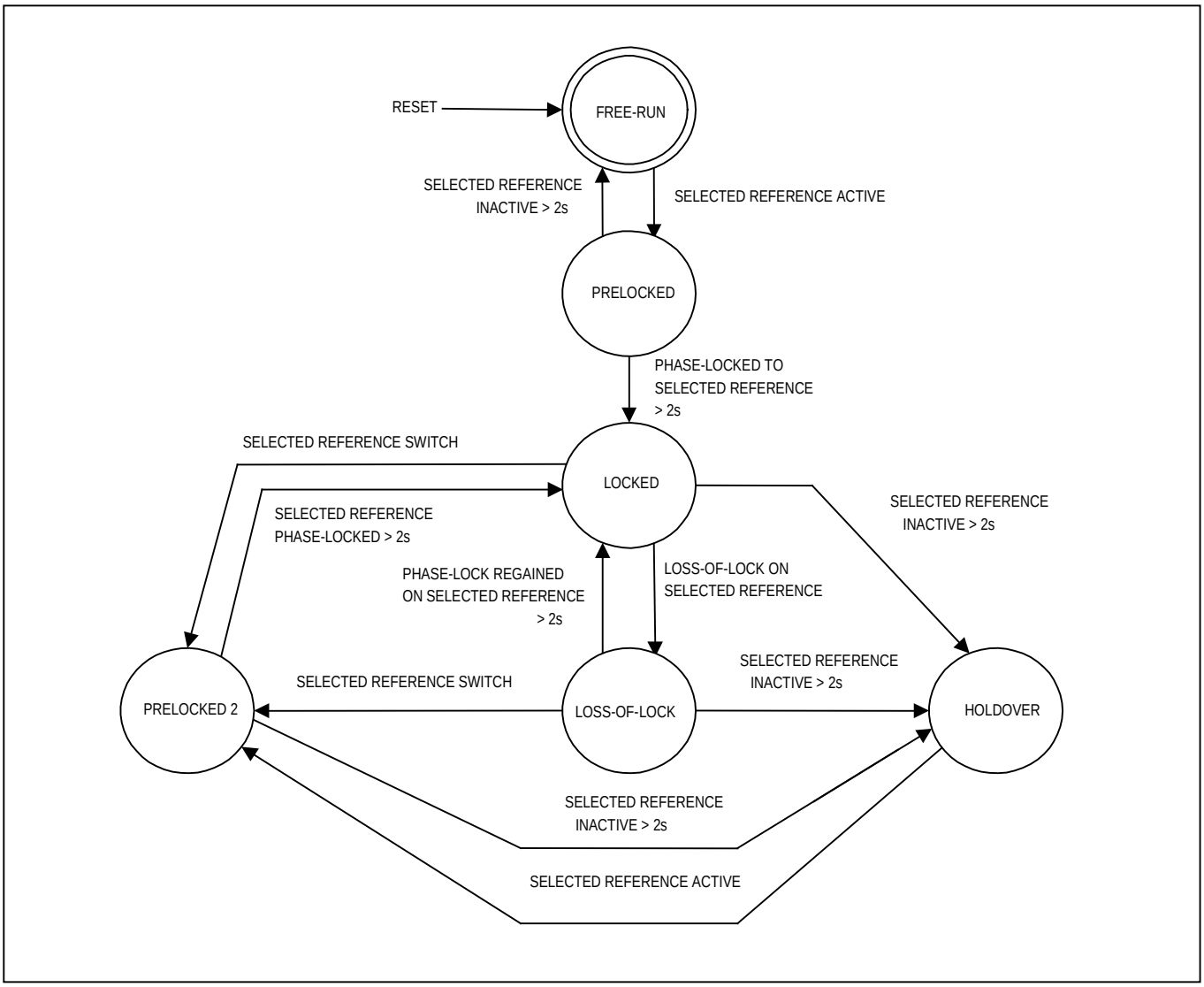
### *7.7.1.7 Mini-Holdover*

When the selected reference fails, the fast activity monitor (Section 7.5.3) isolates the T0 DPLL from the reference within one or two clock cycles to avoid adverse effects on the DPLL frequency. When this fast isolation occurs, the DPLL enters a temporary mini-holdover mode, with a frequency as specified by the MINIHO field of HOCR3. Mini-holdover lasts until the selected reference returns or a new input clock has been chosen as the selected reference or the state machine enters the holdover state. If the manual holdover mode is set (MANHO = 1 in MCR3), the MINIHO field of HOCR3 is ignored and the mini-holdover frequency is the same as the manual holdover frequency.

## *7.7.2 T4 DPLL State Machine*

The T4 DPLL state machine is similar to the T0 DPLL, as shown in Figure 7-3. The T4 DPLL states are similar to the equivalent states of the T0 DPLL, but the only state indicator is the T4LOCK bit in the OPSTATE register. Note that the T4 DPLL only operates in revertive switching mode. The full-holdover and mini-holdover modes are instantaneous (see the first paragraph of Section 7.7.1.6.1).

*Figure 7-3. T4 DPLL State Transition Diagram*



### 7.7.3 Bandwidth

The bandwidth of the T4 DPLL is configured in the T4BW register to be 18Hz to 70Hz.

The bandwidth of the T0 DPLL is configured in the T0ABW and T0LBW registers for various values from 0.5mHz to 400Hz. The AUTOBW bit in the MCR9 register controls automatic bandwidth selection. When AUTOBW = 1, the T0 DPLL uses the T0ABW bandwidth during acquisition (not phase-locked) and the T0LBW bandwidth when phase-locked. When AUTOBW = 0 the T0 DPLL uses the T0LBW bandwidth all the time, both during acquisition and when phase-locked.

When LIMINT = 1 in the MCR9 register, the DPLL's integral path is limited (i.e., frozen) when the DPLL reaches minimum or maximum frequency. Setting LIMINT = 1 minimizes overshoot when the DPLL is pulling in.

### 7.7.4 Damping Factor

The damping factor for the T0 DPLL is configured in the DAMP field of the T0CR2 register, while the damping factor of the T4 DPLL is configured in the DAMP field of the T4CR2 register. The reset default damping factors for both DPLLs are chosen to give a maximum jitter/wander gain peak of approximately 0.1dB. Available settings are a function of DPLL bandwidth (configured in the T4BW, T0ABW, and T0LBW registers). See Table 7-5.

## Table 7-5. Damping Factors and Peak Jitter/Wander Gain

| BANDWIDTH (Hz) | DAMP[2:0] VALUE | DAMPING FACTOR | GAIN PEAK (dB) |
|---|---|---|---|
| 0.5m to 4 | 1, 2, 3, 4, 5 | 5 | 0.1 |
| 8 | 1 | 2.5 | 0.2 |
| | 2, 3, 4, 5 | 5 | 0.1 |
| 18 | 1 | 1.2 | 0.4 |
| | 2 | 2.5 | 0.2 |
| | 3, 4, 5 | 5 | 0.1 |
| 35 | 1 | 1.2 | 0.4 |
| | 2 | 2.5 | 0.2 |
| | 3 | 5 | 0.1 |
| | 4, 5 | 10 | 0.06 |
| 70 to 400 | 1 | 1.2 | 0.4 |
| | 2 | 2.5 | 0.2 |
| | 3 | 5 | 0.1 |
| | 4 | 10 | 0.06 |
| | 5 | 20 | 0.03 |

### 7.7.5 Phase Detectors

Phase detectors are used to compare a PLL's feedback clock with its input clock. Several phase detectors are available in the T0 and T4 DPLLs:

- Phase/frequency detector (PFD)
- Early/late phase detector (PD2) for fine resolution
- Multicycle phase detector (MCPD) for large input jitter tolerance and/or faster lock times

These detectors can be used in combination to give fine phase resolution combined with large jitter tolerance. As with the rest of the DPLL logic, the phase detectors operate at input frequencies up to 77.76MHz. The multicycle phase detector detects and remembers phase differences of many cycles (up to 8191UI). When locking to 8kHz or lower, the normal phase/frequency detectors are always used.

The T0 DPLL phase detectors can be configured for normal phase/frequency locking (±360° capture) or nearest edge phase locking (±180° capture). With nearest edge detection the phase detectors are immune to occasional missing clock cycles. The DPLL automatically switches to nearest edge locking when the multicycle phase detector is disabled and the other phase detectors determine that phase lock has been achieved. Setting D180 = 1 in the TEST1 register disables nearest edge locking and forces the T0 DPLL to use phase/frequency locking. The T4 DPLL always has nearest edge locking enabled.

The early/late phase detector, also known as phase detector 2, is enabled and configured in the PD2 fields of registers T0CR2 and T0CR3 for the T0 DPLL and registers T4CR2 and T4CR3 for the T4 DPLL. The reset default settings of these registers are appropriate for all operating modes. Adjustments only affect small signal overshoot and bandwidth.

The multicycle phase detector is enabled by setting MCPDEN = 1 in the PHLIM2 register. The range of the MCPD—from ±1UI up to ±8191UI—is configured in the COARSELIM field of PHLIM2. The MCPD tracks phase position over many clock cycles, giving high jitter tolerance. Thus, the use of the MCPD is an alternative to the use of LOCK8K mode for jitter tolerance. When a DPLL is direct locking to 8kHz, 4kHz, or 2kHz, or in LOCK8K mode, the multicycle phase detector is automatically disabled.

When USEMCPD = 1 in PHLIM2, the MCPD is used in the DPLL loop, giving faster pull-in but more overshoot. In this mode the loop has similar behavior to LOCK8K mode. In both cases large phase differences contribute to the dynamics of the loop. When enabled by MCPDEN = 1, the MCPD tracks the phase position whether or not it is used in the DPLL loop.

When the input clock is divided before being sent to the phase detector, the divider output clock edge gets aligned to the feedback clock edge before the DPLL starts to lock to a new input clock signal or after the input clock signal has a temporary signal loss. This helps ensure locking to the nearest input clock edge, which reduces output transients and decreases lock times.

### 7.7.6 Loss-of-Lock Detection

Loss-of-lock can be triggered by any of the following in both the T0 and T4 DPLLs:

- The fine phase-lock detector (measures phase between input and feedback clocks)
- The coarse phase-lock detector (measures whole cycle slips)
- Hard frequency limit detector
- Inactivity detector

The fine phase-lock detector is enabled by setting FLEN = 1 in the PHLIM1 register. The fine phase limit is configured in the FINELIM field of PHLIM1.

The coarse phase-lock detector is enabled by setting CLEN = 1 in the PHLIM2 register. The coarse phase limit is configured in the COARSELIM field of PHLIM2. This coarse phase-lock detector is part of the multicycle phase detector (MCPD) described in Section 7.7.5. The COARSELIM field sets both the MCPD range and the coarse phase limit, since the two are equivalent. If loss-of-lock should not be declared for multiple-UI input jitter, the fine phase-lock detector should be disabled and the coarse phase-lock detector should be used instead.

The hard frequency limit detector is enabled by setting FLLOL = 1 in the DLIMIT3 register. The hard limit for the T0 DPLL is configured in registers DLIMIT1 and DLIMIT2. The T4 DPLL hard limit is fixed at ±80ppm. When the DPLL frequency reaches the hard limit, loss-of-lock is declared. The DLIMIT3 register also has the SOFTLIM field to specify a soft frequency limit. Exceeding the soft frequency limit does not cause loss-of-lock to be declared. When the T0 DPLL frequency reaches the soft limit, the T0SOFT status bit is set in the OPSTATE register. When the T4 DPLL frequency reaches the soft limit, the T4SOFT status bit is set in OPSTATE.

The inactivity detector is enabled by setting NALOL = 1 in the PHLIM1 register. When this detector is enabled the DPLL declares loss-of-lock after one or two missing clock cycles on the selected reference. See Section 7.5.3.

When the T0 DPLL declares loss-of-lock, the state machine immediately transitions to the loss-of-lock state, which sets the STATE bit in the MSR2 register and requests an interrupt if enabled.

When the T4 DPLL declares loss-of-lock, the T4LOCK bit is cleared in the OPSTATE register, which sets the T4LOCK bit in the MSR3 register and requests an interrupt if enabled.

### 7.7.7 Phase Build-Out

#### 7.7.7.1 Phase Monitor

The T0 DPLL has a phase monitor that measures the phase error between the input clock reference and the DPLL output. The phase monitor is enabled by setting PHMON:PMEN = 1. When the T0 DPLL is set for low bandwidth, a phase transient on the input causes an immediate phase error that is gradually reduced as the DPLL tracks the input. When the measured phase error exceeds the limit set in the PHMON:PMLIM field, the phase monitor declares a phase monitor alarm by setting the MSR3:PHMON bit. The PMLIM field can be configured for a limit ranging from about 1µs to about 3.5µs.

#### 7.7.7.2 Phase Build-Out in Response to Input Phase Transients

See Telcordia GR-1244-CORE Section 5.7 for an explanation of phase build-out (PBO) and the requirement for Stratum 2 and 3E clocks to perform PBO in response to input phase transients.

When the phase monitor is enabled (as described in Section 7.7.7.1) and PHMON:PMPBEN = 1, the T0 DPLL automatically triggers PBO events in response to input transients greater than the limit set in PHMON:PMLIM. The range of limits available in the PMLIM field allows the T0 DPLL to be configured to build out input transients greater than 3.5µs, greater than 1µs, or any threshold in between.

To determine when to perform PBO, the phase monitor watches for phase changes greater than 100ns in a 10ms interval on the selected reference. When such a phase change occurs, an internal 0.1 second timer is started. If during this interval the phase change is greater than the PMLIM threshold then a PBO event occurs. During a PBO event the device enters a temporary holdover state in which the phase difference between the selected reference and the output is measured and fed into the DPLL loop to absorb the input transient. After a PBO event, regardless of the input phase transient, the output phase transient is less than or equal to 5ns. Phase build-out can be frozen at the current phase offset by setting MCR10:PBOFRZ = 1. When PBO is frozen the T0 DPLL ignores subsequent phase build-out events and maintains the current phase offset between input and outputs.

#### 7.7.7.3 Automatic Phase Build-Out in Response to Reference Switching

When MCR10:PBOEN = 0, phase build-out is not performed during reference switching. The T0 DPLL always locks to the selected reference at zero degrees of phase. With PBO disabled, transitions from a failed reference to the next highest priority reference and transitions from holdover or free-run to locked mode cause phase transients on output clocks as the T0 DPLL jumps from its previous phase to the phase of the new selected reference.

When MCR10:PBOEN = 1, phase build-out is performed during reference switching (or exiting from holdover). With PBO enabled, if the selected reference fails and another valid reference is available, the device enters a temporary holdover state in which the phase difference between the new reference and the output is measured and fed into the DPLL loop to absorb the input phase difference. Similarly, during transitions from full holdover, mini-holdover, or free-run to locked mode, the phase difference between the new reference and the output is measured and fed into the DPLL loop to absorb the input phase difference. After a PBO event, regardless of the input phase difference, the output phase transient is less than or equal to 5ns.

Any time that PBO is enabled it can also be frozen at the current phase offset by setting MCR10:PBOFRZ = 1. When PBO is frozen, the T0 DPLL ignores subsequent phase build-out events and maintains the current phase offset between inputs and outputs.

Disabling PBO while the T0 DPLL is not in the free-run or holdover states (locking or locked) causes a phase change on the output clocks while the DPLL switches to tracking the selected reference with zero degrees of phase error. The rate of phase change on the output clocks depends on the DPLL bandwidth. Enabling PBO (which includes unfreezing) while locking or locked also causes a PBO event.

#### 7.7.7.4 PBO Phase Offset Adjustment

An uncertainty of up to 5ns is introduced each time a phase build-out event occurs. This uncertainty results in a phase hit on the output. Over a large number of phase build-out events the mean error should be zero. The PBOFF register specifies a small fixed offset for each phase build-out event to skew the average error toward zero and eliminate accumulation of phase shifts in one direction.

### 7.7.8 Input to Output (Manual) Phase Adjustment

When phase build-out is disabled (PBOEN = 0 in MCR10), the OFFSET registers can be used to adjust the phase of the T0 DPLL output clocks with respect to the selected reference when locked. Output phase offset can be adjusted over a ±200ns range in 6ps increments. This phase adjustment occurs in the feedback clock so that the output clocks are adjusted to compensate. The rate of change is therefore a function of DPLL bandwidth. Simply writing to the OFFSET registers with phase build-out disabled causes a change in the input to output phase, which can be considered to be a delay adjustment. Changing the OFFSET adjustment while in free-run or holdover state does not cause an output phase offset until it exits the state and enters one of the locking states.

### 7.7.9 Phase Recalibration

When a phase buildout occurs, either automatic or manual, the feedback frequency synthesizer does not get an internal alignment signal to keep it aligned with the output dividers, and, therefore, the phase difference between input and output can become incorrect. Setting the FSCR3:RECAL bit periodically causes a recalibration process to be executed, which corrects any phase error that may have occurred.

During the recalibration process the device puts the DPLL into mini-holdover, internally ramps the phase offset to zero, resets all clock dividers, ramps the phase offset to the value stored in the OFFSET registers, and switches the DPLL out of mini-holdover. If the OFFSET registers are written during the recalibration process, the process ramps the phase offset to the new offset value.

### 7.7.10 Frequency and Phase Measurement

When the T4 DPLL is not needed to generate an output frequency locked to an input clock, it can measure precise frequency by locking onto any input. It can also measure phase between the T0 selected reference and any input by setting the T0CR1.T4MT0 bit. The T4 APLL can still be used to clean up jitter on a synthesized clock from the T0 DPLL. When the T0CR1.T4MT0 bit is set the T4 DPLL goes to the free-run state.

Standard input clock frequency monitoring is described in Section 7.5.1. The input clock monitors report measured frequency with 3.8ppm resolution. More accurate measurement of frequency and phase can be accomplished using the DPLLs. The T0 DPLL is always monitoring its selected reference, but if the T4 DPLL is not otherwise used to lock to an input, it can be configured as a high-resolution phase monitor. The REFCLK signal accuracy after being adjusted with MCLKFREQ is used for the frequency reference. Software can then connect the T4 DPLL to various input clocks on a rotating basis to measure phase between the T0 DPLL input and another input. See the T4FORCE field of MCR4.

DPLL frequency measurements can be read from the FREQ field spanning registers FREQ1, FREQ2, and FREQ3. This field indicates the frequency of the selected reference for either the T0 DPLL or the T4 DPLL, depending on the setting of the T4T0 bit in MCR11. This frequency measurement has a resolution of 0.0003068ppm over a ±80ppm range. The value read from the FREQ field is the DPLL's integral path value, which is an averaged measurement with an averaging time inversely proportional to DPLL bandwidth.

DPLL phase measurements can be read from the PHASE field spanning registers PHASE1 and PHASE2. This field indicates the phase difference seen by the phase detector for either the T0 DPLL or the T4 DPLL, depending on the setting of the T4T0 bit in MCR11. This phase measurement has a resolution of approximately 0.703 degrees and is internally averaged with a -3dB attenuation point of approximately 100Hz. Thus, for low DPLL bandwidths, the PHASE field gives input phase wander in the frequency band from the DPLL corner frequency up to 100Hz. This information could be used by software to compute a crude MTIE measurement.

For the T0 DPLL the PHASE field always indicates the phase difference between the selected reference and the internal feedback clock. The T4 DPLL, however, can be configured to measure the phase difference between two input clocks. When T0CR1:T4MT0 = 1, the T4 DPLL locking capability is disabled, and the T4 phase detector is configured to compare the T0 DPLL selected reference with the T4 DPLL selected reference. Any input clock can then be forced to be the T4 DPLL selected reference using the T4FORCE field of MCR4. This feature can be used, for example, to measure the phase difference between the T0 DPLL's selected reference and its next highest priority reference. Software could compute MTIE and TDEV with respect to the T0 DPLL selected reference for any or all the other input clocks.

When comparing the phase of the T0 and T4 selected references by setting T0CR1:T4MT0 = 1, several details must be considered. In this mode, the T4 path receives a copy of the T0 selected reference, either directly or through a divider to 8kHz. If the T4 selected reference is divided down to 8kHz using LOCK8K or DIVN modes (see Section 7.4.2), the copy of the T0 selected reference is also divided down to 8kHz. If the T4 selected reference is configured for direct-lock mode, the copy of the T0 selected reference is not divided down and must be the same frequency as the T4 selected reference. See Table 7-6 for more details. (While T0CR1:T4MT0 = 1, the T0 path continues to lock to the T0 selected reference in the manner specified in the corresponding ICR register.)

## Table 7-6. T0 DPLL Adaptation for the T4 DPLL Phase Measurement Mode

| LOCKING MODE FOR T4 SELECTED REFERENCE | LOCKING MODE FOR T0 SELECTED REFERENCE | LOCKING MODE FOR COPY OF T0 SELECTED REFERENCE | FREQUENCY OF THE T4 SELECTED REFERENCE FOR T4MT0 PHASE MEASUREMENT | FREQUENCY OF THE T0 SELECTED REFERENCE FOR T4MT0 PHASE MEASUREMENT |
|---|---|---|---|---|
| LOCK8K or DIVN(8K) | DIRECT | LOCK8K | 8kHz | 8kHz |
| LOCK8K or DIVN(8K) | LOCK8K | LOCK8K | 8kHz | 8kHz |
| LOCK8K or DIVN(8K) | DIVN (8K) | DIVN | 8kHz | 8kHz |
| LOCK8K or DIVN(8K) | DIVN (not 8K) | DIRECT | 8kHz | 8kHz |
| DIVN (not 8K) | Any | DIRECT | Same as the T4 forced reference input frequency | Same as the T0 selected reference input frequency(1) |
| DIRECT | Any | DIRECT | Same as the T4 forced reference input frequency | Same as the T0 selected reference input frequency(1) |

**Note 1:** In this case the T0 select reference must be the same frequency as the T4 selected reference.

**Note 2:** If the T4 selected reference frequency is 8kHz and the T0 selected reference is a different frequency, the two references can be compared by configuring the T4 selected reference for 8kHz and LOCK8K mode. This forces the copy of the T0 selected reference to be divided down to 8kHz using either LOCK8K or DIVN mode.

**Note 3:** DIVN(8K) means that the FREQ field is set to 8kHz, DIVN(not 8K) means the FREQ field is not set to 8kHz.

### *7.7.11 Input Jitter and Wander Tolerance*

The device is compliant with the jitter and wander tolerance requirements of the standards listed in Table 1-1. Wander can be tolerated up to the point where wander causes an apparent long-term frequency offset larger than the limits specified in the ILIMIT and/or SRLIMIT registers. In such a situation the input clock would be declared invalid. When using the ±360°/±180° PFD, jitter can be tolerated up to the point of eye closure. Either LOCK8K mode (see Section 7.4.2.3) or the multicycle phase detector (see Section 7.7.5) should be used for high jitter tolerance.

### *7.7.12 Jitter and Wander Transfer*

The transfer of jitter and wander from the selected reference to the output clocks has a programmable transfer function that is determined by the DPLL bandwidth. (See Section 7.7.3.) In the T0 DPLL, the 3dB corner frequency of the jitter transfer function can be set to any of 21 positions from 0.5mHz to 400Hz. In the T4 DPLL the 3dB corner frequency of the jitter transfer function can be set to various values from 18Hz to 70Hz.

During locked mode, the transfer of wander from the local oscillator clock (connected to the REFCLK pin) to the output clocks is not significant as long as the DPLL bandwidth is set high enough to allow the DPLL to quickly compensate for oscillator frequency changes. During free-run and holdover modes, local oscillator wander has a much more significant effect. See Section 7.3.

### 7.7.13 Output Jitter and Wander

Several factors contribute to jitter and wander on the output clocks, including:

- Jitter and wander amplitude on the selected reference (while in the locked state)
- The jitter/wander transfer characteristic of the device (while in the locked state)
- The jitter and wander on the local oscillator clock signal (especially wander while in the holdover state)

The DPLL in the device has programmable bandwidth (see Section 7.7.3). With respect to jitter and wander, the DPLL behaves as a lowpass filter with a programmable pole. The bandwidth of the DPLL is normally set low enough to strongly attenuate jitter. The wander and jitter attenuation depends on the DPLL bandwidth chosen.

Over time, frequency changes in the local oscillator can cause a phase difference between the selected reference and the output clocks. This is especially true at lower frequency DPLL bandwidths because the DPLL's rate of change may be slower than the oscillator's rate of change. Oscillators with better stability will minimize this effect. In some applications, an OCXO may be required rather than a TCXO. In the most demanding applications, the OCXO may need to be shielded to further reduce the rate of temperature change and thus the rate of frequency change.

## 7.8 Output Clock Configuration

A total of 16 output clock pins, OC1 to OC5, OC1B to OC5B, OC4POS/NEG to OC7POS/NEG, FSYNC, and MFSYNC are available on the device. Output clocks OC1 to OC7 are individually configurable for a variety of frequencies derived from either the T0 DPLL or the T4 DPLL. OC1B to OC5B are powered from a dedicated I/O power pin that can be set to any voltage from 2.2V to 3.3V. Output clocks FSYNC and MFSYNC serve as 8kHz frame-sync and 2kHz multiframe-sync outputs, respectively. Table 7-7 provides more detail on the capabilities of the output clock pins.

### Table 7-7. Output Clock Capabilities

| OUTPUT CLOCK | SIGNAL FORMAT | FREQUENCIES SUPPORTED |
|---|---|---|
| OC1 | CMOS/TTL 3.3V powered | Frequency selection per Section 7.8.2.3 and Table 7-8 to Table 7-14. |
| OC2 | | |
| OC3 | | |
| OC4 | | |
| OC5 | | |
| OC1B | CMOS/TTL 2.5V or 3.3V powered | |
| OC2B | | |
| OC3B | | |
| OC4B | | |
| OC5B | | |
| OC4 | LVDS/LVPECL | |
| OC5 | | |
| OC6 | | |
| OC7 | | |
| FSYNC | CMOS/TTL | 8kHz frame sync with programmable pulse width and polarity. |
| MFSYNC | | 2kHz multiframe sync with programmable pulse width and polarity. |

### 7.8.1 Signal Format Configuration

Output clocks OC4, OC5, OC6, and OC7 are LVDS-compatible, LVPECL level-compatible outputs. The type of output can be selected or the output can be disabled using the OCnSF configuration bits in the MCR8 register. The LVPECL level-compatible mode generates a differential signal that is large enough for most LVPECL receivers. Some LVPECL receivers have a limited common mode signal range which can be accommodated for by using an AC-coupled signal. The LVDS electrical specifications are listed in Table 10-5, and the recommended LVDS termination is shown in Figure 10-1. The LVPECL level-compatible electrical specifications are listed in Table 10-6, and the recommended LVPECL receiver termination is shown in Figure 10-3. These differential outputs can be easily interfaced to LVDS, LVPECL, and CML inputs on neighboring ICs using a few external passive components. See App Note HFAN-1.0 for details.

The other output clocks are CMOS/TTL signal format.

### 7.8.2 Frequency Configuration

The frequency of output clocks OC1 to OC7 is a function of the settings used to configure the components of the T0 and T4 PLL paths. These components are shown in the detailed block diagram of Figure 7-1.

The DS3102 uses digital frequency synthesis (DFS) to generate various clocks. In DFS a high-speed master clock (204.8MHz) is divided down to the desired output frequency by adding a number to an accumulator. The DFS output is a coding of the clock output phase that is used by a special circuit to determine where to put the edges of the output clock between the clock edges of the master clock. The edges of the output clock, however, are not ideally located in time resulting in jitter with an amplitude typically less than 1ns pk-pk.

#### 7.8.2.1 T0 and T4 DPLL Details

See Figure 7-1. The T0 and T4 forward-DFS blocks use the 204.8MHz master clock and DFS technology to synthesize internal clocks from which the output and feedback clocks are derived. The T4 DPLL only has a single DFS output clock signal for both the output clocks and the feedback clock, whereas there are two DFS output clock signals in the T0 DPLL—one for the output clocks and one for the feedback clock.

In the T0 DPLL, the feedback clock-signal output handles phase build-out or any phase offset configured in the OFFSET registers. Thus, the T0 DPLL output clock signals and the feedback clock signal are frequency-locked but may have a phase offset. The T0 and T4 feedback-DFS blocks are always connected to the T0 forward DFS and the T4 forward DFS, respectively. The feedback-DFS blocks synthesize the appropriate locking frequencies for use by the phase-frequency detectors (PFDs). See Section 7.4.2.

#### 7.8.2.2 Output DFS and APLL Details

See Figure 7-1. The output clock frequencies are determined by two 2kHz/8kHz DFS blocks, two DIG12 DFS blocks, and three APLL DFS blocks. Four of the DFS blocks can be connected to either the T0 DPLL or the T4 DPLL, and three are always connected to the T0 DPLL. The T0 APLL, the T0 APLL2 and the T4 APLL (and their output dividers) get their frequency references from three associated APLL DFS blocks. All the output DFS blocks are connected to the T0 DPLL when MCR4:LKT4T0 = 1.

The 2K8K DFS and FSYNC DFS blocks generate both 2kHz and 8kHz signals which have about 1ns pk-pk jitter. The FSYNC (8kHz) and MFSYNC(2 kHz) signals come from the FSYNC DFS block, which is always connected to the T0 DPLL when not in independent mode (FSCR2:INDEP = 1). The 2kHz and 8kHz signals available on output clocks OC1 to OC7 come from the 2K8K DFS, which can be connected to either the T0 DPLL or the T4 DPLL depending on FSCR1:2K8KSRC and MCR4:LKT4T0.

The DIG1 DFS can generate an N x DS1 or NxE1 signal with about 1ns pk-pk jitter. The DIG2 DFS can generate an N x DS1, N x E1, 6.312MHz, 10MHz, or N x 19.44MHz clock with approximately 1ns pk-pk jitter. Each DIG12 DFS can be connected to either the T0 DPLL or the T4 DPLL using MCR7:DIG1SRC or MCR7:DIG2SRC and MCR4:LKT4T0. The frequency of the DIG1 clock is configured by the DIG1SS bit in MCR6 and the DIG1F[1:0] field in MCR7. The frequency of the DIG2 clock is configured by the DIG2AF and DIG2SS bits in MCR6 and the

DIG2F[1:0] field in MCR7. DIG1 and DIG2 can be independently configured for any of the frequencies shown in Table 7-8 and Table 7-9, respectively.

The APLL DFS blocks and their associated output APLLs and output dividers can generate many different frequencies. The T0 APLL DFS and the T0 APLL2 DFS are always connected to the T0 DPLL. The T4 APLL DFS can be connected to either the T0 DPLL or the T4 DPLL depending on T0CR1:T4APT0 and MCR4:LKT4T0. The T0 APLL frequencies that can be generated are listed in Table 7-11. The T0 APLL2 frequency is always 312.500MHz. The T4 APLL frequencies that can be generated are listed in Table 7-13. The output frequencies that can be generated from the APLL circuits are listed in Table 7-10.

The T4 APLL is disabled and powered down when T4CR1:T4FREQ = 0000 and T0CR1:T4APT0 = 0. In this mode all outputs connected to the T4 APLL are driven low.

Together the T0 APLL, T0 APLL2, and T4 APLL can simultaneously generate SONET/SDH clock rates, Gigabit Ethernet clock rates (e.g., 125MHz), and 10G Ethernet clock rates (e.g., 156.25MHz), all locked to the same selected reference. This capability supports mixed SONET/SDH and Synchronous Ethernet line cards.

#### *7.8.2.3 OC1 to OC7 Configuration*

The following is a step-by-step procedure for configuring the frequencies of output clocks OC1 to OC7:

1) Determine whether the T4 APLL must be independent of the T0 DPLL. If the T4 APLL must be independent, set T4APT0 = 0 in register T0CR1. If the T4 APLL must be locked to the T0 DPLL, set T4APT0 = 1.
2) Use Table 7-10 to select a set of output frequencies for each APLL, T0 and T4. Each APLL can only generate one set of output frequencies. (In SONET/SDH equipment, the T0 APLL is typically configured for a frequency of 311.04MHz to get 19.44MHz and/or 38.88MHz output clocks to distribute to system line cards.)
3) Determine from Table 7-10 the T0 and T4 APLL frequencies required for the frequency sets chosen in step 2.
4) Configure the T0FREQ field in register T0CR1 as shown in Table 7-11 for the T0 APLL frequency determined in step 3. Configure the T4FREQ field in register T4CR1 as shown in Table 7-13 for the T4 APLL frequency determined in step 3. If the T4 APLL is locked to the T0 DPLL, the T4APT0 and T0FT4 fields in T0CR1 must also be configured as shown in Table 7-13.
5) Using Table 7-10 and Table 7-14, configure the frequencies of output clocks OC1 to OC7 in the OFREQn fields of registers OCR1 to OCR4 and the AOFn bit in the OCR5 register.

Table 7-15 lists all standard frequencies for the output clocks and specifies how to configure the T0 APLL and/or the T4 APLL to obtain each frequency. Table 7-15 also indicates the expected jitter amplitude for each frequency.

### Table 7-8. Digital1 Frequencies

| DIG1F[1:0] SETTING IN MCR7 | DIG1SS SETTING IN MCR6 | FREQUENCY (MHz) | JITTER (pk-pk ns, typ) |
|---|---|---|---|
| 00 | 0 | 2.048 | < 1 |
| 01 | 0 | 4.096 | < 1 |
| 10 | 0 | 8.192 | < 1 |
| 11 | 0 | 16.384 | < 1 |
| 00 | 1 | 1.544 | < 1 |
| 01 | 1 | 3.088 | < 1 |
| 10 | 1 | 6.176 | < 1 |
| 11 | 1 | 12.352 | < 1 |

## Table 7-9. Digital2 Frequencies

| DIG2AF SETTING IN MCR6 | DIG2F[1:0] SETTING IN MCR7 | DIG2SS SETTING IN MCR6 | FREQUENCY (MHz) | JITTER (pk-pk ns, typ) |
|---|---|---|---|---|
| 1 | 00 | 0 | 6.312 | < 1 |
| 1 | 10 | 0 | 10.000 | <1 |
| 1 | 00 | 1 | 19.440 | < 1 |
| 1 | 01 | 1 | 38.880 | < 1 |
| 0 | 00 | 0 | 2.048 | < 1 |
| 0 | 01 | 0 | 4.096 | < 1 |
| 0 | 10 | 0 | 8.192 | < 1 |
| 0 | 11 | 0 | 16.384 | < 1 |
| 0 | 00 | 1 | 1.544 | < 1 |
| 0 | 01 | 1 | 3.088 | < 1 |
| 0 | 10 | 1 | 6.176 | < 1 |
| 0 | 11 | 1 | 12.352 | < 1 |

## Table 7-10. APLL Frequency to Output Frequencies (T0 APLL and T4 APLL)

| APLL FREQUENCY | APLL / 2 | APLL / 4 | APLL / 5 | APLL / 6 | APLL / 8 | APLL / 10 | APLL / 12 | APLL / 16 | APLL / 20 | APLL / 48 | APLL / 64 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 312.500 | **156.250** | — | **62.500** | — | — | 31.250 | — | — | — | — | — |
| 311.040 | **155.520** | **77.760** | 62.208 | **51.840** | **38.880** | 31.104 | 25.920 | **19.440** | 15.552 | **6.480** | 4.860 |
| 274.944 | 137.472 | 68.376 | — | 45.824 | **34.368** | — | 22.912 | 17.184 | — | 5.728 | 4.296 |
| 250.000 | **125.000** | **62.500** | 50.000 | — | 31.250 | **25.000** | — | — | 12.500 | — | — |
| 178.944 | 89.472 | **44.736** | — | 29.824 | 22.368 | — | 14.912 | 11.184 | — | 3.728 | 2.796 |
| 160.000 | 80.000 | 40.000 | 32.00 | — | 20.000 | 16.000 | — | **10.000** | 8.000 | — | 2.500 |
| 148.224 | 74.112 | 37.056 | — | 24.704 | 18.528 | — | 12.352 | 9.264 | — | **3.088** | 2.316 |
| 131.072 | 65.536 | **32.768** | — | — | **16.384** | — | — | **8.192** | — | — | **2.048** |
| 122.880 | 61.440 | **30.720** | 24.576 | 20.48 | 15.360 | 12.288 | **10.240** | 7.680 | 6.144 | 2.560 | 1.920 |
| 104.000 | 52.000 | 26.000 | 20.800 | — | **13.000** | 10.400 | — | 6.500 | 5.200 | — | — |
| 100.992 | 50.496 | 25.248 | — | 16.832 | 12.624 | — | 8.416 | **6.312** | — | 2.104 | 1.578 |
| 98.816 | 49.408 | 24.704 | — | — | 12.352 | — | — | **6.176** | — | — | **1.544** |
| 98.304 | 49.152 | 24.576 | — | **16.384** | 12.288 | — | **8.192** | 6.144 | — | **2.048** | 1.536 |

***Note:*** *All frequencies in MHz. Common telecom, datacom, and synchronization frequencies are in* ***bold*** *type.*

## Table 7-11. T0 APLL Frequency Configuration

| T0 APLL FREQUENCY (MHz) | T0 APLL DFS FREQUENCY (MHz) | T0 APLL FREQUENCY MODE | T0FREQ[2:0] SETTING IN T0CR1 | OUTPUT JITTER (pk-pk, ns, typ) |
|---|---|---|---|---|
| 311.04 | 77.76 | 77.76MHz | 000 | < 0.5 |
| 311.04 | 77.76 | 77.76MHz | 001 | < 0.5 |
| 98.304 | 24.576 | 12 x E1 | 010 | < 0.5 |
| 131.072 | 32.768 | 16 x E1 | 011 | < 0.5 |
| 148.224 | 37.056 | 24 x DS1 | 100 | < 0.5 |
| 98.816 | 24.704 | 16 x DS1 | 101 | < 0.5 |
| 100.992 | 25.248 | 4 x 6312kHz | 110 | < 0.5 |
| 250.000 | 62.5 | GbE ÷ 16 | 111 | < 0.5 |

## Table 7-12. T0 APLL2 Frequency Configuration

| T0 APLL2 FREQUENCY (MHz) | T0 APLL2 DFS FREQUENCY(MHz) | OUTPUT JITTER (pk-pk, ns, typ) |
|---|---|---|
| 312.500 | 62.500 | < 0.5 |

## Table 7-13. T4 APLL Frequency Configuration

| T4 APLL FREQUENCY (MHz) | T4 APLL DFS FREQUENCY (MHz) | T4 APLL FREQUENCY MODE | T4APT0 SETTING IN T0CR1 | T4FREQ[3:0] SETTING IN T4CR1 | T0FT4[2:0] SETTING IN T0CR1 | OUTPUT JITTER (pk-pk, ns, typ) |
|---|---|---|---|---|---|---|
| Disabled | 77.76 | Squelched | 0 | 0000 | XXX | < 0.5 |
| 311.04 | 77.76 | 77.76MHz | 0 | 0001 | XXX | < 0.5 |
| 98.304 | 24.576 | 12 x E1 | 0 | 0010 | XXX | < 0.5 |
| 131.072 | 32.768 | 16 x E1 | 0 | 0011 | XXX | < 0.5 |
| 148.224 | 37.056 | 24 x DS1 | 0 | 0100 | XXX | < 0.5 |
| 98.816 | 24.704 | 16 x DS1 | 0 | 0101 | XXX | < 0.5 |
| 274.944 | 68.736 | 2 x E3 | 0 | 0110 | XXX | < 0.5 |
| 178.944 | 44.736 | DS3 | 0 | 0111 | XXX | < 0.5 |
| 100.992 | 25.248 | 4 x 6312kHz | 0 | 1000 | XXX | < 0.5 |
| 250.000 | 62.500 | GbE ÷ 16 | 0 | 1001 | XXX | < 0.5 |
| 122.88 | 30.720 | 3 x 10.24 | 0 | 1010 | XXX | < 0.5 |
| 160.000 | 40.000 | 4 x 10 | 0 | 1011 | XXX | < 0.5 |
| 104.000 | 26.000 | 2 x 13 | 0 | 1100 | XXX | < 0.5 |
| 98.304 | 24.576 | T0 12 x E1 | 1 | XXXX | 000 | < 0.5 |
| 250.000 | 62.500 | T0 GbE ÷ 16 | 1 | XXXX | 001 | < 0.5 |
| 131.072 | 32.768 | T0 16 x E1 | 1 | XXXX | 010 | < 0.5 |
| 148.224 | 37.056 | T0 24 x DS1 | 1 | XXXX | 100 | < 0.5 |
| 98.816 | 24.704 | T0 16 x DS1 | 1 | XXXX | 110 | < 0.5 |
| 100.992 | 25.248 | T0 4 x 6312kHz | 1 | XXXX | 111 | < 0.5 |

## Table 7-14. OC1 to OC7 Output Frequency Selection

| AOF BIT | OFREQ(1) | FREQUENCY | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | OC1 | OC2 | OC3 | OC4 | OC5 | OC6 | OC7 |
| 0 | 0000 | Disabled | Disabled | Disabled | Disabled | Disabled | Disabled | Disabled |
| 0 | 0001 | 2kHz | 2kHz | 2kHz | 2kHz | 2kHz | 2kHz | 2kHz |
| 0 | 0010 | 8kHz | 8kHz | 8kHz | 8kHz | 8kHz | 8kHz | 8kHz |
| 0 | 0011 | Digital2 | Digital2 | Digital2 | Digital2 | Digital2 | T0 / 2 | Digital2 |
| 0 | 0100 | Digital1 | Digital1 | Digital1 | Digital1 | Digital1 | Digital1 | T0 / 2 |
| 0 | 0101 | T0 / 48 | T0 / 48 | T0 / 48 | T0 / 48 | T0 / 48 | T0 / 1 | T0 / 48 |
| 0 | 0110 | T0 / 16 | T0 / 16 | T0 / 16 | T0 / 16 | T0 / 16 | T0 / 16 | T0 / 16 |
| 0 | 0111 | T0 / 12 | T0 / 12 | T0 / 12 | T0 / 12 | T0 / 12 | T0 / 12 | T0 / 12 |
| 0 | 1000 | T0 / 8 | T0 / 8 | T0 / 8 | T0 / 8 | T0 / 8 | T0 / 8 | T0 / 8 |
| 0 | 1001 | T0 / 6 | T0 / 6 | T0 / 6 | T0 / 6 | T0 / 6 | T0 / 6 | T0 / 6 |
| 0 | 1010 | T0 / 4 | T0 / 4 | T0 / 4 | T0 / 4 | T0 / 4 | T0 / 4 | T0 / 4 |
| 0 | 1011 | T4 / 64 | T4 / 64 | T4 / 64 | T4 / 2 | T4 / 2 | T4 / 64 | T4 / 64 |
| 0 | 1100 | T4 / 48 | T4 / 48 | T4 / 48 | T4 / 48 | T4 / 48 | T4 / 48 | T4 / 48 |
| 0 | 1101 | T4 / 16 | T4 / 16 | T4 / 16 | T4 / 16 | T4 / 16 | T4 / 16 | T4 / 16 |
| 0 | 1110 | T4 / 8 | T4 / 8 | T4 / 8 | T4 / 8 | T4 / 8 | T4 / 8 | T4 / 8 |
| 0 | 1111 | T4 / 4 | T4 / 4 | T4 / 4 | T4 / 4 | T4 / 4 | T4 / 4 | T4 / 4 |
| 1 | 0000 | Disabled | Disabled | Disabled | Disabled | Disabled | Disabled | Disabled |
| 1 | 0001 | T0 / 64 | T0 / 64 | T0 / 64 | T0 / 2 | T0 / 2 | T4 / 5 | T4 / 5 |
| 1 | 0010 | T4 / 20 | T4 / 20 | T4 / 20 | T0 / 1 | T0 / 1 | T4 / 2 | T4 / 2 |
| 1 | 0011 | T4 / 12 | T4 / 12 | T4 / 12 | T4 / 10 | T4 / 10 | T4 / 1 | T4 / 1 |
| 1 | 0100 | T4 / 10 | T4 / 10 | T4 / 10 | T02 / 10 | T02 / 10 | T02 / 5 | T02 / 5 |
| 1 | 0101 | T02 / 10 | T4 / 5 | T4 / 5 | T02 / 2 | T02 / 2 | T02 / 2 | T02 / 2 |
| 1 | 0110 | T02 / 5 | T4 / 2 | T4 / 2 | T02 / 1 | T02 / 1 | T02 / 1 | T02 / 1 |
| 1 | 0111 | T4SELREF | T4SELREF | T4SELREF | T4SELREF | T4SELREF | T4SELREF | T4SELREF |

**Note 1:** The value of the OFREQn field (in the OCR1 to OCR4 registers) corresponding to output clock OCn.

**Note 2:** T0 = T0 APLL. T02 = T0 APLL2. T4 = T4 APLL.

## Table 7-15. Standard Frequencies for Programmable Outputs

| FREQUENCY (MHz) | | T0 APLL | T4 APLL | | OFREQn | JITTER (TYP) | |
|---|---|---|---|---|---|---|---|
| | | T0FREQ | T4FT0 | T4FREQ | | RMS (ps) | PK-PK (ns) |
| **2kHz** | | | | | 2 kHz | 100 | 1.00 |
| **8kHz** | | | | | 8 kHz | 100 | 1.00 |
| 1.536 | Not OC4, OC5 from T4 APLL<br>Not OC4 to OC7 from T0 APLL | 12 x E1 | 12 x E1 | 12 x E1 | APLL/64 | 100 | 1.00 |
| **1.544** | Not OC6 from DIG2 | | | | DIG1,DIG2 | 100 | 1.00 |
| **1.544** | Not OC4, OC5 from T4 APLL<br>Not OC4 to OC7 from T0 APLL | 16 x DS1 | 16 x DS1 | 16 x DS1 | APLL/64 | 75 | 0.75 |
| 1.578 | Not OC4, OC5 from T4 APLL<br>Not OC4 to OC7 from T0 APLL | 4 x 6.312 | 4 x 6.312 | 4 x 6.312 | APLL/64 | 60 | 0.60 |
| **2.048** | Not OC6 from DIG2 | | | | DIG1,DIG2 | 100 | 1.00 |
| **2.048** | Not OC6 from T0 APLL | 12 x E1 | 12 x E1 | 12 x E1 | APLL/48 | 100 | 1.00 |
| **2.048** | Not OC4, OC5 from T4 APLL<br>Not OC4 to OC7 from T0 APLL | 16 x E1 | 16 x E1 | 16 x E1 | APLL/64 | 70 | 0.70 |
| 2.104 | Not OC6 from T0 APLL | 4 x 6.312 | 4 x 6.312 | 4 x 6.312 | APLL/48 | 60 | 0.60 |
| 2.316 | Not OC4, OC5 from T4 APLL<br>Not OC4 to OC7 from T0 APLL | 24 x DS1 | 24 x DS1 | 24 x DS1 | APLL/64 | 60 | 0.60 |
| 2.500 | Not OC4, OC5 | | | 4 x 10 | APLL/64 | 80 | 0.80 |
| 2.560 | | | | 3 x 10.24 | APLL/48 | 90 | 0.90 |
| 2.796 | Not OC4, OC5 | | | DS3 | APLL/64 | 50 | 0.50 |
| 3.088 | Not OC6 from DIG2 | | | | DIG1,DIG2 | 100 | 1.00 |
| 3.088 | Not OC6 from T0 APLL | 24 x DS1 | 24 x DS1 | 24 x DS1 | APLL/48 | 60 | 0.60 |
| 3.728 | | | | DS3 | APLL/48 | 50 | 0.50 |
| 4.096 | Not OC6 from DIG2 | | | | DIG1,DIG2 | 100 | 1.00 |
| 4.296 | Not OC4, OC5 | | | 2 x E3 | APLL/64 | 70 | 0.70 |
| 4.860 | Not OC4, OC5 from T4 APLL<br>Not OC4 to OC7 from T0 APLL | 77.76 | | 77.76 | APLL/64 | 50 | 0.50 |
| 5.200 | OC1–OC3 only | | | 2 x 13 | APLL/20 | 90 | 0.90 |
| 5.728 | | | | 2 x E3 | APLL/48 | 70 | 0.70 |
| 6.144 | OC1–OC3 only | | | 3 x 10.24 | APLL/20 | 90 | 0.90 |
| 6.144 | | 12 x E1 | 12 x E1 | 12 x E1 | APLL/16 | 100 | 1.00 |
| 6.176 | Not OC6 from DIG2 | | | | DIG1,DIG2 | 100 | 1.00 |
| 6.176 | | 16 x DS1 | 16 x DS1 | 16 x DS1 | APLL/16 | 75 | 075 |
| **6.312** | Not OC6 | | | | DIG2 | 100 | 1.00 |
| **6.312** | | 4 x 6.312 | 4 x 6.312 | 4 x 6.312 | APLL/16 | 60 | 0.60 |
| **6.480** | Not OC6 from T0 APLL | 77.76 | | 77.76 | APLL/48 | 60 | 0.6 |
| 8.000 | OC1–OC3 only | | | 4 x 10 | APLL/20 | 80 | 0.80 |
| 8.192 | Not OC6 from DIG2 | | | | DIG1,DIG2 | 100 | 1.00 |
| 8.192 | | 12 x E1 | | | APLL/12 | 100 | 1.00 |
| 8.192 | | 16 x E1 | 16 x E1 | 16 x E1 | APLL/16 | 70 | 0.70 |
| 8.416 | | 4 x 6.312 | | | APLL/12 | 60 | 0.60 |
| 9.264 | | 24 x DS1 | 24 x DS1 | 24 x DS1 | APLL/16 | 60 | 0.60 |
| **10.000** | Not OC6 | | | | DIG2 | 100 | 1.00 |
| **10.000** | | | | 4 x 10 | APLL/16 | 80 | 0.80 |
| **10.240** | OC1–OC3 only | | | 3 x 10.24 | APLL/12 | 90 | 0.90 |
| 10.400 | Not OC6, OC7 | | | 3 x 10.24 | APLL/10 | 90 | 0.90 |
| 11.184 | | | | DS3 | APLL/16 | 50 | 0.50 |
| 12.288 | | 12 x E1 | 12 x E1 | 12 x E1 | APLL/8 | 100 | 1.00 |
| 12.288 | Not OC6, OC7 | | | 2 x 13 | APLL/10 | 90 | 0.90 |
| 12.352 | | 24 x DS1 | | | APLL/12 | 60 | 0.60 |
| 12.352 | | 16 x DS1 | 16 x DS1 | 16 x DS1 | APLL/8 | 75 | 0.75 |
| 12.352 | Not OC6 from DIG2 | | | | DIG1,DIG2 | 100 | 1.00 |
| 12.500 | OC1–OC3 only | | GbE ÷ 16 | GbE ÷ 16 | APLL/20 | 60 | 0.60 |
| 12.624 | | 4 x 6.312 | 4 x 6.312 | 4 x 6.312 | APLL/8 | 60 | 0.60 |
| **13.000** | | | | 2 x 13 | APLL/8 | 90 | 0.90 |
| 15.360 | | | | 3 x 10.24 | APLL/8 | 90 | 0.90 |

| FREQUENCY (MHz) | | T0 APLL | T4 APLL | | OFREQn | JITTER (TYP) | |
|---|---|---|---|---|---|---|---|
| | | T0FREQ | T4FT0 | T4FREQ | | RMS (ps) | PK-PK (ns) |
| 15.552 | OC1–OC3 only | | | 77.76 | APLL/20 | 50 | 0.50 |
| 16.000 | Not OC6, OC7 | | | 4 x 10 | APLL/10 | 80 | 0.80 |
| 16.384 | Not OC6 from DIG2 | | | | DIG1,DIG2 | 100 | 1.00 |
| 16.384 | | 12 x E1 | | | APLL/6 | 100 | 1.00 |
| 16.384 | | 16 x E1 | 16 x E1 | 16 x E1 | APLL/8 | 70 | 0.70 |
| 16.832 | | 4 x 6.312 | | | APLL/6 | 60 | 0.60 |
| 17.184 | | | | 2 x E3 | APLL/16 | 70 | 0.70 |
| 18.528 | | 24 x DS1 | 24 x DS1 | 24 x DS1 | APLL/8 | 60 | 0.60 |
| **19.440** | Not OC6 | | | | DIG2 | 100 | 1.00 |
| **19.440** | | 77.76 | | 77.76 | APLL/16 | 50 | 0.50 |
| 20.000 | | | | 4 x 10 | APLL/8 | 80 | 0.80 |
| 20.800 | OC2, OC3, OC6, OC7 only | | | 2 x 13 | APLL/5 | 90 | 0.90 |
| 22.368 | | | | DS3 | APLL/8 | 50 | 0.50 |
| 24.576 | | 12 x E1 | 12 x E1 | 12 x E1 | APLL/4 | 100 | 1.00 |
| 24.576 | OC2, OC3, OC6, OC7 only | | | 3 x 10.24 | APLL/5 | 90 | 0.90 |
| 24.704 | | 24 x DS1 | | | APLL/6 | 60 | 0.60 |
| 24.704 | | 16 x DS1 | 16 x DS1 | 16 x DS1 | APLL/4 | 75 | 0.75 |
| **25.000** | Not OC6, OC7 | | GbE ÷ 16 | GbE ÷ 16 | APLL/10 | 60 | 0.60 |
| 25.248 | | 4 x 6.312 | 4 x 6.312 | 4 x 6.312 | APLL/4 | 60 | 0.60 |
| 25.920 | | 77.76 | | | APLL/12 | 50 | 0.50 |
| 26.000 | | | | 2 x 13 | APLL/4 | 90 | 0.90 |
| **30.720** | | | | 3 x 10.24 | APLL/4 | 90 | 0.90 |
| 31.104 | Not OC6, OC7 | | | 77.76 | APLL/10 | 50 | 0.50 |
| 31.250 | | GbE ÷ 16 | GbE ÷ 16 | GbE ÷ 16 | APLL/8 | 60 | 0.60 |
| 31.250 | OC1, OC4, OC5 from T0 APLL2 | | | | APLL/10 | 60 | 0.60 |
| 32.000 | OC2, OC3, OC6, OC7 only | | | 4 x 10 | APLL/5 | 80 | 0.80 |
| 32.768 | | 16 x E1 | 16 x E1 | 16 x E1 | APLL/4 | 70 | 0.70 |
| **34.368** | | | | 2 x E3 | APLL/8 | 70 | 0.70 |
| 37.056 | | 24 x DS1 | 24 x DS1 | 24 x DS1 | APLL/4 | 60 | 0.60 |
| **38.880** | | 77.76 | | 77.76 | APLL/8 | 50 | 0.50 |
| 40.000 | | | | 4 x 10 | APLL/4 | 80 | 0.80 |
| **44.736** | | | | DS3 | APLL/4 | 50 | 0.50 |
| 49.152 | Not OC1–OC3 from T0 APLL<br>Not OC1, OC2 from T4 APLL | 12 x E1 | 12 x E1 | 12 x E1 | APLL/2 | 100 | 1.00 |
| 49.408 | Not OC1–OC3 from T0 APLL<br>Not OC1, OC2 from T4 APLL | 16 x DS1 | 16 x DS1 | 16 x DS1 | APLL/2 | 75 | 0.75 |
| **50.000** | OC2, OC3, OC6, OC7 only | | GbE ÷ 16 | GbE ÷ 16 | APLL/5 | 60 | 0.60 |
| 50.496 | Not OC1–OC3 from T0 APLL<br>Not OC1, OC2 from T4 APLL | 4 x 6.312 | 4 x 6.312 | 4 x 6.312 | APLL/2 | 60 | 0.60 |
| **51.840** | | 77.76 | | | APLL/6 | 50 | 0.50 |
| 52.000 | Not OC1, OC2 | | | 2 x 13 | APLL/2 | 90 | 0.90 |
| 61.440 | Not OC1, OC2 | | | 3 x 10.24 | APLL/2 | 90 | 0.90 |
| 62.208 | OC2, OC3, OC6, OC7 only | | | 77.76 | APLL/5 | 50 | 0.50 |
| **62.500** | | GbE ÷ 16 | GbE ÷ 16 | GbE ÷ 16 | APLL/4 | 60 | 0.60 |
| **62.500** | OC1, OC6, OC7 from T0 APLL2 | | | | APLL/5 | 60 | 0.60 |
| 65.536 | Not OC1–OC3 from T0 APLL<br>Not OC1, OC2 from T4 APLL | 16 x E1 | 16 x E1 | 16 x E1 | APLL/2 | 70 | 0.70 |
| 68.736 | | | | 2 x E3 | APLL/4 | 70 | 0.70 |
| 74.112 | Not OC1–OC3 from T0 APLL<br>Not OC1, OC2 from T4 APLL | 24 x DS1 | 24 x DS1 | 24 x DS1 | APLL/2 | 60 | 0.60 |
| **77.76** | | 77.76 | | 77.76 | APLL/4 | 50 | 0.50 |
| 80.000 | Not OC1, OC2 | | | 4 x 10 | APLL/2 | 80 | 0.80 |
| 89.472 | Not OC1, OC2 | | | DS3 | APLL/2 | 50 | 0.50 |
| 98.304 | Not OC1–OC3 from T0 APLL<br>OC6, OC7 only from T4 APLL | 12 x E1 | 12 x E1 | 12 x E1 | APLL/1 | 100 | 1.00 |
| 98.816 | Not OC1–OC3 from T0 APLL<br>OC6, OC7 only from T4 APLL | 16 x DS1 | 16 x DS1 | 16 x DS1 | APLL/1 | 75 | 0.75 |
| 100.992 | Not OC1–OC3 from T0 APLL | 4 x 6312 kHz | 4 x 6312 kHz | 4 x 6312 kHz | APLL/1 | 60 | 0.60 |

| FREQUENCY (MHz) | | T0 APLL | T4 APLL | | OFREQn | JITTER (TYP) | |
|---|---|---|---|---|---|---|---|
| | | T0FREQ | T4FT0 | T4FREQ | | RMS (ps) | PK-PK (ns) |
| | OC6, OC7 only from T4 APLL | | | | | | |
| 104.000 | OC6, OC7 only | | | 2 x 13 | APLL/1 | 90 | 0.90 |
| 122.880 | OC6, OC7 only | | | 3 x 10.24 | APLL/1 | 90 | 0.90 |
| **125.000** | Not OC1–OC3 from T0 APLL<br>Not OC1, OC2 from T4 APLL | GbE ÷ 16 | GbE ÷ 16 | GbE ÷ 16 | APLL/2 | 60 | 0.60 |
| 131.072 | Not OC1–OC3 from T0 APLL<br>OC6, OC7 only from T4 APLL | 16 x E1 | 16 x E1 | 16 x E1 | APLL/1 | 70 | 0.70 |
| 137.472 | OC6, OC7 only | | | 2 x E3 | APLL/2 | 70 | 0.70 |
| 148.224 | Not OC1-OC3 from T0 APLL<br>OC6, OC7 only from T4 APLL | 24 x DS1 | 24 x DS1 | 24 x DS1 | APLL/1 | 60 | 0.60 |
| **155.520** | Not OC1–OC3 from T0 APLL<br>Not OC1, OC2 from T4 APLL | 77.76 | | 77.76 | APLL/2 | 50 | 0.50 |
| **156.250** | OC4–OC7 only from T0 APLL2 | | | | APLL/2 | 60 | 0.60 |
| 160.000 | OC6, OC7 only | | | 4 x 10 | APLL/1 | 80 | 0.80 |
| 178.944 | OC6, OC7 only | | | DS3 | APLL/1 | 50 | 0.50 |
| 250.000 | OC4–OC7 only | GbE ÷ 16 | | | APLL/1 | 60 | 0.60 |
| 274.944 | OC6, OC7 only | | | 2 x E3 | APLL/1 | 70 | 0.70 |
| **311.040** | OC4–OC7 only | 77.76 | | | APLL/1 | 50 | 0.50 |
| **312.500** | OC4–OC7 only from T0 APLL2 | | | | APLL/2 | 60 | 0.60 |

### *7.8.2.4 FSYNC and MFSYNC Configuration*

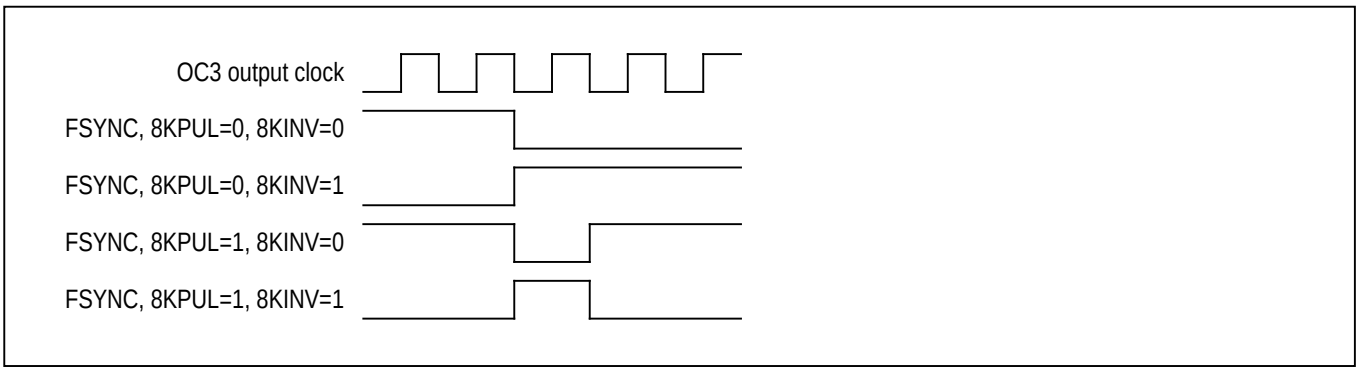
The FSYNC output is enabled by setting FSEN = 1 in the OCR4 register, while the MFSYNC output is enabled by setting MFSEN = 1 in OCR4. When disabled, these pins are driven low.

When 8KPUL = 0 in FSCR1, FSYNC is configured as an 8kHz clock with 50% duty cycle. When 8KPUL = 1, FSYNC is an 8kHz frame sync that pulses *low* once every 125µs with pulse width equal to one cycle of output clock OC3. When 8KINV = 1 in FSCR1, the clock or pulse polarity of FSYNC is inverted.

When 2KPUL = 0 in FSCR1, MFSYNC is configured as an 2kHz clock with 50% duty cycle. When 2KPUL = 1, MFSYNC is a 2kHz frame sync that pulses *low* once every 500µs with pulse width equal to one cycle of output clock OC3. When 2KINV = 1 in FSCR1, the clock or pulse polarity f MFSYNC is inverted.

If either 8KPUL = 1 or 2KPUL = 1, output clock OC3 must be generated from the T0 DPLL and must be configured for a frequency of 1.544MHz or higher or the FSYNC/MFSYNC pulses may not be generated correctly. Figure 7-4 shows how the 8KPUL and 8KINV control bits affect the FSYNC output. The 2KPUL and 2KINV bits have an identical effect on MFSYNC.

*Figure 7-4. FSYNC 8kHz Options*



#### 7.8.2.5 Custom Output Frequencies

In addition to the many standard frequencies available in the device, any of the seven output DFS blocks can be configured to generate a custom frequency. Possible custom frequencies include any multiple of 2kHz up to 77.76MHz and any multiple of 8kHz up to 311.04MHz. (An APLL must be used to achieve frequencies above 77.76MHz.) Any of the programmable output clocks can be configured to output the custom frequency or submultiples thereof. Contact Microsemi timing products technical support for help with custom frequencies.

## 7.9 Equipment Redundancy Configuration

Most high-reliability SONET/SDH systems require two identical timing cards for equipment redundancy. The DS3102 directly supports this requirement. In such a system, one timing card is designated the master while the other is designated the slave. The rest of the system, outside the timing cards, is set up to take timing from the master normally, but to automatically switch to taking timing from the slave if the master fails. To avoid excessive phase transients when switching between master timing and slave timing, the clocks from the master and the slave must be frequency-locked and usually phase-locked as well. To accomplish this requires a method involving both static configuration and ongoing oversight by system software. Table 7-16 lists the elements of this methodology.

### Table 7-16. Equipment Redundancy Methodology

| | |
|---|---|
| 1. | The various clock sources available in the system should be wired to the same pins on the slave as on the master, except:<br>A. One output clock from the master device should be wired to an input clock on the slave.<br>B. One output clock from the slave device should be wired to an input clock on the master. |
| 2. | The input clock priorities (IPR registers) on master and slave should be identical, for both T0 and T4 paths, except:<br>A. The master output clock is the highest priority input on the slave.(1)<br>B. The slave output clock is disabled (priority 0) on the master.<br>This ensures that the frequency of the slave matches the frequency of the master. |
| 3. | Any input declared invalid in one device (VALSR registers) must be marked invalid by software in the other device (VALCR registers). This and item 2 together ensure that when the master is performing properly, the slave locks to the master, and when the master fails, the slave locks to the input clock the master was previously locked to. |
| 4. | The slave's T0 DPLL bandwidth should be set higher than the master's bandwidth (T0LBW, T0ABW registers) to ensure that the slave follows any transients coming from the master. (70 Hz is recommended.) |
| 5. | Phase build-out should be disabled (MCR10:PBOEN = 0) on the slave when it is locked to the master to ensure that the slave maintains phase lock with the master. This also allows the use of phase offset (OFFSET registers) to compensate for delays between master and slave. |
| 6. | Revertive mode should be enabled on the slave (REVERT = 1 in MCR3) to ensure the slave switches from any other reference to the master as soon as the master's clock is valid. |

**Note 1:** This must be done for the slave's T0 path, but is not necessary for the slave's T4 path. In the slave's T4 path the input clock priorities should match those of the master except the input connected to the master's output clock should be disabled. This causes the slave's T4 path to only lock to external references.

### 7.9.1 Master-Slave Output Clock-Phase Alignment

When the T0 DPLL is direct-locked to a selected reference with frequency Fref, any output clocks derived from T0 with frequency Fref are phase-aligned with the selected reference (if phase build-out is disabled). Any output clocks derived from T0 with frequency greater than Fref are "falling edge aligned" with the frequency Fref output clock. Any output clocks derived from T0 with frequency less than Fref may or may not be aligned, depending on whether their frequencies are integer submultiples of f. These statements also apply to output clocks derived from the T4 DPLL.

Given this information, if master and slave devices are crosswired with 19.44MHz clocks, for example, the output clocks at N x 19.44MHz (N = 1, 2, 4, 8, or 16) from the two devices are phase-aligned with one another. Output clocks at lower frequencies (6.48MHz, 1.544MHz, 2.048MHz, 2kHz, 8kHz, etc.) from the two devices would not necessarily be phase-aligned. In many systems, lack of phase alignment between the two devices at these clock rates is not an issue. In some systems, however, the 2kHz and/or 8kHz clocks of the two devices must be aligned to avoid framing errors during switchover between master and slave.

One way to align the 2kHz and/or 8kHz clocks of the master and slave devices is to configure the slave to lock to a 2kHz or 8kHz output of the master. Another way is to use the external frame-sync signal as described in Section 7.9.2.

### *7.9.2 Master-Slave Frame and Multiframe Alignment with the External Frame-Sync Signals*

With this method of aligning the 2kHz and 8kHz clocks of the master and slave devices, both a higher speed clock (such as 6.48MHz or 19.44MHz) and a frame (or multiframe) sync signal from the master are passed to the slave (and vice versa when their roles are reversed). The higher speed clock from the master is connected to a regular input clock pin on the slave, such as IC3 or IC4, while the frame-sync signal from the master is connected to a SYNCn input pin on the slave, such as SYNC1 or SYNC2. The slave locks to the higher speed clock and samples the frame-sync signal on the associated SYNCn pin. The slave then uses the SYNCn signal to falling-edge align some or all the output clocks. When the SYNCn signal is a 2kHz clock, output clocks 2kHz and above are falling-edge aligned. A 4kHz or 8kHz clock can also be used on the SYNCn pins without any changes to the register configuration, but only output clocks of 8kHz and above are aligned in this case. Phase build-out should be disabled on the slave (PBOEN = 0 in MCR10) when using SYNCn signals for output clock alignment.

An external frame-sync signal is only allowed to aligh output clocks if the T0 DPLL is locked and the SYNCn signal is enabled and qualified. Section 7.9.2.1 discusses enable, while Section 7.9.2.4 covers qualification.

#### *7.9.2.1 Enable and SYNCn Pin Selection*

Table 7-17 shows how to configure the device for various external frame-sync modes. When MCR3:EFSEN = 0, external frame sync is disabled. When EFSEN = 1, three different external frame-sync modes are available: SYNC1 Manual, SYNC1 Auto, and SYNC123.

In SYNC1 Manual mode, external frame sync is enabled on the SYNC1 pin whenever the T0 DPLL is locked, regardless of which input clock is the selected reference. When the T0 DPLL is not locked, external frame sync is disabled. In this mode the SYNC2 and SYNC3 pins are ignored.

In SYNC1 Auto mode, external frame sync is automatically enabled on the SYNC1 pin when the T0 DPLL is locked to the input clock pin specified by FSCR3:SOURCE. If the T0 DPLL is not locked or is locked to a different input clock than the one specified by the SOURCE field, then external frame sync is disabled. In this mode the SYNC2 and SYNC3 pins are ignored.

In SYNC123 mode, the SYNC1, SYNC2, and SYNC3 pins are each associated with one or more input clock pins as specified by FSCR1:SYNCSRC. SYNC1 can be associated with IC3 or IC5 or both. SYNC2 can be associated with IC4 or IC6 or both. SYNC3 is always associated with IC9. When the T0 DPLL is locked to one of the input clock pins associated with a SYNCn pin, external frame sync is automatically enabled with the corresponding SYNCn pin as the source. When the T0 DPLL is not locked or is locked to an input clock pin that is not associated with a SYNCn pin then external frame sync is disabled.

Since SYNC123 mode is always automatic, MCR3:AEFSEN takes on a different meaning in this mode, specifying whether or not MCR3:EFSEN is automatically cleared when the T0 DPLL's selected reference changes.

## Table 7-17. External Frame-Sync Mode and Source

| T0 DPLL LOCKED[1] | MCR3: EFSEN | FSCR3: SOURCE | MCR3: AEFSEN | FSCR1: SYNCSRC | PTAB1: SELREF | FRAME-SYNC MODE | FRAME-SYNC SOURCE |
|---|---|---|---|---|---|---|---|
| 0 | X | XXXX[2] | X | XXX | XXXX | Disabled | Internal[3] |
| 1 | 0 | XXXX | X | XXX | XXXX | Disabled | Internal |
| 1 | 1 | <>11XX | 0 | XXX | XXXX | SYNC1 Manual | SYNC1 |
| 1 | 1 | <>11XX | 1 | XXX | =FSCR3: SOURCE | SYNC1 Auto | SYNC1 |
| | | | | | <>FSCR3: SOURCE | | Internal |
| 1 | 1 | 11XX | X[4] | 0XX | IC3 or IC5 | SYNC123 (Auto[4]) | SYNC1 |
| | | | | | IC4 or IC6 | | SYNC2 |
| | | | | 1X0 | IC3 | | SYNC1 |
| | | | | | IC4 | | SYNC2 |
| | | | | 1X1 | IC5 | | SYNC1 |
| | | | | | IC6 | | SYNC2 |
| | | | | 10X | IC9 | | SYNC3 |
| | | | | 11X | IC2 | | SYNC3 |
| | | | | All other cases | | | Internal |

**Note 1:** That is, when OPSTATE:T0STATE= 100.
**Note 2:** X = Don't care.
**Note 3:** None of the SYNCn pins is used. The internal 2kHz alignment generators free-run at their existing alignment. See Section 7.9.2.5.
**Note 4:** When SOURCE = 11XX, selection and enable of SYNCn pins is automatic regardless of the setting of AEFSEN. In this mode the AEFSEN bit is retasked to specify whether or not MCR3:EFSEN is automatically cleared when the T0 DPLL's selected reference changes.

### *7.9.2.2 Sampling*

By default the external frame-sync signal on the enabled SYNCn pin is first sampled on the rising edge of the selected reference. This gives the most margin, given that the SYNCn signal is falling-edge aligned with the selected reference since both come from the master device. The expected timing of the SYNCn signal with respect to the sampling clock can be adjusted from 0.5 cycles early to 1 cycle late using the FSCR2:PHASEn[1:0] field.

### *7.9.2.3 Resampling*

The SYNCn signal is then resampled by an internal clock derived from the T0 DPLL. The resampling resolution is a function of the frequency of the selected reference and FSCR2:OCN. When OCN = 0, the resampling resolution is 6.48MHz, which gives the highest sampling margin and also aligns clocks at 6.48MHz and multiples thereof. When OCN = 1, if the selected reference is 19.44MHz the resampling resolution is 19.44MHz. If the selected reference is 38.88MHz the resampling resolution is 38.88MHz. The selected reference must be either 19.44MHz or 38.88MHz.

### *7.9.2.4 Qualification*

The SYNCn signal is qualified when it has consistent phase and correct frequency. Specifically, it is qualified when its significant edge has been found at exact 2kHz boundaries (when resampled as previously described) for 64 SYNCn cycles in a row. It is disqualified when one significant edge is not found at the 2kHz boundary.

### *7.9.2.5 Output Clock Alignment*

When the T0 DPLL is locked, external frame sync is enabled and the SYNCn signal is qualified, the SYNCn signal can be used to falling-edge align the T0 DPLL derived output clocks. Output clocks FSYNC and MFSYNC share a 2kHz alignment generator, while the rest of the T0 DPLL derived output clocks share a second 2kHz alignment generator. When external frame sync is not enabled or the SYNCn signal is not qualified, these 2Hz alignment generators free-run with their existing 2kHz alignments. When external frame sync is enabled and the SYNCn signal is qualified, the FSYNC/MFSYNC 2kHz alignment generator is always synchronized by SYNCn, and, therefore, FSYNC and MFSYNC are always falling-edge aligned with SYNCn. When FSCR2:INDEP = 0, the T0 DPLL 2kHz alignment generator is also synchronized with the FSYNC/MFSYNC 2kHz alignment generator to falling-edge align all T0-derived output clocks with SYNCn. When INDEP = 1, the T0 DPLL 2kHz alignment

generator is *not* synchronized with the FSYNC/MFSYNC 2kHz alignment generator and continues to free-run with its existing 2kHz alignment. This avoids any disturbance on the T0 DPLL derived output clocks when SYNCn has a change of phase position.

#### *7.9.2.6 Frame-Sync Monitor*

The frame-sync monitor signal OPSTATE:FSMON operates in two modes, depending on the setting of the enable bit (MCR3:EFSEN).

When EFSEN = 1 (external frame sync enabled), the OPSTATE:FSMON bit is set when SYNCn is not qualified and cleared when SYNCn is qualified. If SYNCn is disqualified, both 2kHz alignment generators are immediately disconnected from SYNCn to avoid phase movement on the T0-derived outputs clocks. When OPSTATE:FSMON is set, the latched status bit MSR3:FSMON is also set, which can cause an interrupt if enabled in the IER3 register. If SYNCn immediately stabilizes at a new phase and proper frequency, it is requalified after 64 2kHz cycles (nominally 32ms). Unless system software intervenes, after SYNCn is requalified the 2kHz alignment generators will synchronize with SYNCn's new phase alignment, causing a sudden phase movement on the output clocks. System software can avoid this sudden phase movement on the output clocks by responding to the FSMON interrupt within the 32ms window with appropriate action, which might include disabling external frame sync (MCR3:EFSEN = 0) to prevent the resynchronization of the 2kHz alignment generators with SYNCn, forcing the T0 DPLL into holdover (MCR1:T0STATE = 010) to avoid affecting the output clocks with any other phase hits, and possibly even disabling the master timing card and promoting the slave timing card to master since the 2kHz signal from the master should not have such phase movements.

When EFSEN = 0 (external frame sync disabled), OPSTATE:FSMON is set when the negative edge of the resampled SYNCn signal is outside the window determined by FSCR3:MONLIM relative to the MFSYNC negative edge (or positive edge if MFSYNC is inverted) and clear when within the window. When OPSTATE:FSMON is set, the latched status bit MSR3:FSMON is also set, which can cause an interrupt if enabled in the IER3 register.

### *7.9.3 SYNCn Pins*

FSYNC and MFSYNC are always produced from the T0 DPLL. The other output clocks can also be configured as 2kHz or 8kHz outputs, derived from the T0 DPLL.

**Table 7-18. External Frame-Sync Source**

| SYNCSRC[2:0] | SELECTED REFERENCE | EXTERNAL FRAME-SYNC SOURCE |
|---|---|---|
| 0XX | IC3 or IC5 | SYNC1 |
| | IC4 or IC6 | SYNC2 |
| | IC9 or IC2 | SYNC3 |
| 1X0 | IC3 | SYNC1 |
| | IC4 | SYNC2 |
| 10X | IC9 | SYNC3 |
| 1X1 | IC5 | SYNC1 |
| | IC6 | SYNC2 |
| 11X | IC2 | SYNC3 |

There are three PHASEn[1:0] (n = 1, 2, 3) select fields in the FSCR2 register. PHASE1[1:0] is associated with SYNC1, PHASE2[1:0] is associated with SYNC2, and PHASE3[1:0] is associated with SYNC3. All three SYNCn inputs can have their timing adjusted to account for frame-sync signal vs. clock signal delay differences in each path.

When this function is enabled with FSCR3.SOURCE = 11XX, MCR3.AEFSEN, and MCR3.EFSEN, the monitoring and qualification function described in Section 7.9.2 is only performed on the selected SYNCn input pin.

### 7.9.4 Other Configuration Options

FSYNC and MFSYNC are always produced from the T0 DPLL. Output clocks OC1 to OC7 can also be configured as 2kHz or 8kHz outputs, derived from either the T0 DPLL or the T4 DPLL (as specified by the 2K8KSRC bit in FSCR1). If needed, the T4 DPLL can be used as a separate DPLL for the frame-sync path by configuring it for a 2kHz input and 2kHz and/or 8kHz frame-sync outputs.

## 7.10 Microprocessor Interface

The device presents an SPI interface on the $\overline{CS}$, SCLK, SDI, and SDO pins. SPI is a widely used master/slave bus protocol that allows a master device and one or more slave devices to communicate over a serial bus. The DS3102 is always a slave device. Masters are typically microprocessors, ASICs, or FPGAs. Data transfers are always initiated by the master device, which also generates the SCLK signal. The DS3102 receives serial data on the SDI pin and transmits serial data on the SDO pin. SDO is high impedance except when the DS3102 is transmitting data to the bus master.

**Bit Order.** When both bit 3 and bit 4 are low at device address 3FFFh, the register address and all data bytes are transmitted MSB first on both SDI and SDO. When either bit 3 or bit 4 is set to 1 at device address 3FFFh, the register address and all data bytes are transmitted LSB first on both SDI and SDO. The reset default setting and Motorola SPI convention is MSB first.

**Clock Polarity and Phase.** The CPOL pin defines the polarity of SCLK. When CPOL = 0, SCLK is normally low and pulses high during bus transactions. When CPOL = 1, SCLK is normally high and pulses low during bus transactions. The CPHA pin sets the phase (active edge) of SCLK. When CPHA = 0, data is latched in on SDI on the leading edge of the SCLK pulse and updated on SDO on the trailing edge. When CPHA = 1, data is latched in on SDI on the trailing edge of the SCLK pulse and updated on SDO on the following leading edge. SCLK does not have to toggle between access, i.e., when $\overline{CS}$ is high. See Figure 7-5.

**Device Selection.** Each SPI device has its own chip-select line. To select the DS3102, pull its $\overline{CS}$ pin low.

**Control Word.** After $\overline{CS}$ is pulled low, the bus master transmits the control word during the first 16 SCLK cycles. In MSB-first mode, the control word has the form:

R/$\overline{W}$ A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0 BURST

where A[13:0] is the register address, R/$\overline{W}$ is the data direction bit (1 = read, 0 = write), and BURST is the burst bit (1 = burst access, 0 = single-byte access). In LSB-first mode, the order of the 14 address bits is reversed. In the discussion that follows, a control word with R/$\overline{W}$ = 1 is a read control word, while a control word with R/$\overline{W}$ = 0 is a write control word.

**Single-Byte Writes.** See Figure 7-6. After $\overline{CS}$ goes low, the bus master transmits a write control word with BURST = 0 followed by the data byte to be written. The bus master then terminates the transaction by pulling $\overline{CS}$ high.

**Single-Byte Reads.** See Figure 7-6. After $\overline{CS}$ goes low, the bus master transmits a read control word with BURST = 0. The DS3102 then responds with the requested data byte. The bus master then terminates the transaction by pulling $\overline{CS}$ high.

**Burst Writes.** See Figure 7-6. After $\overline{CS}$ goes low, the bus master transmits a write control word with BURST = 1 followed by the first data byte to be written. The DS3102 receives the first data byte on SDI, writes it to the specified register, increments its internal address register, and prepares to receive the next data byte. If the master continues to transmit, the DS3102 continues to write the data received and increment its address counter. After the address counter reaches 3FFFh it rolls over to address 0000h and continues to increment.

**Burst Reads.** See Figure 7-6. After $\overline{CS}$ goes low, the bus master transmits a read control word with BURST = 1. The DS3102 then responds with the requested data byte on SDO, increments its address counter, and prefetches the next data byte. If the bus master continues to demand data, the DS3102 continues to provide the data on SDO,

increment its address counter, and prefetch the following byte. After the address counter reaches 3FFFh, it rolls over to address 0000h and continues to increment.

**Early Termination of Bus Transactions.** The bus master can terminate SPI bus transactions at any time by pulling $\overline{CS}$ high. In response to early terminations, the DS3102 resets its SPI interface logic and waits for the start of the next transaction. If a write transaction is terminated prior to the SCLK edge that latches the LSB of a data byte, the data byte is not written.

**Design Option: Wiring SDI and SDO Together.** Because communication between the bus master and the DS3102 is half-duplex, the SDI and SDO pins can be wired together externally to reduce wire count. To support this option, the bus master must not drive the SDI/SDO line when the DS3102 is transmitting.

**AC Timing.** See Table 10-10 and Figure 10-4 for AC timing specifications for the SPI interface.

*Figure 7-5. SPI Clock Phase Options*

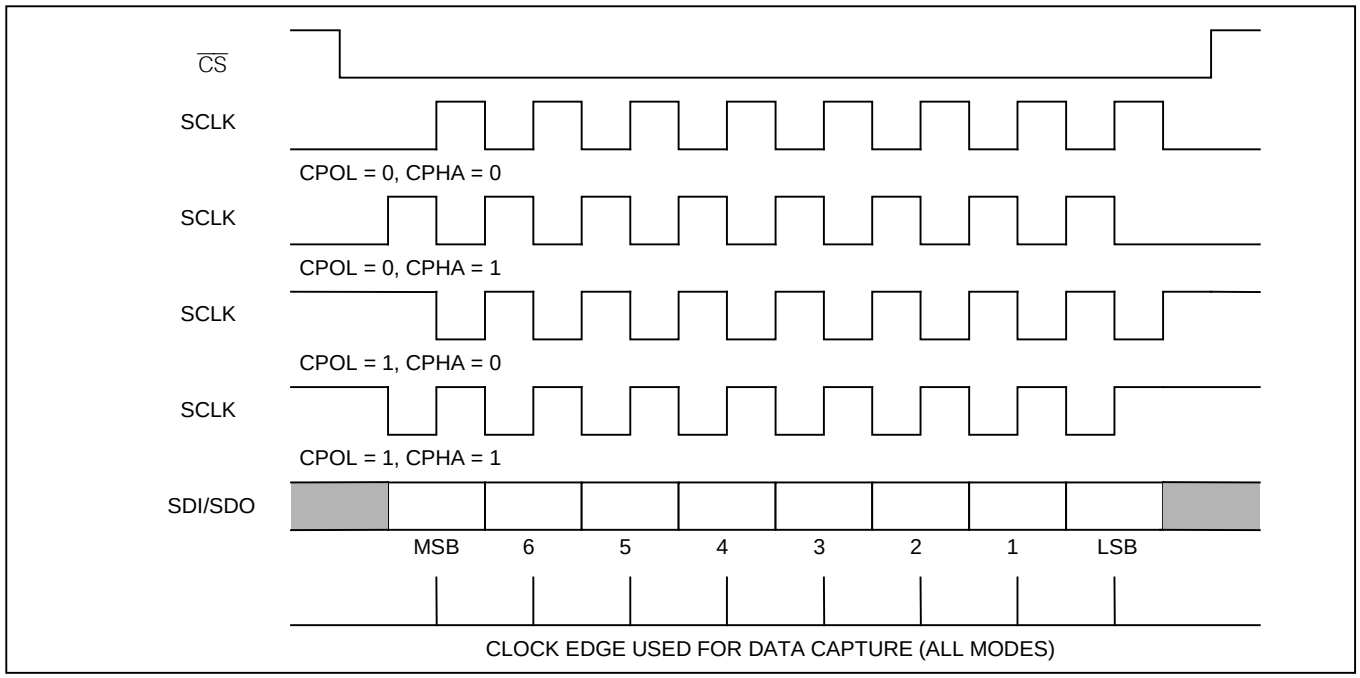
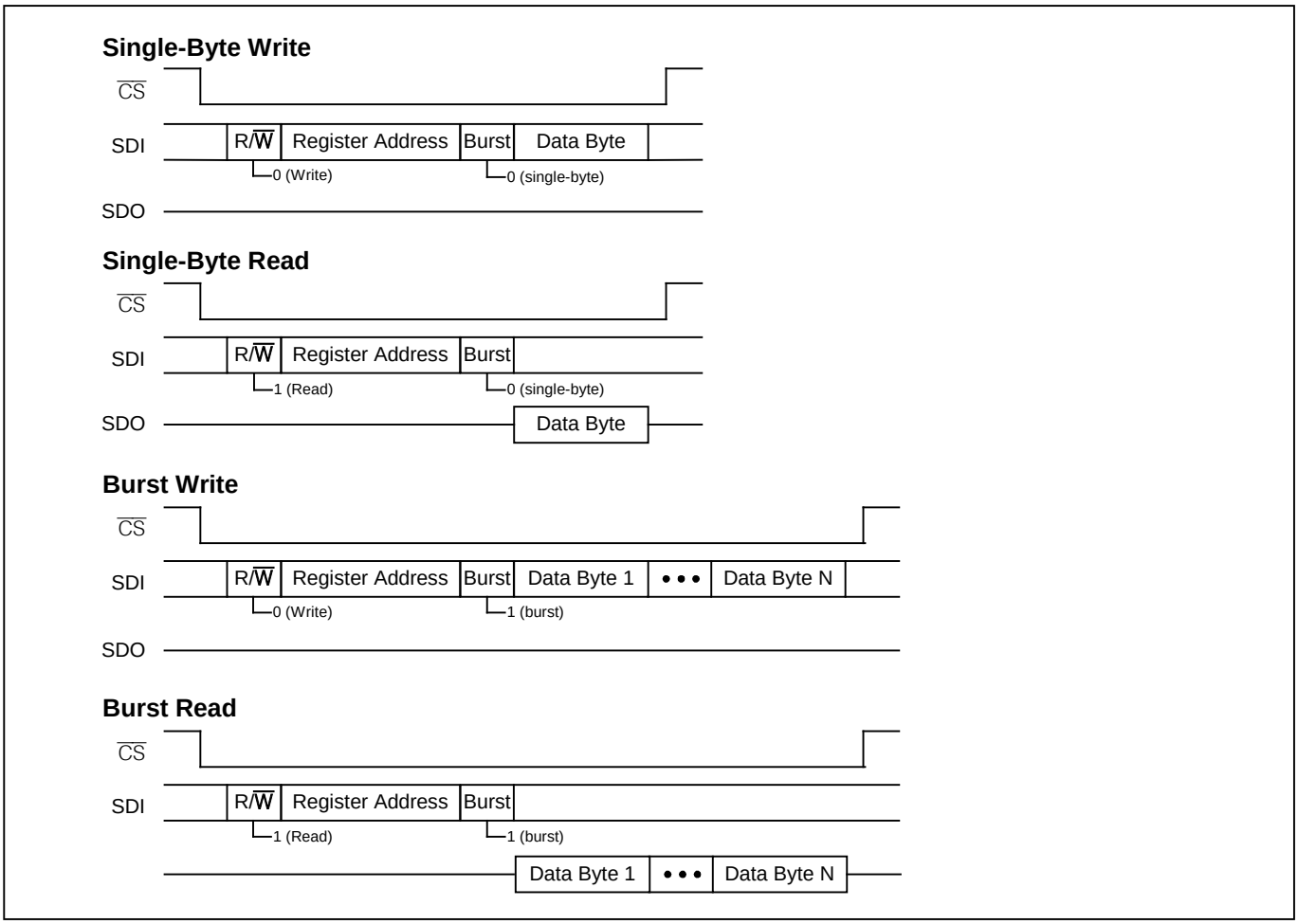


*Figure 7-6. SPI Bus Transactions*



## 7.11 Reset Logic

The device has three reset controls: the $\overline{RST}$ pin, the RST bit in MCR1, and the JTAG reset pin $\overline{JTRST}$. The $\overline{RST}$ pin asynchronously resets the entire device, except for the JTAG logic. When the $\overline{RST}$ pin is low all internal registers are reset to their default values, including those fields that latch their default values from, or based on, the states of configuration input pins when the $\overline{RST}$ goes high. **The $\overline{RST}$ pin must be asserted once after power-up while the external oscillator is stabilizing.**

The MCR1:RST bit resets the entire device (except for the microprocessor interface, the JTAG logic, and the RST bit itself), but when RST is active, the register fields with pin-programmed defaults do not latch their values from, or based on, the corresponding input pins. Instead, these fields are reset to the default values that were latched when the $\overline{RST}$ pin was last active.

Microsemi recommends holding $\overline{RST}$ low while the external oscillator starts up and stabilizes. Some OCXOs take 250ms or more to start up and stabilize their output signals to valid logic levels and pulse widths. An incorrect reset condition could result if $\overline{RST}$ is released before the oscillator has started up completely.

**Important:** System software must wait at least 100µs after reset ($\overline{RST}$ pin or RST bit) is deasserted before initializing the device as described in Section 7.13.

## 7.12 Power-Supply Considerations

Due to the dual-power-supply nature of the DS3102, some I/Os have parasitic diodes between a 1.8V supply and a 3.3V supply. When ramping power supplies up or down, care must be taken to avoid forward-biasing these diodes because it could cause latchup. Two methods are available to prevent this. The first method is to place a Schottky diode external to the device between the 1.8V supply and the 3.3V supply to force the 3.3V supply to be within one parasitic diode drop below the 1.8V supply (i.e., $V_{DDIO} > V_{DD}$ - ~0.4V). The second method is to ramp up the 3.3V supply first and then ramp up the 1.8V supply.

## 7.13 Initialization

After power-up or reset, a series of writes must be done to the DS3102 to tune it for optimal performance. This series of writes is called the initialization script. Each DS3102 die revision has a different initialization script. For the latest initialization scripts contact Microsemi timing products technical support.

**Note: System software must wait at least 100µs after reset is deasserted before initializing the device.**

# 8. Register Descriptions

The DS3102 has an overall address range from 000h to 1FFh. Table 8-1 in Section 8.4 shows the register map. In each register, bit 7 is the MSB and bit 0 is the LSB. Register addresses not listed and bits marked "—" are reserved and must be written with 0. Writing other values to these registers may put the device in a factory test mode resulting in undefined operation. Bits labeled "0" or "1" must be written with that value for proper operation. Register fields with underlined names are read-only fields; writes to these fields have no effect. All other fields are read-write. Register fields are described in detail in the register descriptions that follow Table 8-1.

Note: Systems must be able to access the entire address range from 0 to 01FFh. Proper device initialization requires a sequence of writes to addresses in the range 0180-01FFh.

## 8.1 Status Bits

The device has two types of status bits. Real-time status bits are read-only and indicate the state of a signal at the time it is read. Latched status bits are set when a signal changes state (low-to-high, high-to-low, or both, depending on the bit) and cleared when written with a logic 1 value. Writing a 0 has no effect. When set, some latched status bits can cause an interrupt request on the INTREQ pin if enabled to do so by corresponding interrupt enable bits. ISR#.LOCK# are special-case latched status bits because they cannot create an interrupt request on the INTREQ pin and a "write 0" is needed to clear them.

## 8.2 Configuration Fields

Configuration fields are read-write. During reset, each configuration field reverts to the default value shown in the register definition. Configuration register bits marked "—" are reserved and must be written with 0.

## 8.3 Multiregister Fields

Multiregister fields—such as FREQ[18:0] in registers FREQ1, FREQ2, and FREQ3—must be handled carefully to ensure that the bytes of the field remain consistent. A write access to a multiregister field is accomplished by writing all the registers of the field in any order, with no intervening accesses to other registers in the device. If the write sequence is interrupted by another access, none of the bytes are written and the MSR4:MRAA latched status bit is set to indicate the write was aborted. A read access from a multiregister field is accomplished by reading the registers of the field in any order, with no intervening accesses to other registers in the device. When one register of a multiregister field is read, the other register(s) in the field are frozen until after they are all read. If the read sequence is interrupted by another access, the registers of the multibyte field are unfrozen and the MSR4:MRAA bit is set to indicate the read was aborted. For best results, interrupt servicing should be disabled in the microprocessor before a multiregister access and then enabled again after the access is complete. The multiregister fields are:

| FIELD | REGISTERS | ADDRESSES | TYPE |
|---|---|---|---|
| FREQ[18:0] | FREQ1, FREQ2, FREQ3 | 0Ch, 0Dh, 07h | Read Only |
| MCLKFREQ[15:0] | MCLK1, MCLK2 | 3Ch, 3Dh | Read/Write |
| HOFREQ[18:0] | HOCR1, HOCR2, HOCR3* | 3Eh, 3Fh, 40h | Read/Write |
| HARDLIM[9:0] | DLIMIT1, DLIMIT2 | 41h, 42h | Read/Write |
| DIVN[15:0] | DIVN1, DIVN2 | 46h, 47h | Read/Write |
| OFFSET[15:0] | OFFSET1, OFFSET2 | 70h, 71h | Read/Write |
| PHASE[15:0] | PHASE1, PHASE2 | 77h, 78h | Read Only |

**HOCR3* *is a special case because its upper 5 bits are not part of a multiregister field, but its lower 3 bits are part of the HOFREQ[18:0] multiregister field. Writes to HOCR3 immediately update the upper 5 bits without any requirement to also write HOCR1 and HOCR2. The lower 3 bits of HOCR3 (HOFREQ[18:16]), however, can only be written as part of a proper write sequence for a multiregister field, as described above. A write to HOCR3 contiguous with writes to HOCR1 and HOCR2 can simultaneously write the upper 5 bits immediately and start/continue/complete a multiregister write of HOFREQ[18:0].*

## 8.4 Register Definitions

### Table 8-1. Register Map

***Note:*** *Register names are hyperlinks to register definitions. Underlined fields are read-only.*

| ADDR | REGISTER | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|---|---|
| 00h | ID1 | ID[7:0] | | | | | | | |
| 01h | ID2 | ID[15:8] | | | | | | | |
| 02h | REV | REV[7:0] | | | | | | | |
| 03h | TEST1 | PALARM | D180 | — | RA | 0 | 8KPOL | 0 | 0 |
| 05h | MSR1 | IC8 | — | IC6 | IC5 | IC4 | IC3 | IC2 | IC1 |
| 06h | MSR2 | STATE | SRFAIL | — | — | — | — | — | IC9 |
| 07h | FREQ3 | — | — | — | — | — | FREQ[18:16] | | |
| 08h | MSR3 | FSMON | T4LOCK | PHMON | T4NOIN | — | — | — | — |
| 09h | OPSTATE | FSMON | T4LOCK | T0SOFT | T4SOFT | — | T0STATE[2:0] | | |
| 0Ah | PTAB1 | REF1[3:0] | | | | SELREF[3:0] | | | |
| 0Bh | PTAB2 | REF3[3:0] | | | | REF2[3:0] | | | |
| 0Ch | FREQ1 | FREQ[7:0] | | | | | | | |
| 0Dh | FREQ2 | FREQ[15:8] | | | | | | | |
| 0Eh | VALSR1 | IC8 | — | IC6 | IC5 | IC4 | IC3 | IC2 | IC1 |
| 0Fh | VALSR2 | FHORDY | SHORDY | — | — | — | — | — | IC9 |
| 10h | ISR1 | SOFT2 | HARD2 | ACT2 | LOCK2 | SOFT1 | HARD1 | ACT1 | LOCK1 |
| 11h | ISR2 | SOFT4 | HARD4 | ACT4 | LOCK4 | SOFT3 | HARD3 | ACT3 | LOCK3 |
| 12h | ISR3 | SOFT6 | HARD6 | ACT6 | LOCK6 | SOFT5 | HARD5 | ACT5 | LOCK5 |
| 13h | ISR4 | SOFT8 | HARD8 | ACT8 | LOCK8 | — | — | — | — |
| 14h | ISR5 | — | — | — | — | SOFT9 | HARD9 | ACT9 | LOCK9 |
| 17h | MSR4 | FHORDY | SHORDY | MRAA | — | — | — | — | — |
| 18h | IPR1 | PRI2[3:0] | | | | PRI1[3:0] | | | |
| 19h | IPR2 | PRI4[3:0] | | | | PRI3[3:0] | | | |
| 1Ah | IPR3 | PRI6[3:0] | | | | PRI5[3:0] | | | |
| 1Bh | IPR4 | PRI8[3:0] | | | | — | | | |
| 1Ch | IPR5 | — | | | | PRI9[3:0] | | | |
| 20h | ICR1 | DIVN | LOCK8K | BUCKET[1:0] | | FREQ[3:0] | | | |
| 21h | ICR2 | DIVN | LOCK8K | BUCKET[1:0] | | FREQ[3:0] | | | |
| 22h | ICR3 | DIVN | LOCK8K | BUCKET[1:0] | | FREQ[3:0] | | | |
| 23h | ICR4 | DIVN | LOCK8K | BUCKET[1:0] | | FREQ[3:0] | | | |
| 24h | ICR5 | DIVN | LOCK8K | BUCKET[1:0] | | FREQ[3:0] | | | |
| 25h | ICR6 | DIVN | LOCK8K | BUCKET[1:0] | | FREQ[3:0] | | | |
| 27h | ICR8 | DIVN | LOCK8K | BUCKET[1:0] | | FREQ[3:0] | | | |
| 28h | ICR9 | DIVN | LOCK8K | BUCKET[1:0] | | FREQ[3:0] | | | |
| 30h | VALCR1 | IC8 | — | IC6 | IC5 | IC4 | IC3 | IC2 | IC1 |
| 31h | VALCR2 | — | — | — | — | — | — | — | IC9 |
| 32h | MCR1 | RST | — | FREN | LOCKPIN | — | T0STATE[2:0] | | |
| 33h | MCR2 | — | — | — | — | T0FORCE[3:0] | | | |
| 34h | MCR3 | AEFSEN | LKATO | XOEDGE | MANHO | EFSEN | SONSDH | — | REVERT |
| 35h | MCR4 | LKT4T0 | — | — | — | T4FORCE[3:0] | | | |
| 36h | MCR5 | RSV4 | RSV3 | RSV2 | RSV1 | IC2SF | IC1SF | IC6SF | IC5SF |
| 37h | OCR6 | — | OC5EN | OC4EN | OC5BEN | OC4BEN | OC3BEN | OC2BEN | OC1BEN |
| 38h | MCR6 | DIG2AF | DIG2SS | DIG1SS | — | — | — | — | — |
| 39h | MCR7 | DIG2F[1:0] | | DIG1F[1:0] | | — | — | DIG2SRC | DIG1SRC |

| ADDR | REGISTER | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|---|---|
| 3Ah | MCR8 | OC5SF | | OC4SF | | OC7SF | | OC6SF | |
| 3Bh | MCR9 | AUTOBW | — | — | — | LIMINT | — | — | — |
| 3Ch | MCLK1 | MCLKFREQ[7:0] | | | | | | | |
| 3Dh | MCLK2 | MCLKFREQ[15:8] | | | | | | | |
| 3Eh | HOCR1 | HOFREQ[7:0] | | | | | | | |
| 3Fh | HOCR2 | HOFREQ[15:8] | | | | | | | |
| 40h | HOCR3 | AVG | FAST | RDAVG | MINIHO[1:0] | | HOFREQ[18:16] | | |
| 41h | DLIMIT1 | HARDLIM[7:0] | | | | | | | |
| 42h | DLIMIT2 | — | — | — | — | — | — | HARDLIM[9:8] | |
| 43h | IER1 | IC8 | — | IC6 | IC5 | IC4 | IC3 | IC2 | IC1 |
| 44h | IER2 | STATE | SRFAIL | — | — | — | — | — | IC9 |
| 45h | IER3 | FSMON | T4LOCK | PHMON | T4NOIN | — | — | — | — |
| 46h | DIVN1 | DIVN[7:0] | | | | | | | |
| 47h | DIVN2 | DIVN[15:8] | | | | | | | |
| 48h | MCR10 | FMONCLK | SRFPIN | UFSW | EXTSW | PBOFRZ | PBOEN | SOFTEN | HARDEN |
| 49h | ILIMIT | SOFT[3:0] | | | | HARD[3:0] | | | |
| 4Ah | SRLIMIT | SOFT[3:0] | | | | HARD[3:0] | | | |
| 4Bh | MCR11 | — | — | — | T4T0 | FMEASIN[3:0] | | | |
| 4Ch | FMEAS | FMEAS[7:0] | | | | | | | |
| 4Dh | DLIMIT3 | FLLOL | SOFTLIM[6:0] | | | | | | |
| 4Eh | IER4 | FHORDY | SHORDY | — | — | — | — | — | — |
| 4Fh | OCR5 | — | AOF7 | AOF6 | AOF5 | AOF4 | AOF3 | AOF2 | AOF1 |
| 50h | LB0U | LB0U[7:0] | | | | | | | |
| 51h | LB0L | LB0L[7:0] | | | | | | | |
| 52h | LB0S | LB0S[7:0] | | | | | | | |
| 53h | LB0D | — | — | — | — | — | — | LB0D[1:0] | |
| 54h | LB1U | LB1U[7:0] | | | | | | | |
| 55h | LB1L | LB1L[7:0] | | | | | | | |
| 56h | LB1S | LB1S[7:0] | | | | | | | |
| 57h | LB1D | — | — | — | — | — | — | LB1D[1:0] | |
| 58h | LB2U | LB2U[7:0] | | | | | | | |
| 59h | LB2L | LB2L[7:0] | | | | | | | |
| 5Ah | LB2S | LB2S[7:0] | | | | | | | |
| 5Bh | LB2D | — | — | — | — | — | — | LB2D[1:0] | |
| 5Ch | LB3U | LB3U[7:0] | | | | | | | |
| 5Dh | LB3L | LB3L[7:0] | | | | | | | |
| 5Eh | LB3S | LB3S[7:0] | | | | | | | |
| 5Fh | LB3D | — | — | — | — | — | — | LB3D[1:0] | |
| 60h | OCR1 | OFREQ2[3:0] | | | | OFREQ1[3:0] | | | |
| 61h | OCR2 | OFREQ4[3:0] | | | | OFREQ3[3:0] | | | |
| 62h | OCR3 | OFREQ6[3:0] | | | | OFREQ5[3:0] | | | |
| 63h | OCR4 | MFSEN | FSEN | — | — | OFREQ7[3:0] | | | |
| 64h | T4CR1 | — | — | — | — | T4FREQ[3:0] | | | |
| 65h | T0CR1 | T4MT0 | T4APT0 | T0FT4[2:0] | | | T0FREQ[2:0] | | |
| 66h | T4BW | — | — | — | — | — | — | T4BW[1:0] | |
| 67h | T0LBW | — | — | — | T0LBW[4:0] | | | | |
| 69h | T0ABW | — | — | — | T0ABW[4:0] | | | | |
| 6Ah | T4CR2 | — | PD2G8K[2:0] | | | — | DAMP[2:0] | | |
| 6Bh | T0CR2 | — | PD2G8K[2:0] | | | — | DAMP[2:0] | | |
| 6Ch | T4CR3 | PD2EN | — | | | | PD2G[2:0] | | |

| ADDR | REGISTER | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|---|---|
| 6Dh | T0CR3 | PD2EN | — | | | | PD2G[2:0] | | |
| 6Eh | GPCR | GPIO4D | GPIO3D | GPIO2D | GPIO1D | GPIO4O | GPIO3O | GPIO2O | GPIO1O |
| 6Fh | GPSR | — | — | — | — | GPIO4 | GPIO3 | GPIO2 | GPIO1 |
| 70h | OFFSET1 | OFFSET[7:0] | | | | | | | |
| 71h | OFFSET2 | OFFSET[15:8] | | | | | | | |
| 72h | PBOFF | — | — | PBOFF[5:0] | | | | | |
| 73h | PHLIM1 | FLEN | NALOL | 1 | — | — | FINELIM[2:0] | | |
| 74h | PHLIM2 | CLEN | MCPDEN | USEMCPD | — | COARSELIM[3:0] | | | |
| 76h | PHMON | NW | — | PMEN | PMPBEN | PMLIM[3:0] | | | |
| 77h | PHASE1 | PHASE[7:0] | | | | | | | |
| 78h | PHASE2 | PHASE[15:8] | | | | | | | |
| 79h | PHLKTO | PHLKTOM[1:0] | | PHLKTO[5:0] | | | | | |
| 7Ah | FSCR1 | 2K8KSRC | SYNCSRC | | | 8KINV | 8KPUL | 2KINV | 2KPUL |
| 7Bh | FSCR2 | INDEP | OCN | PHASE3[1:0] | | PHASE2[1:0] | | PHASE1[1:0] | |
| 7Ch | FSCR3 | RECAL | MONLIM[2:0] | | | SOURCE[3:0] | | | |
| 7Dh | INTCR | — | — | — | — | LOS | GPO | OD | POL |
| 7Eh | PROT | PROT[7:0] | | | | | | | |
| 7Fh-1FFh | reserved | — | — | — | — | — | — | — | — |

**Register Map Color Coding**

| | |
|---|---|
| | Device Identification and Protection |
| | Local Oscillator and Master Clock Configuration |
| | Input Clock Configuration |
| | Input Clock Monitoring |
| | Input Clock Selection |
| | DPLL Configuration |
| | DPLL State |
| | Output Clock Configuration |
| | Frame/Multiframe-Sync Configuration |

Register Name: **ID1**
Register Description: **Device Identification Register, LSB**
Register Address: **00h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ID[7:0] | | | | | | | |
| Default | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |

**Bits 7 to 0: Device ID (ID[7:0]).** ID[15:0] = 0C1Eh = 3102 decimal.

Register Name: **ID2**
Register Description: **Device Identification Register, MSB**
Register Address: **01h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ID[15:8] | | | | | | | |
| Default | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |

**Bits 7 to 0: Device ID (ID[15:8]).** See the ID1 register description.

Register Name: **REV**
Register Description: **Device Revision Register**
Register Address: **02h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | REV[7:0] | | | | | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Bits 7 to 0: Device Revision (REV[7:0]).** Contact the factory to interpret this value and determine the latest revision.

Register Name: **TEST1**
Register Description: **Test Register 1 (Not Normally Used)**
Register Address: **03h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | PALARM | D180 | — | RA | 0 | 8KPOL | 0 | 0 |
| Default | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 |

**Bit 7: Phase Alarm (PALARM).** This real-time status bit indicates the state of the T0 DPLL phase-lock detector. See Section 7.7.6. (**Note:** This is not the same as T0STATE = locked.)

0 = T0 DPLL phase-lock parameters are met (FLEN, CLEN, NALOL, FLLOL)
1 = T0 DPLL loss-of-phase lock

**Bit 6: Disable 180 (D180).** When locking to a new reference, the T0 DPLL first tries nearest edge locking (±180°) for the first two seconds. If unsuccessful it then tries full phase/frequency locking (±360°). Disabling the nearest edge locking can reduce lock time by up to two seconds but may cause an unnecessary phase shift (up to 360°) when the new reference is close in frequency/phase to the old reference. See Section 7.7.5.

0 = Normal operation: try nearest edge locking then phase/frequency locking
1 = Phase/frequency locking only

**Bit 4: Resync Analog Dividers (RA).** When this bit is set the analog output dividers are always synchronized to ensure that low-frequency outputs are in sync with the higher frequency clock from the DPLL.

0 = Synchronized for the first two seconds after power-up
1 = Always synchronized

**Bits 3, 1, and 0:** Leave set to zero (test control).

**Bit 2: 8kHz Edge Polarity (8KPOL).** Specifies the input clock edge to lock to on the selected reference when it is configured for LOCK8K mode. See Section 7.4.2.

0 = Falling edge
1 = Rising edge

Register Name: **MSR1**
Register Description: **Master Status Register 1**
Register Address: **05h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | IC8 | — | IC6 | IC5 | IC4 | IC3 | IC2 | IC1 |
| Default | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |

**Bits 7 and 5 to 0: Input Clock Status Change (IC8 and IC[6:1]).** Each of these latched status bits is set to 1 when the corresponding VALSR1 status bit changes state (set or cleared). If soft frequency limit alarms are enabled (MCR10:SOFTEN = 1), each of these latched status bits is also set to 1 when the corresponding SOFT bit in the ISR registers changes state (set or cleared). Each bit is cleared when written with a 1 and not set again until the VALSR1 bit changes state again. When one of these latched status bits is set it can cause an interrupt request on the INTREQ pin if the corresponding interrupt enable bit is set in the IER1 register. See Section 7.5 for input clock validation/invalidation criteria.

Register Name: **MSR2**
Register Description: **Master Status Register 2**
Register Address: **06h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | STATE | SRFAIL | — | — | — | — | — | IC9 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

**Bit 7: T0 DPLL State Change (STATE).** This latched status bit is set to 1 when the operating state of the T0 DPLL changes. STATE is cleared when written with a 1 and not set again until the operating state changes again. When STATE is set it can cause an interrupt request on the INTREQ pin if the STATE interrupt enable bit is set in the IER2 register. The current operating state can be read from the T0STATE field of the OPSTATE register. See Section 7.7.1.

**Bit 6: Selected Reference Failed (SRFAIL).** This latched status bit is set to 1 when the selected reference to the T0 DPLL fails, (i.e., no clock edges in two UI). SRFAIL is cleared when written with a 1. When SRFAIL is set it can cause an interrupt request on the INTREQ pin if the SRFAIL interrupt enable bit is set in the IER2 register. SRFAIL is not set in free-run mode or holdover mode. See Section 7.5.3.

**Bit 0: Input Clock Status Change (IC9).** This latched status bit is set to 1 when the corresponding VALSR status bit changes state (set or cleared). If soft frequency limit alarms are enabled (MCR10:SOFTEN = 1), this bit is also set to 1 when the corresponding SOFT bit in the ISR registers changes state (set or cleared). This bit is cleared when written with a 1 and not set again until either the VALSR2 bit or the SOFT bit changes state. When this bit is set it can cause an interrupt request on the INTREQ pin if the corresponding interrupt enable bit is set in the IER2 register. See Section 7.5 for input clock validation/invalidation criteria.

Register Name: **FREQ3**
Register Description: **Frequency Register 3**
Register Address: **07h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | — | — | — | — | — | FREQ[18:16] | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Bits 2 to 0: Current DPLL Frequency (FREQ[18:16]).** See the FREQ1 register description.

Register Name: **MSR3**
Register Description: **Master Status Register 3**
Register Address: **08h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | FSMON | T4LOCK | PHMON | T4NOIN | — | — | — | — |
| Default | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |

**Bit 7: Frame-Sync Input Monitor Alarm (FSMON).** This latched status bit is set to 1 when OPSTATE:FSMON transitions from 0 to 1. FSMON is cleared when written with a 1. When FSMON is set it can cause an interrupt request on the INTREQ pin if the FSMON interrupt enable bit is set in the IER3 register. See Section 7.9.2.

**Bit 6: T4 DPLL Lock Status Change (T4LOCK).** This latched status bit is set to 1 when the lock status of the T4 DPLL (OPSTATE:T4LOCK) changes (becomes locked when previously unlocked or becomes unlocked when previously locked). T4LOCK is cleared when written with a 1 and not set again until the T4 lock status changes again. When T4LOCK is set it can cause an interrupt request on the INTREQ pin if the T4LOCK interrupt enable bit is set in the IER3 register. See Section 7.7.6.

**Bit 5: Phase Monitor Alarm (PHMON).** This latched status bit is set to 1 when the phase monitor alarm limit has been exceeded (PMLIM field of the PHMON register). PHMON is cleared when written with a 1 and not set again until the threshold is exceeded again. When PHMON is set it can cause an interrupt request on the INTREQ pin if the PHMON interrupt enable bit is set in the IER3 register. See Section 7.7.7.

**Bit 4: T4 No Valid Inputs Alarm (T4NOIN).** This latched status bit is set to 1 when the T4 DPLL has no valid inputs available. T4NOIN is cleared when written with a 1 unless the T4 DPLL still has no valid inputs available. When T4NOIN is set it can cause an interrupt request on the INTREQ pin if the T4NOIN interrupt enable bit is set in the IER3 register. See Section 7.5.

Register Name: **OPSTATE**
Register Description: **Operating State Register**
Register Address: **09h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | FSMON | T4LOCK | T0SOFT | T4SOFT | — | T0STATE[2:0] | | |
| Default | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

**Bit 7: Frame-Sync Input Monitor Alarm (FSMON).** This real-time status bit indicates the current status of the frame-sync input monitor. See Section 7.9.2.6.

0 = No alarm
1 = Alarm

**Bit 6: T4 DPLL Lock Status (T4LOCK).** This real-time status bit indicates the current phase-lock status of the T4 DPLL. See Sections 7.5.3 and 7.7.6.

0 = Not locked to selected reference
1 = Locked to selected reference

**Bit 5: T0 DPLL Frequency Soft Alarm (T0SOFT).** This real-time status bit indicates whether the T0 DPLL is tracking its reference within the soft alarm limits specified in the SOFT[6:0] field of the DLIMIT3 register. See Section 7.7.6.

0 = No alarm; frequency is within the soft alarm limits
1 = Soft alarm; frequency is outside the soft alarm limits

**Bit 4: T4 DPLL Frequency Soft Alarm (T4SOFT).** This real-time status bit indicates whether the T4 DPLL is tracking its reference within the soft alarm limits specified in the SOFT[6:0] field of the DLIMIT3 register. See Section 7.7.6.

0 = No alarm; frequency is within the soft alarm limits
1 = Soft alarm; frequency is outside the soft alarm limits

**Bits 2 to 0: T0 DPLL Operating State (T0STATE[2:0]).** This real-time status field indicates the current state of the T0 DPLL state machine. Values not listed below correspond to invalid (unused) states. See Section 7.7.1.

001 = Free-run
010 = Holdover
100 = Locked
101 = Prelocked 2
110 = Prelocked
111 = Loss-of-lock

Register Name: **PTAB1**
Register Description: **Priority Table Register 1**
Register Address: **0Ah**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | REF1[3:0] | | | | SELREF[3:0] | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Bits 7 to 4: Highest Priority Valid Reference (REF1[3:0]).** This real-time status field indicates the highest priority valid input reference. When T4T0 = 0 in the MCR11 register, this field indicates the highest priority reference for the T0 DPLL. When T4T0 = 1, it indicates the highest priority reference for the T4 DPLL. Note that an input reference cannot be indicated in this field if it has been marked invalid in the VALCR1 or VALCR2 register. When the T0 DPLL is in nonrevertive mode (REVERT = 0 in the MCR3 register) this field may not have the same value as the SELREF[3:0] field. See Section 7.6.2.

0000 = No valid input reference available
0001 = Input IC1
0010 = Input IC2
0011 = Input IC3
0100 = Input IC4
0101 = Input IC5
0110 = Input IC6
0111 = {unused value}
1000 = Input IC8
1001 = Input IC9
1010 to 1111 = {unused values}

**Bits 3 to 0: Selected Reference (SELREF[3:0]).** This real-time status field indicates the current selected reference. When T4T0 = 0 in the MCR11 register, this field indicates the selected reference for the T0 DPLL. When T4T0 = 1, it indicates the selected reference for the T4 DPLL. Note that an input clock cannot be indicated in this field if it has been marked invalid in the VALCR1 or VALCR2 register. When the T0 DPLL is in nonrevertive mode (REVERT = 0 in the MCR3 register) this field may not have the same value as the REF1[3:0] field. See Section 7.6.2.

0000 = No source currently selected
0001 = Input IC1
0010 = Input IC2
0011 = Input IC3
0100 = Input IC4
0101 = Input IC5
0110 = Input IC6
0111 = {unused value}
1000 = Input IC8
1001 = Input IC9
1010 to 1111 = {unused values}

Register Name: **PTAB2**
Register Description: **Priority Table Register 2**
Register Address: **0Bh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | REF3[3:0] | | | | REF2[3:0] | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Bits 7 to 4: Third Highest Priority Valid Reference (REF3[3:0]).** This real-time status field indicates the third highest priority validated input reference. When T4T0 = 0 in the MCR11 register, this field indicates the third highest priority reference for the T0 DPLL. When T4T0 = 1, it indicates the third highest reference for the T4 DPLL. Note that an input reference cannot be indicated in this field if it has been marked invalid in the VALCR1 or VALCR2 register. See Section 7.6.2.

0000 = Less than three valid sources available
0001 = Input IC1
0010 = Input IC2
0011 = Input IC3
0100 = Input IC4
0101 = Input IC5
0110 = Input IC6
0111 = {unused value}
1000 = Input IC8
1001 = Input IC9
1010 to 1111 = {unused values}

**Bits 3 to 0: Second Highest Priority Valid Reference (REF2[3:0]).** This real-time status field indicates the second highest priority validated input reference. When T4T0 = 0 in the MCR11 register, this field indicates the second highest priority reference for the T0 DPLL. When T4T0 = 1, it indicates the second highest reference for the T4 DPLL. Note that an input reference cannot be indicated in this field if it has been marked invalid in the VALCR1 or VALCR2 register. See Section 7.6.2.

0000 = Less than two valid sources available
0001 = Input IC1
0010 = Input IC2
0011 = Input IC3
0100 = Input IC4
0101 = Input IC5
0110 = Input IC6
0111 = {unused value}
1000 = Input IC8
1001 = Input IC9
1010 to 1111 = {unused values}

Register Name: **FREQ1**
Register Description: **Frequency Register 1**
Register Address: **0Ch**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | FREQ[7:0] | | | | | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

***Note:*** *The FREQ1, FREQ2, and FREQ3 registers must be read consecutively. See Section 8.3.*

**Bits 7 to 0: Current DPLL Frequency (FREQ[7:0]).** The full 19-bit FREQ[18:0] field spans this register, FREQ2, and FREQ3. FREQ is a two's-complement signed integer that expresses the current frequency as an offset with respect to the master clock frequency (see Section 7.3). When T4T0 = 0 in the MCR11 register, FREQ indicates the current frequency offset of the T0 DPLL. When T4T0 = 1, FREQ indicates the current frequency offset of the T4 path. Because the value in this register field is derived from the DPLL integral path, it can be considered an average frequency with a rate of change inversely proportional to the DPLL bandwidth. If LIMINT = 1 in the MCR9 register, the value of FREQ freezes when the DPLL reaches its minimum or maximum frequency. The frequency offset in ppm is equal to FREQ[18:0] × 0.0003068. See Section 7.7.1.6.

Application Note: Frequency measurements are relative, i.e., they measure the frequency of the selected reference with respect to the local oscillator. As such, when a frequency difference exists, it is difficult to distinguish whether the selected reference is off frequency or the local oscillator is off frequency. In systems with timing card redundancy, the use of two timing cards, master and slave, can address this difficulty. Both master and slave have separate local oscillators, and each measures the selected reference. These two measurements provide the necessary information to distinguish which reference is off frequency, if we make the simple assumption that at most one reference has a significant frequency deviation at any given time (i.e., a single point of failure). If both master and slave indicate a significant frequency offset, then the selected reference must be off frequency. If the master indicates a frequency offset but the slave does not, then the master's local oscillator must be off frequency. Likewise, if the slave indicates a frequency offset but the master does not, then the slave's local oscillator must be off frequency.

Register Name: **FREQ2**
Register Description: **Frequency Register 2**
Register Address: **0Dh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | FREQ[15:8] | | | | | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Bits 7 to 0: Current DPLL Frequency (FREQ[15:8]).** See the FREQ1 register description.

Register Name: **VALSR1**
Register Description: **Input Clock Valid Status Register 1**
Register Address: **0Eh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | IC8 | — | IC6 | IC5 | IC4 | IC3 | IC2 | IC1 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Bits 7 and 5 to 0: Input Clock Valid Status (IC8 and IC[6:1]).** Each of these real-time status bits is set to 1 when the corresponding input clock is valid. An input is valid if it has no active alarms (HARD = 0, ACT = 0, LOCK = 0 in the corresponding ISR register). See also the MSR1 register and Section 7.5.

0 = Invalid
1 = Valid

Register Name: **VALSR2**
Register Description: **Input Clock Valid Status Register 2**
Register Address: **0Fh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | FHORDY | SHORDY | — | — | — | — | — | IC9 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Bit 7: Fast Holdover Frequency Ready (FHORDY).** This real-time status bit is set to 1 when the T0 DPLL has a holdover value that has been averaged over the 8-minute holdover averaging period. See the related latched status bit in MSR4 and Section 7.7.1.6.

**Bit 6: Slow Holdover Frequency Ready (SHORDY).** This real-time status bit is set to 1 when the T0 DPLL has a holdover value that has been averaged over the 110-minute holdover averaging period. See the related latched status bit in MSR4 and Section 7.7.1.6.

**Bit 0: Input Clock Valid Status (IC9).** This bit has the same behavior as the bits in VALSR1 but for the IC9 clock.

Register Name: **ISR1**
Register Description: **Input Status Register 1**
Register Address: **10h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | SOFT2 | HARD2 | ACT2 | LOCK2 | SOFT1 | HARD1 | ACT1 | LOCK1 |
| Default | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |

**Bit 7: Soft Frequency Limit Alarm for Input Clock 2 (SOFT2).** This real-time status bit indicates a soft frequency limit alarm for input clock 2. If IC2 is the selected reference, SOFT2 is set to 1 when the frequency of IC2 is greater than or equal to the soft limit set in the SRLIMIT register. If IC2 is not the selected reference then SOFT2 is set to 1 when the frequency of IC2 is greater than or equal to the soft limit set in the ILIMIT register. Soft alarms are disabled by default but can be enabled by setting SOFTEN = 1 in the MCR10 register. A soft alarm does not invalidate an input clock. See Section 7.5.1.

**Bit 6: Hard Frequency Limit Alarm for Input Clock 2 (HARD2).** This real-time status bit indicates a hard frequency limit alarm for input clock 2. If IC2 is the selected reference, HARD2 is set to 1 when the frequency of IC2 is greater than or equal to the hard limit set in the SRLIMIT register. If IC2 is not the selected reference HARD2 is set to 1 when the frequency of IC2 is greater than or equal to the hard limit set in the ILIMIT register. Hard alarms are enabled by default but can be disabled by setting HARDEN = 0 in the MCR10 register. A hard alarm clears the IC2 status bit in the VALSR1 register, invalidating the IC2 clock. See section 7.5.1.

**Bit 5: Activity Alarm for Input Clock 2 (ACT2).** This real-time status bit is set to 1 when the leaky bucket accumulator for IC2 reaches the alarm threshold specified in the LBxU register (where x in LBxU is specified in the BUCKET field of ICR1). An activity alarm clears the IC2 status bit in the VALSR1 register, invalidating the IC2 clock. See Section 7.5.2.

**Bit 4: Phase-Lock Alarm for Input Clock 2 (LOCK2).** This status bit is set to 1 if IC2 is the selected reference and the T0 DPLL cannot phase lock to IC2 within the duration specified in the PHLKTO register (default = 100 seconds). A phase lock alarm clears the IC2 status bit in VALSR1, invalidating the IC2 clock. If LKATO = 1 in MCR3 then LOCK2 is automatically cleared after a timeout period of 128 seconds. LOCK2 is a read/write bit. System software can clear LOCK4 by writing 0 to it, but writing 1 is ignored. See Section 7.7.1.

**Bit 3: Soft Frequency Limit Alarm for Input Clock 1 (SOFT1).** This bit has the same behavior as the SOFT2 bit but for the IC1 input clock.

**Bit 2: Hard Frequency Limit Alarm for Input Clock 1 (HARD1).** This bit has the same behavior as the HARD2 bit but for the IC1 input clock.

**Bit 1: Activity Alarm for Input Clock 1 (ACT1).** This bit has the same behavior as the ACT2 bit but for the IC1 input clock.

**Bit 0: Phase-Lock Alarm for Input Clock 1 (LOCK1).** This bit has the same behavior as the LOCK2 bit but for the IC1 input clock.

Register Name: **ISR2**
Register Description: **Input Status Register 2**
Register Address: **11h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | SOFT4 | HARD4 | ACT4 | LOCK4 | SOFT3 | HARD3 | ACT3 | LOCK3 |
| Default | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |

**Bit 7: Soft Frequency Limit Alarm for Input Clock 4 (SOFT4).** This real-time status bit indicates a soft frequency limit alarm for input clock 4. If IC4 is the selected reference then SOFT4 is set to 1 when the frequency of IC4 is greater than or equal to the soft limit set in the SRLIMIT register. If IC4 is not the selected reference then SOFT4 is set to 1 when the frequency of IC4 is greater than or equal to the soft limit set in the ILIMIT register. Soft alarms are disabled by default but can be enabled by setting SOFTEN = 1 in the MCR10 register. A soft alarm does not invalidate an input clock. See Section 7.5.1.

**Bit 6: Hard Frequency Limit Alarm for Input Clock 4 (HARD4).** This real-time status bit indicates a hard frequency limit alarm for input clock 4. If IC4 is the selected reference then HARD4 is set to 1 when the frequency of IC4 is greater than or equal to the hard limit set in the SRLIMIT register. If IC4 is not the selected reference then HARD4 is set to 1 when the frequency of IC4 is greater than or equal to the hard limit set in the ILIMIT register. Hard alarms are enabled by default but can be disabled by setting HARDEN = 0 in the MCR10 register. A hard alarm clears the IC4 status bit in the VALSR1 register, invalidating the IC4 clock. See section 7.5.1.

**Bit 5: Activity Alarm for Input Clock 4 (ACT4).** This real-time status bit is set to 1 when the leaky bucket accumulator for IC4 reaches the alarm threshold specified in the LBxU register (where x in LBxU is specified in the BUCKET field of ICR4). An activity alarm clears the IC4 status bit in the VALSR1 register, invalidating the IC4 clock. See Section 7.5.2.

**Bit 4: Phase-Lock Alarm for Input Clock 4 (LOCK4).** This status bit is set to 1 if IC4 is the selected reference and the T0 DPLL cannot phase lock to IC4 within the duration specified in the PHLKTO register (default = 100 seconds). A phase-lock alarm clears the IC4 status bit in VALSR1, invalidating the IC4 clock. If LKATO = 1 in MCR3 then LOCK4 is automatically cleared after a timeout period of 128 seconds. LOCK4 is a read/write bit. System software can clear LOCK4 by writing 0 to it, but writing 1 is ignored. See Section 7.7.1.

**Bit 3: Soft Frequency Limit Alarm for Input Clock 3 (SOFT3).** This bit has the same behavior as the SOFT4 bit but for the IC3 input clock.

**Bit 2: Hard Frequency Limit Alarm for Input Clock 3 (HARD3).** This bit has the same behavior as the HARD4 bit but for the IC3 input clock.

**Bit 1: Activity Alarm for Input Clock 3 (ACT3).** This bit has the same behavior as the ACT4 bit but for the IC3 input clock.

**Bit 0: Phase-Lock Alarm for Input Clock 3 (LOCK3).** This bit has the same behavior as the LOCK4 bit but for the IC3 input clock.

Register Name: **ISR3**
Register Description: **Input Status Register 3**
Register Address: **12h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | SOFT6 | HARD6 | ACT6 | LOCK6 | SOFT5 | HARD5 | ACT5 | LOCK5 |
| Default | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |

This register has the same behavior as the ISR1and ISR2 registers but for input clocks IC5 and IC6.

Register Name: **ISR4**
Register Description: **Input Status Register 4**
Register Address: **13h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | SOFT8 | HARD8 | ACT8 | LOCK8 | — | — | — | — |
| Default | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

This register has the same behavior as the ISR1and ISR2 registers but for input clock IC8.

Register Name: **ISR5**
Register Description: **Input Status Register 5**
Register Address: **14h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | — | — | — | — | SOFT9 | HARD9 | ACT9 | LOCK9 |
| Default | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |

This register has the same behavior as the ISR1and ISR2 registers but for input clock IC9.

Register Name: **MSR4**
Register Description: **Master Status Register 4**
Register Address: **17h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | FHORDY | SHORDY | MRAA | — | — | — | — | — |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Bit 7: Fast Holdover Frequency Ready (FHORDY).** This latched status bit is set to 1 when the T0 DPLL has a holdover value that has been averaged over the 8-minute holdover averaging period. FHORDY is cleared when written with a 1. When FHORDY is set it can cause an interrupt request on the INTREQ pin if the FHORDY interrupt enable bit is set in the IER4 register. See Section 7.7.1.6.

**Bit 6: Slow Holdover Frequency Ready (SHORDY).** This latched status bit is set to 1 when the T0 DPLL has a holdover value that has been averaged over the 110-minute holdover averaging period. SHORDY is cleared when written with a 1. When SHORDY is set it can cause an interrupt request on the INTREQ pin if the SHORDY interrupt enable bit is set in the IER4 register. See Section 7.7.1.6.

**Bit 5: Multiregister Access Aborted (MRAA).** This latched status bit is set to 1 when a multibyte access (read or write) is interrupted by another access to the device. MRAA is cleared when written with a 1. MRAA cannot cause an interrupt to occur. See Section 8.3.

Register Name: **IPR1**
Register Description: **Input Priority Register 1**
Register Address: **18h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | PRI2[3:0] | | | | PRI1[3:0] | | | |
| Default (T0) | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| Default (T4) | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |

**Bits 7 to 4: Priority for Input Clock 2 (PRI2[3:0]).** Priority 0001 is highest; priority 1111 is lowest. When MCR11:T4T0 = 0, PRI2 configures IC2's priority for the T0 DPLL. When T4T0 = 1, PRI2 configures IC2's priority for the T4 path. See Section 7.6.1.

0000 = IC2 unavailable for selection.
0001–1111= IC2 relative priority

**Bits 3 to 0: Priority for Input Clock 1 (PRI1[3:0]).** Priority 0001 is highest; priority 1111 is lowest. When MCR11:T4T0 = 0, PRI1 configures IC1's priority for the T0 DPLL. When T4T0 = 1, PRI1 configures IC1's priority for the T4 path. See Section 7.6.1.

0000 = IC1 unavailable for selection.
0001–1111= IC1 relative priority

Register Name: **IPR2**
Register Description: **Input Priority Register 2**
Register Address: **19h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | PRI4[3:0] | | | | PRI3[3:0] | | | |
| Default (T0) | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |
| Default (T4) | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |

**Bits 7 to 4: Priority for Input Clock 4 (PRI4[3:0]).** Priority 0001 is highest; priority 1111 is lowest. When MCR11:T4T0 = 0, PRI4 configures IC4's priority for the T0 DPLL. When T4T0 = 1, PRI4 configures IC4's priority for the T4 path. See Section 7.6.1.

0000 = IC4 unavailable for selection
0001–1111= IC4 relative priority

**Bits 3 to 0: Priority for Input Clock 3 (PRI3[3:0]).** Priority 0001 is highest; priority 1111 is lowest. When MCR11:T4T0 = 0, PRI3 configures IC3's priority for the T0 DPLL. When T4T0 = 1, PRI3 configures IC3's priority for the T4 path. See Section 7.6.1.

0000 = IC3 unavailable for selection
0001–1111= IC3 relative priority

Register Name: **IPR3**
Register Description: **Input Priority Register 3**
Register Address: **1Ah**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | PRI6[3:0] | | | | PRI5[3:0] | | | |
| Default (T0) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Default (T4) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

These registers have the same behavior as IPR2 but for input clocks IC5 and IC6.

Register Name: **IPR4**
Register Description: **Input Priority Register 4**
Register Address: **1Bh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | PRI8[3:0] | | | | — | — | — | — |
| Default (T0) | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| Default (T4) | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |

These registers have the same behavior as IPR2 but for input clock IC8.

Register Name: **IPR5**
Register Description: **Input Priority Register 5**
Register Address: **1Ch**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | — | — | — | — | PRI9[3:0] | | | |
| Default (T0) | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| Default (T4) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

These registers have the same behavior as IPR2 but for input clock IC9.

Register Name: **ICR1, ICR2, ICR3, ICR4, ICR5, ICR6, ICR8, ICR9**
Register Description: **Input Configuration Register 1, 2, 3, 4, 5, 6, 8, 9**
Register Address: **20h, 21h, 22h, 23h, 24h, 25h, 27h, 28h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DIVN | LOCK8K | BUCKET[1:0] | | FREQ[3:0] | | | |
| Default | 0 | 0 | 0 | 0 | see below | | | |

***Note:*** *These registers are identical in function. ICRx is the control register for input clock ICx.*

**Bit 7: DIVN Mode (DIVN).** When DIVN is set to 1 and LOCK8K = 0, the input clock is divided down by a programmable predivider. The resulting output clock is then passed to the DPLL and frequency monitor. All input clocks for which DIVN = 1 are divided by the factor specified in DIVN1 and DIVN2. When DIVN = 1 and LOCK8K = 0 in an ICR register, the FREQ field of that register must be set to the input frequency divided by the divide factor. When DIVN = 1 and LOCK8K = 1 in an ICR register, the FREQ field of that register is decoded as the alternate frequencies. See Sections 7.4.2.2 and 7.4.2.4.

0 = Disabled
1 = Enabled

**Bit 6: LOCK8K Mode (LOCK8K).** When LOCK8K is set to 1 and DIVN = 0, the input clock is divided down by a preset predivider. The resulting output clock, which is always 8kHz, is then passed to the DPLL. LOCK8K is ignored when DIVN = 0 and FREQ[3:0] = 1001 (2kHz) or 1010 (4kHz). In addition, LOCK8K mode cannot be used with 5MHz input clocks. When DIVN = 1 and LOCK8K = 1 in an ICR register, the FREQ field of that register is decoded as the alternate frequencies. See Sections 7.4.2.2 and 7.4.2.3

0 = Disabled
1 = Enabled

**Bits 5 to 4: Leaky Bucket Configuration (BUCKET[1:0]).** Each input clock has leaky bucket accumulator logic in its activity monitor. The LBxy registers at addresses 50h to 5Fh specify four different leaky bucket configurations. Any of the four configurations can be specified for the input clock. See Section 7.5.2.

00 = leaky bucket configuration 0
01 = leaky bucket configuration 1
10 = leaky bucket configuration 2
11 = leaky bucket configuration 3

**Bits 3 to 0: Input Clock Frequency (FREQ[3:0]).** When DIVN = 0 and LOCK8K = 0 (standard direct-lock mode), this field specifies the input clock's nominal frequency for direct-lock operation. When DIVN = 0 and LOCK8K = 1 (LOCK8K mode) this field specifies the input clock's nominal frequency for LOCK8K operation. When DIVN = 1 and LOCK8K = 0 (DIVN mode), this field specifies the frequency after the DIVN divider (i.e., input frequency divided by DIVN + 1). When DIVN = 1 and LOCK8K = 1 (alternate direct-lock frequencies), this field specifies the input clock's nominal frequency for direct-lock operation.

DIVN = 0 or LOCK8K = 0: (Standard direct-lock mode, LOCK8K mode, or DIVN mode)

0000 = 8kHz
0001 = 1544kHz or 2048kHz (as determined by SONSDH bit in the MCR3 register)
0010 = 6.48MHz
0011 = 19.44MHz
0100 = 25.92MHz
0101 = 38.88MHz
0110 = 51.84MHz
0111 = 77.76MHz
1000 = 155.52MHz (only valid for LVDS inputs)
1001 = 2kHz
1010 = 4kHz
1011 = 6312kHz
1100 = 5MHz
1101 = 31.25 MHz (not a multiple of 8kHz and therefore not valid for LOCK8K mode)
1110–1111 = undefined

DIVN = 1 and LOCK8K = 1: (Alternate direct-lock frequency decode)

0000 = 10MHz (internally divided down to 5MHz)
0001 = 25MHz (internally divided down to 5MHz)
0010 = 62.5MHz (internally down to 31.25MHz)
0011 = 125MHz (internally down to 31.25MHz)
0100 = 156.25MHz (differential inputs only; internally divided down to 31.25MHz)
0101–1111 = undefined

**FREQ[3:0] Default Values:**

ICR1–ICR4: 0000b
ICR5–ICR9: 0011b

Register Name: **VALCR1**
Register Description: **Input Clock Valid Control Register 1**
Register Address: **30h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | IC8 | — | IC6 | IC5 | IC4 | IC3 | IC2 | IC1 |
| Default | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |

**Bits 7 and 5 to 0: Input Clock Valid Control (IC8 and IC[6:1]).** These control bits can be used to force input clocks to be considered invalid. If a clock is invalidated by one of these control bits it will not appear in the priority table in the PTAB1 and PTAB2 registers, even if the clock is otherwise valid. These bits are useful when system software needs to force clocks to be invalid in response to OAM commands. Note that setting a VALCR bit low has no effect on the corresponding bit in the VALSR registers. See Section 7.6.2.

0 = Force invalid
1 = Do not force invalid; determine validity normally

Register Name: **VALCR2**
Register Description: **Input Clock Valid Control Register 2**
Register Address: **31h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | — | — | — | — | — | — | — | IC9 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

**Bit 0: Input Clock Valid Control (IC9).** This bit has the same behavior as the bits in VALCR1 but for the IC9 input clock.

Register Name: **MCR1**
Register Description: **Master Configuration Register 1**
Register Address: **32h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | RST | — | FREN | LOCKPIN | — | T0STATE[2:0] | | |
| Default | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |

**Bit 7: Device Reset (RST).** When this bit is high the entire device is held in reset, and all register fields, except the RST bit itself, are reset to their default states. When RST is active, the register fields with pin-programmed defaults do not latch their values from the corresponding input pins. Instead, these fields are reset to the default values that were latched from the pins when the RST pin was last active. See Section 7.11.

0 = Normal operation
1 = Reset

**Bit 5: Frequency Range Detect Enable (FREN).** When this bit is high the frequency of each input clock is measured and used to quickly declare the input inactive.

0 = Frequency range detect disabled.
1 = Frequency range detect enabled.

**Bit 4: T0 DPLL LOCK Pin Enable (LOCKPIN).** When this bit is high the LOCK pin indicates when the T0 DPLL state machine is in the LOCK state (OPSTATE.T0STATE = 100).

0 = LOCK pin is not driven.
1 = LOCK pin is driven high when the T0 DPLL is in the lock state.

**Bits 2 to 0: T0 DPLL State Control (T0STATE[2:0]).** This field allows the T0 DPLL state machine to be forced to a specified state. The state machine remains in the forced state, and, therefore, cannot react to alarms and other events, as long as T0STATE is not equal to 000. See Section 7.7.1.

000 = Automatic (normal state machine operation)
001 = Free-run
010 = Holdover
011 = {unused value}
100 = Locked
101 = Prelocked 2
110 = Prelocked
111 = Loss-of-lock

Register Name: **MCR2**
Register Description: **Master Configuration Register 2**
Register Address: **33h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | — | — | — | — | T0FORCE[3:0] | | | |
| Default | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |

**Bits 3 to 0: T0 DPLL Force Selected Reference (T0FORCE[3:0]).** This field provides a way to force a specified input clock to be the selected reference for the T0 DPLL. Internally this is accomplished by forcing the clock to have the highest priority (as specified in PTAB1:REF1). In revertive mode (MCR3:REVERT = 1) the forced clock automatically becomes the selected reference (as specified in PTAB1:SELREF) as well. In nonrevertive mode the forced clock only becomes the selected reference when the existing selected reference is invalidated or made unavailable for selection.

When a reference is forced, the activity monitor and frequency monitor for that input and the T0 DPLL's loss-of-lock timeout logic all continue to operate and affect the relevant VALSR and MSR register bits. However, when the reference is declared invalid the T0 DPLL is not allowed to switch to another input clock. The T0 DPLL continues to respond to the fast activity monitor, transitioning to mini-holdover in response to short-term events and to full holdover in response to longer events. See Section 7.6.3.

0000 = Automatic source selection (normal operation)
0001 = Force to IC1
0010 = Force to IC2
0011 = Force to IC3
0100 = Force to IC4
0101 = Force to IC5
0110 = Force to IC6
0111 = {unused value}
1000 = Force to IC8
1001 = Force to IC9
1010–1110 = {unused values}
1111 = Automatic source selection (normal operation)

Register Name: **MCR3**
Register Description: **Master Configuration Register 3**
Register Address: **34h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | AEFSEN | LKATO | XOEDGE | MANHO | EFSEN | SONSDH | — | REVERT |
| Default | 1 | 1 | 0 | 0 | 1 | see below | 1 | 0 |

**Bit 7: Auto External Frame Sync Enable (AEFSEN).** This bit has two functions depending on the external frame sync mode. See Section 7.9.2.1.

SYNC1 Modes:
0 = SYNC1 Manual Mode: External frame sync is manually enabled on the SYNC1 pin when EFSEN = 1.
1 = SYNC1 Auto Mode: External frame sync is automatically enabled on the SYNC1 pin when EFSEN = 1 and the T0 DPLL is locked to the input clock specified in FSCR3:SOURCE.

SYNC123 Mode:
0 = EFSEN is not automatically cleared when the T0 DPLL's selected reference changes.
1 = EFSEN is automatically cleared when the T0 DPLL's selected reference changes.
(EFSEN must be set again by system software to enable it again.)

**Bit 6: Phase-Lock Alarm Timeout (LKATO).** This bit controls how phase alarms on input clocks can be terminated. Phase alarms are indicated by the LOCK bits in the ISR registers.

0 = Phase alarms on input clocks can only be cancelled by software.
1 = Phase alarms are automatically cancelled after a timeout period of 128 seconds.

**Bit 5: Local Oscillator Edge (XOEDGE).** This bit specifies the significant clock edge of the local oscillator clock signal on the REFCLK input pin. The faster edge should be selected for best jitter performance. See Section 7.3.

0 = Rising edge
1 = Falling edge

**Bit 4: Manual Holdover (MANHO).** When this bit is set to 1 the T0 DPLL holdover frequency is set by the HOFREQ field in the HOCR1, HOCR2, and HOCR3 registers. When MANHO = 1, it has priority over any other holdover control fields. See Section 7.7.1.6.

0 = Standard holdover: holdover frequency is learned by the T0 DPLL from the selected reference.
1 = Manual holdover: holdover frequency is taken from the HOFREQ field.

**Bit 3: External Frame-Sync Enable (EFSEN).** When this bit is set to 1, the T0 DPLL looks for an external frame-sync signal on the SYNCn pin(s). In SYNC123 mode if AEFSEN = 1, EFSEN is automatically cleared when the T0 DPLL's selected reference changes. See Section 7.9.2.1.

0 = Disable external frame sync; ignore SYNCn pins.
1 = Enable external frame sync on SYNCn pin(s).

**Bit 2: SONET or SDH Frequencies (SONSDH).** This bit specifies the clock rate for input clocks with FREQ = 0001 in the ICR registers (20h to 28h). During reset the default value of this bit is latched from the SONSDH pin. See Section 7.4.2.

0 = 2048kHz
1 = 1544kHz

**Bit 0: Revertive Mode (REVERT).** This bit configures the T0 DPLL for revertive or nonrevertive operation. (The T4 DPLL is always revertive). In revertive mode, if an input clock with a higher priority than the selected reference becomes valid, the higher priority reference immediately becomes the selected reference. In nonrevertive mode the higher priority reference does not immediately become the selected reference but does become the highest priority reference in the priority table (REF1 field in the PTAB1 register). See Section 7.6.2.

Register Name: **MCR4**
Register Description: **Master Configuration Register 4**
Register Address: **35h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | LKT4T0 | — | — | — | T4FORCE[3:0] | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Bit 7: Lock T4 to T0 (LKT4T0).** When this bit is set to 1 (and T0CR1:T4APT0 = 0) all output clocks are generated from the T0 DPLL, and the T4CR1:T4FREQ field selects the frequency of the T4 APLL. See Section 7.8.2.2. When LKT4T0 = 0, the T4 APLL can be locked to either the T4 DPLL or the T0 DPLL, depending on the setting of T0CR1:T4APT0.

0 = T4 APLL can lock to either T4 or the T0 DPLL.
1 = T4 APLL always locked to the T0 DPLL.

**Bits 3 to 0: T4 DPL Force Selected Reference (T4FORCE[3:0]).** This field provides a way to force a specified input clock to be the selected reference for the T4 DPLL. Internally this is accomplished by forcing the clock to have the highest priority (as specified in PTAB1:REF1). Since the T4 DPLL always operates in revertive mode, the forced clock automatically becomes the selected reference (as specified in PTAB1:SELREF) as well.

When a reference is forced, the activity monitor and frequency monitor for that input continue to operate and affect the relevant ISR, VALSR and MSR register bits. However, when the reference is declared invalid, the T4 DPLL is not allowed to switch to another input clock. See Section 7.6.3.

0000 = Automatic source selection (normal operation)
0001 = Force to IC1
0010 = Force to IC2
0011 = Force to IC3
0100 = Force to IC4
0101 = Force to IC5
0110 = Force to IC6
0111 = {unused value}
1000 = Force to IC8
1001 = Force to IC9
1010–1110 = {unused value}
1111 = Automatic source selection (normal operation)

Register Name: **MCR5**
Register Description: **Master Configuration Register 5**
Register Address: **36h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | RSV[4:1] | | | | IC2SF | IC1SF | IC6SF | IC5SF |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Bits 7 to 4: Reserved Bits 4 to 1 (RSV[4:1]).** These bits are reserved for future use. They can be written to and read back, but they should only be set to 0.

**Bit 3: Input Clock 2 Signal Format (IC2SF).** For backward compatibility this bit can be written to and read back, but it does not affect the IC2POS/NEG inputs pins. See Section 7.4.1.

**Bit 2: Input Clock 1 Signal Format (IC1SF).** For backward compatibility this bit can be written to and read back, but it does not affect the IC1POS/NEG inputs pins. See Section 7.4.1.

**Bit 1: Input Clock 6 Signal Format (IC6SF).** For backward compatibility this bit can be written to and read back, but it does not affect the IC6POS/NEG inputs pins. See Section 7.4.1.

**Bit 0: Input Clock 5 Signal Format (IC5SF).** For backward compatibility this bit can be written to and read back, but it does not affect the IC5POS/NEG inputs pins. See Section 7.4.1.

Register Name: **OCR6**
Register Description: **Output Configuration Register 6**
Register Address: **37h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | — | OC5EN | OC4EN | OC5BEN | OC4BEN | OC3BEN | OC2BEN | OC1BEN |
| Default | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

**Bit 6: OC5 Output Enable (OC5EN).** Enables the OC5 output pin.

0 = Output clock pin disabled, drives low.
1 = Output clock pin controlled by OCR3.OFREQ5.

**Bit 5: OC4 Output Enable (OC4EN).** Enables the OC4 output pin.

0 = Output clock pin disabled, drives low.
1 = Output clock pin controlled by OCR2.OFREQ4.

**Bit 4: OC5B Output Enable (OC5BEN).** Enables the OC5B output pin.

0 = Output clock pin disabled, drives low.
1 = Output clock pin controlled by OCR3.OFREQ5.

**Bit 3: OC4B Output Enable (OC4BEN).** Enables the OC4B output pin.

0 = Output clock pin disabled, drives low.
1 = Output clock pin controlled by OCR2.OFREQ4.

**Bit 2: OC3B Output Enable (OC3BEN).** Selects GPIO3 or OC3B function for the OC3B/GPIO3 pin.

0 = GPIO3 functionality.
1 = Output clock pin controlled by OCR2.OFREQ3.

**Bit 1: OC2B Output Enable (OC2BEN).** Selects GPIO2 or OC2B function for the OC2B/GPIO2 pin.

0 = GPIO2 functionality.
1 = Output clock pin controlled by OCR1.OFREQ2.

**Bit 0: OC1B Output Enable (OC1BEN).** Selects GPIO1 or OC1B function for the OC1B/GPIO1 pin.

0 = GPIO1 functionality.
1 = Output clock pin controlled by OCR1.OFREQ1.

Register Name: **MCR6**
Register Description: **Master Configuration Register 6**
Register Address: **38h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DIG2AF | DIG2SS | DIG1SS | — | — | — | — | — |
| Default | 0 | see below | see below | 1 | 1 | 1 | 1 | 1 |

**Bit 7: Digital Alternate Frequency (DIG2AF).** Selects alternative frequencies.

0 = Digital2 N x E1 or N x DS1 frequency specified by DIG2SS and MCR7:DIG2F.
1 = Digital2 6.312MHz, 10MHz, or N x 19.44MHz frequency specified by DIG2SS and MCR7:DIG2F.

**Bit 6: Digital2 SONET or SDH Frequencies (DIG2SS).** This bit specifies whether the clock rates generated by the Digital2 clock synthesizer are multiples of 1.544MHz (SONET compatible), multiples of 2.048MHz (SDH compatible), or alternate frequencies. The specific multiple is set in the DIG2F field of the MCR7 register. When $\overline{RST}$ = 0 the default value of this bit is latched from the SONSDH pin.

DIG2AF = 0:
0 = Multiples of 2048kHz
1 = Multiples of 1544kHz
DIG2AF = 1:
6.312MHz, 10MHz, or N x 19.44MHz

**Bit 5: Digital1 SONET or SDH Frequencies (DIG1SS).** This bit specifies whether the clock rates generated by the Digital1 clock synthesizer are multiples of 1544kHz (SONET compatible) or multiples of 2048kHz (SDH compatible). The specific multiple is set in the DIG1F field of the MCR7 register. When $\overline{RST}$ = 0 the default value of this bit is latched from the SONSDH pin.

0 = Multiples of 2048kHz
1 = Multiples of 1544kHz

Register Name: **MCR7**
Register Description: **Master Configuration Register 7**
Register Address: **39h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DIG2F[1:0] | | DIG1F[1:0] | | — | — | DIG2SRC | DIG1SRC |
| Default | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |

**Bits 7 and 6: Digital2 Frequency (DIG2F[1:0]).** This field, MCR6:DIG2SS, and MCR6:DIG2AF configure the frequency of the Digital2 clock synthesizer.

| DIG2AF = 0 | | DIG2AF = 1 | |
|---|---|---|---|
| **DIG2SS = 1** | **DIG2SS = 0** | **DIG2SS = 1** | **DIG2SS = 0** |
| 00 = 1544kHz | 00 = 2048kHz | 00 = 19.44MHz | 00 = 6.312MHz |
| 01 = 3088kHz | 01 = 4096kHz | 01 = 38.88MHz | 01 = undefined |
| 10 = 6176kHz | 10 = 8192kHz | 10 = undefined | 10 = 10MHz |
| 11 = 12,352kHz | 11 = 16,384kHz | 11 = undefined | 11 = undefined |

**Bits 5 and 4: Digital1 Frequency (DIG1F[1:0]).** This field and MCR6:DIG1SS configure the frequency of the Digital1 clock synthesizer.

| DIG1SS = 1 | DIG1SS = 0 |
|---|---|
| 00 = 1544kHz | 00 = 2048kHz |
| 01 = 3088kHz | 01 = 4096kHz |
| 10 = 6176kHz | 10 = 8192kHz |
| 11 = 12,352kHz | 11 = 16,384kHz |

**Bit 1: Digital2 Source (DIG2SRC).** This bit selects which DPLL the Digital2 DFS is connected to. When MCR4:LKT4T0 = 1 it is always connected to the T0 DPLL.

0 = T0 DPLL
1 = T4 DPLL

**Bit 0: Digital1 Source (DIG1SRC).** This bit selects which DPLL the Digital1 DFS is connected to. When MCR4:LKT4T0 = 1 it is always connected to the T0 DPLL.

0 = T0 DPLL
1 = T4 DPLL

Register Name: **MCR8**
Register Description: **Master Configuration Register 8**
Register Address: **3Ah**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | OC5SF[1:0] | | OC4SF[1:0] | | OC7SF[1:0] | | OC6SF[1:0] | |
| Default | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |

For rev A2 devices, in LVPECL mode the differential output voltage is higher than the max $V_{ODPECL}$ spec in Table 10-6 unless an adjustment register is written with the proper value. If differential voltages larger than $V_{ODPECL,MAX}$ are unacceptable, the following procedures must be followed when writing the OCxSF fields in this register. If differential voltages larger than $V_{ODPECL,MAX}$ are acceptable, only the OCxSF field must be written.

Procedure to configure an output for LVPECL mode:

1) Set the OCxSF[1:0] field to 01b.
2) Write 01h to address 01FFh.
3) Write 55h to the adjustment register (see below for address).
4) Write 00h to address 01FFh.

Procedure to configure an output for LVDS mode:

1) Set the OCxSF[1:0] field to 10b.
2) Write 01h to address 01FFh.
3) Write 00h to the adjustment register (see below for address).
4) Write 00h to address 01FFh.

**Bits 7 and 6: Output Clock 5 Signal Format (OC5SF[1:0]).** The adjustment register for OC5 is 01D4h. See Section 7.8.1.

00 = Output disabled (powered down)
01 = 3V LVPECL level compatible
10 = 3V LVDS compatible (default)
11 = 3V LVDS compatible

**Bits 5 and 4: Output Clock 4 Signal Format (OC4SF[1:0]).** The adjustment register for OC4 is 01D0h. See Section 7.8.1.

00 = Output disabled (powered down)
01 = 3V LVPECL level compatible
10 = 3V LVDS compatible (default)
11 = 3V LVDS compatible

**Bits 3 and 2: Output Clock 7 Signal Format (OC7SF[1:0]).** The adjustment register for OC7 is 01DCh. See Section 7.8.1.

00 = Output disabled (powered down)
01 = 3V LVPECL level compatible
10 = 3V LVDS compatible (default)
11 = 3V LVDS compatible

**Bits 1 and 0: Output Clock 6 Signal Format (OC6SF[1:0]).** The adjustment register for OC6 is 01D8h. See Section 7.8.1.

00 = Output disabled (powered down)
01 = 3V LVPECL level compatible
10 = 3V LVDS compatible (default)
11 = 3V LVDS compatible

Register Name: **MCR9**
Register Description: **Master Configuration Register 9**
Register Address: **3Bh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | AUTOBW | — | — | — | LIMINT | — | — | — |
| Default | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 |

**Bit 7: Automatic Bandwidth Selection (AUTOBW).** See Section 7.7.3.

0 = Always selects locked bandwidth from the T0LBW register.
1 = Automatically selects either locked bandwidth (T0LBW register) or acquisition bandwidth (T0ABW register) as appropriate.

**Bit 3: Limit Integral Path (LIMINT).** When this bit is set to 1, the T0 DPLL's integral path is limited (i.e., frozen) when the DPLL reaches minimum or maximum frequency, as set by the HARDLIM field in DLIMIT1 and DLIMIT2. When the integral path is frozen, the current DPLL frequency in registers FREQ1, FREQ2 and FREQ3 is also frozen. Setting LIMINT = 1 minimizes overshoot when the DPLL is pulling in. See Section 7.7.3.

0 = Do not freeze integral path at min/max frequency.
1 = Freeze integral path at min/max frequency.

Register Name: **MCLK1**
Register Description: **Master Clock Frequency Adjustment Register 1**
Register Address: **3Ch**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | MCLKFREQ[7:0] | | | | | | | |
| Default | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |

***Note:*** *The MCLK1 and MCLK2 registers must be read consecutively and written consecutively. See Section 8.3.*

**Bits 7 to 0: Master Clock Frequency Adjustment (MCLKFREQ[7:0]).** The full 16-bit MCLKFREQ[15:0] field spans this register and MCLK2. MCLKFREQ is an unsigned integer that adjusts the frequency of the internal 204.8MHz master clock with respect to the frequency of the local oscillator clock on the REFCLK pin by up to +514ppm and -771ppm. The master clock adjustment has the effect of speeding up the master clock with a positive adjustment and slowing it down with a negative adjustment. For example, if the oscillator connected to REFCLK has an offset of +1ppm, the adjustment should be -1ppm to correct the offset.

The formulas below translate adjustments to register values and vice versa. The default register value of 39,321 corresponds to 0ppm. See Section 7.3.

MCLKFREQ[15:0] = adjustment_in_ppm / 0.0196229 + 39,321

adjustment_in_ppm = (MCLKFREQ[15:0] – 39,321) × 0.0196229

Register Name: **MCLK2**
Register Description: **Master Clock Frequency Adjustment Register 2**
Register Address: **3Dh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | MLCKFREQ[15:8] | | | | | | | |
| Default | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |

**Bits 7 to 0: Master Clock Frequency Adjustment (MCLKFREQ[15:8]).** See the MCLK1 register description.

Register Name: **HOCR1**
Register Description: **Holdover Configuration Register 1**
Register Address: **3Eh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | HOFREQ[7:0] | | | | | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Bits 7 to 0: Holdover Frequency (HOFREQ[7:0]).** The full 19-bit HOFREQ[18:0] field spans this register, HOCR2 and HOCR3. HOFREQ is a two's-complement signed integer, and it expresses the holdover frequency as an offset with respect to the master clock frequency (see Section 7.3). Writing this field sets the T0 DPLL's manual holdover frequency, which is used when MANHO = 1 in the MCR3 register. When HOCR3:RDAVG = 0, reading the HOFREQ field returns the manual holdover value previously written. When RDAVG = 1, reading the HOFREQ field returns the T0 DPLL's averaged frequency, either the fast average (if HOCR3:FAST = 1) or the slow average (if FAST = 0). The HOFREQ field has the same size and format as the FREQ[18:0] field (FREQ1, FREQ2, and FREQ3 registers) to allow software to read FREQ, filter the value, and then write to HOFREQ. Holdover frequency offset in ppm is equal to HOFREQ[18:0] × 0.0003068. See Section 7.7.1.6.

**Note:** After either HOCR3:RDAVG or HOCR3:FAST is changed, system software must wait at least 50µs before reading the corresponding holdover value from the HOFREQ[18:0] field.

Register Name: **HOCR2**
Register Description: **Holdover Configuration Register 2**
Register Address: **3Fh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | HOFREQ[15:8] | | | | | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Bits 7 to 0: Holdover Frequency (HOFREQ[15:8]).** See the HOCR1 register description.

Register Name: **HOCR3**
Register Description: **Holdover Configuration Register 3**
Register Address: **40h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | AVG | FAST | RDAVG | MINIHO[1:0] | | HOFREQ[18:16] | | |
| Default | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |

***Note:*** *See Section 8.3 for important information about writing and reading this register.*

**Bit 7: Averaging (AVG).** When this bit is set to 1 the T0 DPLL uses the averaged frequency value during holdover mode. When MANHO = 1 in the MCR3 register, this bit is ignored. See Section 7.7.1.6.

0 = Not averaged frequency; holdover frequency is either manual (MANHO = 1) or instantaneously frozen
1 = Averaged frequency (averaging rate set by the FAST bit below)

**Bit 6: Fast Averaging (FAST).** This bit controls the averaging rate used in the T0 DPLL's frequency averager. Fast averaging has a -3dB response point of approximately 8 minutes. Slow averaging has a -3dB response point of approximately 110 minutes. See Section 7.7.1.6.

0 = Slow frequency averaging
1 = Fast frequency averaging

**Bit 5: Read Average (RDAVG).** This bit controls which value is accessed when reading the HOFREQ field: the manual holdover frequency or the T0 DPLL's averaged frequency. This allows control software, optionally, to make use of the averager and manual holdover mode in a software-controlled holdover algorithm. See Section 7.7.1.6.

0 = Read the manual holdover frequency value previously written
1 = Read the averaged frequency

**Bits 4 and 3: Mini-Holdover Mode (MINIHO[1:0]).** Mini-holdover is the state of the T0 DPLL where it is in the locked state but has temporarily lost its input. In mini-holdover the DPLL behaves exactly the same as in holdover but with holdover frequency selected as specified by this field. See Section 7.7.1.7.

00 = Frequency determined in the same way as holdover mode
01 = Frequency instantaneously frozen (i.e., as if AVG = 0)
10 = Frequency taken from fast averager (i.e., as if AVG = 1 and FAST = 1)
11 = Frequency taken from slow averager (i.e., as if AVG = 1 and FAST = 0)

**Bits 2 to 0: Holdover Frequency (HOFREQ[18:16]).** See the HOCR1 register description.

Register Name: **DLIMIT1**
Register Description: **DPLL Frequency Limit Register 1**
Register Address: **41h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | HARDLIM[7:0] | | | | | | | |
| Default | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 |

***Note:*** *The DLIMIT1 and DLIMIT2 registers must be read consecutively and written consecutively. See Section 8.3.*

**Bits 7 to 0: DPLL Hard Frequency Limit (HARDLIM[7:0]).** The full 10-bit HARDLIM[9:0] field spans this register and DLIMIT2. HARDLIM is an unsigned integer that specifies the hard frequency limit or pull-in/hold-in range of the T0 DPLL. When frequency limit detection is enabled by setting FLLOL = 1 in the DLIMIT3 register, if the DPLL frequency exceeds the hard limit the DPLL declares loss-of-lock. The hard frequency limit in ppm is ±HARDLIM[9:0] x 0.0782. The default value is normally ±9.2ppm. If external reference switching mode is enabled during reset (see Section 7.6.5), the default value is configured to ±79.794ppm (3FFh). See Section 7.7.6.

Register Name: **DLIMIT2**
Register Description: **DPLL Frequency Limit Register 1**
Register Address: **42h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | — | — | — | — | — | — | HARDLIM[9:8] | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Bits 1 to 0: DPLL Hard Frequency Limit (HARDLIM[9:8]).** See the DLIMIT1 register description.

Register Name: **IER1**
Register Description: **Interrupt Enable Register 1**
Register Address: **43h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | IC8 | — | IC6 | IC5 | IC4 | IC3 | IC2 | IC1 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Bits 7 and 5 to 0: Interrupt Enable for Input Clock Status Change (IC8 and IC[6:1]).** Each of these bits is an interrupt enable control for the corresponding bit in the MSR1 register.

0 = Mask the interrupt
1 = Enable the interrupt

Register Name: **IER2**
Register Description: **Interrupt Enable Register 2**
Register Address: **44h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | STATE | SRFAIL | — | — | — | — | — | IC9 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Bit 7: Interrupt Enable for T0 DPLL State Change (STATE).** This bit is an interrupt enable for the STATE bit in the MSR2 register.

0 = Mask the interrupt
1 = Enable the interrupt

**Bit 6: Interrupt Enable for Selected Reference Failed (SRFAIL).** This bit is an interrupt enable for the SRFAIL bit in the MSR2 register.

0 = Mask the interrupt
1 = Enable the interrupt

**Bit 0: Interrupt Enable for Input Clock Status Change (IC9).** This bit is an interrupt enable control for the IC9 bit in the MSR2 register.

0 = Mask the interrupt
1 = Enable the interrupt

Register Name: **IER3**
Register Description: **Interrupt Enable Register 3**
Register Address: **45h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | FSMON | T4LOCK | PHMON | T4NOIN | — | — | — | — |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Bit 7: Interrupt Enable for Frame-Sync Input Monitor Alarm (FSMON).** This bit is an interrupt enable for the FSMON bit in the MSR3 register.

0 = Mask the interrupt
1 = Enable the interrupt

**Bit 6: Interrupt Enable for the T4 DPLL Lock Status Change (T4LOCK).** This bit is an interrupt enable for the T4LOCK bit in the MSR3 register.

0 = Mask the interrupt
1 = Enable the interrupt

**Bit 5: Interrupt Enable for Phase Monitor Alarm (PHMON).** This bit is an interrupt enable for the PHMON bit in the MSR3 register.

0 = Mask the interrupt
1 = Enable the interrupt

**Bit 4: Interrupt Enable for T4 No Valid Inputs Alarm (T4NOIN).** This bit is an interrupt enable for the T4NOIN bit in the MSR3 register.

0 = Mask the interrupt
1 = Enable the interrupt

Register Name: **DIVN1**
Register Description: **DIVN Register 1**
Register Address: **46h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DIVN[7:0] | | | | | | | |
| Default | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

***Note:*** *The DIVN1 and DIVN2 registers must be read consecutively and written consecutively. See Section 8.3.*

**Bits 7 to 0: DIVN Factor (DIVN[7:0]).** The full 16-bit DIVN[15:0] field spans this register and DIVN2. This field contains the integer value used to divide the frequency of input clocks that are configured for DIVN mode. The frequency is divided by DIVN[15:0] + 1. See Section 7.4.2.4.

Register Name: **DIVN2**
Register Description: **DIVN Register 2**
Register Address: **47h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DIVN[15:8] | | | | | | | |
| Default | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |

**Bits 7 to 0: DIVN Factor (DIVN[15:8]).** See the DIVN1 register description.

Register Name: **MCR10**
Register Description: **Master Configuration Register 10**
Register Address: **48h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | FMONCLK | SRFPIN | UFSW | EXTSW | PBOFRZ | PBOEN | SOFTEN | HARDEN |
| Default | 0 | 0 | 0 | see below | 0 | 1 | 0 | 1 |

**Bit 7: Frequency Monitor Clock Source (FMONCLK).** This bit specifies the clock source for the input clock frequency monitors.

0 = T0 DPLL internal frequency
1 = Internal 204.8MHz master clock

**Bit 6: SRFAIL Pin Enable (SRFPIN).** When this bit is set to 1, the SRFAIL pin is enabled. When enabled the SRFAIL pin follows the state of the SRFAIL status bit in the MSR2 register. This gives the system a very fast indication of the failure of the current reference. See Section 7.5.3.

0 = SRFAIL pin disabled (high impedance)
1 = SRFAIL pin enabled

**Bit 5: Ultra-Fast Switching Mode (UFSW).** See Section 7.6.4.

0 = Disabled
1 = Enabled. The current reference source is disqualified after less than three missing clock cycles.

**Bit 4: External Reference Switching Mode (EXTSW).** This bit enables external reference switching mode. In this mode, if the SRCSW pin is high the T0 DPLL is forced to lock to input IC3 (if the priority of IC3 is nonzero) or IC5 (if the priority of IC3 is zero) whether or not the selected input has a valid reference signal. If the SRCSW pin is low the device is forced to lock to input IC4 (if the priority of IC4 is nonzero) or IC6 (if the priority of IC4 is zero) whether or not the selected input has a valid reference signal. During reset the default value of this bit is latched from the SRCSW pin. This mode only controls the T0 DPLL. The T4 DPLL is not affected. See Section 7.6.5.

0 = Normal operation
1 = External switching mode

**Bit 3: Phase Build-Out Freeze (PBOFRZ).** This bit freezes the current input-output phase relationship and does not allow further phase build-out events to occur. This bit affects phase build-out in response to reference switching (Section 7.7.7.3).

0 = Not frozen
1 = Frozen

**Bit 2: Phase Build-Out Enable (PBOEN).** When this bit is set to 1 a phase build-out event occurs every time the T0 DPLL changes to a new reference, including exiting the holdover and free-run states. When this bit is set to 0, the T0 DPLL locks to the new source with zero degrees of phase difference. See Section 7.7.7.

**Bit 1: Soft Frequency Alarm Enable (SOFTEN).** This bit enables input clock frequency monitoring with the soft alarm limits set in the ILIMIT and SRLIMIT registers. Soft alarms are reported in the SOFT status bits of the ISR registers. See Section 7.5.1.

0 = Disabled
1 = Enabled

**Bit 0: Hard Frequency Limit Enable (HARDEN).** This bit enables input clock frequency monitoring with the hard alarm limits set in the ILIMIT and SRLIMIT registers. Hard alarms are reported in the HARD status bits of the ISR registers. See Section 7.5.1.

0 = Disabled
1 = Enabled

Register Name: **ILIMIT**
Register Description: **Input Clock Frequency Limit Register**
Register Address: **49h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | SOFT[3:0] | | | | HARD[3:0] | | | |
| Default | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 |

**Bits 7 to 4: Soft Frequency Alarm Limit (SOFT[3:0]).** This field is an unsigned integer that specifies the soft frequency alarm limit for all input clocks except the T0 DPLL's selected reference. The soft limit for the selected reference is specified by SRLIMIT:SOFT[3:0]. The soft alarm limit is only used for monitoring; soft alarms do not invalidate input clocks. The limit in ppm is ±(SOFT[3:0] + 1) × 3.81. The default limit is ±11.43ppm. Soft alarms are reported in the SOFT status bits of the ISR registers. See Section 7.5.1.

**Bits 3 to 0: Hard Frequency Alarm Limit (HARD[3:0]).** This field is an unsigned integer that specifies the hard frequency alarm limit for all input clocks except the T0 DPLL's selected reference. The hard limit for the selected reference is specified by SRLIMIT:HARD[3:0]. Hard alarms invalidate input clocks. The limit in ppm is ±(HARD[3:0] + 1) × 3.81. The default limit is ±15.24ppm. Hard alarms are reported in the HARD status bits of the ISR registers. See Section 7.5.1.

Register Name: **SRLIMIT**
Register Description: **Selected Reference Frequency Limit Register**
Register Address: **4Ah**

| Bit# | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | SOFT[3:0] | | | | HARD[3:0] | | | |
| Default | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 |

**Bits 7 to 4: Soft Frequency Alarm Limit (SOFT[3:0]).** This field is an unsigned integer that specifies the soft frequency alarm limit for the T0 DPLL's selected reference. The soft limit for all other input clocks is specified by ILIMIT:SOFT[3:0]. The soft alarm limit is only used for monitoring; soft alarms do not invalidate input clocks. The limit in ppm is ±(SOFT[3:0] + 1) × 3.81. The default limit is ±11.43ppm. Soft alarms are reported in the SOFT status bits of the ISR registers. See Section 7.5.1.

**Bits 3 to 0: Hard Frequency Alarm Limit (HARD[3:0]).** This field is an unsigned integer that specifies the hard frequency alarm limit for the T0 DPLL's selected reference. The hard limit for all other input clocks is specified by ILIMIT:HARD[3:0]. Hard alarms invalidate input clocks. The limit in ppm is ±(HARD[3:0] + 1) × 3.81. The default limit is ±15.24ppm. Hard alarms are reported in the HARD status bits of the ISR registers. See Section 7.5.1.

Register Name: **MCR11**
Register Description: **Master Configuration Register 11**
Register Address: **4Bh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | — | — | — | T4T0 | FMEASIN[3:0] | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Bit 4: T4 or T0 Path Select (T4T0).** This bit specifies which path is being accessed when reads or writes are made to the following registers: PTAB1, PTAB2, FREQ1, FREQ2, FREQ3, IPR1, IPR2, IPR3, IPR4, IPR5, PHASE1, and PHASE2.

0 = T0 path
1 = T4 path

**Bits 3 to 0: Frequency Measurement Input Select (FMEASIN[3:0]).** This field specifies the input clock for the frequency measurement reported in the FMEAS register. See Section 7.5.1.

0000 = {unused value, undefined}
0001 = IC1
0010 = IC2
0011 = IC3
0100 = IC4
0101 = IC5
0110 = IC6
0111 = {unused value, undefined}
1000 = IC8
1001 = IC9
1010–1111 = {unused value, undefined}

Register Name: **FMEAS**
Register Description: **Frequency Measurement Register**
Register Address: **4Ch**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | FMEAS[7:0] | | | | | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Bits 7 to 0: Measured Frequency (FMEAS[7:0]).** This read-only field indicates the measured frequency of the input clock specified in the FMEASIN field of the MCR11 register. FMEAS is a two's-complement signed integer that expresses the frequency as an offset with respect to the frequency monitor clock (either the internal master clock or the output of the T0 DPLL, depending on the setting of the FMONCLK bit in the MCR10 register). The measured frequency is FMEAS[7:0] × 3.81ppm. See Section 7.5.1.

Register Name: **DLIMIT3**
Register Description: **DPLL Frequency Limit Register 3**
Register Address: **4Dh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | FLLOL | SOFTLIM[6:0] | | | | | | |
| Default | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 |

**Bit 7: Frequency Limit Loss-of-Lock (FLLOL).** When this bit is set to 1, the T0 DPLL and the T4 DPLL internally declare loss-of-lock when their hard limits are reached. The T0 DPLL hard frequency limit is set in the HARDLIM[9:0] field in the DLIMIT1 and DLIMIT2 registers. The T4 DPLL hard frequency limit is fixed at ±80ppm. See Section 7.7.6.

0 = DPLL declares loss-of-lock normally.
1 = DPLL also declares loss-of-lock when the hard frequency limit is reached.

**Bits 6 to 0: DPLL Soft Frequency Limit (SOFTLIM[6:0]).** This field is an unsigned integer that specifies the soft frequency limit for the T0 DPLL and the T4 DPLL. The soft limit is only used for monitoring; exceeding this limit does not cause loss-of-lock. The limit in ppm is ±SOFTLIM[6:0] × 0.628. The default value is ±8.79ppm. When the T0 DPLL frequency reaches the soft limit the T0SOFT status bit is set in the OPSTATE register. When the T4 DPLL frequency reaches the soft limit the T4SOFT status bit is set in OPSTATE. See Section 7.7.6.

Register Name: **IER4**
Register Description: **Interrupt Enable Register 4**
Register Address: **4Eh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | FHORDY | SHORDY | — | — | — | — | — | — |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Bit 7: Interrupt Enable for Fast Holdover Frequency Ready (FHORDY).** This bit is an interrupt enable for the FHORDY bit in the MSR4 register.

0 = Mask the interrupt
1 = Enable the interrupt

**Bit 6: Interrupt Enable for Slow Holdover Frequency Ready (SHORDY).** This bit is an interrupt enable for the SHORDY bit in the MSR4 register.

0 = Mask the interrupt
1 = Enable the interrupt

Register Name: **OCR5**
Register Description: **Output Configuration Register 1**
Register Address: **4Fh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | — | AOF7 | AOF6 | AOF5 | AOF4 | AOF3 | AOF2 | AOF1 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Bit 6: Alternate Output Frequency Mode Select 7 (AOF7).** This bit controls the decoding of the OCR4.OFREQ7 field for the OC7 pin.

0 = Standard decodes
1 = Alternate decodes

**Bit 5: Alternate Output Frequency Mode Select 6 (AOF6).** This bit controls the decoding of the OCR3.OFREQ6 field for the OC6 pin.

0 = Standard decodes
1 = Alternate decodes

**Bit 4: Alternate Output Frequency Mode Select 5 (AOF5).** This bit controls the decoding of the OCR3.OFREQ5 field for the OC5 pin.

0 = Standard decodes
1 = Alternate decodes

**Bit 3: Alternate Output Frequency Mode Select 4 (AOF4).** This bit controls the decoding of the OCR2.OFREQ4 field for the OC4 pin.

0 = Standard decodes
1 = Alternate decodes

**Bit 2: Alternate Output Frequency Mode Select 3 (AOF3).** This bit controls the decoding of the OCR2.OFREQ3 field for the OC3 pin.

0 = Standard decodes
1 = Alternate decodes

**Bit 1: Alternate Output Frequency Mode Select 2 (AOF2).** This bit controls the decoding of the OCR1.OFREQ2 field for the OC2 pin.

0 = Standard decodes
1 = Alternate decodes

**Bit 0: Alternate Output Frequency Mode Select 1 (AOF1).** This bit controls the decoding of the OCR1.OFREQ1 field for the OC1 pin.

0 = Standard decodes
1 = Alternate decodes

Register Name: **LB0U**
Register Description: **Leaky Bucket 0 Upper Threshold Register**
Register Address: **50h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | LB0U[7:0] | | | | | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |

**Bits 7 to 0: Leaky Bucket 0 Upper Threshold (LB0U[7:0]).** When the leaky bucket accumulator is equal to the value stored in this field, the activity monitor declares an activity alarm by setting the input clock's ACT bit in the appropriate ISR register. Registers LB0U, LB0L, LB0S, and LB0D together specify leaky bucket configuration 0. See Section 7.5.2.

Register Name: **LB0L**
Register Description: **Leaky Bucket 0 Lower Threshold Register**
Register Address: **51h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | LB0L[7:0] | | | | | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

**Bits 7 to 0: Leaky Bucket 0 Lower Threshold (LB0L[7:0]).** When the leaky bucket accumulator is equal to the value stored in this field, the activity monitoring logic clears the activity alarm (if previously declared) by clearing the input clock's ACT bit in the appropriate ISR register. Registers LB0U, LB0L, LB0S, and LB0D together specify leaky bucket configuration 0. See Section 7.5.2.

Register Name: **LB0S**
Register Description: **Leaky Bucket 0 Size Register**
Register Address: **52h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | LB0S[7:0] | | | | | | | |
| Default | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |

**Bits 7 to 0: Leaky Bucket 0 Size (LB0S[7:0]).** This field specifies the maximum value of the leaky bucket. The accumulator cannot increment past this value. Registers LB0U, LB0L, LB0S, and LB0D together specify leaky bucket configuration 0. See Section 7.5.2.

Register Name: **LB0D**
Register Description: **Leaky Bucket 0 Decay Rate Register**
Register Address: **53h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | — | — | — | — | — | — | LB0D[1:0] | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

**Bits 1 and 0: Leaky Bucket 0 Decay Rate (LB0D[1:0]).** This field specifies the decay or "leak" rate of the leaky bucket accumulator. For each period of 1, 2, 4, or 8 128ms intervals in which no irregularities are detected on the input clock, the accumulator decrements by 1. Registers LB0U, LB0L, LB0S, and LB0D together specify leaky bucket configuration 0. See Section 7.5.2.

00 = decrement every 128ms (8 units/second)
01 = decrement every 256ms (4 units/second)
10 = decrement every 512ms (2 units/second)
11 = decrement every 1024ms (1 unit/second)

Register Name: **LB1U, LB2U, LB3U**
Register Description: **Leaky Bucket 1/2/3 Upper Threshold Register**
Register Address: **54h, 58h, 5Ch**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | LBxU[7:0] | | | | | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |

**Bits 7 to 0: Leaky Bucket "x" Upper Threshold (LBxU[7:0]).** See the LB0U register description.

Registers LB1U, LB1L, LB1S, and LB1D together specify leaky bucket configuration 1.
Registers LB2U, LB2L, LB2S, and LB2D together specify leaky bucket configuration 2.
Registers LB3U, LB3L, LB3S, and LB3D together specify leaky bucket configuration 3.

Register Name: **LB1L, LB2L, LB3L**
Register Description: **Leaky Bucket 1/2/3 Lower Threshold Register**
Register Address: **55h, 59h, 5Dh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | LBxL[7:0] | | | | | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

**Bits 7 to 0: Leaky Bucket "x" Lower Threshold (LBxL[7:0]).** See the LB0L register description.

Registers LB1U, LB1L, LB1S, and LB1D together specify leaky bucket configuration 1.
Registers LB2U, LB2L, LB2S, and LB2D together specify leaky bucket configuration 2.
Registers LB3U, LB3L, LB3S, and LB3D together specify leaky bucket configuration 3.

Register Name: **LB1S, LB2S, LB3S**
Register Description: **Leaky Bucket 1/2/3 Size Register**
Register Address: **56h, 5Ah, 5Eh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | LBxS[7:0] | | | | | | | |
| Default | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |

**Bits 7 to 0: Leaky Bucket "x" Size (LBxS[7:0]).** See the LB0S register description.

Registers LB1U, LB1L, LB1S, and LB1D together specify leaky bucket configuration 1.
Registers LB2U, LB2L, LB2S, and LB2D together specify leaky bucket configuration 2.
Registers LB3U, LB3L, LB3S, and LB3D together specify leaky bucket configuration 3.

Register Name: **LB1D, LB2D, LB3D**
Register Description: **Leaky Bucket 1/2/3 Decay Rate Register**
Register Address: **57h, 5Bh, 5Fh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | — | — | — | — | — | — | LBxD[1:0] | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

**Bits 1 to 0: Leaky Bucket "x" Decay Rate (LBxD[1:0]).** See the LB0D register description.

Registers LB1U, LB1L, LB1S, and LB1D together configure leaky bucket algorithm 1.
Registers LB2U, LB2L, LB2S, and LB2D together configure leaky bucket algorithm 2.
Registers LB3U, LB3L, LB3S, and LB3D together configure leaky bucket algorithm 3.

Register Name: **OCR1**
Register Description: **Output Configuration Register 1**
Register Address: **60h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | OFREQ2[3:0] | | | | OFREQ1[3:0] | | | |
| Default | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

**Bits 7 to 4: Output Frequency of OC2 (OFREQ2[3:0]).** This field specifies the frequency of output clock OC2. The frequencies of the T0 APLL and the T4 APLL are configured in the T0CR1 and T4CR1 registers. The Digital1 and Digital2 frequencies are configured in the MCR7 register. See Section 7.8.2.3. The decode of this field is controlled by the value of the OCR5.AOF2 bit.

AOF2 = 0: (standard decodes)

0000 = Output disabled (i.e., low)
0001 = 2kHz
0010 = 8kHz
0011 = Digital2 (see Table 7-9)
0100 = Digital1 (see Table 7-8)
0101 = T0 APLL frequency divided by 48
0110 = T0 APLL frequency divided by 16
0111 = T0 APLL frequency divided by 12
1000 = T0 APLL frequency divided by 8
1001 = T0 APLL frequency divided by 6
1010 = T0 APLL frequency divided by 4
1011 = T4 APLL frequency divided by 64
1100 = T4 APLL frequency divided by 48
1101 = T4 APLL frequency divided by 16
1110 = T4 APLL frequency divided by 8
1111 = T4 APLL frequency divided by 4

AOF2 = 1: (alternate decodes)

0000 = Output disabled (i.e., low)
0001 = T0 APLL frequency divided by 64
0010 = T4 APLL frequency divided by 20
0011 = T4 APLL frequency divided by 12
0100 = T4 APLL frequency divided by 10
0101 = T4 APLL frequency divided by 5
0110 = T4 APLL frequency divided by 2
0111 = T4 selected reference (after dividing)
1000 = T0 selected reference (after dividing)
1001–1111 = undefined

**Bits 3 to 0: Output Frequency of OC1 (OFREQ1[3:0]).** This field specifies the frequency of output clock OC1. The frequencies of the T0 APLL and T4 APLL are configured in the T0CR1 and T4CR1 registers. The Digital1 and Digital2 frequencies are configured in the MCR7 register. See Section 7.8.2.3. The decode of this field is controlled by the value of the OCR5.AOF1 bit.

AOF1 = 0: (standard decodes)

0000 = Output disabled (i.e., low)
0001 = 2kHz
0010 = 8kHz
0011 = Digital2 (see Table 7-9)
0100 = Digital1 (see Table 7-8)
0101 = T0 APLL frequency divided by 48
0110 = T0 APLL frequency divided by 16
0111 = T0 APLL frequency divided by 12
1000 = T0 APLL frequency divided by 8
1001 = T0 APLL frequency divided by 6

1010 = T0 APLL frequency divided by 4
1011 = T4 APLL frequency divided by 64
1100 = T4 APLL frequency divided by 48
1101 = T4 APLL frequency divided by 16
1110 = T4 APLL frequency divided by 8
1111 = T4 APLL frequency divided by 4

AOF1 = 1: (alternate decodes)

0000 = Output disabled (i.e., low)
0001 = T0 APLL frequency divided by 64
0010 = T4 APLL frequency divided by 20
0011 = T4 APLL frequency divided by 12
0100 = T4 APLL frequency divided by 10
0101 = T0 APLL2 frequency divided by 10
0110 = T0 APLL2 frequency divided by 5
0111 = T4 selected reference (after dividing)
1000 = T0 selected reference (after dividing)
1001–1111 = undefined

Register Name: **OCR2**
Register Description: **Output Configuration Register 2**
Register Address: **61h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | OFREQ4[3:0] | | | | OFREQ3[3:0] | | | |
| Default | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |

**Bits 7 to 4: Output Frequency of OC4 (OFREQ4[3:0]).** This field specifies the frequency of output clock OC4. The frequencies of the T0 APLL and T4 APLL are configured in the T0CR1 and T4CR1 registers. The Digital1 and Digital2 frequencies are configured in the MCR7 register. See Section 7.8.2.3. The decode of this field is controlled by the value of the OCR5.AOF4 bit.

AOF4 = 0: (standard decodes)

0000 = Output disabled (i.e., low)
0001 = 2kHz
0010 = 8kHz
0011 = Digital2 (see Table 7-9)
0100 = Digital1 (see Table 7-8)
0101 = T0 APLL frequency divided by 48
0110 = T0 APLL frequency divided by 16
0111 = T0 APLL frequency divided by 12
1000 = T0 APLL frequency divided by 8
1001 = T0 APLL frequency divided by 6
1010 = T0 APLL frequency divided by 4
1011 = T4 APLL frequency divided by 2
1100 = T4 APLL frequency divided by 48
1101 = T4 APLL frequency divided by 16
1110 = T4 APLL frequency divided by 8
1111 = T4 APLL frequency divided by 4

AOF4 = 1: (alternate decodes)

0000 = Output disabled (i.e., low)
0001 = T0 APLL frequency divided by 2
0010 = T0 APLL frequency
0011 = T4 APLL frequency divided by 10
0100 = T0 APLL2 frequency divided by 10
0101 = T0 APLL2 frequency divided by 2
0110 = T0 APLL2 frequency
0111 = T4 selected reference (after dividing)
1000 = T0 selected reference (after dividing)
1001–1111 = undefined

**Bits 3 to 0: Output Frequency of OC3 (OFREQ3[3:0]).** This field specifies the frequency of output clock OC3. The frequencies of the T0 APLL and T4 APLL are configured in the T0CR1 and T4CR1 registers. The Digital1 and Digital2 frequencies are configured in the MCR7 register. See Section 7.8.2.3.The decode of this field is controlled by the value of the OCR5.AOF3 bit.

AOF3 = 0: (standard decodes)

0000 = Output disabled (i.e., low)
0001 = 2kHz
0010 = 8kHz
0011 = Digital2 (see Table 7-9)
0100 = Digital1 (see Table 7-8)
0101 = T0 APLL frequency divided by 48
0110 = T0 APLL frequency divided by 16
0111 = T0 APLL frequency divided by 12
1000 = T0 APLL frequency divided by 8
1001 = T0 APLL frequency divided by 6

1010 = T0 APLL frequency divided by 4
1011 = T4 APLL frequency divided by 64
1100 = T4 APLL frequency divided by 48
1101 = T4 APLL frequency divided by 16
1110 = T4 APLL frequency divided by 8
1111 = T4 APLL frequency divided by 4

AOF3 = 1: (alternate decodes)

0000 = Output disabled (i.e., low)
0001 = T0 APLL frequency divided by 64
0010 = T4 APLL frequency divided by 20
0011 = T4 APLL frequency divided by 12
0100 = T4 APLL frequency divided by 10
0101 = T4 APLL frequency divided by 5
0110 = T4 APLL frequency divided by 2
0111 = T4 selected reference (after dividing)
1000 = T0 selected reference (after dividing)
1001–1111 = undefined

Register Name: **OCR3**
Register Description: **Output Configuration Register 3**
Register Address: **62h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | OFREQ6[3:0] | | | | OFREQ5[3:0] | | | |
| Default | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

**Bits 7 to 4: Output Frequency of OC6 (OFREQ6[3:0]).** This field specifies the frequency of output clock output OC6. The frequencies of the T0 APLL and T4 APLL are configured in the T0CR1 and T4CR1 registers. The Digital1 and Digital2 frequencies are configured in the MCR7 register. See Section 7.8.2.3. The decode of this field is controlled by the value of the OCR5.AOF6 bit.

AOF6 = 0: (standard decodes)

0000 = Output disabled (i.e., low)
0001 = 2kHz
0010 = 8kHz
0011 = T0 APLL frequency divided by 2
0100 = Digital1 (see Table 7-8)
0101 = T0 APLL frequency
0110 = T0 APLL frequency divided by 16
0111 = T0 APLL frequency divided by 12
1000 = T0 APLL frequency divided by 8
1001 = T0 APLL frequency divided by 6
1010 = T0 APLL frequency divided by 4
1011 = T4 APLL frequency divided by 64
1100 = T4 APLL frequency divided by 48
1101 = T4 APLL frequency divided by 16
1110 = T4 APLL frequency divided by 8
1111 = T4 APLL frequency divided by 4

AOF6 = 1: (alternate decodes)

0000 = Output disabled (i.e., low)
0001 = T4 APLL frequency divided by 5
0010 = T4 APLL frequency divided by 2
0011 = T4 APLL frequency
0100 = T0 APLL2 frequency divided by 5
0101 = T0 APLL2 frequency divided by 2
0110 = T0 APLL2 frequency
0111 = T4 selected reference (after dividing)
1000 = T0 selected reference (after dividing)
1001–1111 = undefined

**Bits 3 to 0: Output Frequency of OC5 (OFREQ5[3:0]).** This field specifies the frequency of output clock OC5. The frequencies of the T0 APLL and T4 APLL are configured in the T0CR1 and T4CR1 registers. The Digital1 and Digital2 frequencies are configured in the MCR7 register. See Section 7.8.2.3. The decode of this field is controlled by the value of the OCR5.AOF5 bit.

AOF5 = 0: (standard decodes)

0000 = Output disabled (i.e., low)
0001 = 2kHz
0010 = 8kHz
0011 = Digital2 (see Table 7-9)
0100 = Digital1 (see Table 7-8)
0101 = T0 APLL frequency divided by 48
0110 = T0 APLL frequency divided by 16
0111 = T0 APLL frequency divided by 12
1000 = T0 APLL frequency divided by 8
1001 = T0 APLL frequency divided by 6

1010 = T0 APLL frequency divided by 4
1011 = T4 APLL frequency divided by 2
1100 = T4 APLL frequency divided by 48
1101 = T4 APLL frequency divided by 16
1110 = T4 APLL frequency divided by 8
1111 = T4 APLL frequency divided by 4

AOF5 = 1: (alternate decodes)

0000 = Output disabled (i.e., low)
0001 = T0 APLL frequency divided by 2
0010 = T0 APLL frequency
0011 = T4 APLL frequency divided by 10
0100 = T0 APLL2 frequency divided by 10
0101 = T0 APLL2 frequency divided by 2
0110 = T0 APLL2 frequency
0111 = T4 selected reference (after dividing)
1000 = T0 selected reference (after dividing)
1001–1111 = undefined

Register Name: **OCR4**
Register Description: **Output Configuration Register 4**
Register Address: **63h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | MFSEN | FSEN | — | — | OFREQ7[3:0] | | | |
| Default | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 |

**Bit 7: MFSYNC Enable (MFSEN).** This configuration bit enables the 2kHz output on the MFSYNC pin. See Section 7.8.2.4.

0 = Disabled, driven low
1 = Enabled, output is 2kHz

**Bit 6: FSYNC Enable (FSEN).** This configuration bit enables the 8kHz output on the FSYNC pin. See Section 7.8.2.4.

0 = Disabled, driven low
1 = Enabled, output is 8kHz

**Bits 3 to 0: Output Frequency of OC7 (OFREQ7[3:0]).** This field specifies the frequency of output clock output OC7. The frequencies of the T0 APLL and T4 APLL are configured in the T0CR1 and T4CR1 registers. The Digital1 and Digital2 frequencies are configured in the MCR7 register. See Section 7.8.2.3. The decode of this field is controlled by the value of the OCR5.AOF7 bit.

AOF7 = 0: (standard decodes)

0000 = Output disabled (i.e., low)
0001 = 2kHz
0010 = 8kHz
0011 = Digital2 (see Table 7-9)
0100 = T0 APLL frequency divided by 2
0101 = T0 APLL frequency divided by 48
0110 = T0 APLL frequency divided by 16
0111 = T0 APLL frequency divided by 12
1000 = T0 APLL frequency divided by 8
1001 = T0 APLL frequency divided by 6
1010 = T0 APLL frequency divided by 4
1011 = T4 APLL frequency divided by 64
1100 = T4 APLL frequency divided by 48
1101 = T4 APLL frequency divided by 16
1110 = T4 APLL frequency divided by 8
1111 = T4 APLL frequency divided by 4

AOF7 = 1: (alternate decodes)

0000 = Output disabled (i.e., low)
0001 = T4 APLL frequency divided by 5
0010 = T4 APLL frequency divided by 2
0011 = T4 APLL frequency
0100 = T0 APLL2 frequency divided by 5
0101 = T0 APLL2 frequency divided by 2
0110 = T0 APLL2 frequency
0111 = T4 selected reference (after dividing)
1000 = T0 selected reference (after dividing)
1001–1111 = undefined

Register Name: **T4CR1**
Register Description: **T4 DPLL Configuration Register 1**
Register Address: **64h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | — | — | — | — | T4FREQ[3:0] | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

**Bits 3 to 0: T4 APLL Frequency (T4FREQ[3:0]).** When T0CR1:T4APT0 = 0, the T4 APLL DFS is connected to the T4 DPLL, and this field configures the T4 APLL DFS frequency. The T4 APLL DFS frequency affects the frequency of the T4 APLL which in turn affects the available output frequencies on the output clock pins (see the OCR registers). See Section 7.8.2.

| T4FREQ[3:0] | T4 APLL DFS FREQUENCY | T4 APLL FREQUENCY (4 x T4 APLL DFS) |
|---|---|---|
| 0000 | APLL output disabled | Disabled, output is low |
| 0001 | 77.76MHz | 311.04MHz (4 x 77.76MHz) |
| 0010 | 24.576MHz (12 x E1) | 98.304MHz (48 x E1) |
| 0011 | 32.768MHz (16 x E1) | 131.072MHz (64 x E1) |
| 0100 | 37.056MHz (24 x DS1) | 148.224MHz (96 x DS1) |
| 0101 | 24.704MHz (16 x DS1) | 98.816MHz (64 x DS1) |
| 0110 | 68.736MHz (2 x E3) | 274.944MHz (8 x E3) |
| 0111 | 44.736MHz (DS3) | 178.944MHz (4 x DS3) |
| 1000 | 25.248MHz (4 x 6312kHz) | 100.992MHz (16 x 6312kHz) |
| 1001 | 62.500MHz (GbE ÷ 16) | 250.000MHz (GbE ÷ 4) |
| 1010 | 30.720MHz (3 x 10.24) | 122.880MHz (12 x 10.24) |
| 1011 | 40.000MHz (4 x 10MHz) | 160.000MHz (16 x 10MHz) |
| 1100 | 26.000MHz (2 x 13MHz) | 104.000MHz (8 x 13MHz) |
| 1101–1111 | {unused values} | {unused values} |

Register Name: **T0CR1**
Register Description: **T0 DPLL Configuration Register 1**
Register Address: **65h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | T4MT0 | T4APT0 | T0FT4[2:0] | | | T0FREQ[2:0] | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

**Bit 7: T4 Measure T0 Phase (T4MT0).** When this bit is set to 1 the T4 DPLL goes to the free-run mode, and the T4 phase detector is configured to measure the phase difference between the selected T0 DPLL input clock and the selected the T4 DPLL input clock. See Section 7.7.10.

0 = Normal operation for the T4 path.
1 = Enable T4-measure-T0-phase mode.

**Bit 6: T4 APLL Source from T0 (T4APT0).** When this bit is set to 0, the T4 APLL DFS is connected to the T4 DPLL, and T4CR1:T4FREQ configures the T4 APLL DFS frequency. The T4 APLL DFS frequency affects the frequency of the T4 APLL, which, in turn, affects the available output frequencies on the output clock pins (see the OCR registers). When this bit is set to 1, the T4 APLL DFS is connected to the T0 DPLL rather than the T4 DPLL, and the frequency of the T4 APLL DFS is configured by the T0CR1:T0FT4[2:0] field below. See Section 7.8.2.

0 = T4 APLL locks to T4 DPLL.
1 = T4 APLL locks to T0 DPLL.

**Bits 5 to 3: T0 Frequency to T4 APLL (T0FT4[2:0]).** When the T4APT0 bit is set to 1, this field specifies the frequency of the T4 APLL DFS. This frequency can be different than the frequency specified by T0CR1:T0FREQ. See Section 7.8.2.

| T0FT4 | T4 APLL DFS FREQUENCY | T4 APLL FREQUENCY (4 x T4 APLL DFS) |
|---|---|---|
| 000 = | 24.576MHz (12 x E1) | 98.304MHz (48 x E1) |
| 001 = | 62.500MHz (GbE ÷ 16) | 250.000MHz (GbE ÷ 4) |
| 010 = | 32.768MHz (16 x E1) | 131.072MHz (64 x E1) |
| 011 = | {unused value} | {unused value} |
| 100 = | 37.056MHz (24 x DS1) | 148.224MHz (96 x DS1) |
| 101 = | {unused value} | {unused value} |
| 110 = | 24.704MHz (16 x DS1) | 98.816MHz (64 x DS1) |
| 111 = | 25.248MHz (4 x 6312kHz) | 100.992MHz (16 x 6312kHz) |

**Bits 2 to 0: T0 DPLL Output Frequency (T0FREQ[2:0]).** This field configures the T0 APLL DFS frequency. The T0 APLL DFS frequency affects the frequency of the T0 APLL, which in turn affects the available output frequencies on the output clock pins (see the OCR registers). See Section 7.8.2.

| T0FREQ | T0 APLL DFS FREQUENCY | T0 APLL FREQUENCY (4 x T0 APLL DFS) |
|---|---|---|
| 000 = | 77.76MHz | 311.04MHz (4 x 77.76MHz) |
| 001 = | 77.76MHz | 311.04MHz (4 x 77.76MHz) |
| 010 = | 24.576MHz (12 x E1) | 98.304MHz (48 x E1) |
| 011 = | 32.768MHz (16 x E1) | 131.072MHz (64 x E1) |
| 100 = | 37.056MHz (24 x DS1) | 148.224MHz (96 x DS1) |
| 101 = | 24.704MHz (16 x DS1) | 98.816MHz (64 x DS1) |
| 110 = | 25.248MHz (4 x 6312kHz) | 100.992MHz (16 x 6312kHz) |
| 111 = | 62.500MHz (GbE ÷ 16) | 250.000MHz (GbE ÷ 4) |

Register Name: **T4BW**
Register Description: **T4 Bandwidth Register**
Register Address: **66h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | 0 | 0 | 0 | 0 | 0 | 0 | T4BW[1:0] | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Bits 2 to 0: T4 DPLL Bandwidth (T4BW[2:0]).** See Section 7.7.3.

00 = 18Hz
01 = 35Hz
10 = 70Hz
11 = {unused value, undefined}

Register Name: **T0LBW**
Register Description: **T0 DPLL Locked Bandwidth Register**
Register Address: **67h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | — | — | — | T0LBW[4:0] | | | | |
| Default | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 |

**Bits 4 to 0: T0 DPLL Locked Bandwidth (T0LBW[4:0]).** This field configures the bandwidth of the T0 DPLL when locked to an input clock. When AUTOBW = 0 in the MCR9 register, the T0LBW bandwidth is used for acquisition and for locked operation. When AUTOBW = 1, T0ABW bandwidth is used for acquisition while T0LBW bandwidth is used for locked operation. See Section 7.7.3.

00000 = 0.5mHz
00001 = 1mHz
00010 = 2mHz
00011 = 4mHz
00100 = 8mHz
00101 = 15mHz
00110 = 30mHz
00111 = 60mHz
01000 = 0.1Hz
01001 = 0.3Hz
01010 = 0.6Hz
01011 = 1.2Hz
01100 = 2.5Hz
01101 = 4Hz (default)
01110 = 8Hz
01111 = 18Hz
10000 = 35Hz
10001 = 70Hz
10010 = 120Hz
10011 = 250Hz
10100 = 400Hz
10101–11111 = unused

Register Name: **T0ABW**
Register Description: **T0 DPLL Acquisition Bandwidth Register**
Register Address: **69h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | — | — | — | T0ABW[4:0] | | | | |
| Default | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |

**Bits 4 to 0: T0 DPLL Acquisition Bandwidth (T0ABW[4:0]).** This field configures the bandwidth of the T0 DPLL when acquiring lock. When AUTOBW = 0 in the MCR9 register, the T0LBW bandwidth is used for acquisition and for locked operation. When AUTOBW = 1, T0ABW bandwidth is used for acquisition while T0LBW bandwidth is used for locked operation. See Section 7.7.3.

00000 = 0.5mHz
00001 = 1mHz
00010 = 2mHz
00011 = 4mHz
00100 = 8mHz
00101 = 15mHz
00110 = 30mHz
00111 = 60mHz
01000 = 0.1Hz
01001 = 0.3Hz
01010 = 0.6Hz
01011 = 1.2Hz
01100 = 2.5Hz
01101 = 4Hz
01110 = 8Hz
01111 = 18Hz (default)
10000 = 35Hz
10001 = 70Hz
10010 = 120Hz
10011 = 250Hz
10100 = 400Hz
10101–11111 = unused

Register Name: **T4CR2**
Register Description: **T4 Configuration Register 2**
Register Address: **6Ah**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | — | PD2G8K[2:0] | | | — | DAMP[2:0] | | |
| Default | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 |

**Bits 6 to 4: Phase Detector 2 Gain 8kHz (PD2GA8K[2:0]).** This field specifies the gain of the T4 phase detector 2 with an input clock of 8kHz or less. This value is only used if automatic gain selection is enabled by setting PD2EN = 1 in the T4CR3 register. See Section 7.7.5.

**Bits 2 to 0: Damping Factor (DAMP[2:0]).** This field configures the damping factor of the T4 DPLL. Damping factor is a function of both DAMP[2:0] and the T4 DPLL bandwidth (T4BW register). The default value corresponds to a damping factor of 5. See Section 7.7.4.

| | **18Hz** | **35Hz** | **≥ 70Hz** |
|---|---|---|---|
| 001 = | 1.2 | 1.2 | 1.2 |
| 010 = | 2.5 | 2.5 | 2.5 |
| 011 = | 5 | 5 | 5 |
| 100 = | 5 | 10 | 10 |
| 101 = | 5 | 10 | 20 |
| 000, 110, and 111 = | {unused values} | | |

The gain peak for each damping factor is shown below:

| **DAMPING FACTOR** | **GAIN PEAK (dB)** |
|---|---|
| 1.2 | 0.4 |
| 2.5 | 0.2 |
| 5 | 0.1 |
| 10 | 0.06 |
| 20 | 0.03 |

Register Name: **T0CR2**
Register Description: **T0 Configuration Register 2**
Register Address: **6Bh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | — | PD2G8K[2:0] | | | — | DAMP[2:0] | | |
| Default | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 |

**Bits 6 to 4: Phase Detector 2 Gain, 8kHz (PD2G8K[2:0]).** This field specifies the gain of the T0 phase detector 2 with an input clock of 8kHz or less. This value is only used if automatic gain selection is enabled by setting PD2EN = 1 in the T0CR3 register. See Section 7.7.5.

**Bits 2 to 0: Damping Factor (DAMP[2:0]).** This field configures the damping factor of the T0 DPLL. Damping factor is a function of both DAMP[2:0] and the T0 DPLL bandwidth (T0ABW and T0LBW). The default value corresponds to a damping factor of 5. See Section 7.7.4.

| | **≤ 4Hz** | **8Hz** | **18Hz** | **35Hz** | **≥ 70Hz** |
|---|---|---|---|---|---|
| 001 = | 5 | 2.5 | 1.2 | 1.2 | 1.2 |
| 010 = | 5 | 5 | 2.5 | 2.5 | 2.5 |
| 011 = | 5 | 5 | 5 | 5 | 5 |
| 100 = | 5 | 5 | 5 | 10 | 10 |
| 101 = | 5 | 5 | 5 | 10 | 20 |
| 000, 110, and 111 = | {unused values} | | | | |

The gain peak for each damping factor is shown below:

| **DAMPING FACTOR** | **GAIN PEAK (dB)** |
|---|---|
| 1.2 | 0.4 |
| 2.5 | 0.2 |
| 5 | 0.1 |
| 10 | 0.06 |
| 20 | 0.03 |

Register Name: **T4CR3**
Register Description: **T4 Configuration Register 3**
Register Address: **6Ch**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | PD2EN | — | — | — | — | PD2G[2:0] | | |
| Default | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 |

**Bit 7: Phase Detector 2 Gain Enable (PD2EN).** When this bit is set to 1, the T4 phase detector 2 is enabled and the gain is determined by the input locking frequency. If the frequency is greater than 8kHz, the gain is set by the PD2G field. If the frequency is less or equal to 8kHz, the gain is set by the PD2G8K field in the T4CR2 register. See Section 7.7.5.

0 = Disable
1 = Enable

**Bits 2 to 0: Phase Detector 2 Gain (PD2G[2:0]).** This field specifies the gain of the T4 phase detector 2 when the input frequency is greater than 8kHz. This value is only used if automatic gain selection is enabled by setting PD2EN = 1. See Section 7.7.5.

Register Name: **T0CR3**
Register Description: **T0 Configuration Register 3**
Register Address: **6Dh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | PD2EN | — | — | — | — | PD2G[2:0] | | |
| Default | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 |

**Bit 7: Phase Detector 2 Gain Enable (PD2EN).** When this bit is set to 1, the T0 phase detector 2 is enabled and the gain is determined by the input locking frequency. If the frequency is greater than 8kHz, the gain is set by the PD2G field. If the frequency is less or equal to 8kHz, the gain is set by the PD2G8K field in the T0CR2 register. See Section 7.7.5.

0 = Disable
1 = Enable

**Bits 2 to 0: Phase Detector 2 Gain (PD2G[2:0]).** This field specifies the gain of the T0 phase detector 2 when the input frequency is greater than 8kHz. This value is only used if automatic gain selection is enabled by setting PD2EN = 1. See Section 7.7.5.

Register Name: **GPCR**
Register Description: **GPIO Configuration Register**
Register Address: **6Eh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | GPIO4D | GPIO3D | GPIO2D | GPIO1D | GPIO4O | GPIO3O | GPIO2O | GPIO1O |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Bit 7: GPIO4 Direction (GPIO4D).** This bit configures the data direction for the GPIO4 pin. When GPIO4 is an input, its current state can be read from GPSR:GPIO4. When GPIO4 is an output, its value is controlled by the GPIO4O configuration bit.

0 = Input
1 = Output

**Bit 6: GPIO3 Direction (GPIO3D).** This bit configures the data direction for the GPIO3 pin. When GPIO3 is an input, its current state can be read from GPSR:GPIO3. When GPIO3 is an output, its value is controlled by the GPIO3O configuration bit.

0 = Input
1 = Output

**Bit 5: GPIO2 Direction (GPIO2D).** This bit configures the data direction for the GPIO2 pin. When GPIO2 is an input, its current state can be read from GPSR:GPIO2. When GPIO2 is an output, its value is controlled by the GPIO2O configuration bit.

0 = Input
1 = Output

**Bit 4: GPIO1 Direction (GPIO1D).** This bit configures the data direction for the GPIO1 pin. When GPIO1 is an input, its current state can be read from GPSR:GPIO1. When GPI13 is an output, its value is controlled by the GPIO1O configuration bit.

0 = Input
1 = Output

**Bit 3: GPIO4 Output Value (GPIO4O).** When GPIO4 is configured as an output (GPIO4D = 1), this bit specifies the output value.

0 = Low
1 = High

**Bit 2: GPIO3 Output Value (GPIO3O).** When GPIO3 is configured as an output (GPIO3D = 1), this bit specifies the output value.

0 = Low
1 = High

**Bit 1: GPIO2 Output Value (GPIO2O).** When GPIO2 is configured as an output (GPIO2D = 1), this bit specifies the output value.

0 = Low
1 = High

**Bit 0: GPIO1 Output Value (GPIO1O).** When GPIO1 is configured as an output (GPIO1D = 1), this bit specifies the output value.

0 = Low
1 = High

Register Name: **GPSR**
Register Description: **GPIO Status Register**
Register Address: **6Fh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | — | — | — | — | GPIO4 | GPIO3 | GPIO2 | GPIO1 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Bit 3: GPIO4 State (GPIO4).** This bit indicates the current state of the GPIO4 pin.

0 = Low
1 = High

**Bit 2: GPIO3 State (GPIO3).** This bit indicates the current state of the GPIO3 pin.

0 = Low
1 = High

**Bit 2: GPIO2 State (GPIO2).** This bit indicates the current state of the GPIO2 pin.

0 = Low
1 = High

**Bit 1: GPIO1 State (GPIO1).** This bit indicates the current state of the GPIO1 pin.

0 = Low
1 = High

Register Name: **OFFSET1**
Register Description: **Phase Offset Register 1**
Register Address: **70h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | OFFSET[7:0] | | | | | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

***Note:*** *The OFFSET1 and OFFSET2 registers must be read consecutively and written consecutively. See Section 8.3.*

**Bits 7 to 0: Phase Offset (OFFSET[7:0]).** The full 16-bit OFFSET[15:0] field spans this register and the OFFSET2 register. OFFSET is a two's-complement signed integer that specifies the desired phase offset between the output clocks and the selected input reference. The phase offset in picoseconds is equal to OFFSET[15:0] × actual_internal_clock_period / $2^{11}$. If the internal clock is at its nominal frequency of 77.76MHz, the phase offset equation simplifies to OFFSET[15:0] × 6.279ps. If, however, the DPLL is locked to a reference whose frequency is +1ppm from ideal, for example, then the actual internal clock period is 1ppm shorter and the phase offset is 1ppm smaller. When the OFFSET field is written, the phase of the output clocks is automatically ramped to the new offset value to avoid loss of synchronization. To adjust the phase offset without changing the phase of the output clocks, use the recalibration process enabled by FSCR3:RECAL. The OFFSET field is ignored when phase build-out is enabled (PBOEN = 1 in the MCR10 register) and when the DPLL is not locked. See Section 7.7.8.

Register Name: **OFFSET2**
Register Description: **Phase Offset Register 2**
Register Address: **71h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | OFFSET[15:8] | | | | | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Bits 7 to 0: Phase Offset (OFFSET[15:8]).** See the OFFSET1 register description.

Register Name: **PBOFF**
Register Description: **Phase Build-Out Offset Register**
Register Address: **72h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | — | — | PBOFF[5:0] | | | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Bits 5 to 0: Phase Build-Out Offset Register (PBOFF[5:0]).** An uncertainty of up to 5ns is introduced each time a phase build-out event occurs. This uncertainty results in a phase hit on the output. Over a large number of phase build-out events the mean error should be zero. The PBOFF field specifies a fixed offset for each phase build-out event to skew the average error toward zero. This field is a two's-complement signed integer. The offset in nanoseconds is PBOFF[5:0] × 0.101. Values greater than 1.4ns or less than -1.4ns can cause internal math errors and should not be used. See Section 7.7.7.4.

Register Name: **PHLIM1**
Register Description: **Phase Limit Register 1**
Register Address: **73h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | FLEN | NALOL | 1 | — | — | FINELIM[2:0] | | |
| Default | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |

**Bit 7: Fine Phase Limit Enable (FLEN).** This configuration bit enables the fine phase limit specified in the FINELIM[2:0] field. The fine limit must be disabled for multi-UI jitter tolerance (see PHLIM2 fields). This field controls both T0 and T4. See Section 7.7.6.

0 = Disabled
1 = Enabled

**Bit 6: No Activity Loss-of-Lock (NALOL).** The T0 and the T4 DPLLs can detect that an input clock has no activity very quickly (within two clock cycles). When NALOL = 0, loss-of-lock is not declared when clock cycles are missing, and nearest edge locking (±180°) is used when the clock recovers. This gives tolerance to missing cycles. When NALOL = 1, loss-of-lock is indicated as soon as no activity is detected, and the device switches to phase/frequency locking (±360°). This field controls both T0 and T4. See Sections 7.5.3 and 7.7.6.

0 = No activity does not trigger loss-of-lock.
1 = No activity does trigger loss-of-lock.

**Bit 5:** Leave set to 1 (test control).

**Bits 2 to 0: Fine Phase Limit (FINELIM[2:0]).** This field specifies the fine phase limit window, outside of which loss-of-lock is declared. The FLEN bit enables this feature. The phase of the input clock has to be inside the fine limit window for two seconds before phase lock is declared. Loss-of-lock is declared immediately if the phase of the input clock is outside the phase limit window. The default value of 010 is appropriate for most situations. This field controls both T0 and T4. See Section 7.7.6.

000 = Always indicates loss-of-phase lock—do not use
001 = Small phase limit window, ±45° to ±90°
010 = Normal phase limit window, ±90° to ±180° (default)
100, 101, 110, 111 = Proportionately larger phase limit window

Register Name: **PHLIM2**
Register Description: **Phase Limit Register 2**
Register Address: **74h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | CLEN | MCPDEN | USEMCPD | — | COARSELIM[3:0] | | | |
| Default | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

**Bit 7: Coarse Phase Limit Enable (CLEN).** This configuration bit enables the coarse phase limit specified in the COARSELIM[3:0] field. This field controls both T0 and T4. See Section 7.7.6.

0 = Disabled
1 = Enabled

**Bit 6: Multicycle Phase Detector Enable (MCPDEN).** This configuration bit enables the multicycle phase detector and allows the DPLL to tolerate large-amplitude jitter and wander. The range of this phase detector is the same as the coarse phase limit specified in the COARSELIM[3:0] field. This field controls both T0 and T4. See Section 7.7.5.

0 = Disabled
1 = Enabled

**Bit 5: Use Multicycle Phase Detector in the DPLL Algorithm (USEMCPD).** This configuration bit enables the DPLL algorithm to use the multicycle phase detector so that a large phase measurement drives faster DPLL pull-in. When USEMCPD = 0, phase measurement is limited to ±360°, giving slower pull-in at higher frequencies but with less overshoot. When USEMCPD = 1, phase measurement is set as specified in the COARSELIM[3:0] field, giving faster pull-in. MCPDEN should be set to 1 when USEMCPD = 1. This field controls both T0 and T4. See Section 7.7.5.

0 = Disabled
1 = Enabled

**Bits 3 to 0: Coarse Phase Limit (COARSELIM[3:0]).** This field specifies the coarse phase limit and the tracking range of the multicycle phase detector. The CLEN bit enables this feature. If jitter tolerance greater than 0.5UI is required and the input clock is a high-frequency signal, the DPLL can be configured to track phase errors over many UI using the multicycle phase detector. This field controls both T0 and T4. See Section 7.7.5 and 7.7.6.

0000 = ±1UI
0001 = ±3UI
0010 = ±7UI
0011 = ±15UI
0100 = ±31UI
0101 = ±63UI
0110 = ±127UI
0111 = ±255UI
1000 = ±511UI
1001 = ±1023UI
1010 = ±2047UI
1011 = ±4095UI
1100–1111 = ±8191UI

Register Name: **PHMON**
Register Description: **Phase Monitor Register**
Register Address: **76h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | NW | — | PMEN | PMPBEN | PMLIM[3:0] | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |

**Bit 7: Low-Frequency Input Clock Noise Window (NW).** For 2kHz, 4kHz, or 8kHz input clocks, this configuration bit enables a ±5% tolerance noise window centered around the expected clock edge location. Noise-induced edges outside this window are ignored, reducing the possibility of phase hits on the output clocks. This only applies to the T0 DPLL and should be enabled only when the T0 DPLL is locked to an input and the 180° phase detector is being used (TEST1.D180=0).

0 = All edges are recognized by the T0 DPLL.
1 = Only edges within the ±5% tolerance window are recognized by the T0 DPLL.

**Bit 5: Phase Monitor Enable (PMEN).** This configuration bit enables the phase monitor, which measures the phase error between the input clock reference and the DPLL output. When the DPLL is set for low bandwidth, a phase transient on the input causes an immediate phase error that is gradually reduced as the DPLL tracks the input. When the measured phase error exceeds the limit set in the PMLIM field, the phase monitor declares a phase monitor alarm by setting MSR3:PHMON. See Section 7.7.7.

0 = Disabled
1 = Enabled

**Bit 4: Phase Monitor to Phase Build-Out Enable (PMPBEN).** This bit enables phase build-out in response to phase hits on the selected reference. See Section 7.7.7.

0 = Phase monitor alarm does not trigger a phase build-out event
1 = Phase monitor alarm does trigger a phase build-out event

**Bits 3 to 0: Phase Monitor Limit (PMLIM[3:0]).** This field is an unsigned integer that specifies the magnitude of phase error that causes a phase monitor alarm to be declared (PHMON bit in the MSR3 register). The phase monitor limit in nanoseconds is equal to (PMLIM[3:0] + 7) * 156.25, which corresponds to a range of 1094 ns to 3437 ns in 156.25 ns steps. The phase monitor is enabled by setting PMEN=1. See Section 7.7.7.

Register Name: **PHASE1**
Register Description: **Phase Register 1**
Register Address: **77h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | PHASE[7:0] | | | | | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

***Note:*** *The PHASE1 and PHASE2 registers must be read consecutively. See Section 8.3.*

**Bits 7 to 0: Current DPLL Phase (PHASE[7:0]).** The full 16-bit PHASE[15:0] field spans this register and the PHASE2 register. PHASE is a two's-complement signed integer that indicates the current value of the phase detector. The value is the output of the phase averager. When T4T0 = 0 in the MCR11 register, PHASE indicates the current phase of the T0 DPLL. When T4T0 = 1, PHASE indicates the current phase of the T4 DPLL. The averaged phase difference in degrees is equal to PHASE × 0.707. See Section 7.7.10.

Register Name: **PHASE2**
Register Description: **Phase Register 2**
Register Address: **78h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | PHASE[15:8] | | | | | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Bits 7 to 0: Current DPLL Phase (PHASE[15:8]).** See the PHASE1 register description.

Register Name: **PHLKTO**
Register Description: **Phase-Lock Timeout Register**
Register Address: **79h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | PHLKTOM[1:0] | | PHLKTO[5:0] | | | | | |
| Default | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |

**Bits 7 and 6: Phase-Lock Timeout Multiplier (PHLKTOM[1:0]).** This field is an unsigned integer that specifies the resolution of the phase-lock timeout field PHLKTO[5:0].

00 = 2 seconds
01 = 4 seconds
10 = 8 seconds
11 = 16 seconds

**Bits 5 to 0: Phase-Lock Timeout (PHLKTO[5:0]).** This field is an unsigned integer that, together with the PHLKTOM[1:0] field, specifies the length of time that the T0 DPLL attempts to lock to an input clock before declaring a phase-lock alarm (by setting the corresponding LOCK bit in the ISR registers). The timeout period in seconds is PHLKTO[5:0] × 2^(PHLKTOM[1:0] + 1). The state machine remains in the prelocked, prelocked 2, or phase-lost modes for the specified time before declaring a phase alarm on the selected input. See Section 7.7.1.

Register Name: **FSCR1**
Register Description: **Frame-Sync Configuration Register 1**
Register Address: **7Ah**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | 2K8KSRC | SYNCSRC[2:0] | | | 8KINV | 8KPUL | 2KINV | 2KPUL |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Bit 7: 2kHz/8kHz Source (2K8KSRC).** This configuration bit specifies the source for the 2kHz and 8kHz outputs available on clock outputs. When MCR4:LKT4T0 = 1 it is always connected to the T0 DPLL. See Section 7.8.2.3.

0 = T0 DPLL
1 = T4 DPLL

**Bits 6 to 4: SYNC12 Source (SYNCSRC[2:0]).** When external frame sync is configured for SYNC123 mode, this field specifies the input clocks to associate with the SYNC1 and SYNC2 pins. SYNC3 is always associated with input clock IC9 in this mode. See Section 7.9.2.1.

0XX = SYNC1 pin associated with IC3 or IC5, SYNC2 pin associated with IC4 or IC6, SYC3 pin associated with IC9 or IC2
1X0 = SYNC1 pin associated with IC3, SYNC2 pin associated with IC4
1X1 = SYNC1 pin associated with IC5, SYNC2 pin associated with IC6
10X = SYNC3 pin associated with IC9
11X = SYNC3 pin associated with IC2

**Bit 3: 8kHz Invert (8KINV).** When this bit is set to 1 the 8kHz signal on clock output FSYNC is inverted. See Section 7.8.2.4.

0 = FSYNC not inverted
1 = FSYNC inverted

**Bit 2: 8kHz Pulse (8KPUL).** When this bit is set to 1, the 8kHz signal on clock output FSYNC is pulsed rather than 50% duty cycle. In this mode output clock OC3 must be enabled, and the pulse width of FSYNC is equal to the clock period of OC3. See Section 7.8.2.4.

0 = FSYNC not pulsed; 50% duty cycle
1 = FSYNC pulsed, with pulse width equal to OC3 period

**Bit 1: 2kHz Invert (2KINV).** When this bit is set to 1 the 2kHz signal on clock output MFSYNC is inverted. See Section 7.8.2.4.

0 = MFSYNC not inverted
1 = MFSYNC inverted

**Bit 0: 2kHz Pulse (2KPUL).** When this bit is set to 1, the 2kHz signal on clock output MFSYNC is pulsed rather than 50% duty cycle. In this mode output clock OC3 must be enabled, and the pulse width of MFSYNC is equal to the clock period of OC3. See Section 7.8.2.4.

0 = MFSYNC not pulsed; 50% duty cycle
1 = MFSYNC pulsed, with pulse width equal to OC3 period

Register Name: **FSCR2**
Register Description: **Frame-Sync Configuration Register 2**
Register Address: **7Bh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | INDEP | OCN | PHASE3[1:0] | | PHASE2[1:0] | | PHASE1[1:0] | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Bit 7: Independent Frame Sync and Multiframe Sync (INDEP).** When this bit is set to 0, the 8kHz frame sync on FSYNC and the 2kHz multiframe sync on MFSYNC are aligned with the other output clocks when synchronized with the SYNCn input. When this bit is 1, the frame sync and multiframe sync are independent of the other output clocks, and their edge position may change without disturbing the other output clocks. See Section 7.9.2.5.

0 = FSYNC and MFSYNC are aligned with other output clocks; all are synchronized by the SYNCn input.
1 = FSYNC and MFSYNC are independent of the other clock outputs; only FSYNC and MFSYNC are synchronized by the SYNCn input.

**Bit 6: Sync OC-N Rates (OCN).** See Section 7.9.2.3.

0 = SYNCn is sampled with a 6.48MHz resolution; the selected reference must be 6.48MHz.
1 = If the selected reference is 19.44MHz, SYNCn is sampled at 19.44MHz and output alignment is sampled at 19.44MHz. If the selected reference is 38.88MHz, SYNCn is sampled at 38.88MHz. The selected reference must be either 19.44MHz or 38.88MHz.

**Bits 5 and 4: External Sync-Sampling Phase 3 (PHASE3[1:0]).** This field adjusts the sampling of the SYNC3 input pin. Normally the falling edge of SYNC3 is aligned with the falling edge of the selected reference. All UI numbers listed below are UI of the sampling clock. See Section 7.9.2.2.

00 = Coincident
01 = 0.5UI early
10 = 1UI late
11 = 0.5UI late

**Bits 3 and 2: External Sync-Sampling Phase 2 (PHASE2[1:0]).** This field adjusts the sampling of the SYNC2 input pin. Normally the falling edge of SYNC2 is aligned with the falling edge of the selected reference. All UI numbers listed below are UI of the sampling clock. See Section 7.9.2.2.

00 = Coincident
01 = 0.5UI early
10 = 1UI late
11 = 0.5UI late

**Bits 1 and 0: External Sync-Sampling Phase 1 (PHASE1[1:0]).** This field adjusts the sampling of the SYNC1 input pin. Normally the falling edge of SYNC1 is aligned with the falling edge of the selected reference. All UI numbers listed below are UI of the sampling clock. See Section 7.9.2.2.

00 = Coincident
01 = 0.5UI early
10 = 1UI late
11 = 0.5UI late

Register Name: **FSCR3**
Register Description: **Frame-Sync Configuration Register 3**
Register Address: **7Ch**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | RECAL | MONLIM[2:0] | | | SOURCE[3:0] | | | |
| Default | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 |

**Bit 7: Phase Offset Recalibration (RECAL).** When set to 1, this configuration bit causes a recalibration of the phase offset between the output clocks and the selected reference. This process puts the DPLL into mini holdover, internally ramps the phase offset to zero, resets all clock dividers, ramps the phase offset to the value stored in the OFFSET registers, and then switches the DPLL out of mini holdover. Unlike simply writing the OFFSET registers, the RECAL process causes no change in the phase offset of the output clocks. RECAL is automatically reset to 0 when recalibration is complete. See Section 7.7.8.

0 = Normal operation
1 = Phase offset recalibration

**Bits 6 to 4: Sync Monitor Limit (MONLIM[2:0]).** This field configures the sync monitor limit. When the external frame-sync input is misaligned with respect to the MFSYNC output by the specified number of resampling clock cycles, a frame-sync monitor alarm is declared in the FSMON bit of the OPSTATE register. See Section 7.9.2.6.

000 = ± 1UI
001 = ± 2UI
010 = ± 3UI
011 = ± 4UI
100 = ± 5UI
101 = ± 6UI
110 = ± 7UI
111 = ± 8UI

**Bits 3 to 0: External Frame-Sync Reference Source (SOURCE[3:0]).** When external frame sync is configured for SYNC1 automatic mode, this field specifies the input clock to associate with the SYNC1 pin. See Section 7.9.2.1.

0000 = IC1
0010 = IC2
0011 = IC3
0100 = IC4
0101 = IC5
0110 = IC6
0111 = {unused value, undefined}
1000 = IC8
1001 = IC9
1010–1011 = {unused values, undefined}
11XX = SYNC123 mode

Register Name: **INTCR**
Register Description: **Interrupt Configuration Register**
Register Address: **7Dh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | — | — | — | — | LOS | GPO | OD | POL |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

**Bit 3: INTREQ Pin Mode (LOS).** When GPO = 0, this bit selects the function of the INTREQ pin.

0 = The INTREQ/LOS pin indicates interrupt requests.
1 = The INTREQ/LOS pin indicates the real-time state of the selected reference activity monitor (see Section 7.5.3). This function is most useful when external switching mode (Section 7.6.5) is enabled (MCR10:EXTSW = 1).

**Bit 2: INTREQ Pin General-Purpose Output Enable (GPO).** When set to 1, this bit configures the interrupt request pin to be a general-purpose output whose value is set by the POL bit.

0 = INTREQ is function determined by the LOS bit.
1 = INTREQ is a general-purpose output.

**Bit 1: INTREQ Pin Open-Drain Enable (OD)**

When GPO = 0:
0 = INTREQ is driven in both inactive and active states.
1 = INTREQ is driven high or low in the active state but is high impedance in the inactive state.
When GPO = 1:
0 = INTREQ is driven as specified by POL.
1 = INTREQ is high impedance and POL has no effect.

**Bit 0: INTREQ Pin Polarity (POL)**

When GPO = 0:
0 = INTREQ goes low to signal an interrupt request or LOS = 1 (active low).
1 = INTREQ goes high to signal interrupt request or LOS = 1 (active high).
When GPO = 1:
0 = INTREQ driven low.
1 = INTREQ driven high.

Register Name: **PROT**
Register Description: **Protection Register**
Register Address: **7Eh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | PROT[7:0] | | | | | | | |
| Default | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

**Bits 7 to 0: Protection Control (PROT[7:0]).** This field can be used to protect the rest of the register set from inadvertent writes. In protected mode writes to all other registers are ignored. In single unprotected mode, one register (other than PROT) can be written, but after that write the device reverts to protected mode (and the value of PROT is internally changed to 00h). In fully unprotected mode all register can be written without limitation. See Section 7.2.

1000 0101 = Fully unprotected mode
1000 0110 = Single unprotected mode

All other values = Protected mode

# 9. JTAG Test Access Port and Boundary Scan

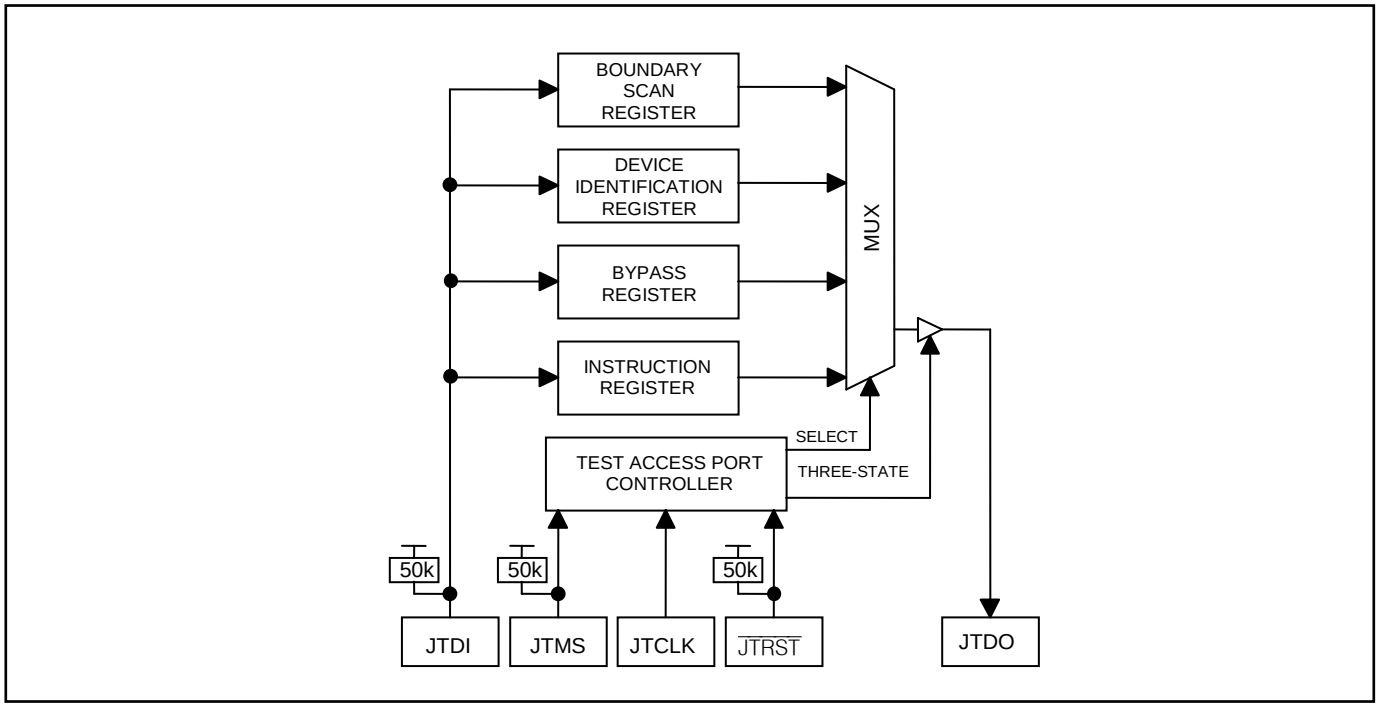
## 9.1 JTAG Description

The DS3102 supports the standard instruction codes SAMPLE/PRELOAD, BYPASS, and EXTEST. Optional public instructions included are HIGHZ, CLAMP, and IDCODE. Figure 9-1 shows a block diagram. The DS3102 contains the following items, which meet the requirements set by the IEEE 1149.1 Standard Test Access Port and Boundary Scan Architecture:

| | |
|---|---|
| Test Access Port (TAP) | Bypass Register |
| TAP Controller | Boundary Scan Register |
| Instruction Register | Device Identification Register |

The TAP has the necessary interface pins, namely JTCLK, $\overline{\text{JTRST}}$, JTDI, JTDO, and JTMS. Details on these pins can be found in Table 6-5. Details about the boundary scan architecture and the TAP can be found in IEEE 1149.1-1990, IEEE 1149.1a-1993, and IEEE 1149.1b-1994.

*Figure 9-1. JTAG Block Diagram*



## 9.2 JTAG TAP Controller State Machine Description

This section discusses the operation of the TAP controller state machine. The TAP controller is a finite state machine that responds to the logic level at JTMS on the rising edge of JTCLK. Each of the states denoted in Figure 9-2 is described in the following paragraphs.

**Test-Logic-Reset.** Upon device power-up, the TAP controller starts in the Test-Logic-Reset state. The instruction register contains the IDCODE instruction. All system logic on the device operates normally.

**Run-Test-Idle.** Run-Test-Idle is used between scan operations or during specific tests. The instruction register and all test registers remain idle.

**Select-DR-Scan.** All test registers retain their previous state. With JTMS low, a rising edge of JTCLK moves the controller into the Capture-DR state and initiates a scan sequence. JTMS high moves the controller to the Select-IR-SCAN state.

**Capture-DR.** Data can be parallel-loaded into the test register selected by the current instruction. If the instruction does not call for a parallel load or the selected test register does not allow parallel loads, the register remains at its current value. On the rising edge of JTCLK, the controller goes to the Shift-DR state if JTMS is low or to the Exit1-DR state if JTMS is high.

**Shift-DR.** The test register selected by the current instruction is connected between JTDI and JTDO and data is shifted one stage toward the serial output on each rising edge of JTCLK. If a test register selected by the current instruction is not placed in the serial path, it maintains its previous state.

**Exit1-DR.** While in this state, a rising edge on JTCLK with JTMS high puts the controller in the Update-DR state, which terminates the scanning process. A rising edge on JTCLK with JTMS low puts the controller in the Pause-DR state.

**Pause-DR.** Shifting of the test registers is halted while in this state. All test registers selected by the current instruction retain their previous state. The controller remains in this state while JTMS is low. A rising edge on JTCLK with JTMS high puts the controller in the Exit2-DR state.

**Exit2-DR.** While in this state, a rising edge on JTCLK with JTMS high puts the controller in the Update-DR state and terminates the scanning process. A rising edge on JTCLK with JTMS low puts the controller in the Shift-DR state.

**Update-DR.** A falling edge on JTCLK while in the Update-DR state latches the data from the shift register path of the test registers into the data output latches. This prevents changes at the parallel output because of changes in the shift register. A rising edge on JTCLK with JTMS low puts the controller in the Run-Test-Idle state. With JTMS high, the controller enters the Select-DR-Scan state.

**Select-IR-Scan.** All test registers retain their previous state. The instruction register remains unchanged during this state. With JTMS low, a rising edge on JTCLK moves the controller into the Capture-IR state and initiates a scan sequence for the instruction register. JTMS high during a rising edge on JTCLK puts the controller back into the Test-Logic-Reset state.

**Capture-IR.** The Capture-IR state is used to load the shift register in the instruction register with a fixed value. This value is loaded on the rising edge of JTCLK. If JTMS is high on the rising edge of JTCLK, the controller enters the Exit1-IR state. If JTMS is low on the rising edge of JTCLK, the controller enters the Shift-IR state.

**Shift-IR.** In this state, the instruction register's shift register is connected between JTDI and JTDO and shifts data one stage for every rising edge of JTCLK toward the serial output. The parallel register and the test registers remain at their previous states. A rising edge on JTCLK with JTMS high moves the controller to the Exit1-IR state. A rising edge on JTCLK with JTMS low keeps the controller in the Shift-IR state, while moving data one stage through the instruction shift register.

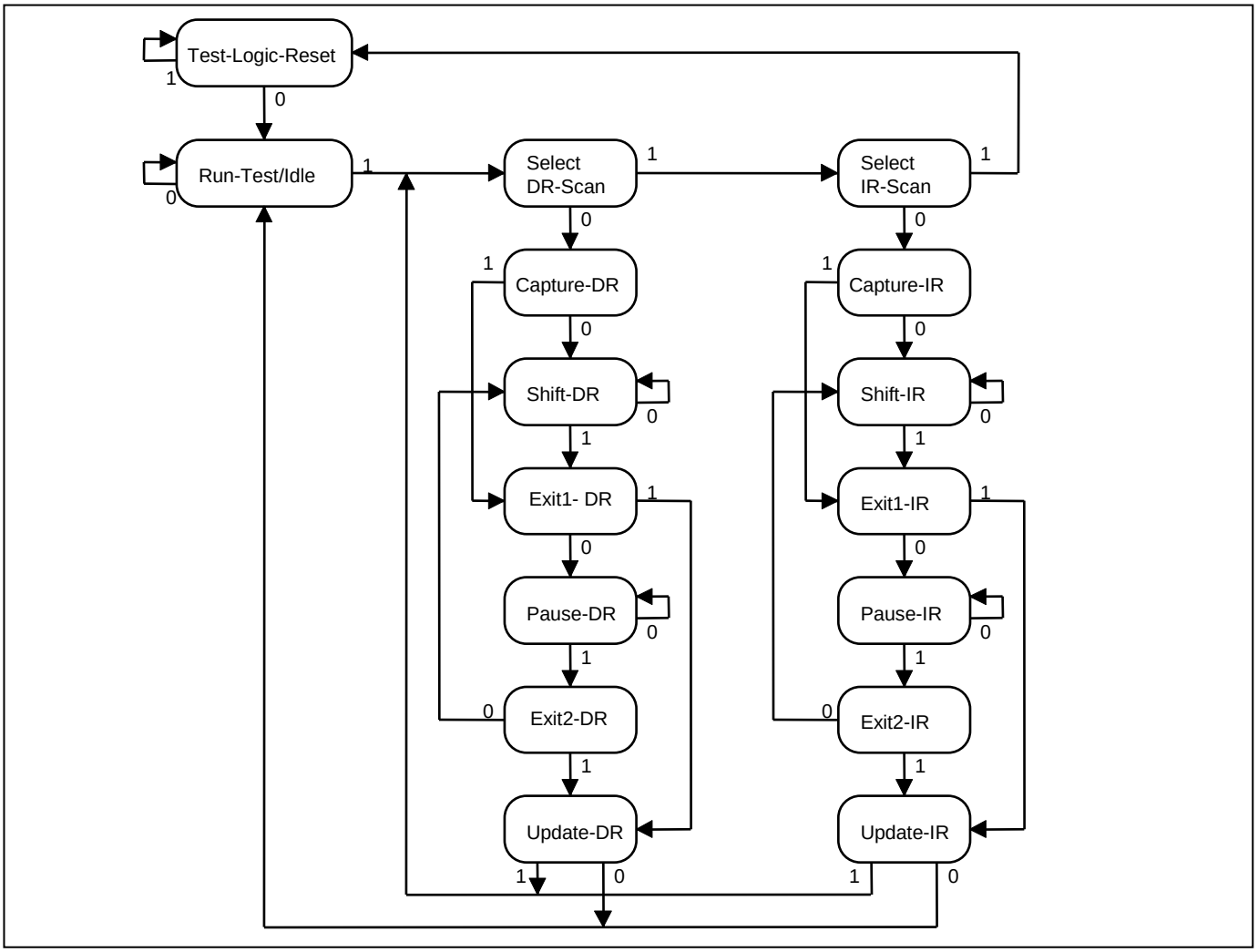
**Exit1-IR.** A rising edge on JTCLK with JTMS low puts the controller in the Pause-IR state. If JTMS is high on the rising edge of JTCLK, the controller enters the Update-IR state and terminates the scanning process.

**Pause-IR.** Shifting of the instruction register is halted temporarily. With JTMS high, a rising edge on JTCLK puts the controller in the Exit2-IR state. The controller remains in the Pause-IR state if JTMS is low during a rising edge on JTCLK.

**Exit2-IR.** A rising edge on JTCLK with JTMS high puts the controller in the Update-IR state. The controller loops back to the Shift-IR state if JTMS is low during a rising edge of JTCLK in this state.

**Update-IR.** The instruction shifted into the instruction shift register is latched into the parallel output on the falling edge of JTCLK as the controller enters this state. Once latched, this instruction becomes the current instruction. A rising edge on JTCLK with JTMS low puts the controller in the Run-Test-Idle state. With JTMS high, the controller enters the Select-DR-Scan state.

*Figure 9-2. JTAG TAP Controller State Machine*



## 9.3 JTAG Instruction Register and Instructions

The instruction register contains a shift register as well as a latched parallel output and is 3 bits in length. When the TAP controller enters the Shift-IR state, the instruction shift register is connected between JTDI and JTDO. While in the Shift-IR state, a rising edge on JTCLK with JTMS low shifts data one stage toward the serial output at JTDO. A rising edge on JTCLK in the Exit1-IR state or the Exit2-IR state with JTMS high moves the controller to the Update-IR state. The falling edge of that same JTCLK latches the data in the instruction shift register to the instruction parallel output. Table 9-1 shows the instructions supported by the DS3102 and their respective operational binary codes.

### Table 9-1. JTAG Instruction Codes

| INSTRUCTIONS | SELECTED REGISTER | INSTRUCTION CODES |
|---|---|---|
| SAMPLE/PRELOAD | Boundary Scan | 010 |
| BYPASS | Bypass | 111 |
| EXTEST | Boundary Scan | 000 |
| CLAMP | Bypass | 011 |
| HIGHZ | Bypass | 100 |
| IDCODE | Device Identification | 001 |

**SAMPLE/PRELOAD.** SAMPLE/RELOAD is a mandatory instruction for the IEEE 1149.1 specification. This instruction supports two functions. First, the digital I/Os of the device can be sampled at the boundary scan register, using the Capture-DR state, without interfering with the device's normal operation. Second, data can be shifted into the boundary scan register through JTDI using the Shift-DR state.

**EXTEST.** EXTEST allows testing of the interconnections to the device. When the EXTEST instruction is latched in the instruction register, the following actions occur: (1) Once the EXTEST instruction is enabled through the Update-IR state, the parallel outputs of the digital output pins are driven. (2) The boundary scan register is connected between JTDI and JTDO. (3) The Capture-DR state samples all digital inputs into the boundary scan register.

**BYPASS.** When the BYPASS instruction is latched into the parallel instruction register, JTDI is connected to JTDO through the 1-bit bypass register. This allows data to pass from JTDI to JTDO without affecting the device's normal operation.

**IDCODE.** When the IDCODE instruction is latched into the parallel instruction register, the device identification register is selected. The device ID code is loaded into the device identification register on the rising edge of JTCLK, following entry into the Capture-DR state. Shift-DR can be used to shift the ID code out serially through JTDO. During Test-Logic-Reset, the ID code is forced into the instruction register's parallel output.

**HIGHZ.** All digital outputs are placed into a high-impedance state. The bypass register is connected between JTDI and JTDO.

**CLAMP.** All digital output pins output data from the boundary scan parallel output while connecting the bypass register between JTDI and JTDO. The outputs do not change during the CLAMP instruction.

## 9.4 JTAG Test Registers

IEEE 1149.1 requires a minimum of two test registers—the bypass register and the boundary scan register. An optional test register, the identification register, has been included in the device design. It is used with the IDCODE instruction and the Test-Logic-Reset state of the TAP controller.

**Bypass Register.** This is a single 1-bit shift register used with the BYPASS, CLAMP, and HIGHZ instructions to provide a short path between JTDI and JTDO.

**Boundary Scan Register.** This register contains a shift register path and a latched parallel output for control cells and digital I/O cells. The BSDL file is available on the DS3102 page of Microsemi's website.

**Identification Register.** This register contains a 32-bit shift register and a 32-bit latched parallel output. It is selected during the IDCODE instruction and when the TAP controller is in the Test-Logic-Reset state. The device identification code for the DS3102 is shown in Table 9-2.

### Table 9-2. JTAG ID Code

| DEVICE | REVISION | DEVICE CODE | MANUFACTURER CODE | REQUIRED |
|---|---|---|---|---|
| DS3102 | Consult factory | 0000000010100000 | 00010100001 | 1 |

# 10. Electrical Characteristics

## ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin with Respect to $V_{SS}$ (except $V_{DD}$)……..-0.3V to +5.5V
Supply Voltage Range ($V_{DD}$) with Respect to $V_{SS}$……..-0.3V to +1.98V
Supply Voltage Range ($V_{DDIO}$) with Respect to $V_{SS}$……-0.3V to +3.63V
Ambient Operating Temperature Range……..-40°C to +85°C (Note 1)
Junction Operating Temperature Range……..-40°C to +125°C
Storage Temperature Range……..-55°C to +125°C
Soldering Temperature (reflow)
Lead(Pb)-free ..... +260°C
Containing lead(Pb)..... +240°C

**Note 1:** Specifications to -40°C are guaranteed by design and not production tested.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to the absolute maximum rating conditions for extended periods may affect device. Ambient operating temperature range when device is mounted on a four-layer JEDEC test board with no airflow.*

**Note:** The typical values listed in the tables of Section 10 are not production tested.

## 10.1 DC Characteristics

### Table 10-1. Recommended DC Operating Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Supply Voltage, Core | $V_{DD}$ | | 1.62 | 1.8 | 1.98 | V |
| Supply Voltage, I/O | $V_{DDIO}$ | | 3.135 | 3.3 | 3.465 | V |
| Ambient Temperature Range | $T_A$ | | -40 | | +85 | °C |
| Junction Temperature Range | $T_J$ | | -40 | | +125 | °C |

### Table 10-2. DC Characteristics

($V_{DD}$ = 1.8V ±10%; $V_{DDIO}$ = 3.3V ±5%, $T_A$ = -40°C to +85°C)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Supply Current, Core | $I_{DD}$ | (Notes 2, 3) | | 153 | 192 | mA |
| Supply Current, I/O | $I_{DDIO}$ | (Notes 2, 3) | | 41 | 52 | mA |
| Supply Current from VDD_OC45 When Outputs OC4 and OC5 Enabled | $I_{DDOC45}$ | (Note 4) | | 16 | | mA |
| Supply Current from VDD_OC67 When Outputs OC6 and OC7 Enabled | $I_{DDOC67}$ | (Note 4) | | 16 | | mA |
| Input Capacitance | $C_{IN}$ | | | 5 | | pF |
| Output Capacitance | $C_{OUT}$ | | | 7 | | pF |

**Note 2:** 12.800MHz clock applied to REFCLK and 19.44MHz clock applied to one CMOS/TTL input clock pin. One 19.44MHz CMOS/TTL output clock pin driving 100pF load; all other inputs at $V_{DDIO}$ or grounded; all other outputs disabled and open.

**Note 3:** TYP current measured at $V_{DD}$ = 1.8V and $V_{DDIO}$ = 3.3V, MAX current measured at $V_{DD}$ = 1.98V and $V_{DDIO}$ = 3.465V.

**Note 4:** 19.44MHz output clock frequency, driving the load shown in Figure 10-1. Enabled means MCR8:OcxSF ≠ 00.

## Table 10-3. CMOS/TTL Pins

($V_{DD}$ = 1.8V ±10%; $V_{DDIO}$ = 3.3V ±5%, $T_A$ = -40°C to +85°C)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Input High Voltage | $V_{IH}$ | | 2.0 | | 5.5 | V |
| Input Low Voltage | $V_{IL}$ | | -0.3 | | +0.8 | V |
| Input Leakage | $I_{IL}$ | (Note 1) | -10 | | +10 | µA |
| Input Leakage, Pins with Internal Pullup Resistor (50kΩ typ) | $I_{ILPU}$ | (Note 1) | -100 | | +10 | µA |
| Input Leakage, Pins with Internal Pulldown Resistor (50kΩ typ) | $I_{ILPD}$ | (Note 1) | -10 | | +100 | µA |
| Output Leakage (when High-Z) | $I_{LO}$ | (Note 1) | -10 | | +10 | µA |
| Output High Voltage ($I_O$ = -4.0mA) | $V_{OH}$ | | 2.4 | | $V_{DDIO}$ | V |
| | | (Note 2) | 2.0 | | $V_{DDIOB}$ | V |
| Output Low Voltage ($I_O$ = +4.0mA) | $V_{OL}$ | | 0 | | 0.4 | V |

**Note 1:** 0V < $V_{IN}$ < $V_{DDIO}$ for all other digital inputs.

**Note 2:** For OC1B to OC5B when $V_{DDIOB}$ = 2.5V.

## Table 10-4. LVDS/LVPECL Input Pins

($V_{DD}$ = 1.8V ±10%; $V_{DDIO}$ = 3.3V ±5%, $T_A$ = -40°C to +85°C)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Input Voltage Tolerance | $V_{TOL}$ | (Note 1) | 0 | | $V_{DDIO}$ | V |
| Input Voltage Range | $V_{IN}$ | $V_{ID}$ = 100mV | 0 | | 2.4 | V |
| Input Differential Voltage | $V_{ID}$ | | 0.1 | | 1.4 | V |
| Input Differential Logic Threshold | $V_{IDTH}$ | | -100 | | +100 | mV |

**Note 1:** The device can tolerate this range of voltages w.r.t. $V_{SS}$ on its ICxPOS and ICxNEG pins without being damaged. Proper operation of the differential input circuitry is only guaranteed when the other specifications in this table are met.

## Table 10-5. LVDS Output Pins

($V_{DD}$ = 1.8V ±10%; $V_{DDIO}$ = 3.3V ±5%, $T_A$ = -40°C to +85°C)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Output High Voltage | $V_{OHLVDS}$ | (Note 1) | | | 1.6 | V |
| Output Low Voltage | $V_{OLLVDS}$ | (Note 1) | 0.9 | | | V |
| Differential Output Voltage | $V_{ODLVDS}$ | | 247 | 350 | 454 | mV |
| Output Offset (Common Mode) Voltage | $V_{OSLVDS}$ | +25°C (Note 1) | 1.125 | 1.25 | 1.375 | V |
| Difference in Magnitude of Output Differential Voltage for Complementary States | $V_{DOSLVDS}$ | | | | 25 | mV |

**Note 1:** With 100Ω load across the differential outputs.

**Note 2:** The differential outputs can easily be interfaced to LVDS, LVPECL, and CML inputs on neighboring ICs using a few external passive components. See App Note HFAN-1.0 for details.

## Table 10-6. LVPECL Level-Compatible Output Pins

($V_{DD}$ = 1.8V ±10%; $V_{DDIO}$ = 3.3V ±5%, $T_A$ = -40°C to +85°C)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Differential Output Voltage | $V_{ODPECL}$ | | 595 | 700 | 930 | mV |
| Output Offset (Common Mode) Voltage | $V_{OSPECL}$ | +25°C (Note 1) | | 0.8 | | V |
| Difference in Magnitude of Output Differential Voltage for Complementary States | $V_{DOSPECL}$ | | | | 50 | mV |

**Note 1:** With 100Ω load across the differential outputs.

**Note 2:** The differential outputs can easily be interfaced to LVDS, LVPECL, and CML inputs on neighboring ICs using a few external passive components. See App Note HFAN-1.0 for details.

*Figure 10-1. Recommended Termination for LVDS Pins*

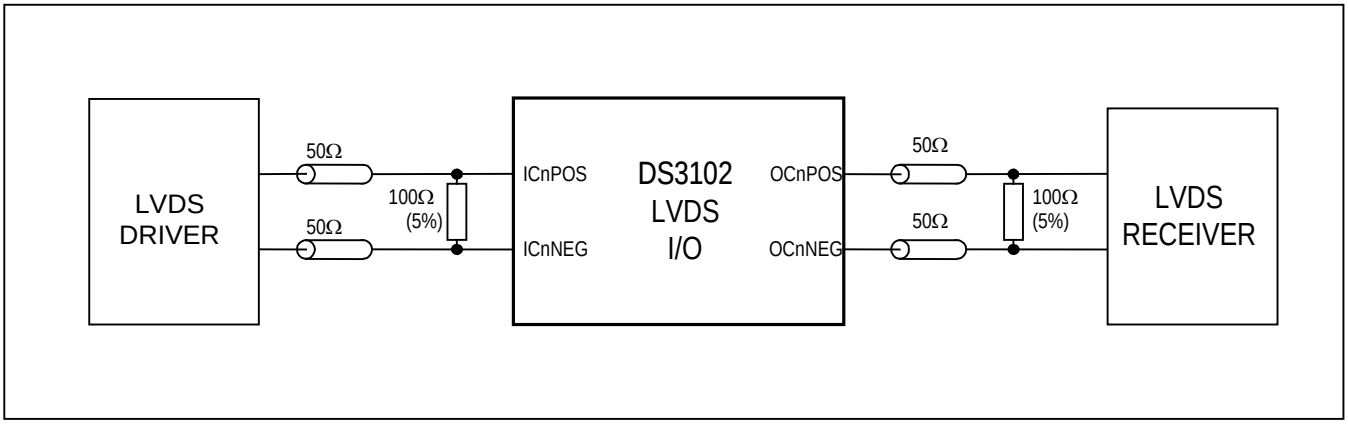



*Figure 10-2. Recommended Termination for LVPECL Signals on LVDS Input Pins*

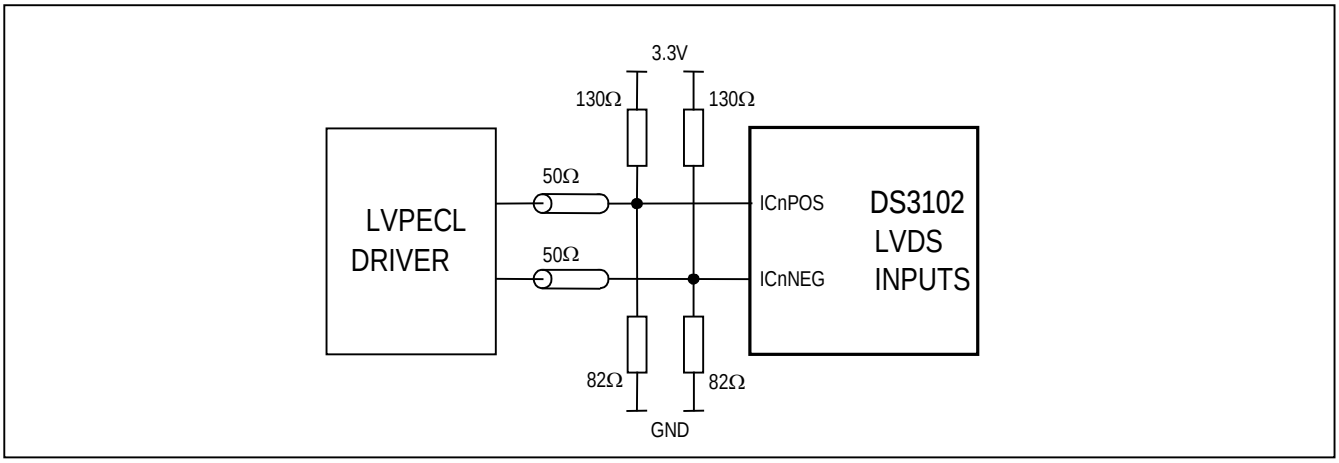
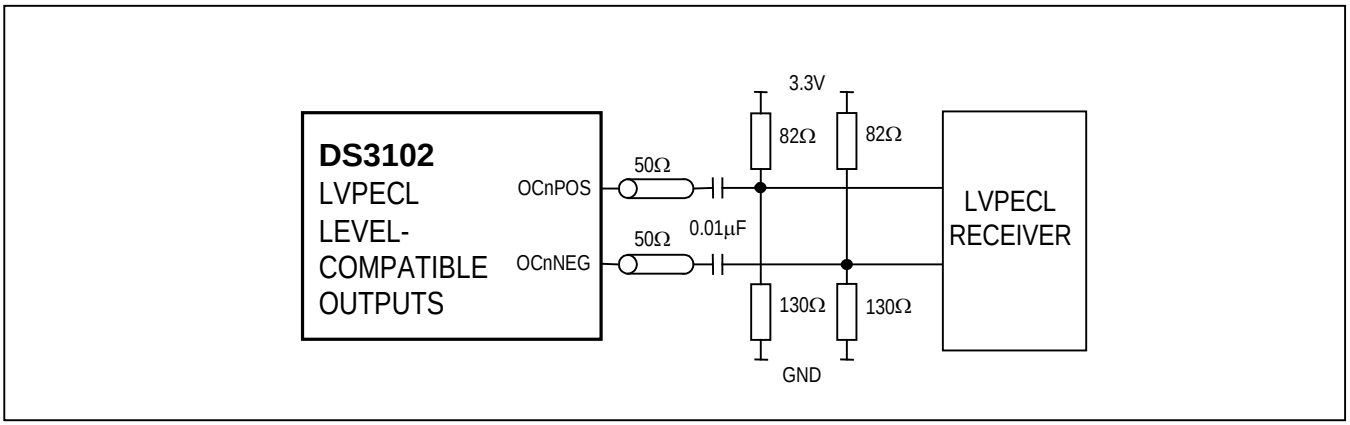


*Figure 10-3. Recommended Termination for LVPECL-Compatible Output Pins*



## 10.2 Input Clock Timing

### Table 10-7. Input Clock Timing

($V_{DD}$ = 1.8V ±10%; $V_{DDIO}$ = 3.3V ±5%, $T_A$ = -40°C to +85°C.)

| PARAMETER | | SYMBOL | MIN | TYP | MAX |
|---|---|---|---|---|---|
| Input Clock Period | CMOS/TTL Input Pins | $t_{CYC}$ | 8ns (125MHz) | | 500µs (2kHz) |
| | LVDS/LVPECL Input Pins | | 6.4ns (156.25MHz) | | 500µs (2kHz) |
| Input Clock High, Low Time | | $t_H$, $t_L$ | 3ns or 30% of $t_{CYC}$, whichever is smaller | | |

## 10.3 Output Clock Timing

### Table 10-8. Input Clock to Output Clock Delay

| INPUT FREQUENCY | OUTPUT FREQUENCY | INPUT CLOCK EDGE TO OUTPUT CLOCK EDGE DELAY (ns) |
|---|---|---|
| 8kHz | 8kHz | 0 ± 1.5 |
| 6.48MHz | 6.48MHz | 0 ± 1.5 |
| 19.44MHz | 19.44MHz | 0 ± 1.5 |
| 25.92MHz | 25.92MHz | 0 ± 1.5 |
| 38.88MHz | 38.88MHz | 0 ± 1.5 |
| 51.84MHz | 51.84MHz | 0 ± 1.5 |
| 77.76MHz | 77.76MHz | 0 ± 1.5 |
| 155.52MHz | 155.52MHz | 0 ± 1.5 |

### Table 10-9. Output Clock Phase Alignment, Frame-Sync Alignment Mode

| OUTPUT FREQUENCY | MFSYNC FALLING EDGE TO OUTPUT CLOCK FALLING EDGE DELAY (ns) |
|---|---|
| 8kHz (FSYNC) | 0 ± 0.5 |
| 2kHz | 0 ± 0.5 |
| 8kHz | 0 ± 0.5 |
| 1.544MHz | 0 ± 1.25 |
| 2.048MHz | 0 ± 1.25 |
| 44.736MHz | -2.0 ± 1.25 |
| 34.368MHz | -2.0 ± 1.25 |
| 6.48MHz | -2.0 ± 1.25 |
| 19.44MHz | -2.0 ± 1.25 |
| 25.92MHz | -2.0 ± 1.25 |
| 38.88MHz | -2.0 ± 1.25 |
| 51.84MHz | -2.0 ± 1.25 |
| 77.76MHz | -2.0 ± 1.25 |
| 155.52MHz | -2.0 ± 1.25 |
| 311.04MHz | -2.0 ± 1.25 |

See Section 7.9.2 for details on frame-sync alignment and the SYNC[1:3] pins.

## 10.4 SPI Interface Timing

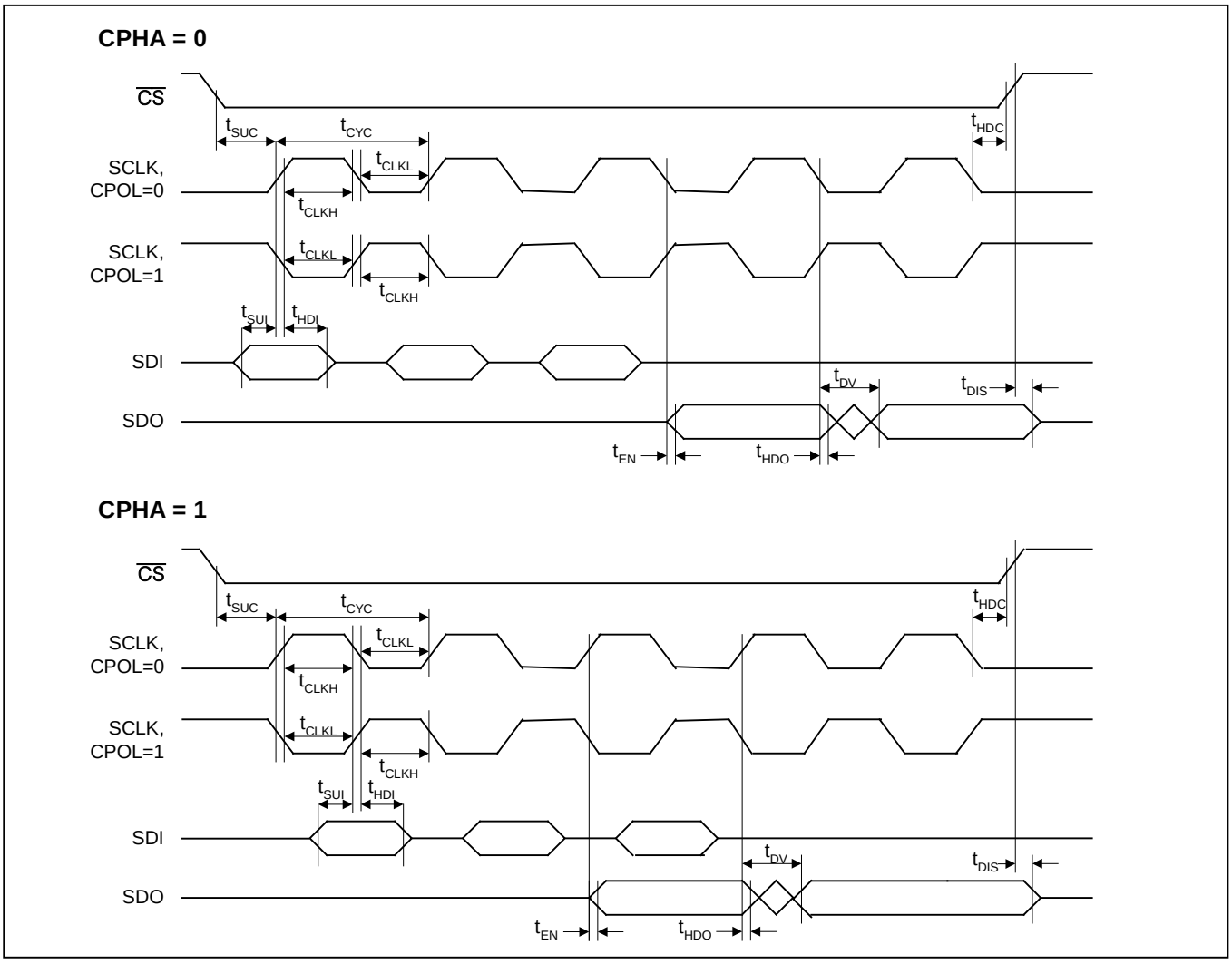
### Table 10-10. SPI Interface Timing

($V_{DD}$ = 1.8V ±10%; $V_{DDIO}$ = 3.3V ±5%, $T_A$ = -40°C to +85°C.) (See Figure 10-4.)

| PARAMETER (Note 1) | SYMBOL | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| SCLK Frequency | $f_{BUS}$ | | | 6 | MHz |
| SCLK Cycle Time | $t_{CYC}$ | 100 | | | ns |
| $\overline{CS}$ Setup to First SCLK Edge | $t_{SUC}$ | 15 | | | ns |
| $\overline{CS}$ Hold Time After Last SCLK Edge | $t_{HDC}$ | 15 | | | ns |
| SCLK High Time | $t_{CLKH}$ | 50 | | | ns |
| SCLK Low Time | $t_{CLKL}$ | 50 | | | ns |
| SDI Data Setup Time | $t_{SUI}$ | 5 | | | ns |
| SDI Data Hold Time | $t_{HDI}$ | 15 | | | ns |
| SDO Enable Time (High-Z to Output Active) | $t_{EN}$ | 0 | | | ns |
| SDO Disable Time (Output Active to High-Z) | $t_{DIS}$ | | | 25 | ns |
| SDO Data Valid Time | $t_{DV}$ | | | 50 | ns |
| SDO Data Hold Time After Update SCLK Edge | $t_{HDO}$ | 5 | | | ns |

**Note 1:** All timing is specified with 100pF load on all SPI pins.

*Figure 10-4. SPI Interface Timing Diagram*



## 10.5 JTAG Interface Timing

### Table 10-11. JTAG Interface Timing

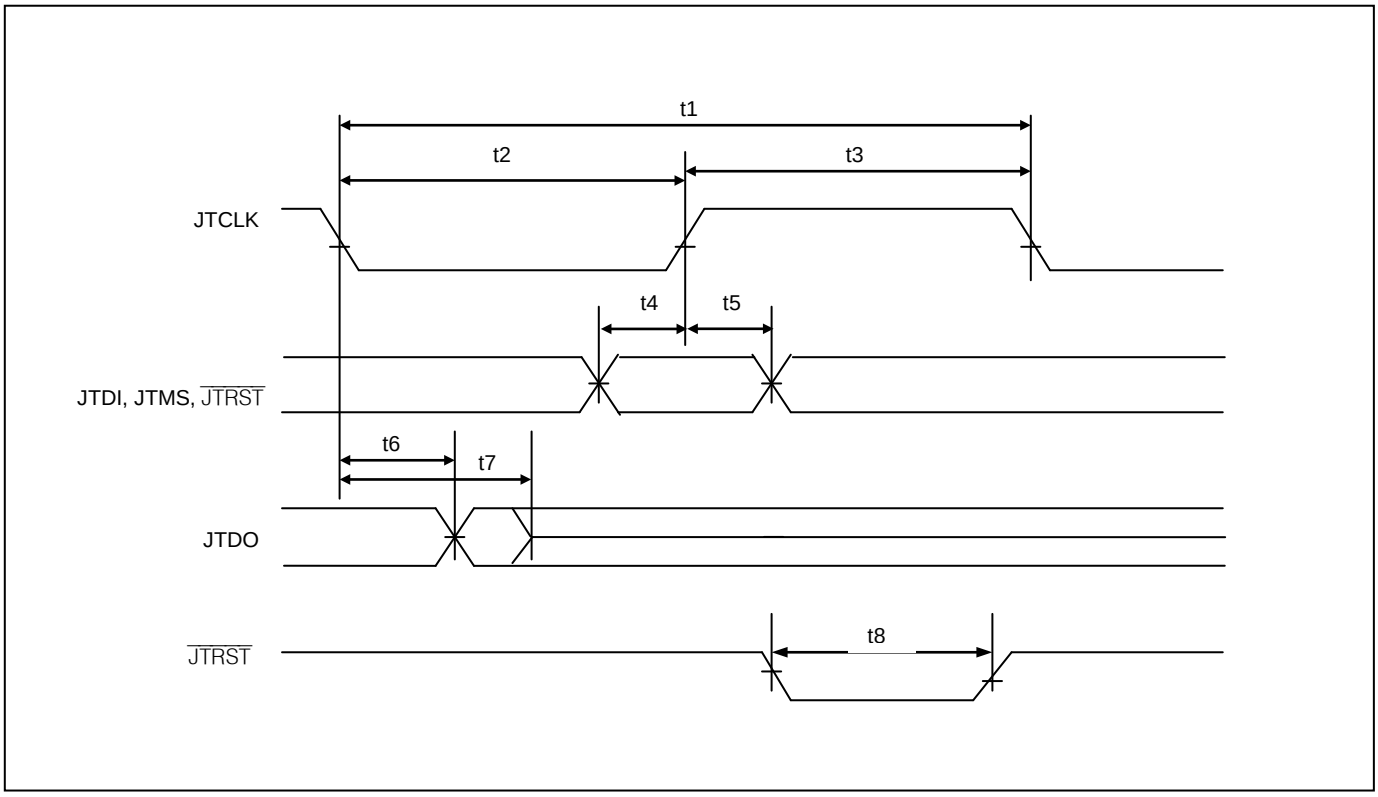
($V_{DD}$ = 1.8V ±10%; $V_{DDIO}$ = 3.3V ±5%, $T_A$ = -40°C to +85°C.) (See Figure 10-5.)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| JTCLK Clock Period | t1 | | 1000 | | ns |
| JTCLK Clock High/Low Time (Note 1) | t2/t3 | 50 | 500 | | ns |
| JTCLK to JTDI, JTMS Setup Time | t4 | 50 | | | ns |
| JTCLK to JTDI, JTMS Hold Time | t5 | 50 | | | ns |
| JTCLK to JTDO Delay | t6 | 2 | | 50 | ns |
| JTCLK to JTDO High-Z Delay (Note 2) | t7 | 2 | | 50 | ns |
| $\overline{\text{JTRST}}$ Width Low Time | t8 | 100 | | | ns |

**Note 1:** Clock can be stopped high or low.

**Note 2:** Not tested during production test.

*Figure 10-5. JTAG Timing Diagram*



## 10.6 Reset Pin Timing

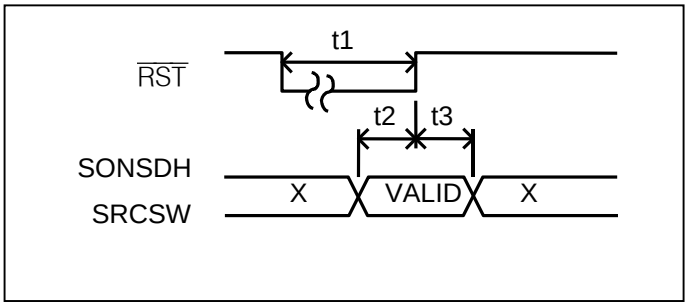
### Table 10-12. Reset Pin Timing

($V_{DD}$ = 1.8V ±10%; $V_{DDIO}$ = 3.3V ±5%, $T_A$ = -40°C to +85°C.) (See Figure 10-6.)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| $\overline{RST}$ Low Time (Note 1) | t1 | 1000 | | | ns |
| SONSDH, SRCSW Setup Time to $\overline{RST}$ | t2 | 0 | | | ns |
| SONSDH, SRCSW Hold Time from $\overline{RST}$ | t3 | 50 | | | ns |

**Note 1:** $\overline{RST}$ should be held low while the REFCLK oscillator stabilizes, which can be 250ms or more for a OCXO after power is applied. It is recommended to force $\overline{RST}$ low during power-up. The 1000ns minimum time applies if the $\overline{RST}$ pulse is applied any time after the device has powered up and the oscillator has stabilized.

*Figure 10-6. Reset Pin Timing Diagram*



## 11. Pin Assignments

Table 11-1 lists pin assignments sorted in alphabetical order by pin name. Figure 11-1 shows pin assignments arranged by pin number.

### Table 11-1. Pin Assignments Sorted by Signal Name

| PIN NAME | PIN NUMBER |
|---|---|
| AVDD_PLL1 | B2 |
| AVDD_PLL2 | C2 |
| AVDD_PLL3 | F2 |
| AVDD_PLL4 | F3 |
| AVSS_PLL1 | A1 |
| AVSS_PLL2 | C3 |
| AVSS_PLL3 | F1 |
| AVSS_PLL4 | G2 |
| CPHA | E7 |
| CPOL | D7 |
| $\overline{CS}$ | D9 |
| FSYNC | H1 |
| IC1NEG | J5 |
| IC1POS | H5 |
| IC2NEG | J7 |
| IC2POS | H7 |
| IC3 | J8 |
| IC4 | J9 |
| IC5NEG | J4 |
| IC5POS | H4 |
| IC6NEG | J6 |
| IC6POS | H6 |
| IC8 | F9 |
| IC9 | G9 |
| INTREQ/LOS | B1 |
| JTCLK | A9 |
| JTDI | A8 |
| JTDO | C8 |
| JTMS | E9 |
| $\overline{JTRST}$ | F8 |
| LOCK | G7 |
| MFSYNC | J1 |
| OC1 | B8 |
| OC1B/GPIO1 | B4 |
| OC2 | A7 |
| OC2B/GPIO2 | A5 |

| PIN NAME | PIN NUMBER |
|---|---|
| OC3 | B7 |
| OC3B/GPIO3 | B5 |
| OC4 | A3 |
| OC4B | A6 |
| OC4NEG | D1 |
| OC4POS | D2 |
| OC5 | A4 |
| OC5B | B6 |
| OC5NEG | E1 |
| OC5POS | E2 |
| OC6NEG | J2 |
| OC6POS | H2 |
| OC7NEG | J3 |
| OC7POS | H3 |
| REFCLK | C1 |
| $\overline{RST}$ | B9 |
| SCLK | C9 |
| SDI | E8 |
| SDO | C7 |
| SONSDH/GPIO4 | B3 |
| SRCSW | G1 |
| SRFAIL | F7 |
| SYNC1 | H8 |
| SYNC2 | H9 |
| SYNC3 | G8 |
| TEST | A2 |
| $V_{DD}$ | C5, E6, G6 |
| VDD_OC45 | E3 |
| VDD_OC67 | G5 |
| $V_{DDIO}$ | C4, D6, F6, G3 |
| $V_{DDIOB}$ | C6 |
| $V_{SS}$ | D4, D5, E4, E5, F4, F5 |
| VSS_OC45 | D3 |
| VSS_OC67 | G4 |
| WDT | D8 |

*Figure 11-1. Pin Assignment Diagram*

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |
|---|---|---|---|---|---|---|---|---|---|
| **A** | AVSS_PLL1 | TEST | OC4 | OC5 | OC2B/ GPIO2 | OC4B | OC2 | JTDI | JTCLK |
| **B** | INTREQ/ LOS | AVDD_PLL1 | SONSDH/ GPIO4 | OC1B/ GPIO1 | OC3B/ GPIO3 | OC5B | OC3 | OC1 | $\overline{RST}$ |
| **C** | REFCLK | AVDD_PLL2 | AVSS_PLL2 | $V_{DDIO}$ | $V_{DD}$ | $V_{DDIOB}$ | SDO | JTDO | SCLK |
| **D** | OC4NEG | OC4POS | VSS_OC45 | $V_{SS}$ | $V_{SS}$ | $V_{DDIO}$ | CPOL | WDT | $\overline{CS}$ |
| **E** | OC5NEG | OC5POS | VDD_OC45 | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | CPHA | SDI | JTMS |
| **F** | AVSS_PLL3 | AVDD_PLL3 | AVDD_PLL4 | $V_{SS}$ | $V_{SS}$ | $V_{DDIO}$ | SRFAIL | $\overline{JTRST}$ | IC8 |
| **G** | SRCSW | AVSS_PLL4 | $V_{DDIO}$ | VSS_OC67 | VDD_OC67 | $V_{DD}$ | LOCK | SYNC3 | IC9 |
| **H** | FSYNC | OC6POS | OC7POS | IC5POS | IC1POS | IC6POS | IC2POS | SYNC1 | SYNC2 |
| **J** | MFSYNC | OC6NEG | OC7NEG | IC5NEG | IC1NEG | IC6NEG | IC2NEG | IC3 | IC4 |

- High-Speed Analog
- Low-Speed Analog
- High-Speed Digital
- Low-Speed Digital
- $V_{DDIO}$ 3.3V
- $V_{DDIOB}$ 3.3V or 2.5V
- $V_{DD}$ 1.8V
- Analog $V_{DD}$ 1.8V
- $V_{SS}$
- Analog $V_{SS}$
- N.C. = No Connection. Lead is not connected to anything inside the device.

## 12. Package Information

For the latest package outline information and land patterns contact Microsemi timing products technical support. Note that a “+”, “#”, or “-” in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

| PACKAGE TYPE | PACKAGE CODE | OUTLINE NO. | LAND PATTERN NO. |
|---|---|---|---|
| 81 CSBGA | X81-1 | 21-0360 | 90-0293 |

### Table 12-1. CSBGA Package Thermal Properties, Natural Convection

| PARAMETER | MIN | TYP | MAX |
|---|---|---|---|
| Ambient Temperature (Note 1) | -40°C | | +85°C |
| Junction Temperature | -40°C | | +125°C |
| Theta-JA ($\theta_{JA}$) (Note 2) | | 33.8°C/W | |
| Theta-JB ($\theta_{JB}$) | | 18.2°C/W | |
| Theta-JC ($\theta_{JC}$) | | 9.0°C/W | |
| Psi-JB | | 17.8°C/W | |
| Psi-JT | | 0.22°C/W | |

**Note 1:** The package is mounted on a four-layer JEDEC standard test board with no airflow and dissipating maximum power.

**Note 2:** Theta-JA ($\theta_{JA}$) is the junction to ambient thermal resistance, when the package is mounted on a four-layer JEDEC standard test board with no airflow and dissipating maximum power.

## 13. Acronyms and Abbreviations

| | |
|---|---|
| AIS | Alarm Indication Signal |
| AMI | Alternate Mark Inversion |
| APLL | Analog Phase-Locked Loop |
| BITS | Building Integrated Timing Supply |
| BPV | Bipolar Violation |
| DFS | Digital Frequency Synthesis |
| DPLL | Digital Phase-Locked Loop |
| ESF | Extended Superframe |
| EXZ | Excessive Zeros |
| GbE | Gigabit Ethernet |
| I/O | Input/Output |
| LOS | Loss of Signal |
| LVDS | Low-Voltage Differential Signal |
| LVPECL | Low-Voltage Positive Emitter-Coupled Logic |
| MTIE | Maximum Time Interval Error |
| OCXO | Oven-Controlled Crystal Oscillator |
| OOF | Out of Frame Alignment |
| PBO | Phase Build-Out |
| PFD | Phase/Frequency Detector |
| PLL | Phase-Locked Loop |
| ppb | Parts per Billion |
| ppm | Parts per Million |
| pk-pk | Peak-to-Peak |
| RMS | Root-Mean-Square |
| RAI | Remote Alarm Indication |
| RO | Read-Only |
| R/W | Read/Write |
| SDH | Synchronous Digital Hierarchy |
| SEC | SDH Equipment Clock |
| SETS | Synchronous Equipment Timing Source |
| SF | Superframe |
| SONET | Synchronous Optical Network |
| SSM | Synchronization Status Message |
| SSU | Synchronization Supply Unit |
| STM | Synchronous Transport Module |
| TDEV | Time Deviation |
| TCXO | Temperature-Compensated Crystal Oscillator |
| UI | Unit Interval |
| $UI_{P-P}$ | Unit Interval, Peak-to-Peak |
| XO | Crystal Oscillator |

## 14. Data Sheet Revision History

| REVISION DATE | DESCRIPTION |
|---|---|
| 102607 | Initial data sheet release. |
| 012108 | Updated Section 7.9.2 and its subsections extensively to more clearly explain the operation of the device. Also updated MCR3:AEFSEN, MCR3:EFSEN, FSCR3:SOURCE and FSCR1:SYNCSRC to match. |
| | In Section 10, added Note 1 to the Absolute Maximum Ratings. |
| 070308 | In Table 6-2, corrected the default output frequenices for OC1–OC5, OC6POS/OC5NEG, and OC7POS/OC7NEG. |
| | In Table 6-3, corrected the WDT resistor value from 20kΩ to 10kΩ. |
| 102808 | In the MCR9.AUTOBW description, deleted sentence referring to slave mode, which does not apply to DS3102.<br>In MCR11.FMEASIN description, corrected 0001 option to IC1 and 0010 option to IC2. These erroneously said “{unused value, undefined}” before. |
| 2009-05 | On page 1 and various locations in the document, added mention of Stratum 2 compliance, expanded G.812 compliance to Types I – IV, and added G.8262 EEC compliance.<br>Added new Sections 7.7.7.1 and 7.7.7.2 to describe the phase monitor and phase build-out in response to input transients.<br>In the PHMON register, added the PMEN, PMPBEN and PMLIM fields.<br>In the MSR3 and IER3 registers, added PHMON at bit 5.<br>In Table 6-2, corrected the default value of OC5 to match power-on default values listed elsewhere in the document.<br>In Section 8, added note indicating systems must be able to access entire address range 0-1FFh. |
| 2010-08 | In Figure 9-1 corrected pullup resistors values to 50kΩ.<br>In PHMON.NW bit description, added "(TEST1.D180=0)".<br>In Table 6-3 edited SRFAIL pin description to indicate state is high impedance when MCR10.SRFPIN=0. Edited MCR10.SRFPIN decription to say this also.<br>In Section 7.5.1 and Section 7.7.6 deleted sentences that said the hard and soft limits have hysteresis as required by GR-1244.<br>Added new Section 7.6.7 to describe how to achieve GR-1244-compliant accept and reject thresholds and hysteresis.<br>Replaced the term "floating" with "unconnected" in several places.<br>Updated soldering temperature information in Section 10. |
| 2012-04 | Reformatted for Microsemi. No content change. |



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