19-4633; 5/09

DS2756

High-Accuracy Battery Fuel Gauge with Programmable Suspend Mode

www.maxim-ic.com

GENERAL DESCRIPTION

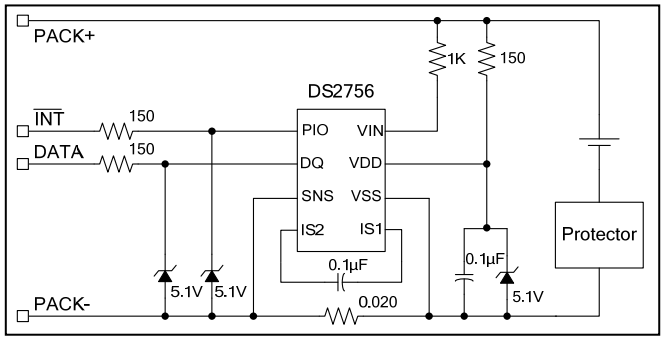
The DS2756 high-precision battery fuel gauge is a data-acquisition and information-storage device tailored for cost-sensitive and space-constrained 1-cell Li+/polymer battery-pack applications. The DS2756 provides the key hardware components required to accurately estimate remaining capacity by integrating low-power, precision measurements of temperature, voltage, current, and current accumulation, as well as nonvolatile (NV) data storage, into the small footprint of a 3.0mm x 4.4mm 8-pin TSSOP package.

Through its 1-Wire® interface, the DS2756 gives the host system read/write access to status and control registers, instrumentation registers, and general-purpose data storage. Each device has a unique factory-programmed 64-bit net address that allows it to be individually addressed by the host system, supporting multibattery operation.

FEATURES

- **Programmable Suspend Mode**
- **Accurate Current Accumulation**
  - **2% ±4µV over ±64mV Input Range**
  - **2% ±200µA over ±3.2A with 20mΩ Sense**
- **Current Measurement**
  - **9-Bit Snapshot Measurement**
  - **12-Bit Average Updated Every 88ms**
  - **15-Bit Average Updated Every 2.8s**
- **Voltage Measurement**
  - **9-Bit Snapshot Measurement**
  - **10-Bit Average Updated Every 4ms**
- **Temperature Measurement**
  - **10-Bit with 0.125°C Resolution**
- **Snapshot Mode Allows Instantaneous Power Measurement**
- **Host Alerted When Accumulated Current or Temperature Exceeds Programmable Limits**
- **96 Bytes of Lockable EEPROM**
- **8 Bytes of General-Purpose SRAM**
- **Dallas 1-Wire Interface with Unique 64-Bit Address and Standard or Overdrive Timing**
- **3mm Dimension of 8-Pin TSSOP Package Allows Mounting on Side of Thin Prismatic Li+ and Li+/Polymer Cells**

TYPICAL OPERATING CIRCUIT



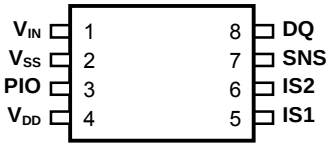
1-Wire is a registered trademark of Maxim Integrated Products, Inc.

ORDERING INFORMATION

PART	TEMP RANGE	PIN-PACKAGE
DS2756E+	-20°C to +70°C	8 TSSOP
DS2756E+T&R	-20°C to +70°C	DS2756E+ on Tape-and-Reel

+ Denotes lead(Pb)-free/RoHS-compliant package.

PIN CONFIGURATION



DS2756E
TSSOP Package

Note: *Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, click here: www.maxim-ic.com/errata.*

ABSOLUTE MAXIMUM RATINGS

Voltage on PIO Pin, Relative to V_{SS}	-0.3V to +12V
Voltage on All Other Pins, Relative to V_{SS}	-0.3V to +6V
Continuous Sink Current, DQ, PIO	12mA
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-55°C to +125°C
Soldering Temperature	See J-STD-020A Specification

This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

($3.0V \le V_{DD} \le 4.5V$, T_A = -20°C to +70°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{DD}	(Note 1)	+3.0		+4.5	V
Data Pin	DQ	(Note 1)	-0.3		+5.5	V
V_{IN} Pin	V_{IN}	(Note 1)	-0.3		+4.5	V

DC ELECTRICAL CHARACTERISTICS

($3.0V \le V_{DD} \le 4.5V$, T_A = -20°C to +70°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Active Mode Supply Current	I_{ACTIVE}	DQ = V_{DD}, EEC bit = 0, 3.0V < V_{DD} < 4.2V		75	100	µA
		DQ = V_{DD}, EEC bit = 0			120	
Sleep Mode Supply Current	I_{SLEEP}	DQ = 0V, PIE = 00b		1	3	µA
Suspend Mode Supply Current	$I_{SUSPEND}$	DQ = 0V, PIE ≠ 00b (Note 11)		1.5	4	µA
Current Measurement Input Range	$V_{IS1-IS2}$	(Note 2)	±64			mV
Current Register Offset Error	I_{OERR}	(Note 4)			±7.813	µV/R
Current Gain Error	I_{GERR}	(Notes 2, 5)			±1	% reading
24 Hour Accumulated Current Error	q_{CA}	$V_{IS1-IS2}$ = 0, OBEN set, (Notes 2, 3, 6)	-200	-100	0	µVhr/R
Current Sampling Frequency	f_{SAMP}			1456		Hz
IS1-VSS, IS2-SNS Filter Resistors	R_{KS}	+25°C		10		kΩ
Input Resistance: V_{IN}	R_{IN}	V_{IN} = V_{DD}	5			MΩ
Voltage Offset Error	V_{OERR}	(Note 7)			±5	mV
Voltage Gain Error	V_{GERR}				±2	%V reading
Temperature Error	T_{ERR}	(Note 8)			±3	°C
Input Logic High: DQ, PIO	V_{IH}	(Note 1)	1.5			V
Input Logic Low: DQ, PIO	V_{IL}	(Note 1)			0.4	V
Output Logic Low: DQ, PIO	V_{OL}	I_{OL} = 4mA (Note 1)			0.4	V
DQ Pulldown Current	I_{PD}			1		µA
DQ Capacitance	C_{DQ}				60	pF
DQ Low-to-Sleep Time	t_{SLEEP}		2.1			s
Suspend Period Accuracy	t_{SUS_ERR}			0	±30	%
Minimum Active Mode	t_{ACT_MIN}		87	90	93	ms

Period						
Undervoltage Detect	V_{UV}	2.4V < V_{DD} < 4.5V (Note 1)	2.45	2.5	2.55	V
Undervoltage Delay	t_{UVD}		79	82	85	ms
Internal Timebase Accuracy	t_{ERR}	(Note 9)		±1	±2	%

ELECTRICAL CHARACTERISTICS—1-WIRE INTERFACE

(3.0V ≤ V_{DD} ≤ 4.5V, T_A = -20°C to +70°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Snapshot Trigger 0	t_{SWL}		1		16	µs
Snapshot Delay	t_{SDLY}		80	100	120	µs
STANDARD TIMING						
Time Slot	t_{SLOT}		60		120	µs
Recovery Time	t_{REC}		1			µs
Write-0 Low Time	t_{LOW0}		60		119	µs
Write-1 Low Time	t_{LOW1}		1		15	µs
Read Data Valid	t_{RDV}				15	µs
Reset Time High	t_{RSTH}		480			µs
Reset Time Low	t_{RSTL}		480		960	µs
Presence-Detect High	t_{PDH}		15		60	µs
Presence-Detect Low	t_{PDL}		60		240	µs
Interrupt Time Low	t_{IL}		480		1920	µs
OVERDRIVE TIMING						
Time Slot	t_{SLOT}		6		16	µs
Recovery Time	t_{REC}		1			µs
Write-0 Low Time	t_{LOW0}		6		16	µs
Write-1 Low Time	t_{LOW1}		1		2	µs
Read Data Valid	t_{RDV}				2	µs
Reset Time High	t_{RSTH}		48			µs
Reset Time Low	t_{RSTL}		48		80	µs
Presence-Detect High	t_{PDH}		2		6	µs
Presence-Detect Low	t_{PDL}		8		24	µs
Interrupt Time Low	t_{IL}		48		192	µs

EEPROM RELIABILITY SPECIFICATION

(3.0V ≤ V_{DD} ≤ 4.5V, T_A = -20°C to +70°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Copy to EEPROM Time	t_{EEC}			2	10	ms
EEPROM Copy Endurance	N_{EEC}	(Note 10)	50,000			cycles

Note 1: All voltages are referenced to V_{SS}.
Note 2: Specifications relative to V_{IS1} - V_{IS2}.
Note 3: Summation of worst case time base and current measurement sampling errors.
Note 4: Continuous offset cancellation corrects offset errors in the current measurement system. Individual values reported by the Current register have a maximum offset of ±0.5 LSb's (±7.8125µV). Individual values reported in the Average Current register have a maximum offset of ±2 LSb's (±7.8125µV).
Note 5: Current Gain Error specifies the gain error in the Current register value compared to a reference voltage between IS1 and IS2. The DS2756 does not compensate for sense resistor characteristics, and any error terms arising from the sense resistor should be taken into account when calculating total current measurement error.
Note 6: Achieving the 24 Hour Accumulated Current Error assumes positive offset accumulation blanking is enabled (OBEN bit set) and can require a one time 3.5s in-system calibration after mounting to the printed circuit board. Variations in temperature and supply voltage are compensated for by periodic offset corrections performed automatically during *Active* mode operation.
Note 7: Voltage offset measurement is with respect to 4.2V at +25°C.
Note 8: Self heating due to output pin loading and sense resistor power dissipation can alter the Temperature reading from ambient conditions.
Note 9: Typical value for t_{ERR} valid at 3.7V and +25°C. t_{ERR} applies to all internal timings (ex. f_{SAMP}, t_{SLEEP}, t_{UVD}) except for the 1-Wire Interface timings and t_{SUS_ERR}.
Note 10: Four year data retention at +50°C.
Note 11: Measured during the Suspend Timeout. Does not include active period of suspend cycle.

DETAILED DESCRIPTION

The DS2756 performs temperature, voltage, and current measurement to a resolution sufficient to support process-monitoring applications such as battery charge control and remaining capacity estimation. Temperature is measured using an on-chip sensor, eliminating the need for a separate thermistor. Bidirectional current measurement supporting current accumulation (coulomb counting) is accomplished using an external current sense resistor.

The host system can configure the DS2756 to signal critical conditions to reduce polling overhead. The alarm interrupt fires when programmable upper and lower thresholds of temperature or coulomb count are crossed. The user can select either the DQ pin or PIO pin as the alarm interrupt signal.

PIO can also function as a *Suspend* mode interrupt output to reduce idle current drain within a battery pack. In *Suspend* mode, the DS2756 cycles between *Active* and *Suspend* power modes to reduce DS2756 supply current and the PIO pin can be used to wake up a microcontroller or other pack circuitry if current flowing through the pack exceeds programmable charge and discharge thresholds (See Figure 12). The interval between current measurements can be programmed to achieve an average current as low as 10μA (See Table 3).

As a general purpose I/O pin, PIO allows the host system to sense and control other electronics in the pack, including switches, vibration motors, speakers, and LEDs.

Three types of memory are provided on the DS2756 for battery information storage: EEPROM, lockable EEPROM, and SRAM. EEPROM memory saves important battery data in true NV memory that is unaffected by severe battery depletion, accidental shorts, or ESD events. Lockable EEPROM becomes ROM when locked to provide additional security for unchanging battery data. SRAM provides inexpensive storage for temporary data.

Figure 1. Application Example with Microcontroller in Pack

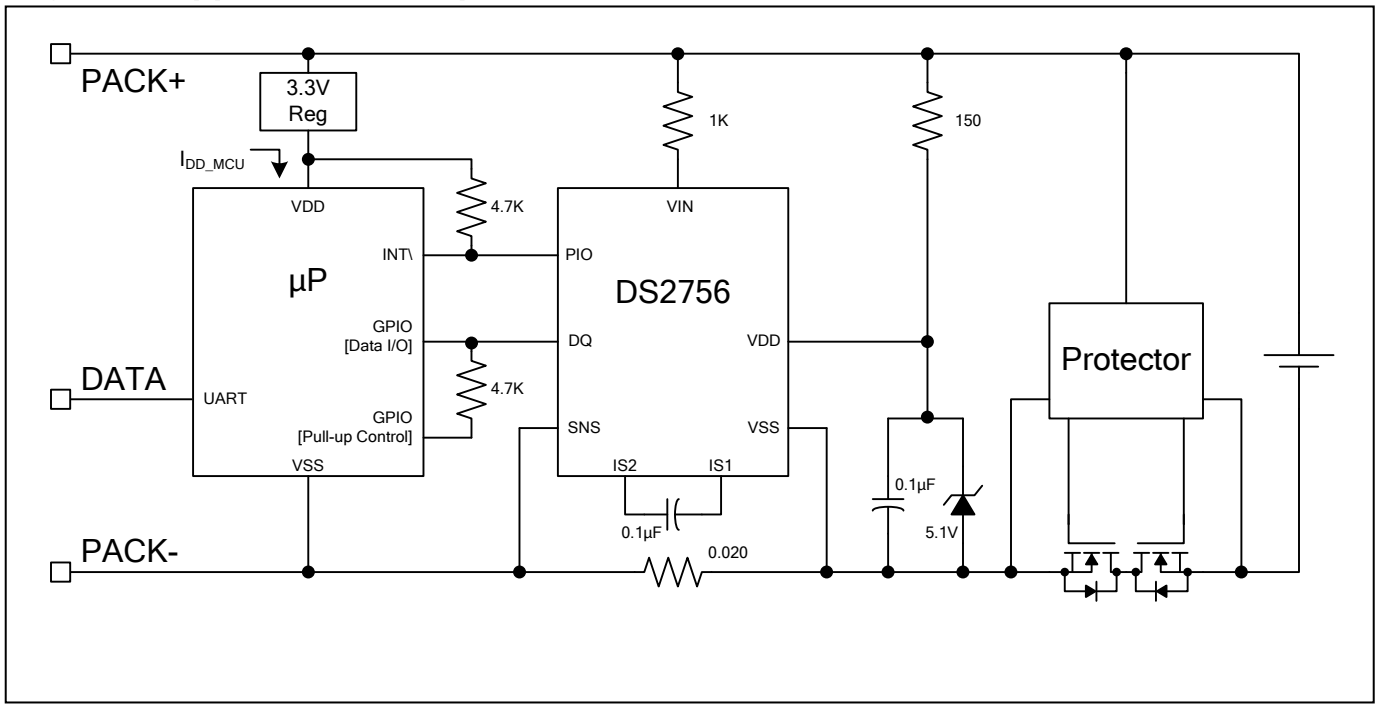
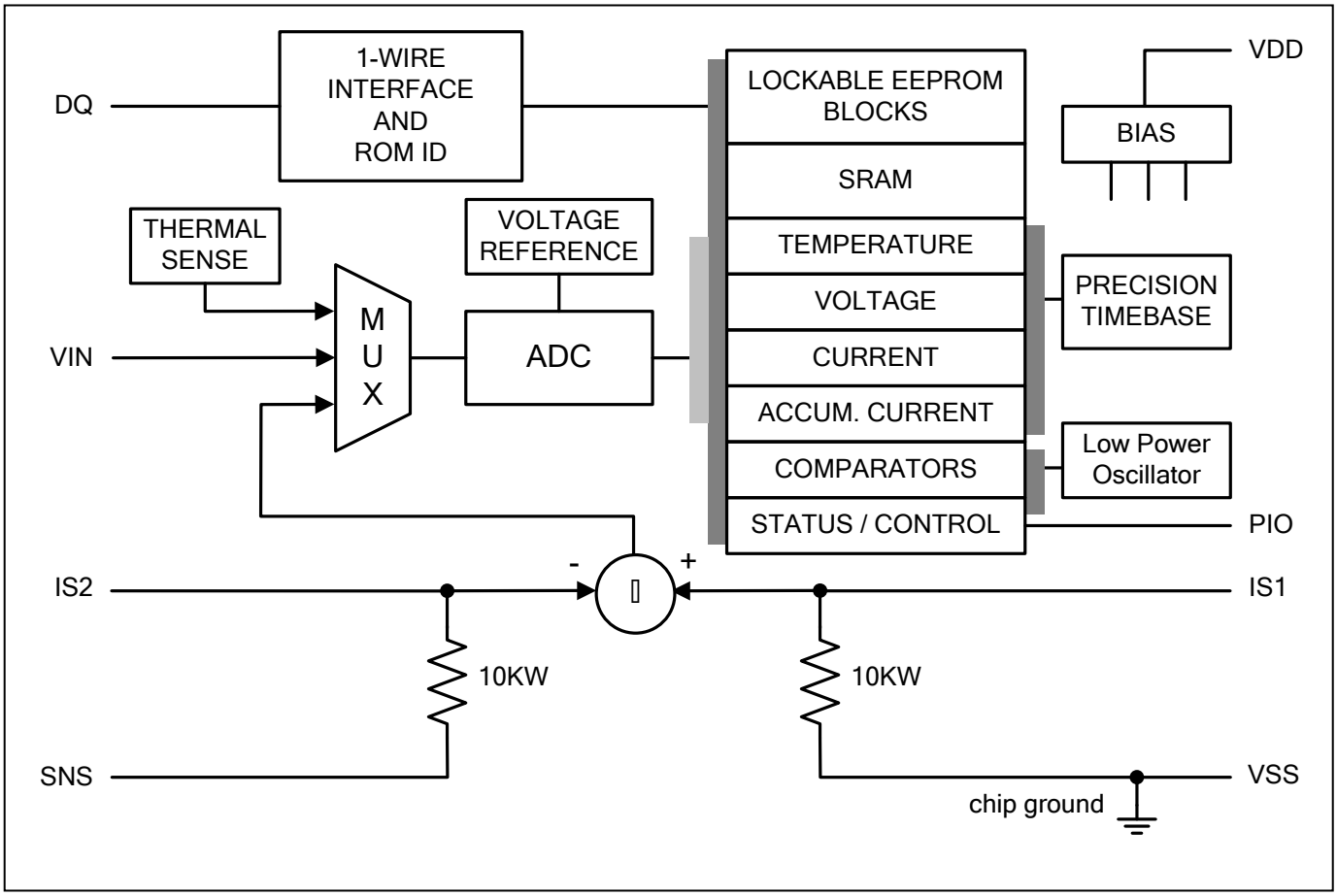


Figure 2. Functional Diagram



DETAILED PIN DESCRIPTION

Pin	Name	Description
1	V_{IN}	Battery Voltage-Sense Input. Voltage measurement performed on V_{IN} input and displayed in Voltage Register.
2	V_{SS}	Device Ground and Current-Sense Resistor Connection. V_{SS} attaches to battery end of sense resistor.
3	PIO	General-Purpose Programmable I/O Pin or Optional Interrupt Output
4	V_{DD}	Input Supply: +3.0V to +4.5V Input Range. Bypass V_{DD} to V_{SS} with 0.1µF.
5	IS1	Current-Sense Filter Input 1
6	IS2	Current-Sense Filter Input 2
7	SNS	Sense Resistor Connection. SNS attaches to pack end of current sense resistor.
8	DQ	Serial Interface Data I/O Pin. Bidirection data transmit and receive at 16kbps or 143kbps. Optional interrupt output.

POWER MODES

The DS2756 has three power modes: *Active, Suspend* and *Sleep*. While in *Active* mode, the DS2756 continuously measures voltage, temperature, current, accumulated current, and monitors for an under voltage condition. In *Suspend and Sleep* modes, the DS2756 ceases these activities. During *Suspend*, the DQ input buffer is active and a low power oscillator runs. In *Sleep* mode, only the DQ input buffer is active.

The DS2756 enters *Suspend* mode when PMOD = 1 **AND** all of the following conditions are true:

- the DQ line is low for longer than t_{SLEEP}
- the Programmable Interval Enable (PIE) bits in the Status Register are set to a non-zero value (PIE =01b, 10b or 11b)
- Current register value is less than the Charge Suspend Threshold **AND** greater than the Discharge Suspend Threshold

Periodically, when a Suspend Period time out occurs, the DS2756 temporarily cycles from *Suspend* to *Active* mode in order to measure current. When the current measurement completes, the result is evaluated against the user programmed Charge and Discharge Suspend Thresholds. If the Current measurement result does not cross either threshold, the DS2756 transitions back to *Suspend*. If the measurement shows that more current is flowing than the level of either threshold, the DS2756 signals a suspend interrupt by driving the PIO pin low, then remains in *Active* mode continuing normal *Active* mode operation.

The DS2756 enters *Sleep* mode when PMOD = 1 **AND** either of the following conditions are true:

- the DQ line is low for longer than t_{SLEEP} (minimum 2.1s) **AND** PIE = 00b
- the UVEN bit in the Status Register is set to 1 **AND** the voltage on V_{IN} drops below undervoltage threshold V_{UV} for t_{UVD} (V_{IN} measurement and comparison to V_{UV}, and t_{UVD} timeout occur in normal *Active* mode and temporary *Active* mode cycle from *Suspend* mode)

The DS2756 returns to *Active* mode from *Suspend* or *Sleep* mode whenever the DQ line is pulled from a low-to-high state.

The factory default for the DS2756 is UVEN = 0, PMOD = 0 and PIE = 00b. The DS2756 defaults to *Active* mode when power is first applied.

CURRENT MEASUREMENT AND ACCUMULATION

The DS2756 current measurement system is designed to provide timely data on charge and discharge current at a moderate resolution level while simultaneously accumulating high resolution average data to support accurate coulomb counting. Current is measured with an Analog-to-Digital Converter (ADC) by sampling the voltage drop across a series sense resistor, R_{SNS}, connected between SNS and V_{SS}. Individual current samples are taken every 687µs (1456^{-1} Hz). Multiple samples are averaged to report Current and Average Current values, and accumulated for coulomb counting.

Current Measurement

The voltage signal developed across the sense resistor (between SNS and V_{SS}) is differentially sampled by the ADC inputs through internal 10kΩ resistors connected between $V_{SS}$and IS1, and SNS and IS2. Isolating the ADC inputs (IS1 and IS2 pins) from the sense resistor with 10kΩ facilitates the use of an RC filter by adding a single external capacitor. The RC filter extends the input range beyond ±64mV in pulse load or pulse charge applications. The ADC accurately measures large peak signals as long as the differential signal level at IS1 and IS2 does not exceed ±64mV.

The Current register operates in two modes, normal and snapshot. In normal mode, the Current register reports the average of 128 individual current samples every 88ms. The reported value represents the average current during the 88ms measurement period. The Average Current register reports the average of 4096 current samples and is updated every 2.8s.

In snapshot mode, the Current register holds the current measured immediately following the snapshot trigger. Current measurements resume immediately after the snapshot value is obtained, however, the SNAP bit must be cleared to re-enable normal mode current reporting in the Current register. The Average Current register continues to be updated while the SNAP bit is set. Current accumulation also continues while SNAP is set. Although a small

error is introduced into both the Average Current and Accumulated Current values by the current sample timing discontinuity introduced with each trigger of the Snapshot mode, use of Snapshot once every 5s does not produce a significant error.

The following register formats specify the update interval and units for the Current and Average Current registers. Values are posted in two's complement format. Positive values represent charge currents ($V_{IS1} > V_{IS2}$) and negative values represent discharge currents ($V_{IS2} > V_{IS1}$). Positive currents above the maximum register value are reported at the maximum value, 0x7FFF. Negative currents below the minimum register value are reported at the minimum value, 0x8000.

Figure 3. Current Register Format

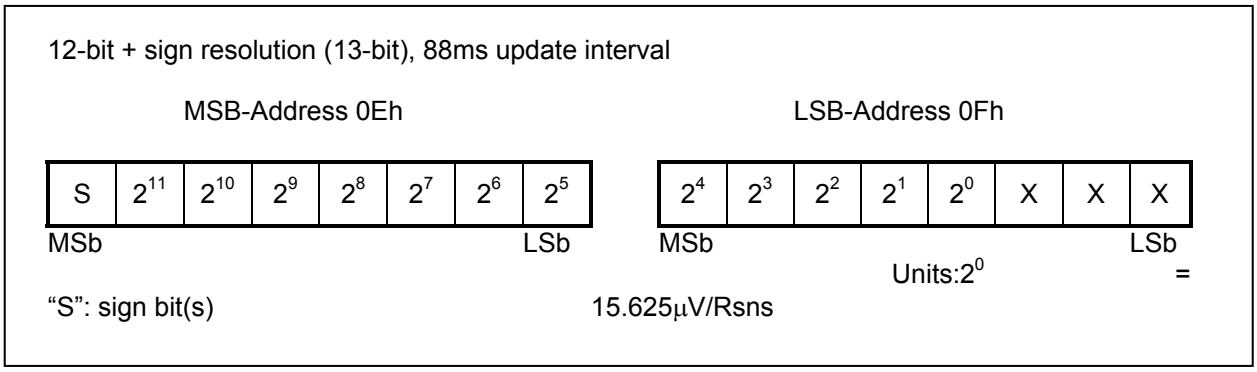
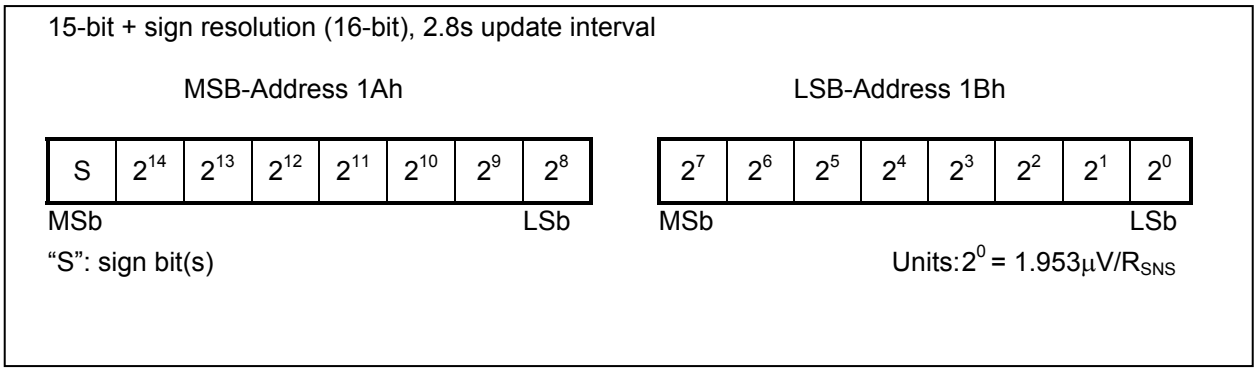


Figure 4. Average Current Register Format



CURRENT OFFSET CORRECTION

Continuous offset cancellation is performed automatically to correct for offsets in the current measurement system. Individual values reported by the Current register have a maximum offset of ±0.5 LSb's (±7.8125µV). Individual values reported in the Average Current register have a maximum offset of ±2 LSb's (±7.8125µV).

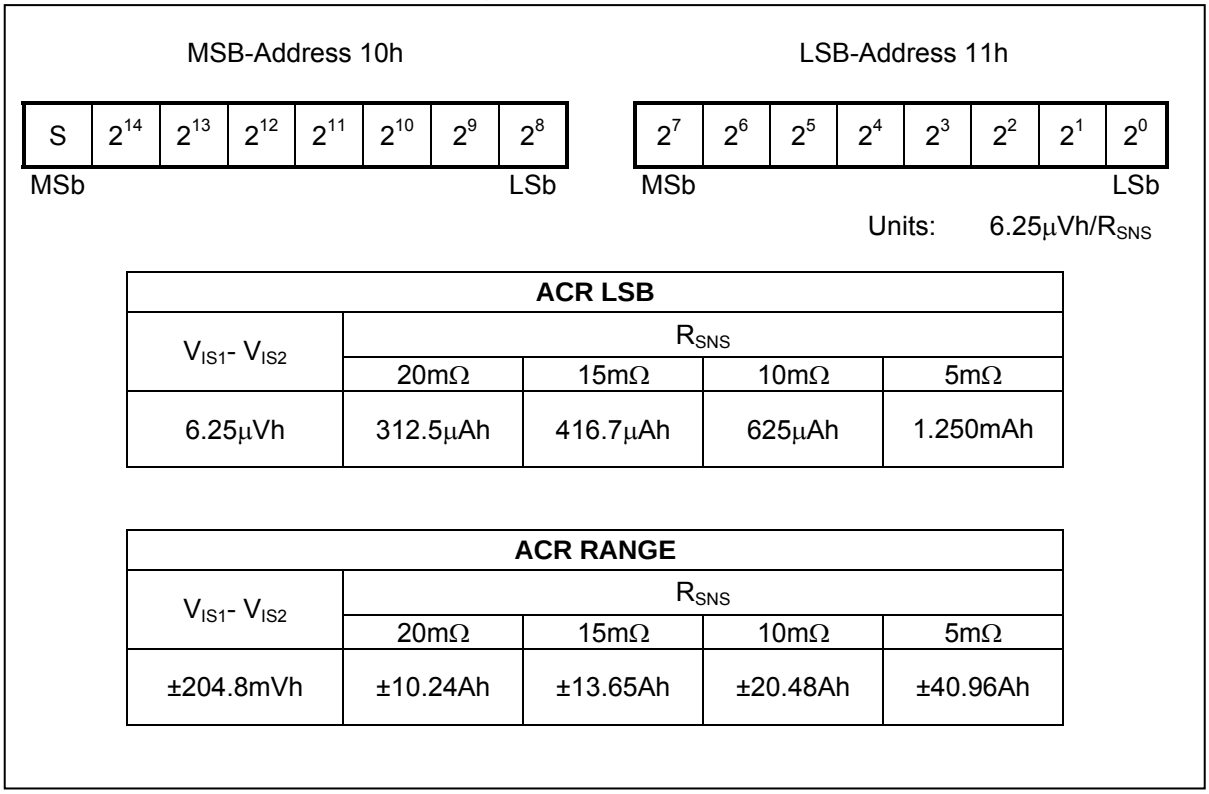
CURRENT ACCUMULATION

The DS2756 measures current for coulomb counting purposes, with an accuracy of ±2% (±3.9µV) over a range of ±64mV. Using a 20mΩ sense resistor, current accumulation is performed over a range of ±3.2A while measuring standby currents with an accuracy of ±195µA. Current measurements are internally summed, or accumulated, with the results displayed in the Accumulated Current Register (ACR). The accuracy of the ACR is dependent on both the current measurement and the accumulation timebase. The 16-bit ACR has a range of ±204.8mVh with an LSb of 6.25µVh. Accumulation of charge current above the maximum register value is reported at the maximum value; conversely, accumulation of discharge current below the minimum register value is reported at the minimum value.

Read and write access is allowed to the ACR. The ACR must be written MSB first then LSB. Whenever the ACR is written, internal fractional accumulation result bits are cleared. In order to preserve the ACR value in case of power loss, the ACR MSB and LSB are automatically backed up to EEPROM after incrementing or decrementing by 100µVh (5.0mAh for R_{SNS} = 20mΩ). The ACR value is recovered from EEPROM on power-up or by a Recall Data

command targeting the ACR register address. A write to the ACR results in an automatic copy of the new value to EEPROM.

Figure 5. Accumulated Current Register Format



ACR LSB				
V_{IS1}- V_{IS2}	R_{SNS}			
	20mΩ	15mΩ	10mΩ	5mΩ
6.25μVh	312.5μAh	416.7μAh	625μAh	1.250mAh

ACR RANGE				
V_{IS1}- V_{IS2}	R_{SNS}			
	20mΩ	15mΩ	10mΩ	5mΩ
±204.8mVh	±10.24Ah	±13.65Ah	±20.48Ah	±40.96Ah

OFFSET ACCUMULATION BLANKING

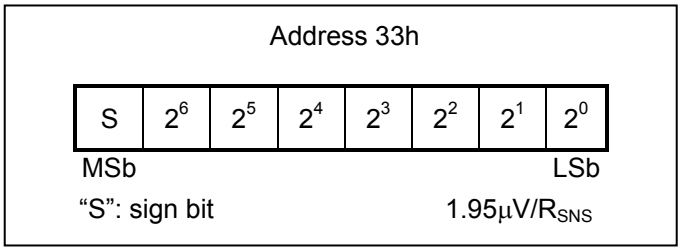
In order to avoid the accumulation of small positive offset errors over long periods, an offset blanking filter is provided. The blanking filter is enabled by setting the OBEN bit in the Status Register. When OBEN is set, charge currents (positive Current register values) between 15.625μV and 62.5μV are not accumulated in the ACR. Therefore, with R_{SNS} = 0.020Ω, positive currents between 0.78mA and 3.125mA are blanked from accumulation in the ACR.

ACCUMULATION BIAS

Systematic errors or an application preference can require the application of an arbitrary bias to the current accumulation process. The Accumulation Bias register is provided to allow a user programmed constant positive or negative polarity bias to the current accumulation process. The Accumulation Bias value can be used to estimate battery currents that do not flow through the sense resistor, estimate battery self-discharge, or correct for offset error in the Current register and ACR register. The user programmed two's complement value in the Accumulation Bias register is added to the Current Register once per current sample. The register format supports the accumulation bias to be applied in 1.95μV increments over a ±250μV range. When using a 20mΩ sense resistor, the bias control is 100μA over a ±12.5mA range.

The Accumulation Bias register is directly read and write accessible. The user value is made non-volatile with a Copy Data command targeting EEPROM block 0. The Accumulation Bias register is loaded from EEPROM memory on power up and a transition from *Sleep* to *Active* mode.

Figure 6. Accumulation Bias Register Format



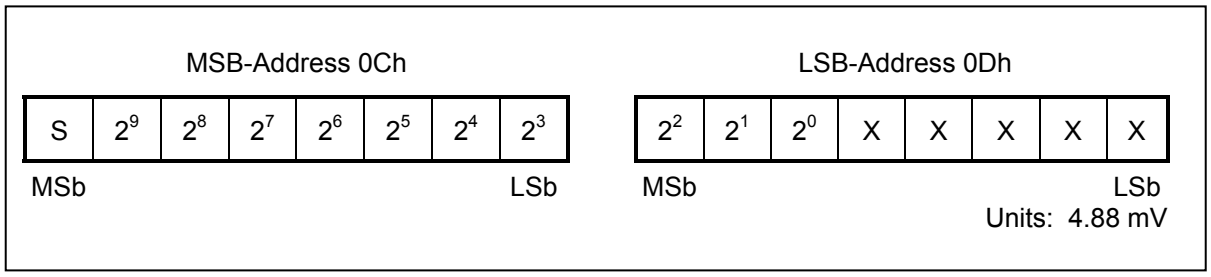
VOLTAGE MEASUREMENT

The voltage register operates in two modes, normal and snapshot. In normal mode, the DS2756 continually measures the voltage between pins V_{IN} and V_{SS} over a 0 to 4.5V range, and the Voltage Register is updated in two's-complement format every 3.4ms with a resolution of 4.88mV.

In snapshot mode, the Voltage register holds the voltage measured immediately following the snapshot trigger. Normal voltage measurements resume after the snapshot value is obtained, however, the SNAP bit must be cleared to re-enable normal mode reporting of voltage measurement to the Voltage register.

Voltages above the maximum register value are reported as the maximum value.

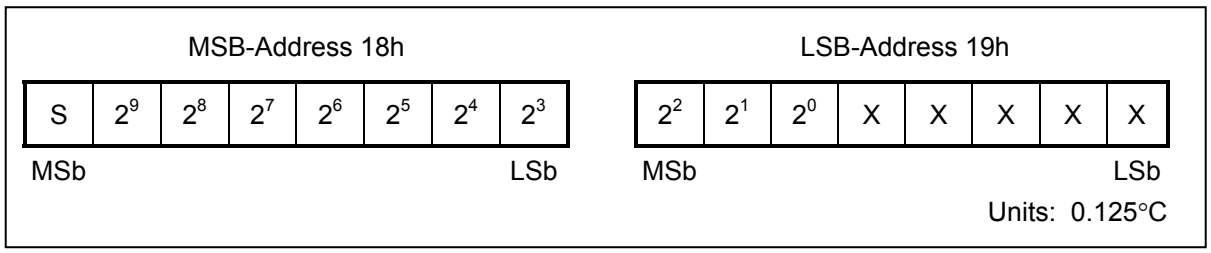
Figure 7. Voltage Register Format



TEMPERATURE MEASUREMENT

The DS2756 uses an integrated temperature sensor to continually measure battery temperature. Temperature measurements are updated in the Temperature Register every 220ms in two's-complement format with a resolution of 0.125°C over a ±127°C range. The Temperature Register format is shown in Figure 8.

Figure 8. Temperature Register Format



PROGRAMMABLE I/O

The PIO pin can be configured as a general purpose programmable I/O pin, or as an interrupt output. To use the PIO pin in the programmable I/O mode described in this section, the PIO interrupt method must not be enabled. See the Interrupt Signaling section for information on disabling interrupts.

As a programmable I/O pin, PIO provides a digital input or an open drain digital output. Writing a 1 to the PIO bit in the Special Feature Register disables the output driver. With the PIO pin Hi-Z, it can be used as an input. The logic level of the PIO pin is reported in the Special Feature Register through the serial interface.

To use the PIO pin as an output, write the desired output value to the PIO bit in the Special Feature Register. Writing a 0 to the PIO bit enables the PIO output driver, pulling the PIO pin to V_{SS}. As stated above, writing a 1 to the PIO bit forces the pin to a Hi-Z state. A pullup resistor or current source must be provided to force the pin high. The PIO pin can be biased several volts above VDD allowing inter-operation with a system voltage which is higher than the battery voltage. Consult the Absolute Maximum Ratings table when operating the PIO pin significantly above VDD. The DS2756 turns off the PIO output driver and sets the PIO bit high when in *Sleep* mode or when DQ is low for more than t_{SLEEP}, regardless of the state of the PMOD bit.

INTERRUPT SIGNALING

The DS2756 interrupt can be configured as the Suspend interrupt that is signaled on the PIO pin, or as an Alarm Comparator interrupt (based on Current Accumulator and Temperature Alarm Comparator thresholds) that is signaled on either the PIO pin or DQ pin.

The Suspend interrupt is used to signal that the current level is greater than the user programmable Charge Suspend Threshold or less than (more negative) than the Discharge Suspend Threshold. The *Suspend interrupt* is enabled by setting one or both of the PIE bits in the Status Register. The PIE bits select one of three intervals for the Suspend Period, t_{SUS}. If either PIE bit is set, the Alarm Comparator interrupt is disabled. The Suspend interrupt event is signaled by internally clearing the PIO bit in the SFR in order to force the PIO output from high to low. The PIO output remains low in *Active* mode until the PIO bit in the SFR is written to a 1 by the host to disable the PIO output. Note that the PIO output is disabled in *Suspend* mode, allowing the PIO pin to be pulled high and ensuring the DS2756 can always signal a Suspend interrupt with a high to low transition.

The Temperature and ACR Alarm Comparator interrupt is enabled by setting the Interrupt Enable (IE) bit in the Special Feature Register with PIE cleared. When IE is set and both PIE bits are cleared, an interrupt will be signaled if the Alarm Comparator thresholds are crossed. A 1-Wire RESET always clears the IE bit. The host must re-enable interrupts by setting IE in the last transaction on the bus. Note that when either PIE bit is set, the state of IE has no effect.

The interrupt signal pin for the Alarm Comparator interrupt is selected by setting or clearing the Interrupt Output Select (IOS) bit in the Status Register. When IOS is set, the DQ pin performs Alarm Comparator interrupt signaling, when IOS is cleared, the PIO pin performs Alarm Comparator interrupt signaling. Note that when either PIE bit is set, the state of IOS has no effect.

DQ signals an Alarm Comparator interrupt condition by driving the 1-Wire bus low for t_{IL}. The DS2756 and all other 1-Wire devices present on the bus interpret this signal as a 1-Wire RESET. A Presence Pulse should be expected from all 1-Wire devices, including the DS2756 following the alarm interrupt signal. The host system can sense the alarm interrupt signal on the falling or rising edge of either the RESET or Presence Pulse.

PIO signals an Alarm Comparator interrupt by driving low. PIO remains low until the host clears the condition by writing a 1 to the PIO bit (bit 6 in the Special Feature Register). A pullup resistor or current source must be provided to force the pin high. The host must sense the alarm interrupt on the falling edge of PIO.

Table 1. PIO/DQ Pin Function

REGISTER BIT SETTING				PIO/DQ PIN FUNCTION
PIE	IOS	IE	PIO	
xx	x	x	0	PIO pin: GPIO—Output LOW
00	x	0	1	PIO pin: GPIO—Output High-Z, Input mode
00	0	1	1	PIO pin: Alarm Comparator Interrupt Output
00	1	1	0	DQ pin: Alarm Comparator Interrupt Output (low for t_{IL}) PIO pin: GPIO—Output LOW
00	1	1	1	DQ pin: Alarm Comparator Interrupt Output (low for t_{IL}) PIO pin: GPIO—Output High-Z, Input mode
01 10 11	x	x	1	PIO pin: Suspend Interrupt Output

x—Don't care.

SUSPEND THRESHOLDS

The suspend thresholds set the current level to enter and exit *Suspend* mode. The threshold levels are programmable with a magnitude range of 0 to 4mV, and are compared against the value in the Current register. Values are programmed in two's complement format with an implied sign bit in a virtual 9th bit position. The Charge Suspend Threshold register is always a positive value. The Discharge Suspend Threshold register is always a negative value.

The thresholds define an inclusive, continuous range of currents in which the DS2756 enters or re-enters *Suspend* mode from *Active* mode. The Charge Suspend Threshold represents the minimum measured charge current which will cause the DS2756 to transition modes. The Discharge Suspend Threshold represents the minimum discharge current which will cause the DS2756 to transition modes.

The user values of the suspend thresholds are programmed into two bytes located within EEPROM block 0. These memory locations serve as current threshold values only when either PIE bit is set, and can be used as general purpose EEPROM if PIE = 00b. A copy command is required to save the byte values to EEPROM. See the *Memory* section for information on copying shadow RAM to EEPROM.

Figure 9. Charge Suspend Threshold Format

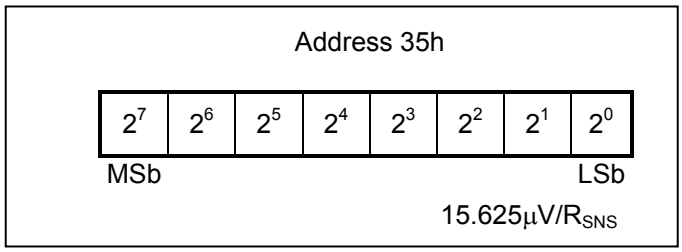
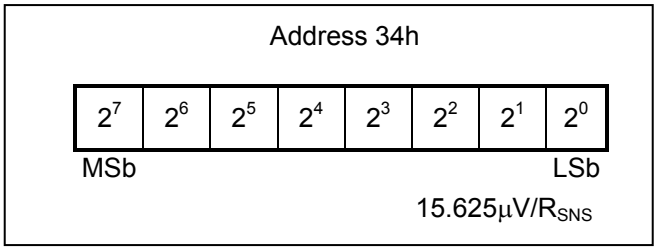


Figure 10. Discharge Suspend Threshold Format



ALARM COMPARATORS AND INTERRUPT THRESHOLDS

Alarm interrupt threshold values can be programmed by the user in the designated SRAM memory registers in the formats and locations found in Figure 11. Since these thresholds are located in SRAM memory, they must be reprogrammed if a loss of power to the DS2756 occurs. The DS2756 generates an alarm interrupt to indicate that one of the following events has occurred:

- Accumulated Current ≥ Current Accumulator Interrupt High Threshold
- Accumulated Current ≤ Current Accumulator Interrupt Low Threshold
- Temperature ≥ Temperature Interrupt High Threshold
- Temperature ≤ Temperature Interrupt Low Threshold

The host may then poll the DS2756 to determine which threshold has been met or exceeded.

Figure 11. Alarm Interrupt Threshold Register Formats

Current Accumulator Interrupt High Threshold

MSB-Address 80h

S	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}

MSb LSb

LSB-Address 81h

2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

MSb LSb

Units: 6.25µVhrs

Current Accumulator Interrupt Low Threshold

MSB-Address 82h

S	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}

MSb LSb

LSB-Address 83h

2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

MSb LSb

Units: 6.25µVhrs

Temperature Interrupt High Threshold

Address 84h

S	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

MSb LSb

Units: 1.0°C

Temperature Interrupt Low Threshold

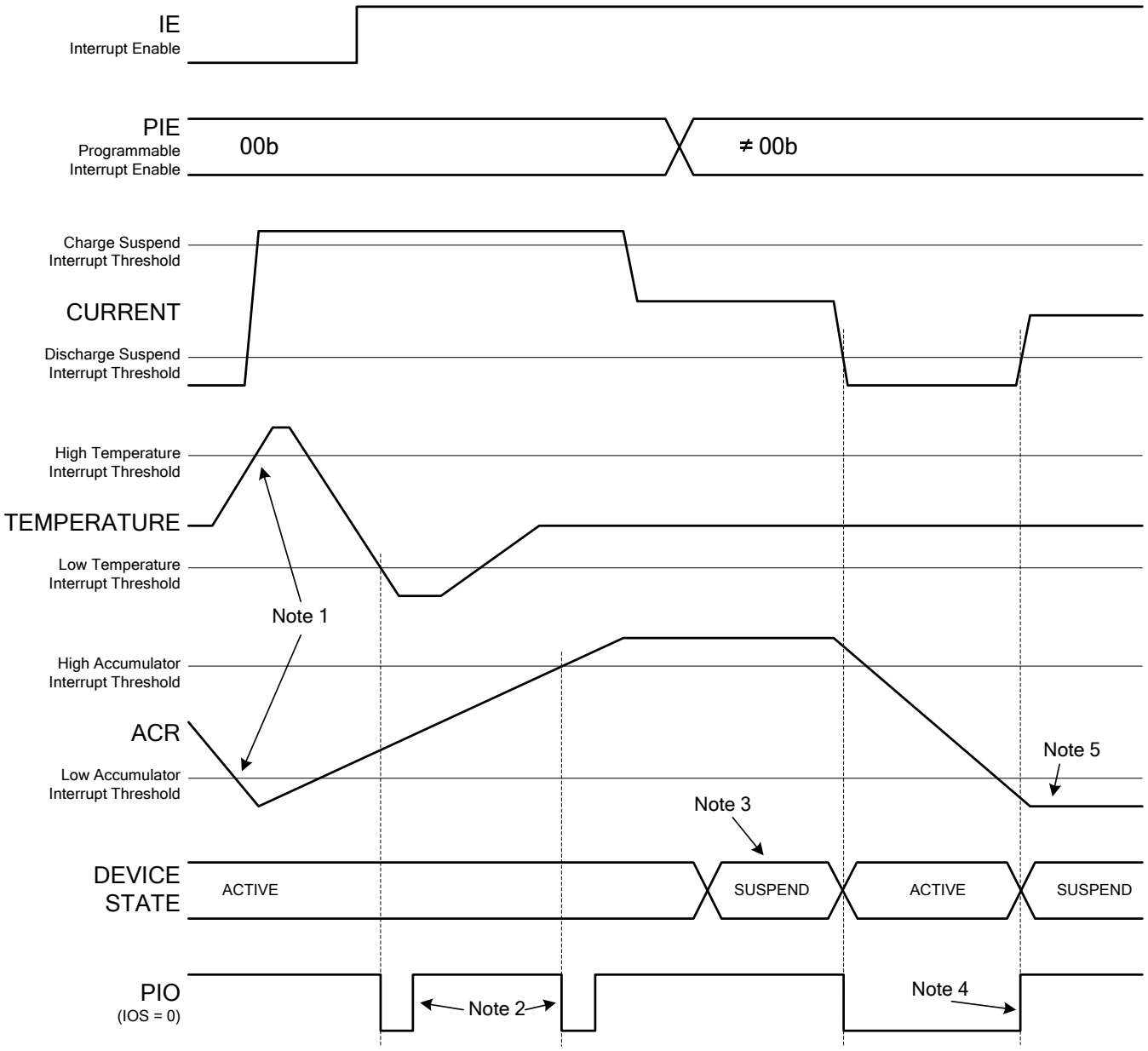
Address 85h

S	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

MSb LSb

Units: 1.0°C

Figure 12. Alarm And Suspend Mode Operating Diagram



Note 1. Threshold violations do not generate alarm interrupts until the Interrupt Enable (IE) bit is set.
Note 2. PIO Interrupts are cleared by resetting the PIO bit in the Special Feature Register.
Note 3. SUSPEND state shown in this timing diagram refers to the DS2756 cycling between Active and Suspend mode at a rate determined by the PIE bit settings. Suspend state is entered by setting PIE bits to a non-zero value, setting PMOD=1, and then driving DQ low for longer than 2s.
Note 4. Interrupts on PIO not reset by software are automatically cleared when entering suspend mode.
Note 5. Alarm threshold violations do not generate interrupts if Suspend mode is enabled (PIE ≠ 00b).

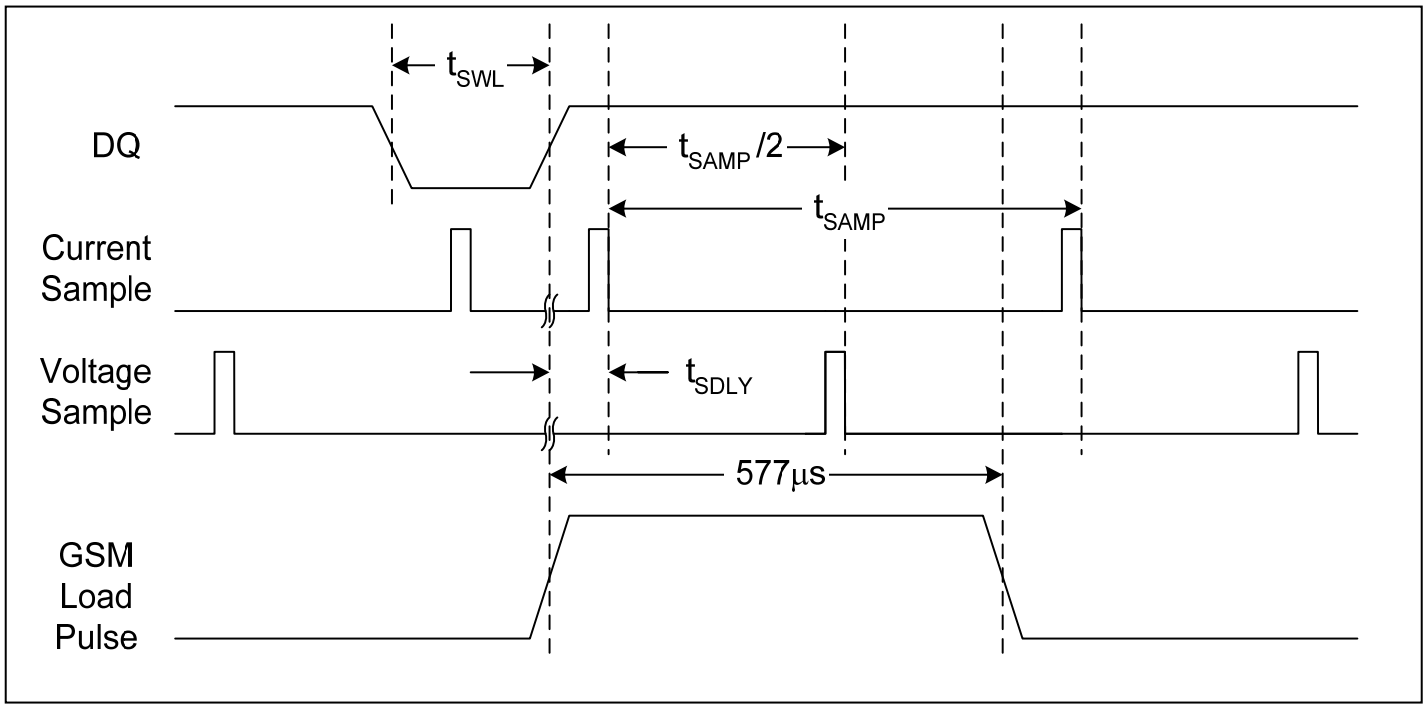
SNAPSHOT MODE

Measurement of the current and voltage can be synchronized to a system event with the Snapshot mode. Triggering a Snapshot event causes the ADC to abandon the current conversion and capture one current and one voltage sample. The Snapshot results are reported in the Current and Voltage registers for retrieval by the host. Normal current, voltage and temperature measurements and current accumulation resume immediately following a Snapshot event, though the Snapshot current and voltage values persist until the host system writes the SNAP bit in the Special Function Register to a 0. Since the snapshot mode disrupts the continuity of the coulomb counting process, it should be used sparingly.

The Sync Function Command [D2h] signals the ADC control to expect a Snapshot trigger on DQ. Following the Sync command, the host can trigger a Snapshot event by toggling the DQ line. Synchronization occurs on the rising edge of the DQ high to low to high pulse. The Snapshot mode can be abandoned by sending a 1-Wire Reset instead of the synchronization pulse. The rising edge DQ trigger is formed by the first data bit after issuing the Sync Function command. A full byte can be issued, but the rising edge of the first bit sets the trigger point. The SNAP bit is set after the rising edge trigger. Timing is not critical and could be several 100µs later since it cannot be read quickly via 1-Wire. If a 1-Wire reset is issued instead of a data bit, then the Snapshot is abandoned (SNAP bit not set).

The Snapshot Synchronization Timing in Figure 13 illustrates the timing of the Snapshot current and voltage sample apertures relative to the DQ rising edge trigger and one timeslot GSM power amp load pulse. In the diagram, $t_{SAMP} = 1/ f_{SAMP} = 1456^{-1} = 687\mu s$. The current and voltage measurements are taken 343µs apart but within a single GSM timeslot.

Figure 13. Snapshot Synchronization Timing



MEMORY

The DS2756 has a 256-byte linear address space with registers for instrumentation, status, and control in the lower 32 bytes, with lockable EEPROM and SRAM memory occupying portions of the remaining address space. All EEPROM and SRAM memory is general-purpose except addresses 31h, 33h, 34h and 35h, which should be written with the default values for the Status Register, Accumulation Bias Register, Charge Suspend Threshold and Discharge Suspend Threshold, respectively. If the Suspend interrupt is not used, addresses 34h and 35h can be used as general-purpose EEPROM. When the MSB of any two-byte register is read, the MSB and LSB values are latched and held for the duration of the Read Data command. This prevents updates during the read to ensure synchronization between the two register bytes. For consistent results, always read the MSB and the LSB of a two-byte register during the same Read Data command sequence. In describing register control and status bits, the terms set and clear refer to internal operations which manipulate bit values. The terms read and write refer to 1-Wire access to the bit values. Several bits are set internally but require the host system to write them to a 0 value.

EEPROM memory is shadowed by RAM to eliminate programming delays between writes and to allow the data to be verified by the host system before being copied to EEPROM. The Read Data and Write Data protocols to/from EEPROM memory addresses access the shadow RAM. The Recall Data function command transfers data from the EEPROM to the shadow RAM. The Copy Data function command transfers data from the shadow RAM to the EEPROM and requires t_{EEC} to complete programming of the EEPROM cells. In unlocked EEPROM blocks, writing data updates shadow RAM. In locked EEPROM blocks, the Write Data command is ignored. The Copy Data function command copies the contents of shadow RAM to EEPROM in an unlocked block of EEPROM but has no effect on locked blocks. The Recall Data function command copies the contents of a block of EEPROM to shadow RAM regardless of whether the block is locked or not.

Figure 14. EEPROM Access via Shadow RAM

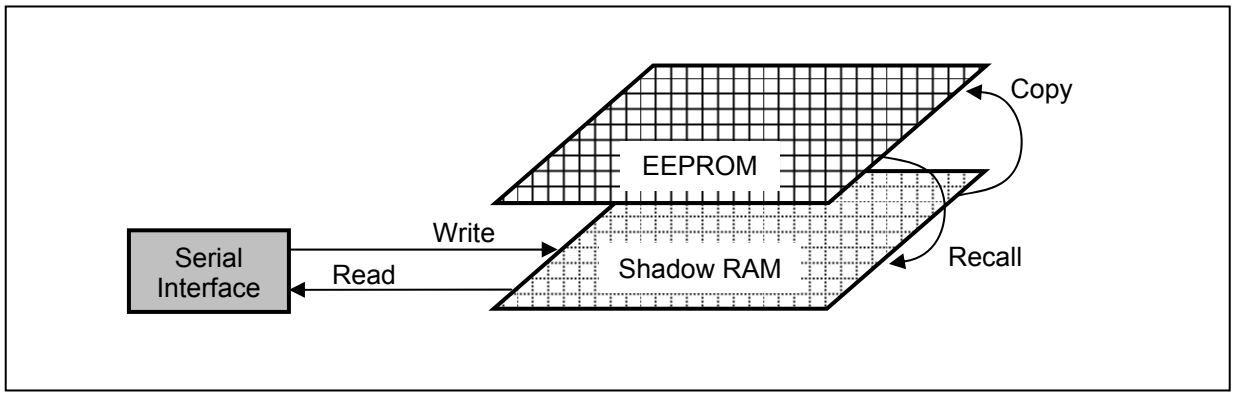


Table 2. Memory Map

ADDRESS (HEX)	DESCRIPTION	READ/WRITE
00	Reserved	
01	Status Register	R
02 to 06	Reserved	
07	EEPROM Register	R/W
08	Special Feature Register	R/W
09 to 0B	Reserved	
0C	Voltage Register MSB	R
0D	Voltage Register LSB	R
0E	Current Register MSB	R
0F	Current Register LSB	R
10	Accumulated Current Register MSB	R/W
11	Accumulated Current Register LSB	R/W
12 to 17	Reserved	
18	Temperature Register MSB	R
19	Temperature Register LSB	R
1A	Average Current Register MSB	R
1B	Average Current Register LSB	R
1C to 1F	Reserved	
20 to 3F	EEPROM, block 0	R/W*
40 to 5F	EEPROM, block 1	R/W*
60 to 7F	EEPROM, block 2	R/W*
80 to 8F	SRAM	R/W
90 to FF	Reserved	

**Each EEPROM block is read/write until locked by the LOCK command, after which it is read-only.*

STATUS REGISTER

The default values for the Status Register bits are stored in lockable EEPROM in the corresponding bits of address 31h. A Recall Data command for EEPROM block 1 recalls the default values into the Status Register bits. The format of the Status Register is shown in Figure 15. The function of each bit is described in detail in the following paragraphs. Note that all bits are Read Only.

Figure 15. STATUS REGISTER FORMAT

Address 01h

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
PIE1	PIE0	PMOD	RNAOP	UVEN	IOS	OBEN	OVD

PIE1, PIE0—Programmable Suspend Interrupt Enable. A non zero value in these bits enables the DS2756 to enter *Suspend* mode, and sets the Suspend Period (t_{SUS}) for the low power oscillator timeout. A value of 00b disables the DS2756 from entering *Suspend* mode and allows the DS2756 to enter *Sleep* mode.

Table 3. SUMMARY OF SUSPEND MODES

PIE1	PIE0	SAMPLE RATE WHILE IN SUSPEND MODE	AVERAGE IDD WHILE IN SUSPEND MODE
0	0	Suspend mode disabled	Suspend mode disabled
0	1	2.0Hz	$\frac{(500ms \times I_{SUSPEND}) + (90ms \times I_{ACTIVE})}{590ms}$
1	0	1.0Hz	$\frac{(1000ms \times I_{SUSPEND}) + (90ms \times I_{ACTIVE})}{1090ms}$
1	1	0.5Hz	$\frac{(2000ms \times I_{SUSPEND}) + (90ms \times I_{ACTIVE})}{2090ms}$

The desired default value should be set in bit 6 and bit 7 of address 31h. The factory default is 00b.

PMOD—Power Mode Enable. A value of 1 in this bit enables the DS2756 to enter *Sleep* mode or *Suspend* mode. A value of 0 disables the DS2756 from entering the *Sleep* or *Suspend* mode. When PMOD is 0, only *Active* mode operation is allowed. The desired default value must be set in bit 5 of address 31h. The factory default is 0.

RNAOP—Read Net Address Opcode. A value of 0 in this bit sets the opcode for the Read Net Address command to 33h, while a 1 sets the opcode to 39h. This bit is read-only. The desired default value should be set in bit 4 of address 31h. The factory default is 0.

UVEN—Undervoltage *Sleep* Enable. A value of 1 in UVEN along with a value of 1 in PMOD enables the DS2756 to enter *Sleep* mode when the voltage on V_{IN} drops below undervoltage threshold V_{UV} for t_{UVD} (cell depletion). A value of 0 disables the DS2756 from entering the *Sleep* mode due to undervoltage events. The desired default value must be set in bit 3 of address 31h. The factory default is 0.

IOS—Interrupt output select. IOS set to a 1 selects the DQ alarm interrupt signaling method for the Alarm Comparator interrupt. IOS cleared to 0 selects the PIO alarm interrupt signaling method. The IE bit must be set and PIE bits cleared to signal an Alarm Comparator interrupt using either method. The desired default value must be set in bit 2 of address 31h. The factory default is 0.

OBEN—Offset Blanking Enable. A value of 1 in this bit location enables the offset blanking function described in the Current Accumulation section. If set to 0, the offset blanking function is disabled. The desired default value must be set in bit 1 of address 31h. The factory default is 0.

OVD—Overdrive Timing Enable. A value of 1 in this bit location enables the Overdrive 1-Wire timings. If set to 0, the Regular mode timings are enabled. The desired bit value must be written to bit 1 of address 31h, (an EEPROM block 0 location), then recalled before any change to the 1-Wire speed becomes effective. A power-on reset forces a recall of settings from EEPROM block 0. The factory default in bit 1 of address 31h is 0 (Standard 1-Wire timing).

X—Reserved Bits.

EEPROM REGISTER

The format of the EEPROM Register is shown in Figure 16. The function of each bit is described in detail in the following paragraphs.

Figure 16. EEPROM Register Format

Address 07h

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
EEC	LOCK	X	X	X	BL2	BL1	BL0

EEC—EEPROM Copy Flag. A 1 in this read-only bit indicates that a Copy Data command is in progress. While this bit is high, writes to EEPROM addresses are ignored. A 0 in this bit indicates that data can be written to unlocked EEPROM blocks.

LOCK—EEPROM Lock Enable. When this bit is 0, the Lock command is ignored. Writing a 1 to this bit enables the Lock command. After the Lock command is executed, the LOCK bit is reset to 0. The factory default is 0.

BL2—EEPROM Block 2 Lock Flag. A 1 in this read-only bit indicates that EEPROM block 2 (addresses 60h to 7Fh) is locked (read-only), while a 0 indicates block 1 is unlocked (read/write).

BL1—EEPROM Block 1 Lock Flag. A 1 in this read-only bit indicates that EEPROM block 1 (addresses 40h to 5Fh) is locked (read-only), while a 0 indicates block 1 is unlocked (read/write).

BL0—EEPROM Block 0 Lock Flag. A 1 in this read-only bit indicates that EEPROM block 0 (addresses 20h to 3Fh) is locked (read-only), while a 0 indicates block 0 is unlocked (read/write).

X—Reserved Bits.

SPECIAL FEATURE REGISTER

The format of the Special Feature Register is shown in Figure 17. The function of each bit is described in detail in the following paragraphs.

Figure 17. Special Feature Register Format

Address 08h

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
POR	PIO	X	X	X	IE	X	SNAP

POR—POR Indicator bit. This bit is set to a 1 when the DS2756 experiences a power-on-reset (POR) event. To use the POR bit to detect a power-on-reset, the POR bit must be set to a 0 by the host system upon power-up and after each subsequent occurrence of a POR. This bit is read/write to 0.

PIO—PIO Pin Sense and Control. See the *Programmable I/O* section for details on this read/write bit.

IE—Interrupt Enable. A value of 1 in this bit location enables Alarm Comparator interrupt signaling to the host system. When IE is 0, Alarm Comparator interrupt signaling is disabled and the alarm comparator registers are available as SRAM and have no effect on device operation. IE bit is read/write to 1. IE is cleared to 0 by a 1-Wire RESET on DQ.

SNAP—Snapshot Control. This bit is set to a 1 immediately after the DS2756 executes a Snapshot conversion pair. SNAP = 1 indicates that the Current and Voltage registers contain Snapshot results. While SNAP = 1, the Snapshot results persist in the Current and Voltage registers until the SNAP bit is written to a 0 by the host system. This bit is read/write to 0.

X—Reserved Bits.

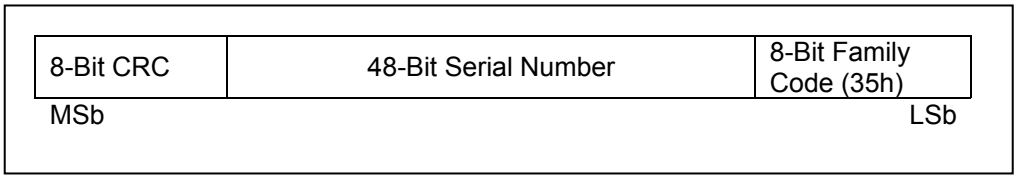
1-Wire BUS SYSTEM

The 1-Wire bus is a system that has a single bus master and one or more slaves. A multidrop bus is a 1-Wire bus with multiple slaves. A single-drop bus has only one slave device. In all instances, the DS2756 is a slave device. The bus master is typically a microprocessor in the host system. The discussion of this bus system consists of four topics: 64-Bit Net Address, Hardware Configuration, Transaction Sequence, and 1-Wire Signaling.

64-BIT NET ADDRESS

Each DS2756 has a unique, factory-programmed 1-Wire net address that is 64 bits in length. The first 8 bits are the 1-Wire family code (35h for DS2756). The next 48 bits are a unique serial number. The last 8 bits are a CRC of the first 56 bits (see Figure 18). The 64-bit net address and the 1-Wire I/O circuitry built into the device enable the DS2756 to communicate through the 1-Wire protocol detailed in the 1-Wire Bus System section of this data sheet.

Figure 18. 1-Wire Net Address Format

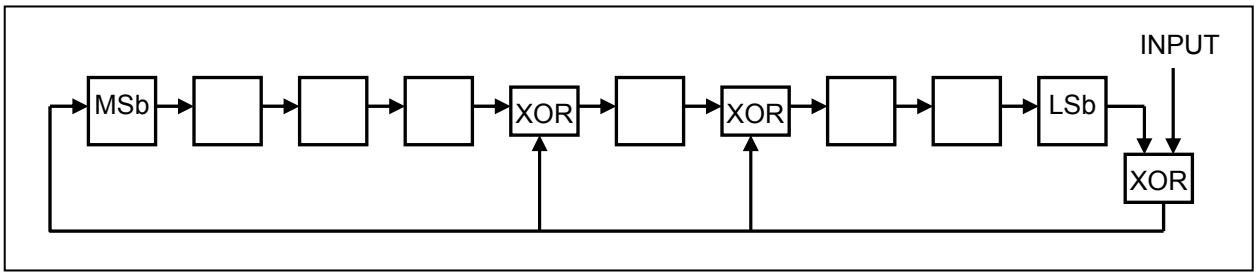


CRC GENERATION

The DS2756 has an 8-bit CRC stored in the most significant byte of its 1-Wire net address. To ensure error-free transmission of the address, the host system can compute a CRC value from the first 56 bits of the address and compare it to the CRC from the DS2756. The host system is responsible for verifying the CRC value and taking action as a result. The DS2756 does not compare CRC values and does not prevent a command sequence from proceeding as a result of a CRC mismatch. Proper use of the CRC can result in a communication channel with a very high level of integrity.

The CRC can be generated by the host using a circuit consisting of a Shift Register and XOR gates as shown in Figure 19, or it can be generated in software. Additional information about the Dallas 1-Wire CRC is available in Application Note 27: *Understanding and Using Cyclic Redundancy Checks with Dallas Semiconductor iButton® Products*.

Figure 19. 1-Wire CRC Generation Block Diagram



In the circuit in Figure 19, the shift bits are initialized to 0. Then, starting with the least significant bit of the family code, one bit at a time is shifted in. After the 8th bit of the family code has been entered, then the serial number is entered. After the 48th bit of the serial number has been entered, the Shift Register contains the CRC value.

HARDWARE CONFIGURATION

Because the 1-Wire bus has only a single line, it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1-Wire bus must connect to the bus with open-drain or tri-state output drivers. The DS2756 uses an open-drain output driver as part of the bidirectional interface circuitry shown in Figure 20. If a bidirectional pin is not available on the bus master, separate output, and input pins can be connected together.

The 1-Wire bus must have a pullup resistor at the bus-master end of the bus. For short line lengths, the value of this resistor should be approximately 5kΩ. The idle state for the 1-Wire bus is high. If, for any reason, a bus transaction must be suspended, the bus must be left in the idle state in order to properly resume the transaction

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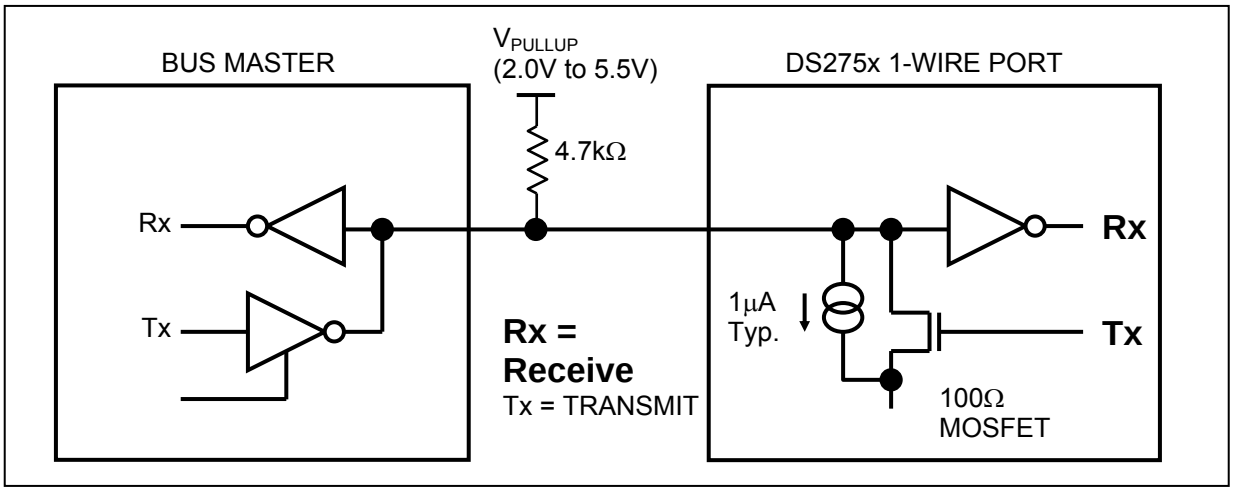
later. If the bus is left low for more than 120µs, slave devices on the bus begin to interpret the low period as a reset pulse, effectively terminating the transaction.

Figure 20. Typical 1-Wire Bus Interface Circuitry



The pullup must be disabled to allow the DS2756 to enter *Suspend* mode. The internal pulldown on the DS2756 DQ input ensures that DQ will be pulled to a logic low when the pullup is simply disconnected. With a microcontroller, the pullup resistor can be connected between a general purpose port pin and the DS2756 DQ terminal as shown in Figure 1. The GPIO pin, labeled Pullup Control, can be driven high for *Active* mode. The pin labeled Data I/O is used bidirectionally for serial communication. When *Standby* mode is desired, the Pullup Control pin can be driven low or floated in the high-Z state. If the current reading falls within the range of the suspend thresholds, the DS2756 will enter *Suspend* if configured to do so (PMOD = 1 and PIE ≠ 00).

TRANSACTION SEQUENCE

The protocol for accessing the DS2756 through the 1-Wire port is as follows:

- Initialization
- Net Address Command
- Function Command
- Transaction/Data

The sections that follow describe each of these steps in detail.

All transactions of the 1-Wire bus begin with an initialization sequence consisting of a reset pulse transmitted by the bus master followed by a presence pulse simultaneously transmitted by the DS2756 and any other slaves on the bus. The presence pulse tells the bus master that one or more devices are on the bus and ready to operate. For more details, see the *I/O Signaling* section.

NET ADDRESS COMMANDS

Once the bus master has detected the presence of one or more slaves, it can issue one of the net address commands described in the following paragraphs. The name of each command is followed by the 8-bit opcode for that command in square brackets. Figure 21 presents a transaction flowchart of the net address commands.

Read Net Address [33h or 39h]. This command allows the bus master to read the DS2756's 1-Wire net address. This command can only be used if there is a single slave on the bus. If more than one slave is present, a data collision occurs when all slaves try to transmit at the same time (open drain produces a wired-AND result). The RNAOP bit in the Status Register selects the opcode for this command, with RNAOP = 0 indicating 33h and RNAOP = 1 indicating 39h.

Match Net Address [55h]. This command allows the bus master to specifically address one DS2756 on the 1-Wire bus. Only the addressed DS2756 responds to any subsequent function command. All other slave devices ignore

the function command and wait for a reset pulse. This command can be used with one or more slave devices on the bus.

Skip Net Address [CCh]. This command saves time when there is only one DS2756 on the bus by allowing the bus master to issue a function command without specifying the address of the slave. If more than one slave device is present on the bus, a subsequent function command can cause a data collision when all slaves transmit data at the same time.

Search Net Address [F0h]. This command allows the bus master to use a process of elimination to identify the 1-Wire net addresses of all slave devices on the bus. The search process involves the repetition of a simple three-step routine: read a bit, read the complement of the bit, then write the desired value of that bit. The bus master performs this simple three-step routine on each bit location of the net address. After one complete pass through all 64 bits, the bus master knows the address of one device. The remaining devices can then be identified on additional iterations of the process. See Chapter 5 of the *Book of DS19xx iButton Standards* for a comprehensive discussion of a net address search, including an actual example. This publication can be found on the Maxim/Dallas website at www.maxim-ic.com.

FUNCTION COMMANDS

After successfully completing one of the net address commands, the bus master can access the features of the DS2756 with any of the function commands described in the following paragraphs. The name of each function is followed by the 8-bit opcode for that command in square brackets.

Read Data [69h, XX]. This command reads data from the DS2756 starting at memory address XX. The LSb of the data in address XX is available to be read immediately after the MSb of the address has been entered. Because the address is automatically incremented after the MSb of each byte is received, the LSb of the data at address XX + 1 is available to be read immediately after the MSb of the data at address XX. If the bus master continues to read beyond address FFh, the DS2756 outputs logic 1 until a reset pulse occurs. Addresses labeled “reserved” in the memory map contain undefined data. The Read Data command can be terminated by the bus master with a reset pulse at any bit boundary.

Write Data [6Ch, XX]. This command writes data to the DS2756 starting at memory address XX. The LSb of the data to be stored at address XX can be written immediately after the MSb of the address has been entered. Because the address is automatically incremented after the MSb of each byte is written, the LSb to be stored at address XX + 1 can be written immediately after the MSb to be stored at address XX. If the bus master continues to write beyond address FFh, the DS2756 ignores the data. Writes to read-only addresses, reserved addresses and locked EEPROM blocks are ignored. Incomplete bytes are not written. Writes to unlocked EEPROM blocks are to shadow RAM rather than EEPROM. See the *Memory* section for more details.

Copy Data [48h, XX]. This command copies the contents of shadow RAM to EEPROM for the 32-byte EEPROM block containing address XX. Copy Data commands that address locked blocks are ignored. While the Copy Data command is executing, the EEC bit in the EEPROM Register is set to 1 and writes to EEPROM addresses are ignored. Reads and writes to non-EEPROM addresses can still occur while the copy is in progress. The Copy Data command execution time, t_{EEC}, is 2ms typical and starts after the last address bit is transmitted.

Recall Data [B8h, XX]. This command recalls the contents of the 32-byte EEPROM block containing address XX to shadow RAM.

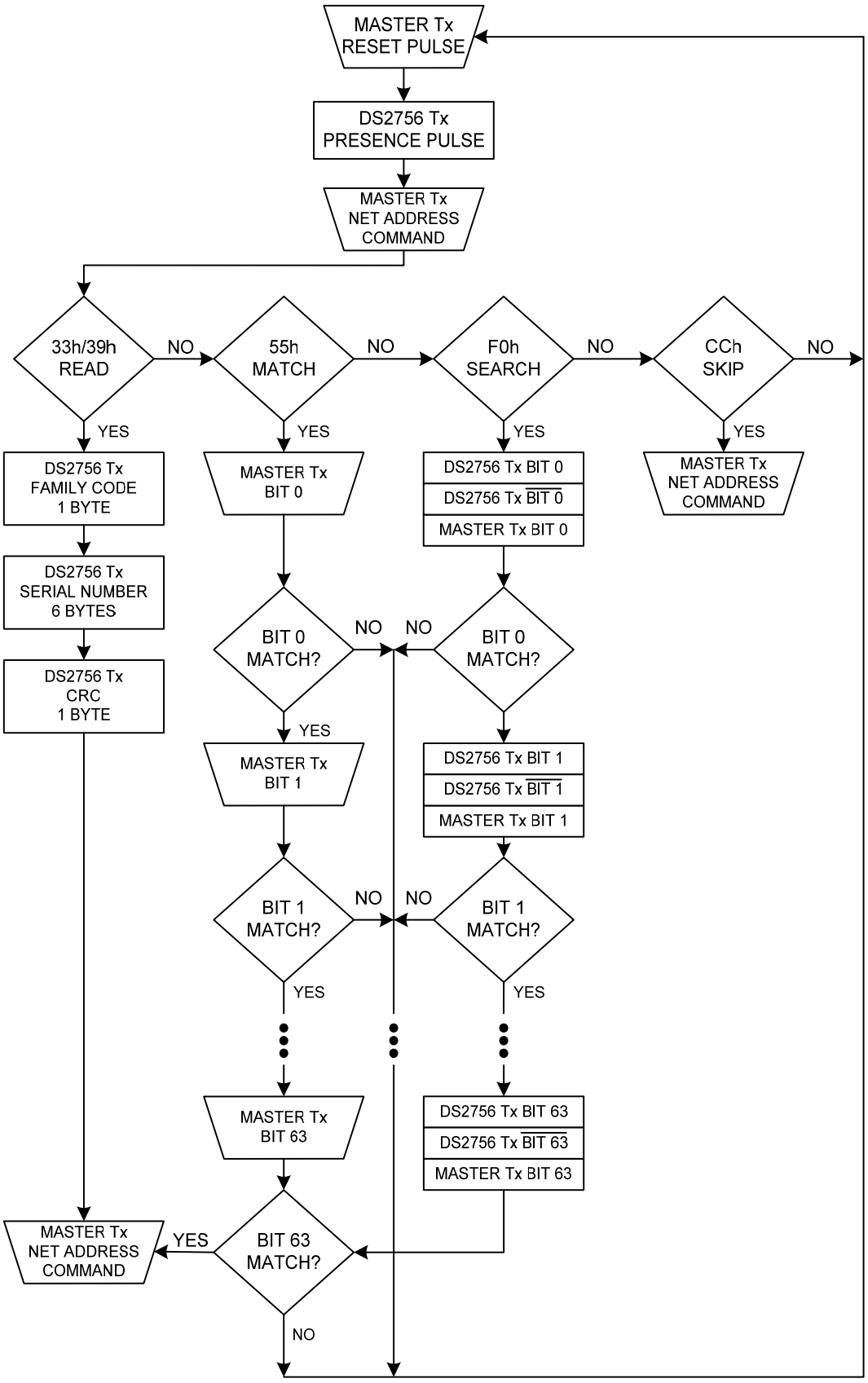
Lock [6Ah, XX]. This command locks (write-protects) the 32-byte block of EEPROM memory containing memory address XX. The LOCK bit in the EEPROM Register must be set to l before the Lock command is executed. If the LOCK bit is 0, the Lock command has no effect. The Lock command is permanent; a locked block can never be written again.

Sync [D2h, XX]. This command allows the bus to be used to trigger current and voltage Snapshot readings. Following the issue of the Sync command, the bus returns to the idle state awaiting the measurement trigger. When the bus transitions high to low and then low to high on the first data bit issued after the command byte, the Snapshot measurements are performed. Only one bit of the data byte is required to trigger the Snapshot measurements. One Snapshot command must be issued for each Snapshot trigger event.

Table 4. FUNCTION COMMANDS

COMMAND	DESCRIPTION	COMMAND PROTOCOL	BUS STATE AFTER COMMAND PROTOCOL	BUS DATA
Read Data	Reads data from memory starting at address XX	69h, XX	Master Rx	Up to 256 bytes of data
Write Data	Writes data to memory starting at address XX	6Ch, XX	Master Tx	Up to 256 bytes of data
Copy Data	Copies shadow RAM data to EEPROM block containing address XX	48h, XX	Bus idle	None
Recall Data	Recalls EEPROM block containing address XX to shadow RAM	B8h, XX	Bus idle	None
Lock	Permanently locks the block of EEPROM containing address XX	6Ah, XX	Bus idle	None
Sync	Arms the Snapshot Measurement Mode	D2h, XX	Bus idle	None

Figure 21. Net Address Command Flow Chart



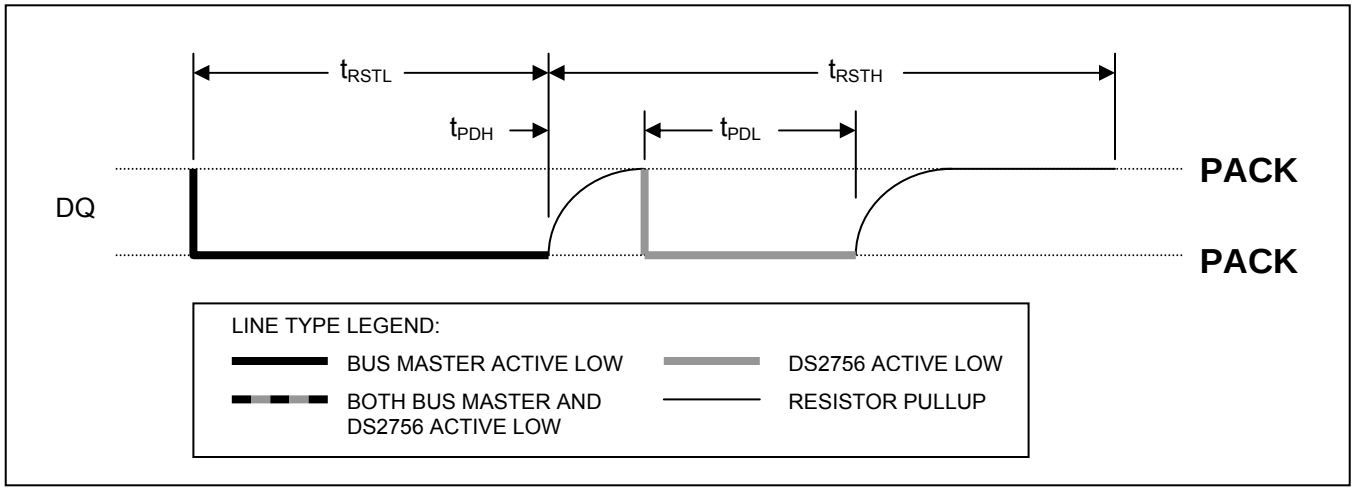
I/O SIGNALING

The 1-Wire bus requires strict signaling protocols to ensure data integrity. The four protocols or signaling types used are:

1) Initialization sequence (Reset Pulse followed by Presence Pulse)
2) Write 0
3) Write 1
4) Read Data

All signaling is initiated by the bus master. Except for the Presence Pulse, all falling edges are created by the bus master. The initialization sequence required to begin communication with the DS2756 is shown in Figure 22. A presence pulse following a reset pulse indicates the DS2756 is ready to accept a net address command. The bus master transmits (Tx) a reset pulse for t_{RSTL}. The bus master then releases the line and goes into receive mode (Rx). The 1-Wire bus line is then pulled high by the pullup resistor. After detecting the rising edge on the DQ pin, the DS2756 waits for t_{PDH} and then transmits the Presence Pulse for t_{PDL}.

Figure 22. 1-Wire Initialization Sequence



WRITE-TIME SLOTS

A write-time slot is initiated when the bus master pulls the 1-Wire bus from a logic-high (inactive) level to a logic-low level. There are two types of write-time slots: write 1 and write 0. All write-time slots must be t_{SLOT} in duration with a 1µs minimum recovery time, t_{REC}, between cycles.

The bus master generates a write 1 time slot by pulling 1-Wire bus line low for t_{LOW1} and then releasing it. The bus must be pulled high within 15µs in Standard mode or 2µs in Overdrive mode after the start of the write-time slot. The bus master generates a write 0 time slot by pulling 1-Wire bus line low and then holding it low for t_{LOW0}, or up to the end of the write-time slot.

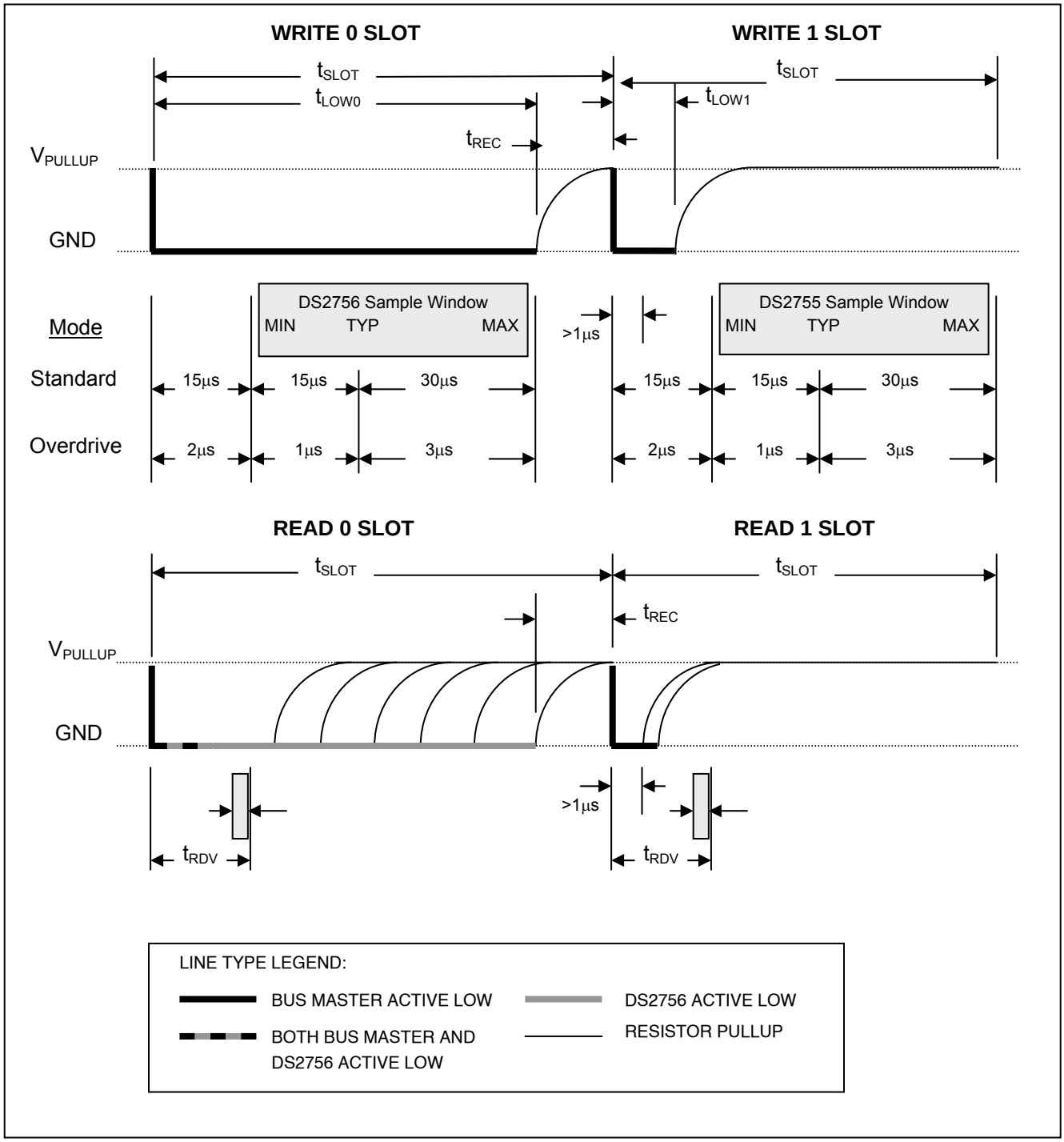
The DS2756 samples the 1-Wire bus after the line falls, sampling occurs between 15µs and 60µs in Standard mode and between 2µs and 6µs in Overdrive mode. If the line is high when sampled by the DS2756, a write 1 occurs, that is, the DS2756 accepts the bit value to be a 1. If the line is low when sampled, a write 0 occurs, that is, the DS2756 accepts the bit value to be a 0. See Figure 23 for more information.

READ-TIME SLOTS

A read-time slot is initiated when the bus master pulls the 1-Wire bus line from a logic-high level to a logic-low level. The bus master generated read-time slot results in a read 1 and read 0 depending on the data presented by the DS2756. All read-time slots must be t_{SLOT} in duration with a 1µs minimum recovery time, t_{REC}, between cycles.

The bus master initiates a read-time slot by pulling the bus line low for at least 1µs and then releasing it to allow the DS2756 to present valid data. The DS2756 generates a read 0 by holding the line low. The line is held low for at least the Read Data Valid time (t_{RDV}) from the start of the read-time slot. The DS2756 releases the bus line and allows it to be pulled high by the external pullup resistor some time after t_{RDV} but before the end of the read-time slot. A read 1 is generated by not holding the line low after the time slot is initiated by the master. The line is allowing it to be pulled high as soon as it is released by the master. The bus master must sample the bus after initializing the time slot and before t_{RDV} to read the data value transmitted by the DS2756. Sampling should occur as close to t_{RDV} as possible to allow for the rise time of the passive pullup 1-Wire bus. See Figure 23 for more information.

Figure 23. 1-Wire Write- And Read-Time Slots



PACKAGE INFORMATION

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PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
8 TSSOP	H8+2	**21-0175**

REVISION HISTORY

REVISION DATE	DESCRIPTION	PAGES CHANGED
051209	Changed the V_{DD} maximum operating range in the *Electrical Characteristics* table to 4.5V.	2, 3
	Added "V_{IN} pin is limited to V_{DD} voltage" text in the *Voltage Measurement* section.	9

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