

DALLAS

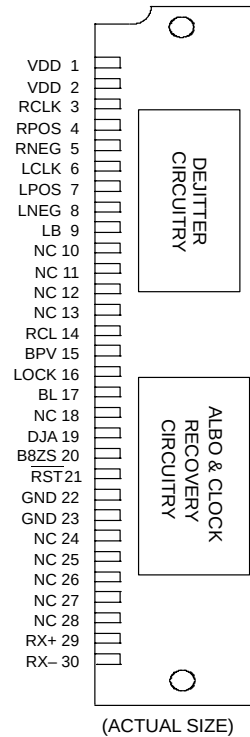
SEMICONDUCTOR

DS2291 T1 Long Loop Stik

FEATURES

- Recovers clock and data off of T1 lines from 0 to 6,000 feet in length
- +0 to -30dBX receiver sensitivity
- Built-in Automatic Line Build Out (ALBO) circuitry; no tuning or external components required
- Dejitters the recovered clock and data
- Meets TR 62411 (Dec. 1990) for jitter tolerance and attenuation
- Companion to the DS2290 T1 Isolation Stik
- Connects to a standard 30-pin single in-line connector
- Single +5V supply
- Compatible with the DS2180A or DS2141A T1 Transceivers

PIN ASSIGNMENT



DESCRIPTION

The DS2291 T1 Long Loop Stik contains all the circuitry necessary to recover clock and data from a T1 line. The DS2291 contains an Automatic Line Build Out (ALBO) circuit that allows it to adapt to T1 lines varying in length from 0 to 6,000 feet. It also will dejitter the recovered clock and data according to the jitter attenuation curves outlined in AT&T Communications Document TR 62411 (Accunet* T1.5 Service Description and Interface specification - December 1990). Applications area include Channel Service Units (CSU), T1 monitoring equipment, and T1 test equipment.

OVERVIEW

The DS2291 contains onboard ALBO circuitry that allows it to recover clock and data from T1 lines up to 6,000 feet in length. (See Figure 1.) Unlike alternative methods of clock and data recovery from T1 lines, the DS2291 does not require any tuning, nor does it need any additional external circuitry. The state of the LOCK pin indicates whether the DS2291 has been able to phase and frequency lock to the incoming T1 signal. If the LOCK pin is high, the DS2291 is properly locked onto the incoming signal. The DS2291 meets the latest T1 specification for jitter tolerance. The jitter tolerance curve in Figure 2 is applicable over the full dynamic input range of the DS2291.

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Once the Long Loop Stik has recovered data from the T1 line, it can decode B8ZS code words and check for bipolar violations and carrier loss. If the B8ZS pin is tied high, the DS2291 will automatically replace incoming B8ZS code words with eight zeros. If the B8ZS pin is tied low or left open, no replacement occurs. Bipolar violations are reported via the BPV pin. The BPV pin will transition high for a full T1 bit period (648 ns) each time a violation is detected. Bipolar violations inherent in B8ZS code words are not reported if the B8ZS pin is tied high. The DS2291 also checks for carrier loss. The RCL pin will transition high when the DS2291 detects 192 consecutive zeros at RX+ and RX-.

The recovered clock and data are passed to the dejitter circuitry. If the DJA is tied low or left open, the DS2291 will attenuate the jitter present at RX+ and RX- according to the curves outlined in Figure 3. These curves meet the latest T1 specifications. If the DJA pin is tied high, the DS2291 will not attenuate jitter. Hence, all the jitter inherent in the signal at RX+ and RX- will be passed to RCLK, RPOS, and RNEG. If the recovered clock at RCLK is used to transmit data onto T1 lines, it is recommended that the dejitter circuitry be enabled (DJA = 0). The dejitter circuitry contains a 128-bit buffer. This buffer can be recentered on command via the $\overline{\text{RST}}$ pin. In normal applications, the $\overline{\text{RST}}$ is left open or tied high. The Buffer Limit (BL) output will transition high when the

DS2291 is receiving more than 120 unit intervals peak-to-peak (Ulp) of jitter at RX+ and RX-. As long as the incoming jitter is less than 120Ulp, the BL pin will remain low.

The DS2291 contains a data mux that allows data to be routed from either the T1 recovery circuitry or from a local source. The mux is helpful locating faults in a system. For example, it could be used to implement a "local" loopback.

Two typical applications with the DS2291 are shown in Figure 4 and Figure 5. In both applications, the DS2291 is used to recover data from T1 lines up to 6,000 feet in length. The application in Figure 4 is with an unprotected interface; it might be used in T1 test equipment. The application in Figure 5 is with the DS2290 T1 Isolation Stik, which provides all the necessary protection as required by FCC Part 68. This could be used in a Channel Service Unit (CSU) or in similar types of equipment in which full surge and isolation protection is required.

SINGLE IN-LINE CONNECTOR

The DS2291 is designed to connect directly into a 30-pin single in-line connector. These connectors are available from a number of vendors.

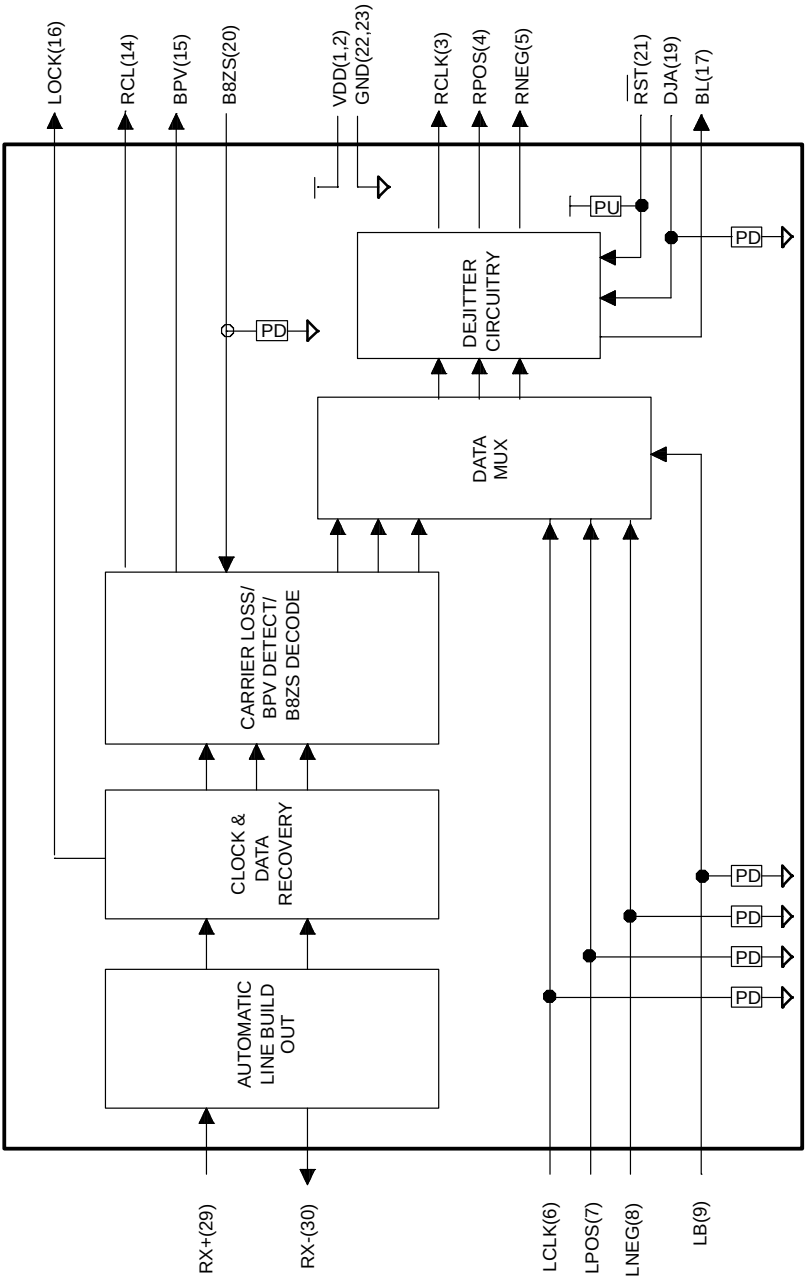
PIN DESCRIPTION Table 1

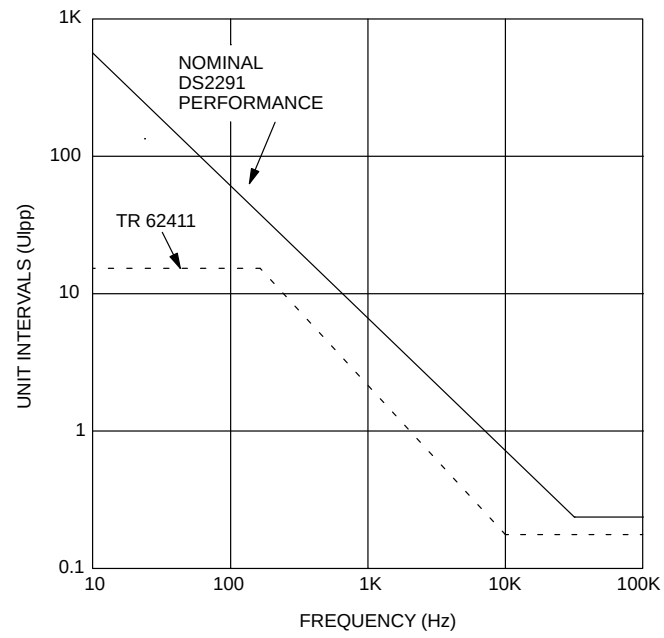
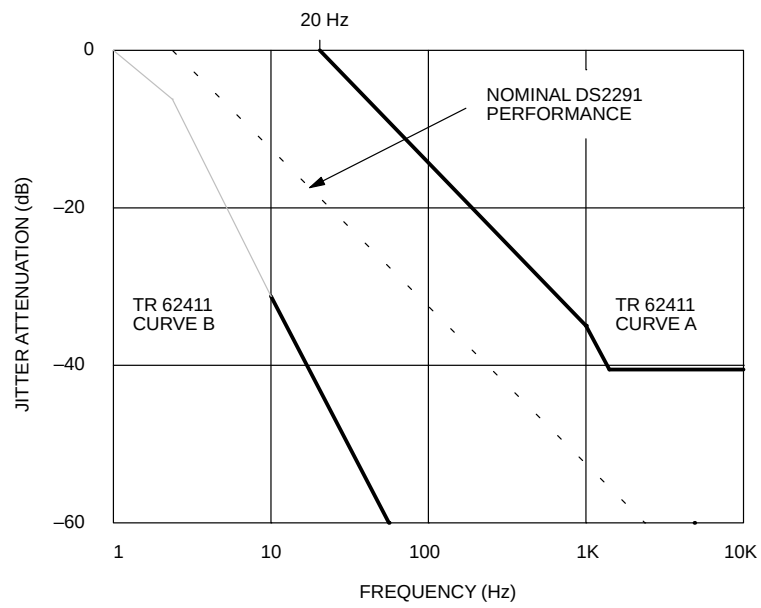
PIN	SYMBOL	I/O	DESCRIPTION
1,2	V _{DD}	-	Positive Supply. 5.0 volts.
3	RCLK	O	Receive Clock. Recovered 1.544 MHz clock.
4	RPOS	O	Receive Bipolar Data. Recovered bipolar data; updated on the rising edge of RCLK. Bipolar violations are not corrected.
5	RNEG		
6	LCLK	I	Loopback Clock. Clock for loopback data. Internally pulled low by 100K ohm.
7	LPOS	I	Loopback Bipolar Data. Samples on the falling edge of LCLK if LB is tied high. Internally pulled low by 100K ohm.
8	LNEG		
9	LB	I	Loopback Enable. Tie high to loopback data from the LPOS and LNEG inputs to RPOS and RNEG; tie low or leave open to obtain recovered data out of the ALBO circuitry at RPOS and RNEG. Internally pulled low by 100K ohm.
14	RCL	O	Receive Carrier Loss. Transitions high when 192 consecutive zeros have been received at RX+ and RX-; reset on the next ones occurrence.
15	BPV	O	Receive Bipolar Violation. Transitions high for a full bit period when a bipolar violation appears at RX+ and RX-. B8ZS code words are not reported if B8ZS is tied high.
16	LOCK	O	Lock Indication. High state indicates that the recovery circuit is phase-and frequency-locked to the signal at RX+ and RX-.
17	BL	O	Buffer Limit. Transitions high when the incoming jitter at RX+ and RX- is greater than 120U _{lpp} .
19	DJA	I	Disable Jitter Attenuation. Tie high to disable the jitter attenuation circuitry; tie low to enable the jitter attenuation circuitry. Internally pulled low by 100K ohm.
20	B8ZS	I	B8ZS Enable. If tied high, incoming B8ZS code words are decoded and replaced with eight zeros. If tied low, B8ZS code words are not decoded. Internally pulled low by 100K ohm.
21	RST	I	Reset. Active low; a high-low-high transition will recenter the dejitter buffer. Internally pulled high by 100K ohm.
22, 23	GND	-	Ground. 0.0 volts.
29	RX+	I	Receive Analog Input. Connects to T1 line through a 2:1 transformer. See Figure 4.
30	RX-	O	

NOTE:

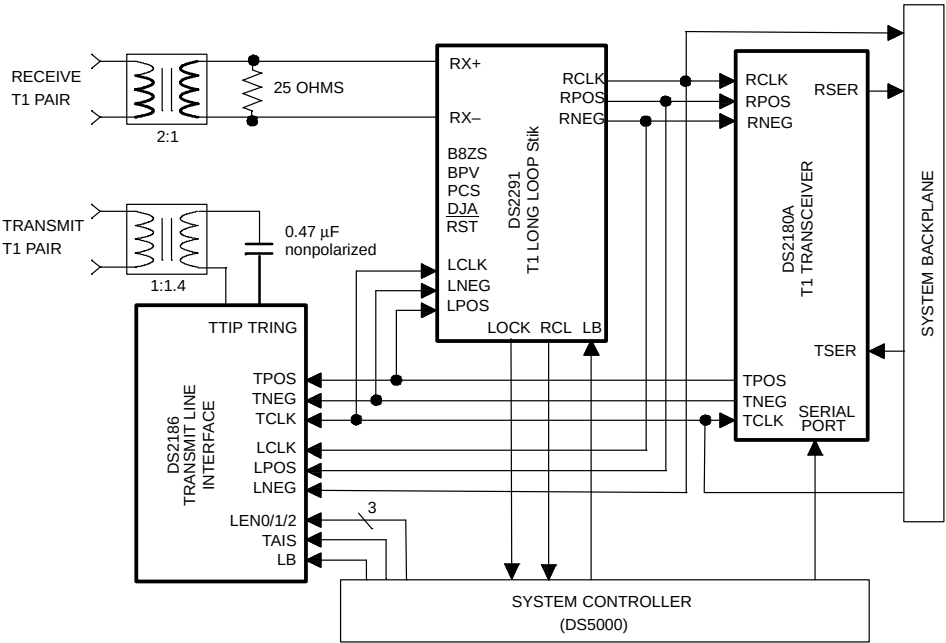
Do not connect any signal to pins 10, 11, 12, 13, 18, 24, 25, 26, 27, or 28.

DS2291 BLOCK DIAGRAM Figure 1

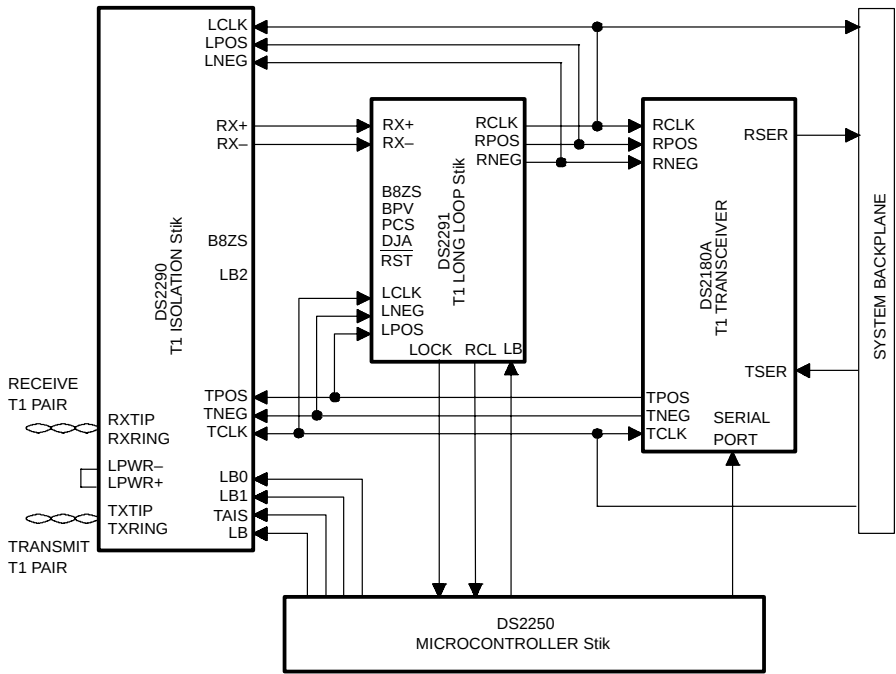


DS2291 JITTER TOLERANCE Figure 2**DS2291 JITTER ATTENUATION PERFORMANCE** Figure 3

DS2291 APPLICATION (UNISOLATED INTERFACE) Figure 4



DS2291 APPLICATION (ISOLATED INTERFACE) Figure 5



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-0.3V to $V_{CC} + 0.3V$
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.0		$V_{CC} + 0.3$	V	3, 4
Logic 0	V_{IL}	-0.3		+0.8	V	3, 4
Supply	V_{DD}	4.75		5.25	V	

CAPACITANCE(t_A=25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			30	pF	3
Output Capacitance	C_{OUT}			50	pF	3

DC ELECTRICAL CHARACTERISTICS(0°C to 70°C; $V_{DD} = 5V \pm 5\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{DD}		40	50	mA	1
Input Leakage	I_I	-100		+100	μA	2, 3
Output Current (2.4V)	I_{OH}	-1.0			mA	3
Output Current (0.4V)	I_{OL}	+4.0			mA	3

NOTES:

1. $V_{DD} = 5.25V$; output open.
2. $V_{SS} < V_{in} < V_{DD}$.
3. Does not apply to RX+ and RX-.
4. Inputs LCLK, LPOS, and LNEG are HC inputs; $V_{IH}=3.5V$ and $V_{IL}=1.0V$.

DIGITAL ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{DD} = 5V ± 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
LPOS, LNEG Setup to LCLK Falling	t _{SD}	50			ns	
LPOS, LNEG Hold from LCLK Falling	t _{HD}	50			ns	
Propagation Delay from RCLK to RPOS, RNEG Valid	t _{PD}			50	ns	
RCLK Period	t _P		648		ns	
RCLK Pulse Width	t _{WL} , t _{WH}		324		ns	
RST Pulse Width	t _{RST}	1			μs	

ANALOG ELECTRICAL CHARACTERISTICS

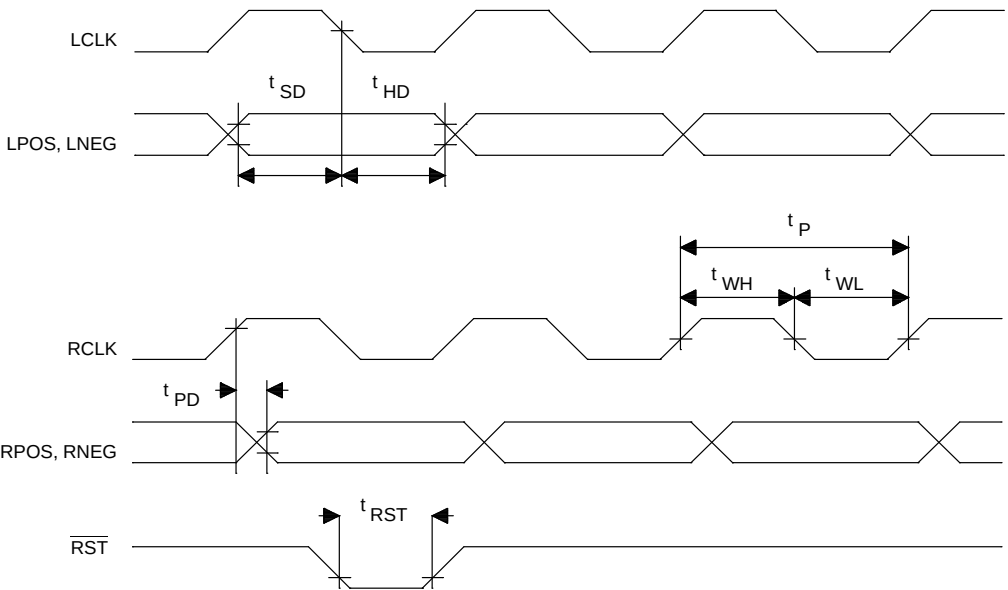
(0°C to 70°C; V_{DD} = 5V ± 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Signal Range	V _{IR}	-30		+0	dBSX	1
Input Impedance at 772 KHz	Z _{IN}		1100		ohms	1

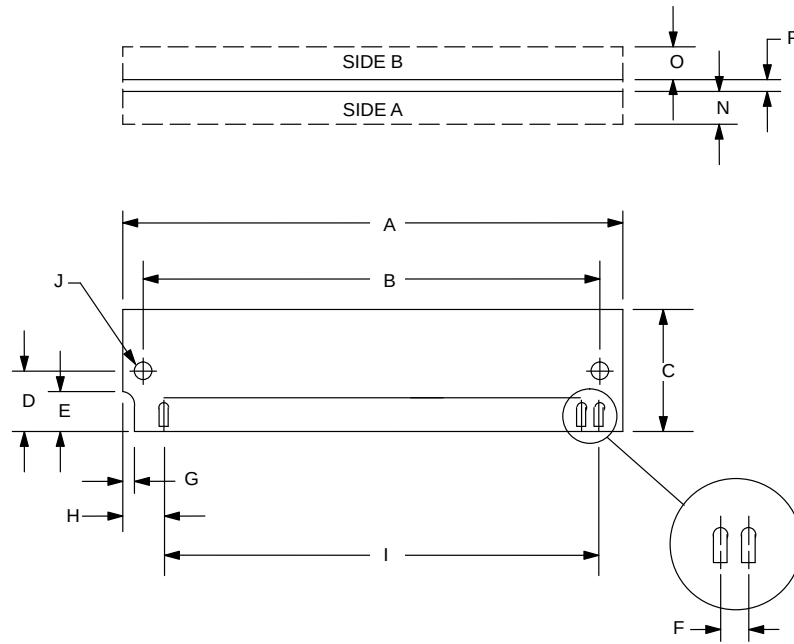
NOTE:

1. dBSX = 3Vpk; signal defined at the primary side of a 2:1 transformer with the secondary shunted by 25Ω and connected to RX+ and RX- (see Figure 4 for an example).

AC TIMING DIAGRAM Figure 6



DS2291 T1 LONG LOOP Stik



PKG	30-PIN	
DIM	MIN	MAX
A IN.	3.455	3.505
B IN.	3.229	3.239
C IN.	0.845	0.855
D IN.	0.395	0.405
E IN.	0.245	0.255
F IN.	0.100 BSC	
G IN.	0.075	0.085
H IN.	0.295	0.305
I IN.	2.900 BSC	
J IN.	0.120	0.130
N IN.		0.180
O IN.		0.115
P IN.		0.054