

DS2155DK/DS2156DK T1/E1/J1 Single-Chip Transceiver Design Kit Daughter Cards

www.maxim-ic.com

GENERAL DESCRIPTION

The DS2155/DS2156 design kits are evaluation boards for the DS2155 and DS2156. The DS2155/DS2156 design kits are intended to be used as daughter cards with either the DK2000 or the DK101 motherboards. The boards are complete with a single-chip transceiver (SCT), transformers, termination resistors, configuration switches, line protection circuitry, network connectors, and an interface to the motherboard.

ORDERING INFORMATION

PART	DESCRIPTION
DS2155DK	DS2155 Design Kit Daughter Card
DS2156DK	DS2156 Design Kit Daughter Card

FEATURES

- Expedites New Designs by Eliminating First-Pass Prototyping
- Interfaces Directly to the DK101 or DK2000 Motherboards
- Demonstrates Key Functions of the DS2156 and DS2155
- High-Level Software Provides Visual Access to Registers
- Software-Controlled (Register Mapped) Configuration Switches to Facilitate Clock and Signal Routing
- BNC Connections for 75Ω E1
- Bantam and RJ48 Connectors for 120Ω E1 and 100Ω T1
- Multitap Transformer to Facilitate True Impedance Matching for 75Ω and 120Ω/100Ω Paths
- Network Interface Protection for Overvoltage and Overcurrent Events
- UTOPIA II Bus Connection for MPC8260 (DS2156 Only)
- UTOPIA II Prototype Connectors (DS2156 Only)
- Test Points and Prototype Area Available for Further Customization

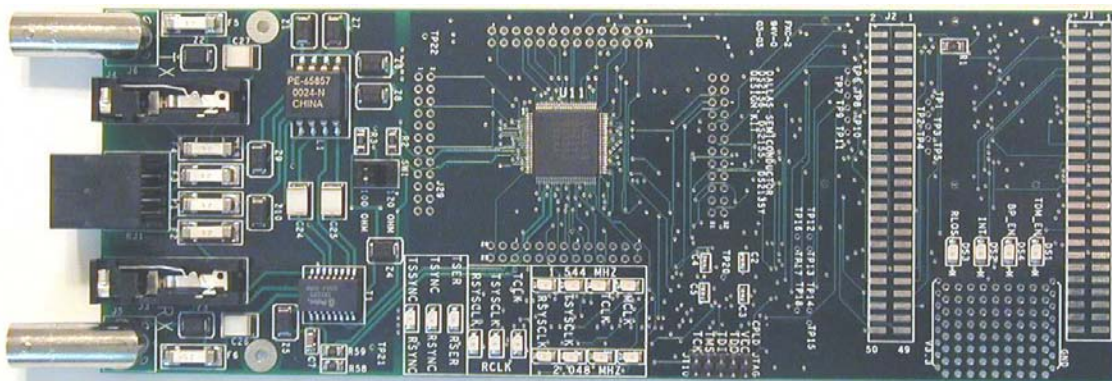


TABLE OF CONTENTS

COMPONENT LIST	3
BASIC OPERATION.....	4
HARDWARE CONFIGURATION	4
QUICK SETUP (DEMO MODE).....	4
QUICK SETUP (REGISTER VIEW)	4
SAMPLE UTOPIA II CONFIGURATION (DS2156 ONLY).....	5
REGISTER MAP	5
CPLD REGISTER MAP	6
DS2155/DS2156 INFORMATION	8
DS2155DK/DS2156DK INFORMATION.....	8
TECHNICAL SUPPORT	8
SCHEMATICS	8

LIST OF TABLES

Table 1. Daughter Card Address Map	5
Table 2. CPLD Register Map	6

COMPONENT LIST

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
C1–C5, C8–C12, C15–C19, C21, C22, C29–C34	23	0.1 μ F 10%, 16V ceramic capacitors (0603)	Digi-Key	311-1088-1-ND
C7, C36	2	1 μ F 10%, 16V ceramic capacitors (1206)	Digi-Key	PCC1882CT-ND
C13, C14	2	0.1 μ F 10%, 16V ceramic capacitors (0805)	Digi-Key	311-1142-1-ND
C23	1	0.1 μ F 10%, 25V ceramic capacitor (1206)	Digi-Key	PCC1883CT-ND
C24–C27	4	0.22 μ F, 50V ceramic capacitors	Digi-Key	UNK
C35	1	10 μ F 20%, 16V tantalum capacitor (B case)	Digi-Key	PCS3106CT-ND
DS1, DS4–DS18	16	LED, green, SMD	Digi-Key	P501CT-ND
DS2, DS3	2	LED, red, SMD	Digi-Key	P500CT-ND
F1–F6	6	250V, 1.25A fuse, SMT	Teccor Electronics	F1250T
J1, J2	2	Male 0.1, SMD, 50-pin, dual-row vertical	Samtec	TSM-125-01-T-DV
J3, J4	2	Bantam connectors	SWK	RTT34B02
J5, J6	2	Connector BNC RA 5-pin	Kruvand	UCBJR220
J7–J9	3	Socket, SMD, 50-pin, dual-row vertical	Samtec	TFM-125-02-S-D-LC
JT10	1	Connector, 10-pin, dual-row vertical	Digi-Key	S2012-05-ND
L1	1	Choke, dual 4-line 24 μ H, 8-pin SO	Pulse Engineering	PE-65857
R1, R14, R21	3	51.1 Ω 1%, 1/8W resistors (1206)	Digi-Key	P51.1FCT-ND
R2, R3, R58, R59	4	0 Ω 5%, 1/8W resistors (1206)	Digi-Key	P0.0ETR-ND
R4, R5, R60	3	51.1 Ω 1%, 1/10W resistors (0805)	Digi-Key	P51.1CCT-ND
R6, R9, R10, R13, R15–R19, R22, R23, R25–R29, R32, R37, R38, R44, R47–R49, R61	24	10k Ω 1%, 1/10W resistors (0805)	Digi-Key	P10.0KCCT-ND
R7, R8, R11, R12, R30, R31, R35, R36, R39–R43, R45, R50–R53	18	330 Ω 0.1%, 1/10W MF resistors (0805)	Digi-Key	P330ZCT-ND
R24	1	1.0k Ω 1%, 1/10W resistor (0805)	Digi-Key	P1.00KCCT-ND
R33, R34	2	NOPOP	—	NOPOP
R46	1	4.7k Ω 1%, 1/8W resistor (0805)	Digi-Key	9C08052A4701FK HFT
R54, R55	2	61.9 Ω 1%, 1/8W resistors (1206)	Digi-Key	P61.9FCT-ND
R56, R57	2	49.9 Ω 1%, 1/8W resistors (1206)	Digi-Key	P49.9FCT-ND
RJ1	1	RJ48 connector	Molex	43223
SW1	1	Switch DPDT slide 6-pin TH	Avnet	SSA22
T1	1	XFMR 16-pin SMT	Pulse Engineering	TX1099
U11	1	T1/E1/J1 XCVR 100-pin QFP, 0°C to +70°C	Dallas Semiconductor	DS2156L
U1–U4, U6	5	BBUS switch 10-bit CMOS, 150-mil, 24-pin SO	IDT	IDTQS3R861Q
U5	1	144-pin macrocell CPLD	Avnet	XC95144XL-10TQ100C
U7–U10	4	Quad bus switch, 150-mil, 16-pin SO	IDT	IDTQS3125Q
Z1, Z6–Z8	4	160V, 500A Sidactor	Teccor Electronics	P1800SCMC
Z2, Z3	2	58V, 500A Sidactor	Teccor Electronics	P0640SCMC
Z4, Z5	2	6V, 50A Sidactor	Teccor Electronics	P0080SAMC
Z9, Z10	2	25V, 500A Sidactor	Teccor Electronics	P0300SCMC

BASIC OPERATION

This design kit relies upon several supporting files, which can be downloaded from our website at www.maxim-ic.com/DS2155DK.

Hardware Configuration

Using the DK101 processor board:

- Connect the daughter card to the DK101 processor board.
- Supply 3.3V to the banana-plug receptacles marked GND and VCC_3.3V. (The external 5V connector and the TIM 5V supply headers are unused.)
- All processor board DIP switch settings should be in the ON position with exception for the flash programming switch, which should be OFF.
- From the Programs menu launch the host application named ChipView.exe. Run the ChipView application. If the default installation options were used, click the Start button on the Windows toolbar and select Programs→ChipView→ChipView.

Using the DK2000 processor board:

- Connect the daughter card to the DK2000 processor board.
- Connect J1 to the power supply that is delivered with the kit. Alternately, a PC power supply can be connected to connector J2.
- From the Programs menu launch the host application named ChipView.exe. Run the ChipView application. If the default installation options were used, click the Start button on the Windows toolbar and select Programs→ChipView→ChipView.

General:

- Upon power-up the RLOS LED is lit, as well as the MCLK-2.048MHz and TCLK-2.048MHz LEDs.
- Due to the dual winding transformer, only the 120Ω line build-out configuration setting is needed to cover 75Ω E1 and 120Ω E1.

Quick Setup (Demo Mode)

- The PC loads the program, offering a choice among Demo Mode, Register View, and Terminal Mode. Select Demo Mode.
- The program requests a configuration file, then select between the displayed files. (DS2155_E1_DSNCOM_DRVR.cfg or DS2155_T1_DSNCOM_DRVR.cfg).
- The Demo Mode screen appears. Upon external loopback, the LOS and OOF indicators extinguish.

Quick Setup (Register View)

- The PC loads the program, offering a choice among Demo Mode, Register View, and Terminal Mode. Select Register View.
- The program requests a definition file, then select DS2155.def.
- The Register View screen appears, showing the register names, acronyms, and values.
- Predefined register settings for several functions are available as initialization files.
 - INI files are loaded by selecting the menu File→Reg Ini File→Load Ini File.
 - Load the INI file DS2155_T1_BERT_ESF.ini.
 - After loading the INI file the following may be observed:
 - The RLOS LED extinguishes upon external loopback.
 - The DS2155/DS2156 begins transmitting a Daly pattern. When external loopback is applied, the BERT bit-count registers BBC1–3 and BEC1–3 may be updated by clearing and setting BC1.LC and clicking the Read All button.

Miscellaneous:

- Clock frequencies and certain pin bias levels are provided by a register-mapped CPLD, which is on the DS2155/DS2156 daughter card.
- The definition file for this CPLD is named DS215x_35x_CPLD_V2.def. See the [CPLD Register Map](#) section for definitions.
- All files referenced above are available for download at www.maxim-ic.com/DS2155DK.

Sample UTOPIA II Configuration (DS2156 Only)

The following register settings configure the DS2156 daughter card for UTOPIA II, single CLAV, 8-bit mode on PHY port 0. UTOPIA II bus connection is provided by header J1 (Tx) and header J2 (Rx).

After configuring the following registers toggle the MSTREG.URST bit to reset the UTOPIA II core.

UTOPIA II Setup, Register Settings for daughter card CPLD

NAME	VALUE		NAME	VALUE
SWITCH 1	0x0F		SWITCH 4	0x0F
SWITCH 2	0x03		LEVELS	0x07
SWITCH 3	0x0F			

UTOPIA II Setup, Register Settings for DS2156 E1 Configuration

NAME	VALUE		NAME	VALUE
MSTREG	0x02		LBCR	0x00
E1RCR1	0x68		TAF	0x9B
E1RCR2	0x00		TNAF	0xC0
E1TCR1	0x15		LIC1	0x11
E1TCR2	0x00		LIC2	0x90
CCR1	0x00		LIC3	0x00
CCR4	0x00		LIC4	0x00
IOCR1	0x00			
IOCR2	0x00			

UTOPIA II Setup, Register Settings for DS2156 UTOPIA II Configuration

NAME	VALUE		NAME	VALUE
U_TCFR	0x01		U_RCR2	0x0
U_TCR1	0x05		U_TIUPB	0x0
U_TCR2	0x00		PCPR	0x22
U_RCFR	0x01		PCDR1, 2, 3, 4	0x0
U_RCR1	0x01			

REGISTER MAP

The DK101 daughter card address space begins at 0x81000000.

The DK2000 daughter card address space begins at:

0x30000000 for slot 0
 0x40000000 for slot 1
 0x50000000 for slot 2
 0x60000000 for slot 3

All offsets given in [Table 1](#) are relative to the beginning of the daughter card address space.

Table 1. Daughter Card Address Map

OFFSET	DEVICE	DESCRIPTION
0X0000 to 0X0015	CPLD	Board identification and clock/signal routing
0X1000 to 0X10ff	Single-Chip Transceiver	Board is populated with one of the following: DS2156, DS2155, DS21352, or DS21354. Please see data sheet for details.

Registers in the CPLD can be easily modified using the ChipView.exe, a host-based user interface software along with the definition file named *DS215x_35x_CPLD_V2.def*. Definition files for the SCT are named *DS2155.def*, *DS21352.def*, or *DS21354.def*, depending on the board population option.

CPLD Register Map

Table 2. CPLD Register Map

OFFSET	NAME	TYPE	DESCRIPTION
0X0000	BID	Read-Only	Board ID
0X0002	XBIDH	Read-Only	High-Nibble Extended Board ID
0X0003	XBIDM	Read-Only	Middle-Nibble Extended Board ID
0X0004	XBIDL	Read-Only	Low-Nibble Extended Board ID
0X0005	BREV	Read-Only	Board FAB Revision
0X0006	AREV	Read-Only	Board Assembly Revision
0X0007	PREV	Read-Only	PLD Revision
0X0011	SWITCH1	Read-Write	Pin to 1.544MHz
0X0012	SWITCH2	Read-Write	Pin to 2.048MHz
0X0013	SWITCH3	Read-Write	Pin-to-Pin Connect
0X0014	SWITCH4	Read-Write	Pin-to-Pin Connect
0X0015	LEVELS	Read-Write	Set Level On Pin 1 = 3.3V

ID Registers

OFFSET	NAME	TYPE	VALUE	DESCRIPTION
0X0000	BID	Read-Only	0xD	Board ID
0X0002	XBIDH	Read-Only	0x0	High-Nibble Extended Board ID
0X0003	XBIDM	Read-Only	0x0	Middle-Nibble Extended Board ID
0X0004	XBIDL	Read-Only	0x5	Low-Nibble Extended Board ID
0X0005	BREV	Read-Only	Displays current FAB revision	Board FAB Revision
0X0006	AREV	Read-Only	Displays current assembly revision	Board Assembly Revision
0X0007	PREV	Read-Only	Displays current PLD firmware revision	PLD Revision

Control Registers

The control registers are used primarily to control several banks of FET switches that route clocks and backplane signals. Please note that certain register settings cause line contention, e.g., setting SWITCH1.4 and SWITCH2.4 both to 0 would drive MCLK with both 1.544MHz and 2.048MHz.

SWITCH1: PIN TO 1.544MHz (OFFSET = 0x0011) INITIAL VALUE = 0xF

(MSB)

(LSB)

—	—	—	—	MCLK	TCLK	RSYSCLK	TSYSCLK
---	---	---	---	------	------	---------	---------

NAME	POSITION	FUNCTION
MCLK	SWITCH1.3	0 = Connect MCLK to the 1.544MHz clock 1 = Open Switch 1.4
TCLK	SWITCH1.2	0 = Connect TCLK to the 1.544MHz clock 1 = Open Switch 1.3
RSYSCLK	SWITCH1.1	0 = Connect RSYSCLK to the 1.544MHz clock 1 = Open Switch 1.2
TSYSCLK	SWITCH1.0	0 = Connect TSYSCLK to the 1.544MHz clock 1 = Open Switch 1.1

SWITCH2: PIN TO 2.048MHz (Offset = 0X0012) INITIAL VALUE = 0x3**(MSB)****(LSB)**

—	—	—	—	MCLK	TCLK	RSYSCLK	TSYSCLK
---	---	---	---	------	------	---------	---------

NAME	POSITION	FUNCTION
MCLK	SWITCH2.3	0 = Connect MCLK to the 2.048MHz clock 1 = Open Switch 2.4
TCLK	SWITCH2.2	0 = Connect TCLK to the 2.048MHz clock 1 = Open Switch 2.3
RSYSCLK	SWITCH2.1	0 = Connect RSYSCLK to the 2.048MHz clock 1 = Open Switch 2.2
TSYSCLK	SWITCH2.0	0 = Connect TSYSCLK to the 2.048MHz clock 1 = Open Switch 2.1

SWITCH3: PIN-TO-PIN CONNECT (Offset = 0X0013) INITIAL VALUE = 0xF**(MSB)****(LSB)**

—	—	—	—	TSS_RS	TCL_RC	RSY_RC	TSY_RC
---	---	---	---	--------	--------	--------	--------

NAME	POSITION	FUNCTION
TSS_RS	SWITCH3.3	0 = Connect TSSYNC to RSYNC 1 = Open Switch 3.4
TCL_RC	SWITCH3.2	0 = Connect TCLK to RCLK 1 = Open Switch 3.3
RSY_RC	SWITCH3.1	0 = Connect RSYSCLK to RCLK 1 = Open Switch 3.2
TSY_RC	SWITCH3.0	0 = Connect TSYSCLK to RCLK 1 = Open Switch 3.1

SWITCH4: PIN-TO-PIN CONNECT (Offset = 0X0014) INITIAL VALUE = 0x3**(MSB)****(LSB)**

—	—	—	—	UTCLK_2048	UT_CLK_2048	RSER_TSER	RSYNC_TSYNC
---	---	---	---	------------	-------------	-----------	-------------

NAME	POSITION	FUNCTION		
URCLK_2048	SWITCH4.3	0 = Connect UR_CLK (TSSYNC) to 2.048MHz 1 = Open Switch 4.4		
UTCLK_2048	SWITCH4.2	0 = Connect UT_CLK (TCHCLK) to 2.048MHz 1 = Open Switch 4.3		
RSER_TSER	SWITCH4.1	0 = Connect RER to TSER 1 = Open Switch 4.2		
RSYNC_TSYNC	SWITCH4.0	0 = Connect RSYNC to TSYNC 1 = Open Switch 4.1		

LEVELS: SET LEVEL ON PIN (Offset = 0X0015) INITIAL VALUE = 0x6

(MSB)

(LSB)

—	—	—	—	—	BP_EN	PPCTDM_EN	TUSEL
---	---	---	---	---	-------	-----------	-------

NAME	POSITION	FUNCTION
—	LEVELS1.3	—
BP_EN	LEVELS1.2	0 = Enable IDT switches that connect the UTOPIA bus to daughter card header
PPCTDM_EN	LEVELS1.1	0 = Enable IDT switches that connect the TDM bus to the daughter card header
TUSEL	LEVELS1.0	0 = Set DS2156.TUSEL to enable TDM backplane 1 = Set DS2156.TUSEL to enable UTOPIA backplane

Note: When the UTOPIA backplane is enabled (LEVELS.TUSEL = 1) there is a possibility for contention between the UTOPIA bus master and TSYSCCLK, TSER, and RSER. To avoid this, the following switches should be opened when the UTOPIA backplane is enabled: SWITCH1.0, SWITCH2.0, SWITCH3.0, and SWITCH4.1

DS2155/DS2156 INFORMATION

For more information about the DS2155 and DS2156, please consult the DS2155 and DS2156 data sheets available on our website at www.maxim-ic.com/DS2155 and www.maxim-ic.com/DS2156. Software downloads are also available for this design kit.

DS2155DK/DS2156DK INFORMATION

For more information about the DS2155DK and DS2156DK, including software downloads, please consult the DS2155DK/DS2156DK data sheet available on our website at www.maxim-ic.com/DS2155DK.

TECHNICAL SUPPORT

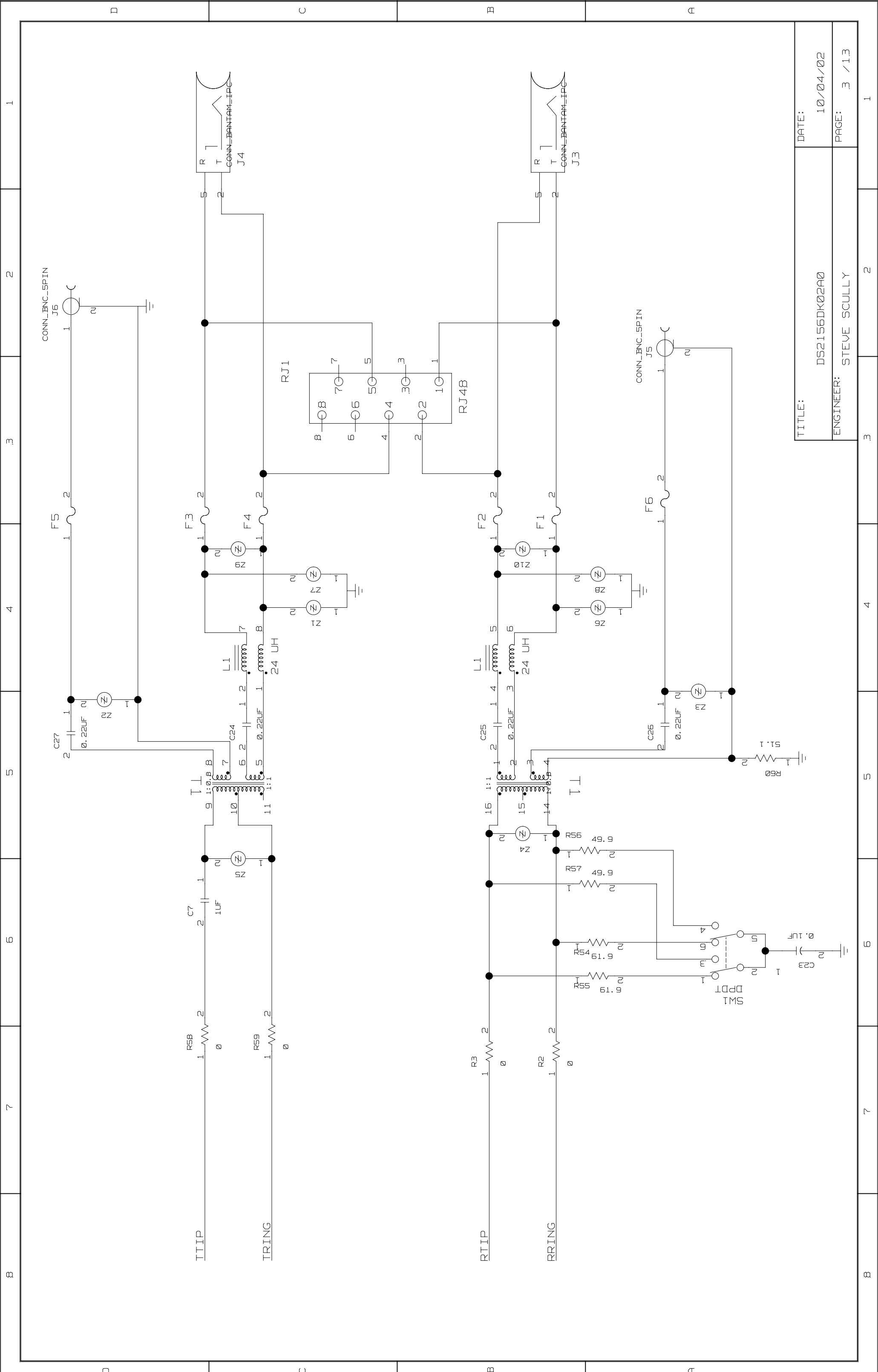
For additional technical support, please e-mail your questions to telecom.support@dalsemi.com.

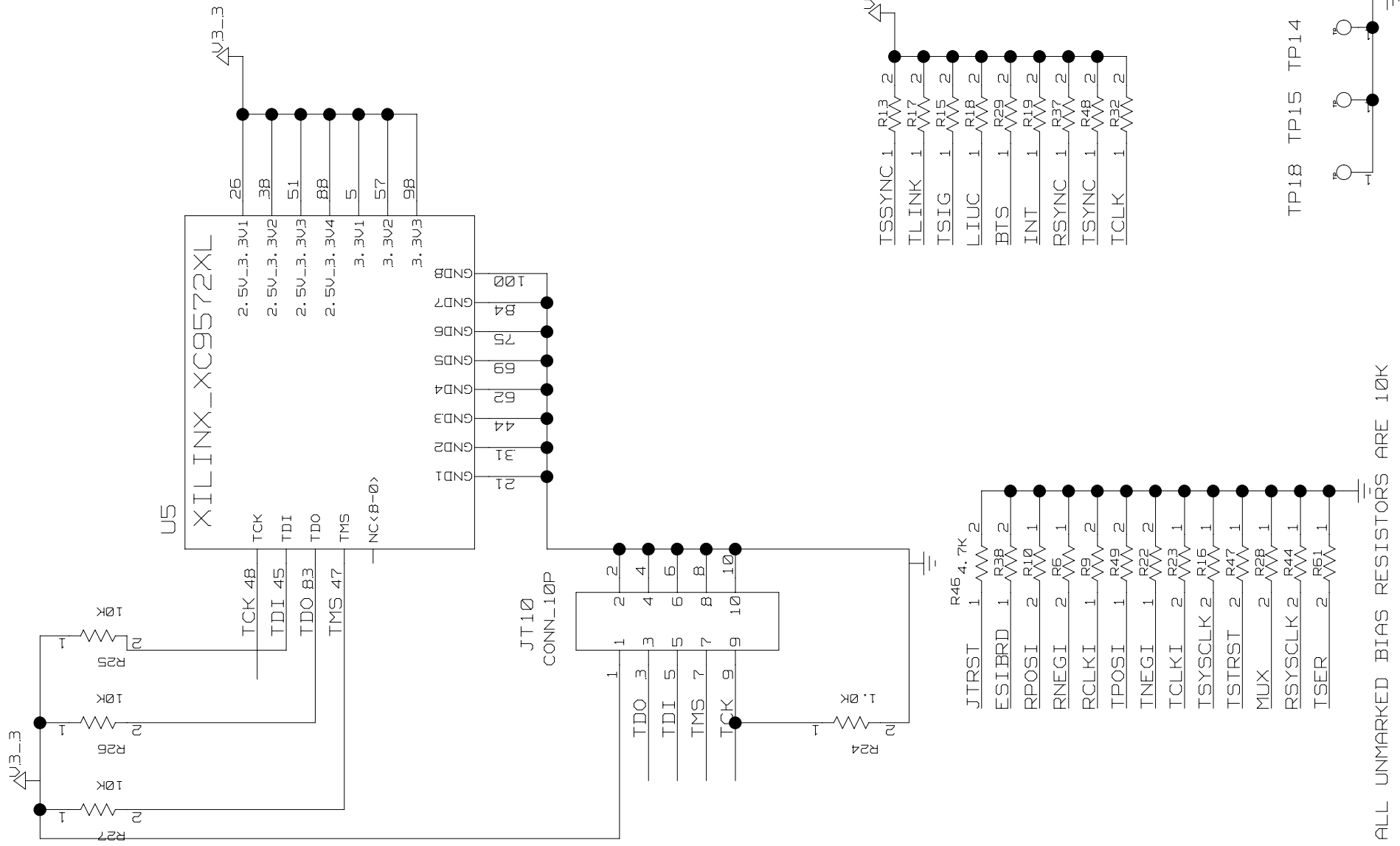
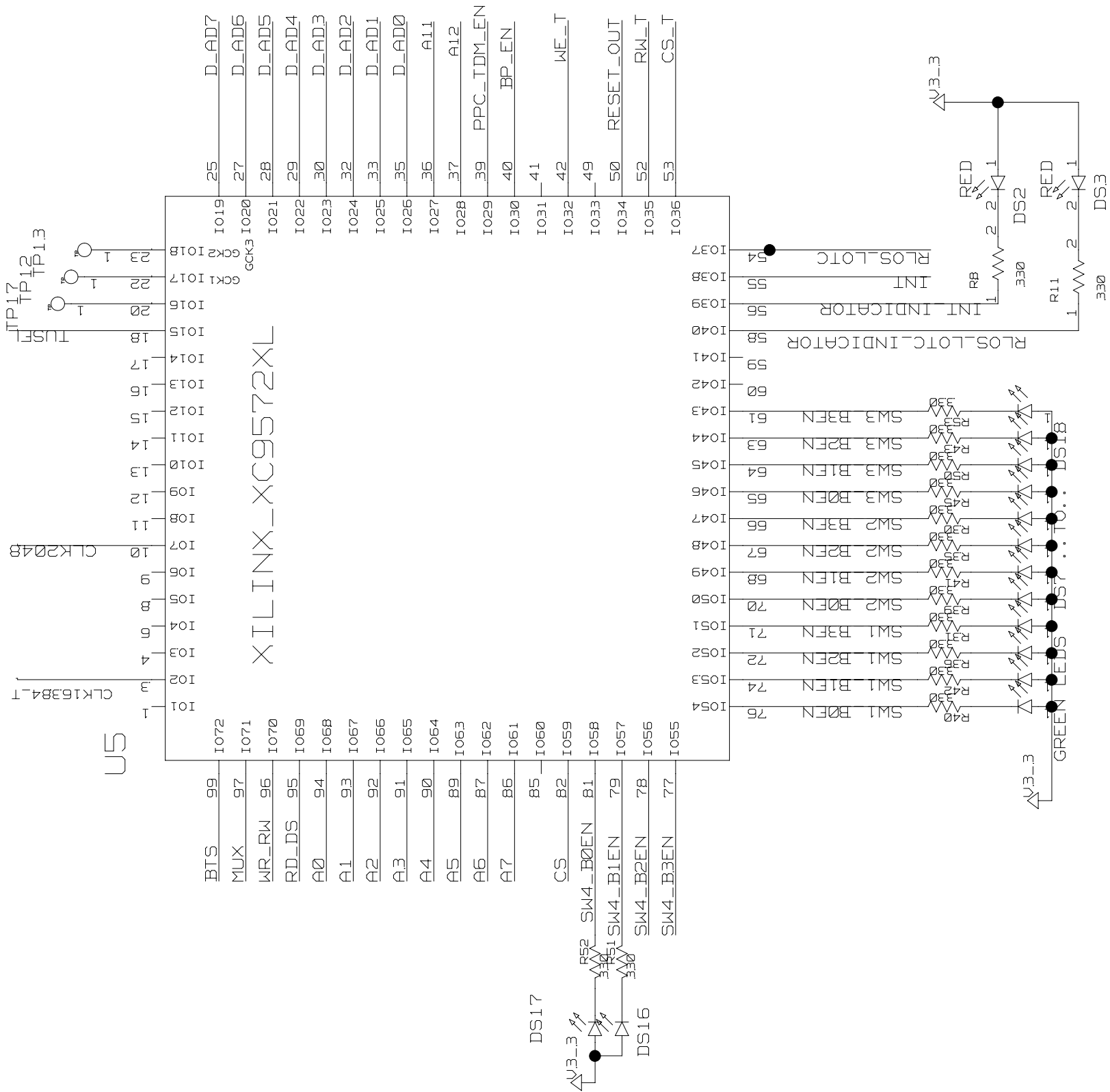
SCHEMATICS

The DS2155DK/DS2156DK schematics are featured in the following 13 pages.

DOCUMENT REVISION HISTORY

REVISION DATE	DESCRIPTION
032503	Initial DS2155DK/DS2156DK data sheet release.
060303	Updated the <i>Title</i> , <i>General Description</i> , <i>Features</i> , and <i>Basic Operation</i> sections; "TIM" replaced with "daughter card."
012705	Updated schematics (removed component values for Fuse and Sidactor; see <i>Component List</i>).
110106	Updated schematics.





TITLE:	DS2156DK02A0	DATE:	10/04/02
ENGINEER:	STEVE SCULLY	PAGE:	5 / 13

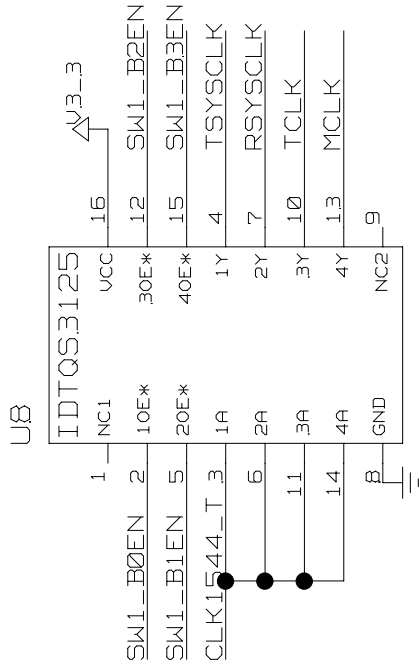
8		7	6	5	4	3	2	1
RXADDR0 == RXA_0 == UR_ADDR0 == RCHCLK							TXDATA_6 == TXDATA_6 == UT_DATA6 == TSIG	
RXADDR1 == RXA_1 == UR_ADDR1 == RSIGF								
RXADDR2 == RXA_2_RXCLAV_1 == UR_ADDR2 == RSIG							TXDATA_7 == TXDATA_7 == UT_DATA7 == TSYSCLK	
RXADDR3 == RXA_3_RXCLAV_2 == UR_ADDR3 == RMSYNC								
RXADDR4 == RXA_4_RXCLAV_3 == UR_ADDR4 == RFSYNC							TXENABLE == TXENA == UT_ENB == UOP1	
RXCLAV0 == RXCLAV_0 == UR_CLAV == RSER								
RXDATA_0 == RXDATA_0 == UR_DATA0 == RLINK							TXSOC == TXSOC == UT_SOC == UOP0	
RXDATA_1 == RXDATA_1 == UR_DATA1 == RLCLK								
RXDATA_2 == RXDATA_2 == UR_DATA2 == RPOSI								
RXDATA_3 == RXDATA_3 == UR_DATA3 == RNEGI								
RXDATA_4 == RXDATA_4 == UR_DATA4 == RCLKI							UT_CLK == TSSYNC	
RXDATA_5 == RXDATA_5 == UR_DATA5 == RCLKO							UR_CLK == TCHCLK	
RXDATA_6 == RXDATA_6 == UR_DATA6 == RNEGO								
RXDATA_7 == RXDATA_7 == UR_DATA7 == RPOSO								
<div><div><div><div><div>C13</div><div>0.1uF</div><div>NOPOP</div></div><div><div>C14</div><div>0.1uF</div><div>NOPOP</div></div><div><div>R33</div><div>20k</div><div>NOPOP</div></div><div><div>R34</div><div>20k</div><div>NOPOP</div></div></div></div></div>								
TITLE:						DS2156DK02A0		DATE:
						ENGINEER: STEVE SCULLY		PAGE: 8 / 13
8		7	6	5	4	3	2	1

D

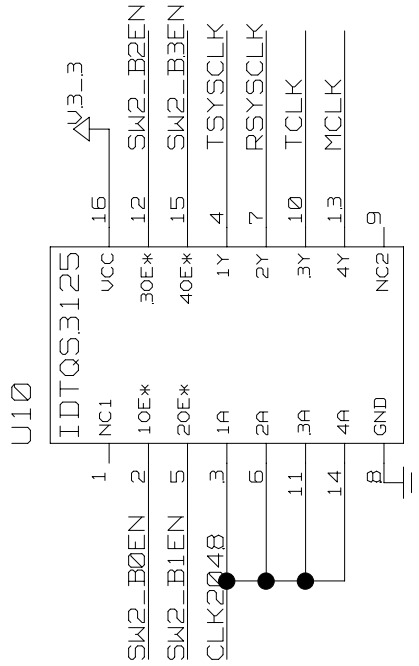
C

B

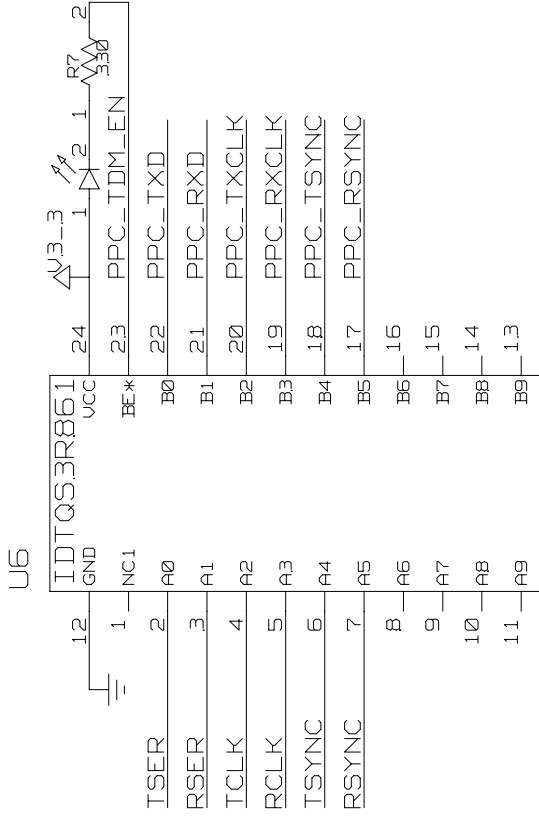
A



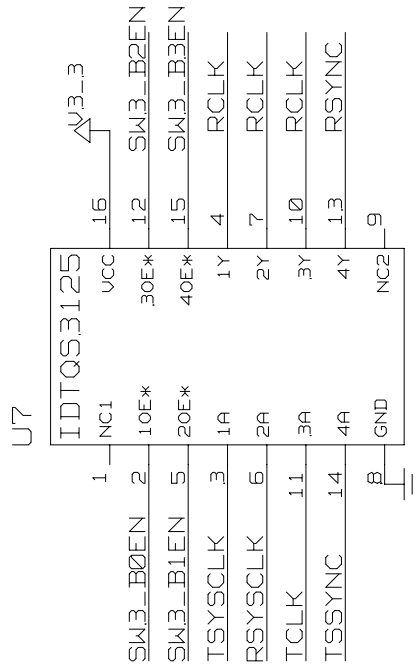
```
SWITCH_1 IS MEMORY MAPPED  
TO PLD REGISTER 0X11  
LOGIC 0 CLOSSES SWITCH  
LOGIC 1 OPENS SWITCH
```



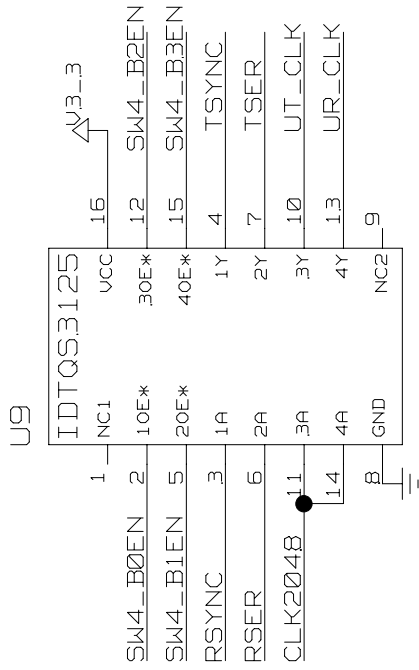
SWITCH 2 IS MEMORY MAPPED
TO PLD REGISTER 0X12
LOGIC 0 CLOSSES SWITCH
LOGIC 1 OPENS SWITCH



PPC-TDM-EN IS BIT MAPPED TO
PLD-ADDRESX IS BIT 1
LOGIC CLOSURES SWITCHES



SWITCH 3 IS MEMORY MAPPED
TO PLD REGISTER 13
LOGIC 0 CLEANS SWITCH
LOGIC 1 OPENS SWITCH



SWITCH 4 IS MEMORY MAPPED
TO PLD REGISTER 0X14
LOGIC 0 CLOSSES SWITCH
LOGIC 1 OPENS SWITCH

8	7	6	5	4	3	2	1
D				A			
C				B			
D				A			
DS2156							
TQFP							
RTIP	16	RTIP	33	TCHBLK	33	TCHBLK	
RRING	17	RRING	1	RCHBLK	1	RCHBLK	
RPOSI	86	RPOSI	99	RLOS_LOTC	99	RLOS_LOTC	
RNEGI	87	RNEGI	25	INT*	25	INT*	
RCLKI	88	RCLKI	75	CS*	75	CS*	
RPOSO	91	RPOSO	65	D_AD7	65	D_AD7	
RNEGO	90	RNEGO	64	D_AD6	64	D_AD6	
RCLKO	89	RCLKO	63	D_AD5	63	D_AD5	
			62	D_AD4	62	D_AD4	
			59	D_AD3	59	D_AD3	
			58	D_AD2	58	D_AD2	
			57	D_AD1	57	D_AD1	
			56	D_AD0	56	D_AD0	
TTIP	29	TTIP	73	A7	73	A7	
TRING	32	TRING	72	A6	72	A6	
TPOSI	38	TPOSI	71	A5	71	A5	
TNEGI	39	TNEGI	70	A4	70	A4	
TCLKI	40	TCLKI	69	A3	69	A3	
TPOSO	43	TPOSO	68	A2	68	A2	
TNEGO	42	TNEGO	67	A1	67	A1	
TCLKO	41	TCLKO	66	A0	66	A0	
JTMS	2	JTMS	11	BTS	11	BTS	
JTRST	5	JTRST	55	MUX	55	MUX	
JTDI	7	JTDI	74	RD_DS	74	RD_DS	
JTCLK	4	JTCLK	77	WR_RW	77	WR_RW	
JTDO	10	JTDO	28	N_P28	28	N_P28	
	</						

B		7	6	5	4	3	2	1
*** Signal Cross-Reference for the entire design ***						5C4<> 2A3< 11A3< 2A5> 11A4>		WR_RW XTALD
BXCLK	2CB> 11C7>	RLINK	2D6> BB7> 11D6>	TNEG1	BB4> 2BB< 5AB< 11B7<			
A0	4C6<> 5C4<> 2B3< 11B3<	RLOS_LOTC	2C3> 5B2<> 11C3>	TNEG0	2BB> BA4> 11B7>			
A1	4C6<> 5C4<> 2B3< 11B3<	RLOS_LOTC_INDICATOR	SA2<>	TPOSI	BC4> 2BB< 5AB< 11B7<			
A2	4C6<> 5C4<> 2B3< 11B3<	RMSYNC	2A5> BC7> 11A5>	TPOSO	2BB> BA4> 11B7>			
A3	4C6<> 5C4<> 2B3< 11B3<	RNEGI	BB7> 2CB< 5AB< 11C7<	TRING	2BB> 11B7> 3CB<			
A4	4C6<> 5C4<> 2B3< 11B3<	RNEGO	2CB> BA7> 11C7>	TSE	BA4> 9A6<> 9B2<> 2A5< 5AB< 11A4<			
A5	4C6<> 5C4<> 2B3< 11B3<	RPOSI	BB7> 2CB< 5AB< 11C7<	TSIG	BD1> 2D5< 5B6< 11D4<			
A6	4C6<> 5C4<> 2B3< 11B3<	RPOSO	2CB> BA7> 11C7>	TSSYNC	9C3<> 2D5< 5B6< 8A1< 11D4<			
A7	4C6<> 5C4<> 2B3< 11B3<	RRING	2CB< 3BB< 11C7<	TSTRST	2A5< 5AB< 11A4<			
A8	4C6<> 5C4<> 2B3< 11B3<	RSE	2A5> BC7> 9A6<> 9B3<> 11A5>	TSYNC	2D5<> 9A6<> 9B2<> 11D5<> 5A6<			
A9	4C6<> 5C4<> 2B3< 11B3<	RSIG	2A5> BD7> 11A5>	TSYSCLK	BD1> 9B6<> 9D3<> 9D6<> 2D5< 5AB<			
A10	4C6<> 7B1<>	RSIGF	2A5> BD7> 11A4>	TTIP	11D4<			
A11	4B6<> 7B1<>	RSYNC	2D6<> 9A6<> 9B3<> 9C1<> 11D5<>	TUSEL	2BB> 11B7> 3CB<			
A12	4C3<> 7C3<>	RSYSCLK	5A6<	TXADDR0	SD2<> 2A4< 11A4<			
A13	4C3<> 5C1<> 7C3<>	RTIP	9B6<> 9C3<> 9D6<> 2D6< 5AB< 11D5<	TXADDR1	7B5<> BD5			
A14	4B3<> 7B3<>	RALT	2CB< 3BB< 11C7<	TXADDR2	7B4<> BC5			
A15	4B3<>	RXADDR0	4B6<> 5B1<> 7B1<>	TXADDR3	7B4<> 8C5			
BPCLK	2A5> BD4> 11A4>	RXADDR1	7BB<> BDB	TXADDR4	7B5<> BC5			
BP_EN	5C1<> 6B2< 6B6< 6C2< 6C6<	RXADDR2	7BB<> BDB	TXA_0	7B4<> BC5			
BTS	5D4<> 2B3< 5A6< 11A3<	RXADDR3	7BB<> BCB	TXA_1	6C2<> BD4>			
CLK1544_T	7B3<> 9DB<> 4B2<	RXA_0	7B6<> BCB	TXA_2	6C7<> BC4>			
CLK204B	5D3<> 9B3<> 9BB<>	RXA_1	6B7<> BD7>	TXA_3	6B2<> 6C2<> 8C4>			
CLK163B4_T	4B4<> 5D3<> 7B3<>	RXA_2_RXCLAV_1	6A7<> 6B2<> BD7>	TXA_4	6C7<> 6C7<> BC4>			
CS_T	5B4<> 2C3< 11C3<	RXA_3_RXCLAV_2	6A7<> 6C7<> BC7>	TXA_5	6C2<> 6C2<> 8C4>			
D_AD0	4BB<> 5B1<> 7B3<>	RXA_4_RXCLAV_3	6A7<> 6B2<> BC7>	TXA_6	7B5<> BB5			
D_AD1	2B3<> 4B6<> 5C1<> 11B3<>	RXCLAV0	7AB<> BCB	TXA_7	6C7<> BB5			
D_AD2	2C3<> 4B6<> 5C1<> 11B3<>	RXCLAV_0	6B7<> BC7>	TXA_8	6C7<> 7C5<> 8B4> BB5			
D_AD3	2C3<> 4B6<> 5C1<> 11C3<>	RXCLAV_1	6B7<> 7CB<> BB7> BB8	TXA_9	6C2<> 7C4<> BB4> BB5			
D_AD4	2C3<> 4B6<> 5C1<> 11C3<>	RXCLAV_2	6A2<> 7C6<> BB7> BB8	TXA_10	6C7<> 7C5<> 8A4> BA5			
D_AD5	2C3<> 4B6<> 5C1<> 11C3<>	RXCLAV_3	6B7<> 7CB<> BB7> BB8	TXA_11	6C2<> 7C4<> 8A4> BA5			
D_AD6	2C3<> 4B6<> 5C1<> 11C3<>	RXCLAV_4	6B2<> 7C6<> BB7> BB8	TXA_12	6C7<> 7C4<> 8A4> BA5			
D_AD7	2C3<> 4A6<> 5D1<> 11C3<>	RXCLAV_5	6B7<> 7C6<> BA7> BAB	TXA_13	6C7<> 7C4<> 8D1> BD2			
ESI0	2A5<> 11A4<> 5AB<	RXCLAV_6	6B2<> 7CB<> BA7> BAB	TXA_14	6C2<> 7C5<> 8D1> BD2			
ESI00	2A6<> 11A6<>	RXCLAV_7	6B7<> 7C6<> BA7> BAB	TXA_15	6C2<> 7C5<> 8D1> BD2			
ESI01	2A6<> 11A5<>	RXENA	6A2<> BD4>	TXA_16	6C2<> 7C5<> 8D1> BD2			
INT	2C3> 4AB<> 5A2<> 11C3> 5A6<	RXENB	7A6<> BD5	TXA_17	6C2<> 7C5<> 8D1> BD2			
INT_INDICATOR	5A2<>	RXPRTY	6B5<>	TXA_18	6C5<>			
JTCLK	2AB< 11A7<	RXSOC	6B7<> 7B6<> BD4> BD5	TXA_19	6C7<> 7B4<> BB1> BB2			
JTDI	2AB< 11A7<	SNIM_B2	4C2<>	TXA_20	2A6> BB1> 11A5>			
JTDO	2AB> 11A7>	SNIM_B3	4C2<>	TXA_21	2A6> BC1> 11A5>			
JTMS	2BB< 11B7<	SNIM_B4	4C2<>	TXA_22	2A6> 11A5>			
JTRST	2BB< 5AB< 11A7<	SNIM_B5	4C2<>	TXA_23	2A6> BD4> 11A5>			
LIUC	BB4> 2CB< 5A6< 11B7<	SNIM_B6	4C2<>	TXA_24	BD8			
MCLK	9B6<> 9C6<> 2A5< 11A5<	SNIM_B7	4C2<>	TXA_25	UR_ADDR1			
MUX	5C4<> 2A3< 5AB< 11A3<	SW1_B0EN	5A4<> 9DB<	TXA_26	UR_ADDR2			
NIMD8	4B2<>	SW1_B1EN	5A4<> 9DB<	TXA_27	UR_ADDR3			
NIMD9	4B2<>	SW1_B2EN	5A3<> 9D6<	TXA_28	UR_ADDR4			
NIMD10	4B2<>	SW1_B3EN	5A3<> 9D6<	TXA_29	UR_CLAV			
NIMD11	4B2<>	SW2_B0EN	5A3<> 9B8<	TXA_30	UR_CLK			
NIMD12	4B2<>	SW2_B1EN	5A3<> 9BB<	TXA_31	9B2<> 6A1< 7AB< 8A2<			
NIMD13	4B2<>	SW2_B2EN	5A3<> 9B6<	TXA_32	UR_CLK			
NIMD14	4B2<>	SW2_B3EN	5A3<> 9B6<	TXA_33	UR_DATA0			
NIMD15	4C2<>	SW3_B0EN	5A3<> 9D3<	TXA_34	UR_DATA1			
N_P27	2A4< 11A4<	SW3_B1EN	5A3<> 9D1<	TXA_35	UR_DATA2			
N_P28	2A3< 11A3<	SW3_B2EN	5A3<> 9D1<	TXA_36	UR_DATA3			
PPC_RSYNC	4CB<> 9A4<>	SW3_B3EN	5B4<> 9B3<	TXA_37	UR_DATA4			
PPC_RXCLK	4CB<> 9A4<>	SW4_B0EN	5B4<> 9B3<	TXA_38	UR_DATA5			
PPC_RXD	4CB<> 9A4<>	SW4_B1EN	5B4<> 9B2<	TXA_39	UR_DATA6			
PPC_TDM_EN	5C1<> 9A4<	SW4_B2EN	5B4<> 9B2<	TXA_40	UR_DATA7			
PPC_TSYNC	4BB<> 9A4<>	SW4_B3EN	5B4<> 9B2<	TXA_41	UR_ENB			
PPC_TXCLK	4CB<> 9A4<>	TCHCLK	2D3> BC4> 11C3>	TXA_42	UT_ADDR0			
PPC_TXD	4CB<> 9A4<>	TCHCLK	2D5> 11D4> 8A1<	TXA_43	UT_ADDR1			
RCHCLK	2C3> BD4> 11C3>	TCK	5BB<> 5DB<	TXA_44	UT_ADDR2			
RCHCLK	2D6> BD7> 11D5>	TCLK	9A6<> 9B6<> 9C3<> 9C6<> 2D5< 5A6<	TXA_45	UT_ADDR3			
RCL	2CB> 11C7>	TCLK	11D5<	TXA_46	UT_ADDR4			
RCLK	2D6> 9A6<> 9C1<> 9C1<> 9D1<> 11D6>	TCLKI	BB4> 2BB< 5AB< 11B7<	TXA_47	UT_CLAV			
RCLKI	BA7> 2CB< 5AB< 11C7<	TCLKO	2BB> BA4> 11B7>	TXA_48	UT_CLK			
RCLKO	2CB> BA7> 11C7>	TDATA	2D5<> 11D4<>	TXA_49	UT_DATA0			
RDATA	2D6> 11D5>	TDI	5BB<> 5D7<	TXA_50	UT_DATA1			
RD_DS	5C4<> 2A3< 11A3<	TDO	5BB<> 5C7<	TXA_51	UT_DATA2			
RESET_OUT	4B6<> 5B1<> 7B1<>	TIMSV	4D3<> 4DB<>	TXA_52	UT_DATA3			
RFSYNC	2D6> BC7> 11D5>	TLCLK	2D5> BC4> 11D4>	TXA_53	UT_DATA4			
RLCLK	2D6> BB7> 11D5>	TLINK	BC4> 2D5< 5B6< 11D5<	TXA_54	UT_DATA5			
		TMS	5BB<> 5C7<	TXA_55	UT_DATA6			
				TXA_56	UT_DATA7			
				TXA_57	UT_ENB			
				TXA_58	UT_SOC			
				TXA_59	WE_T			
				TXA_60				
				TXA_61				
				TXA_62				
				TXA_63				
				TXA_64				
				TXA_65				
				TXA_66				
				TXA_67				
				TXA_68				
				TXA_69				
				TXA_70				
				TXA_71				
				TXA_72				
				TXA_73				
				TXA_74				
				TXA_75				
				TXA_76				
				TXA_77				
				TXA_78				
				TXA_79				
				TXA_80				
				TXA_81				
				TXA_82				
				TXA_83				
				TXA_84				
				TXA_85				
				TXA_86				
				TXA_87				
				TXA_88				
				TXA_89				
				TXA_90				
				TXA_91				
				TXA_92				
				TXA_93				
				TXA_94				
				TXA_95				
				TXA_96				
				TXA_97				
				TXA_98				
				TXA_99				
				TXA_100				
				TXA_101				
				TXA_102				
				TXA_103				
				TXA_104				
				TXA_105				
				TXA_106				
				TXA_107				
				TXA_108				
				TXA_109				
				TXA_110				
				TXA_111				
				TXA_112				
				TXA_113				
				TXA_114				
				TXA_115				
				TXA_116				
				TXA_117				
				TXA_118				
				TXA_119				
				TXA_120				
				TXA_121				
				TXA_122				
				TXA_123				
				TXA_124				
				TXA_125				
				TXA_126				
				TXA_127				
				TXA_128				
				TXA_129				
				TXA_130				
				TXA_131				
				TXA_132				
				TXA_133				
				TXA_134				
				TXA_135				
				TXA_136				
				TXA_137				
				TXA_138				
				TXA_139				
				TXA_140				
				TXA_141				
				TXA_142				
				TXA_143				
				TXA_144				
				TXA_145				
				TXA_146				
				TXA_147				
				TXA_148				
				TXA_149				
				TXA_150				
				TXA_151				
				TXA_152				
				TXA_153				
				TXA_154				
				TXA_155				
				TXA_156				
				TXA_157				
				TXA_158				
				TXA_159				
				TXA_160				
				TXA_161				
				TXA_162				
				TXA_163				
				TXA_164				
				TXA_165				
				TXA_166				
				TXA_167				
				TXA_168				
				TXA_169				
				TXA_170				
				TXA_171				
				TXA_172				
				TXA_173				
				TXA_174				
				TXA_175				
				TXA_176				
				TXA_177				
				TXA_178				
				TXA_179				
				TXA_180				
				TXA_181				
				TXA_182				
				TXA				

B		7		6		5		4		3		2		1	
*** Part Cross-Reference for the entire design ***															
1	DS2156_TQFP 11D7														
C1	CAP 10B5														
C2	CAP 10B3														
C3	CAP 10B2														
C4	CAP 10B2														
C5	CAP 10B2														
C7	CAP 3D5														
C8	CAP 10B4														
C9	CAP 10B4														
C10	CAP 10B4														
C11	CAP 10B4														
C12	CAP 10B2														
C13	CAP 8A1														
C14	CAP 8A1														
C15	CAP 10B3														
C16	CAP 10B3														
C17	CAP 10B2														
C18	CAP 10B3														
C19	CAP 10B3														
C21	CAP 10B2														
C22	CAP 10B5														
C23	CAP 3A6														
C24	CAP 3C5														
C25	CAP 3B5														
C26	CAP 3A5														
C27	CAP 3D5														
C29	CAP 10B4														
C30	CAP 10B4														
C31	CAP 10B6														
C32	CAP 10B5														
C33	CAP 10B5														
C34	CAP 10B5														
C35	CAP 10B6														
C36	CAP 10B6														
DS1	LED 9B4														
DS2	LED 5A2														
DS3	LED 5A2														
DS4	LED 6D5														
DS5	LED 5A3														
DS6	LED 5A4														
DS7	LED 5A3														
DS8	LED 5A4														
DS9	LED 5A4														
DS10	LED 5A3														
DS11	LED 5A4														
DS12	LED 5A3														
DS13	LED 5A3														
DS14	LED 5A3														
DS15	LED 5A3														
DS16	LED 5B5														
DS17	LED 5B5														
DS18	LED 5A3														
F1	FUSE 3B4														
F2	FUSE 3B4														
F3	FUSE 3D4														
F4	FUSE 3C4														
F5	FUSE 3D4														
F6	FUSE 3A3														
J1	CONN_50P1 7D5														
J2	CONN_50P1 7D7														
J3	CONN_BANTAM_IPC 3B1														
J4	CONN_BANTAM_IPC 3C1														
J5	CONN_BNC_SPIN 3A3														
J6	CONN_BNC_SPIN 3D2														
J7	CONN_50P2 6D4														
J8	CONN_50P2 4D3														
J9	CONN_50P2 4D7														
JT10	CONN_10P 5CB														
L1	CHOKE_DUAL-T1 3B4 3C4														
R1	RES1 4B2														
R2	RES 3B7														
R3	RES 3B7														
R4	RES 6A2														
R5	RES 6C2														
R6	RES1 5A7														