Rev 1; 10/08

PON Triplexer and SFP Controller

General Description

The DS1875 controls and monitors all functions for burst-mode transmitters, APD receivers, and video receivers. It also includes a power-supply controller for APD bias generation, and provides all SFF-8472 diagnostic and monitoring functionality. The combined solution of the DS1875 and the MAX3643 laser driver provides APC loop, modulation current control, and eye safety functionality. Ten ADC channels monitor V_{CC}, temperature (both internal signals), and eight external monitor inputs (MON1–MON8) that can be used to meet transmitter, digital receiver, video receiver, and APD receiver-signal monitoring requirements. Four total DAC outputs are available. A PWM controller with feedback and compensation pins can be used to generate the bias for an APD or as a step-down converter. Five I/O pins allow additional monitoring and configuration.

Applications

BPON, GPON, or EPON Optical Triplexers

SFF, SFP, and SFP+ Transceiver Modules

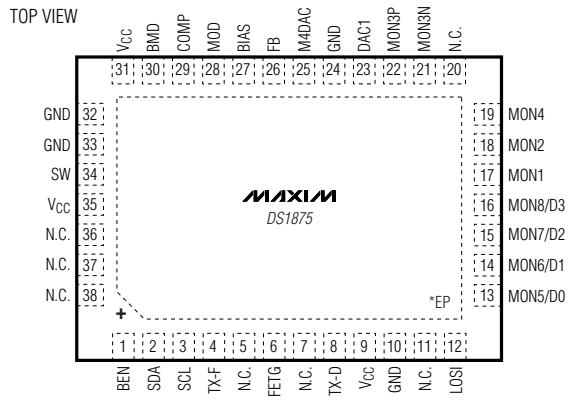
APD Controller

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
DS1875T+	-40°C to +95°C	38 TQFN-EP*
DS1875T+T&R	-40°C to +95°C	38 TQFN-EP*

+Denotes a lead-free/RoHS-compliant package.
T&R = Tape and reel.
**EP = Exposed pad.*

Pin Configuration



TQFN
(5mm x 7mm x 0.8mm)

*EXPOSED PAD.

Features

- **Meets All PON Burst-Timing Requirements for Burst-Mode Operation**
- **Laser Bias Controlled by APC Loop and Temperature Lookup Table (LUT)**
- **Laser Modulation Controlled by Temperature LUT**
- **Six Total DACs: Four External, Two Internal**
- **Two 8-Bit DACs, One of Which is Optionally Controlled by MON4 Voltage**
- **Internal 8-Bit DAC Controlled by a Temperature-Indexed LUT**
- **PWM Controller**
- **Boost or Buck Mode**
- **Boost Mode: Uses Optional External Components, Up to 90V Bias Generation**
- **131kHz, 262kHz, 525kHz, or 1050kHz Selectable-Switching Frequency**
- **APD Overcurrent Protection Using Optional Fast Shutdown**
- **10 Analog Monitor Channels: Temperature, V_{CC}, Eight Monitors**
- **Internal, Factory-Calibrated Temperature Sensor**
- **RSSI with 29dB Electrical Dynamic**
- **Five I/O Pins for Additional Control and Monitoring Functions, Four of Which are Either Digital I/O or Analog Monitors**
- **Comprehensive Fault-Measurement System with Maskable Laser Shutdown Capability**
- **Two-Level Password Access to Protect Calibration Data**
- **120 Bytes of Password-1 Protected Memory**
- **128 Bytes of Password-2 Protected Memory in Main Device Address**
- **256 Additional Bytes Located at A0h Slave Address**
- **I^2C-Compatible Interface for Calibration and Monitoring**
- **2.85V to 3.9V Operating Voltage Range**
- **-40°C to +95°C Operating Temperature Range**
- **38-Pin TQFN (5mm x 7mm) Package**

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

PON Triplexer and SFP Controller

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ABSOLUTE MAXIMUM RATINGS

Voltage Range on MON1–MON8, BEN, BMD, and TX-D Pins Relative to Ground .....-0.5V to (V_{CC} + 0.5V)*
Voltage Range on V_{CC}, SDA, SCL, D0–D3, and TX-F Pins Relative to Ground.....-0.5V to 6V

Operating Temperature Range .....-40°C to +95°C
Programming Temperature Range .....0°C to +85°C
Storage Temperature Range .....-55°C to +125°C
Soldering Temperature.....Refer to the IPC/JEDEC J-STD-020 Specification.

**Subject to not exceeding +6V.*

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Main Supply Voltage	V_{CC}	(Note 1)	+2.85		+3.9	V
High-Level Input Voltage (SDA, SCL, BEN)	$V_{IH:1}$		0.7 x V_{CC}		V_{CC} + 0.3	V
Low-Level Input Voltage (SDA, SCL, BEN)	$V_{IL:1}$		-0.3		0.3 x V_{CC}	V
High-Level Input Voltage (TX-D, LOSI, D0, D1, D2, D3)	$V_{IH:2}$		2.0		V_{CC} + 0.3	V
Low-Level Input Voltage (TX-D, LOSI, D0, D1, D2, D3)	$V_{IL:2}$		-0.3		+0.8	V

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.85V to +3.9V, T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_{CC}	(Notes 1, 2)		5.5	10	mA
Output Leakage (SDA, TX-F, D0, D1, D2, D3)	I_{LO}	(Note 2)			1	µA
Low-Level Output Voltage (SDA, TX-F, FETG, D0, D1, D2, D3)	V_{OL}	I_{OL} = 4mA			0.4	V
		I_{OL} = 6mA			0.6	
High-Level Output Voltage (FETG)	V_{OH}	I_{OH} = 4mA	V_{CC} - 0.4			V
FETG Before Recall		(Note 3)		10	100	nA
Input Leakage Current (SCL, BEN, TX-D, LOSI)	$I_{LI:1}$				1	µA
Digital Power-On Reset	POD		1.0		2.2	V
Analog Power-On Reset	POA		2.1		2.75	V

ELECTRICAL CHARACTERISTICS (DAC1 AND M4DAC)

(V_{CC} = +2.85V to +3.9V, T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DAC Output Range				2.5		V
DAC Output Resolution				8		Bits
DAC Output Integral Nonlinearity			-1		+1	LSB
DAC Output Differential Nonlinearity			-1		+1	LSB
DAC Error		T_A = +25°C	-1.25		+1.25	%FS
DAC Temperature Drift			-2		+2	%FS
DAC Offset			-12		+12	mV
Maximum Load			-500		+500	µA
Maximum Load Capacitance					250	pF

ANALOG INPUT CHARACTERISTICS (BMD, TXP HI, TXP LO, HBIAS)

(V_{CC} = +2.85V to +3.9V, T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
BMD, TXP HI, TXP LO Full-Scale Voltage	V_{APC}	(Note 4)		2.5		V
HBIAS Full-Scale Voltage		(Note 5)		1.25		V
BMD Input Resistance			35	50	65	kΩ
Resolution				8		Bits
Error		T_A = +25°C (Note 6)		±2		%FS
Integral Nonlinearity			-1		+1	LSB
Differential Nonlinearity			-1		+1	LSB
Temperature Drift			-2.5		+2.5	%FS

ANALOG OUTPUT CHARACTERISTICS

(V_{CC} = +2.85V to +3.9V, T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
BIAS Current	I_{BIAS}	(Note 1)		1.2		mA
I_{BIAS} Shutdown Current	$I_{BIAS:OFF}$			10	100	nA
Voltage at I_{BIAS}			0.7	1.2	1.4	V
MOD Full-Scale Voltage	V_{MOD}	(Note 5)		1.25		V
MOD Output Impedance		(Note 7)		3		kΩ
V_{MOD} Error		T_A = +25°C (Note 8)	-1.25		+1.25	%FS
V_{MOD} Integral Nonlinearity			-1		+1	LSB
V_{MOD} Differential Nonlinearity			-1		+1	LSB
V_{MOD} Temperature Drift			-2		+2	%FS

PWM CHARACTERISTICS

(V_{CC} = +2.85V to +3.9V, T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PWM-DAC Full-Scale Voltage	$V_{PWM-DAC}$			1.25		V
PWM-DAC Resolution					8	Bits
$V_{PWM-DAC}$ Full-Scale Voltage Error		T_A = +25°C		1.25		%
$V_{PWM-DAC}$ Integral Nonlinearity			-1		1	LSB
$V_{PWM-DAC}$ Differential Nonlinearity			-1		1	LSB
$V_{PWM-DAC}$ Temperature Drift			-2		+2	%FS
SW Output Impedance					20	Ω
SW Frequency Error	f_{SWER}	(Note 9)	-5		+7	%
SW Duty Cycle	D_{MAX}		89	90	91	%
Error-Amplifier Source Current				-10		µA
Error-Amplifier Sink Current				+10		µA
COMP High-Voltage Clamp				2.1		V
COMP Low-Voltage Clamp				0.8		V
Error-Amplifier Transconductance	G_M			425		µS
Error-Amplifier Output Impedance	R_{EA}			260		MΩ
FB Pin Capacitance				5		pF

TIMING CHARACTERISTICS (CONTROL LOOP AND QUICK TRIP)

(V_{CC} = +2.85V to +3.9V, T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
First BMD Sample Following BEN	t_{FIRST}	(Note 10)				
Remaining Updates During BEN	t_{UPDATE}	(Note 10)				
BEN High Time	$t_{BEN:HIGH}$		400			ns
BEN Low Time	$t_{BEN:LOW}$		96			ns
Output-Enable Time Following POA	t_{INIT}		10			ms
BIAS and MOD Turn-Off Delay	t_{OFF}				5	µs
BIAS and MOD Turn-On Delay	t_{ON}				5	µs
FETG Turn-On Delay	$t_{FETG:ON}$				5	µs
FETG Turn-Off Delay	$t_{FETG:OFF}$				5	µs

ANALOG VOLTAGE MONITORING

(V_{CC} = +2.85V to +3.9V, T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ADC Resolution					13		Bits
Input/Supply Accuracy (MON1–MON8, V_{CC})		ACC	At factory setting		0.25	0.50	%FS
Update Rate for Temp, MON1–MON4, and V_{CC}		$t_{FRAME:1}$			78	95	ms
Update Rate for MON5–MON8		$t_{FRAME:2}$	Bit EN5TO8B is enabled in Table 02h, Register 89h		156	190	ms
Input/Supply Offset (MON1–MON8, V_{CC})		V_{OS}	(Note 11)		0	5	LSB
Factory Setting	MON1–MON8		Full scales are user programmable		2.5		V
	V_{CC}				6.5536		
	MON3 Fine				312.5		µV

DIGITAL THERMOMETER

(V_{CC} = +2.85V to +3.9V, T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Thermometer Error	T_{ERR}	-40°C to +95°C			±3.0	°C

NONVOLATILE MEMORY CHARACTERISTICS

(V_{CC} = +2.85V to +3.9V, T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EEPROM Write Cycles		At +85°C (Note 11)	50,000			
		At +25°C (Note 11)	200,000			

I²C TIMING SPECIFICATIONS

(V_{CC} = +2.85V to +3.9V, T_A = -40°C to +95°C, timing referenced to $V_{IL(MAX)}$ and $V_{IH(MIN)}$.) (See Figure 15.)

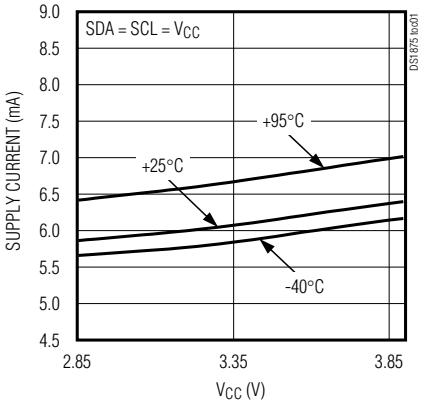
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}	(Note 12)	0		400	kHz
Clock Pulse-Width Low	t_{LOW}		1.3			µs
Clock Pulse-Width High	t_{HIGH}		0.6			µs
Bus-Free Time Between STOP and START Condition	t_{BUF}		1.3			µs
START Hold Time	$t_{HD:STA}$		0.6			µs
START Setup Time	$t_{SU:STA}$		0.6			µs
Data in Hold Time	$t_{HD:DAT}$		0		0.9	µs
Data in Setup Time	$t_{SU:DAT}$		100			ns
Capacitive Load for Each Bus Line	C_B				400	pF
Rise Time of Both SDA and SCL Signals	t_R	(Note 13)	20 + 0.1C_B		300	ns
Fall Time of Both SDA and SCL Signals	t_F	(Note 13)	20 + 0.1C_B		300	ns
STOP Setup Time	$t_{SU:STO}$		0.6			µs
EEPROM Write Time	t_W	(Note 14)			20	ms

Note 1: All voltages are referenced to ground. Current into IC is positive, and current out of the IC is negative.
Note 2: Digital inputs are at rail. FETG is disconnected. SDA = SCL = V_{CC}. SW, DAC1, and M4DAC are not loaded.
Note 3: See the *Safety Shutdown (FETG) Output* section for details.
Note 4: Eight ranges allow the full scale to change from 625mV to 2.5V.
Note 5: Eight ranges allow the full scale to change from 312.5mV to 1.25V.
Note 6: This specification applies to the expected full-scale value for the selected range. See the COMP RANGING register description for available full-scale ranges.
Note 7: The output impedance of the DS1875 is proportional to its scale setting. For instance, if using the 1/2 scale, the output impedance would be approximately 1.56kΩ.
Note 8: This specification applies to the expected full-scale value for the selected range. See the MOD RANGING register description for available full-scale ranges.
Note 9: The switching frequency is selectable between four values: 131.25kHz, 262.5kHz, 525kHz, and 1050kHz.
Note 10: See the *APC and Quick-Trip Shared Comparator Timing* section for details.
Note 11: Guaranteed by design.
Note 12: I²C interface timing shown is for fast-mode (400kHz) operation. This device is also backward compatible with I²C standard mode.
Note 13: C_B—Total capacitance of one bus line in pF.
Note 14: EEPROM write begins after a STOP condition occurs.

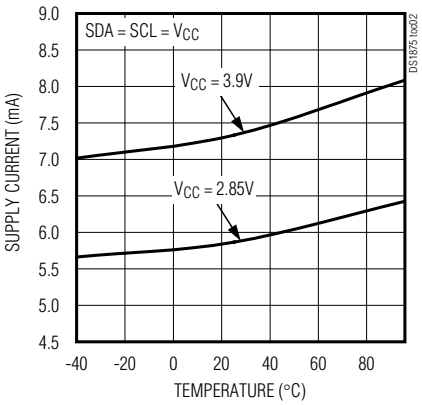
Typical Operating Characteristics

(V_{CC} = +2.85V to +3.9V, T_A = +25°C, unless otherwise noted.)

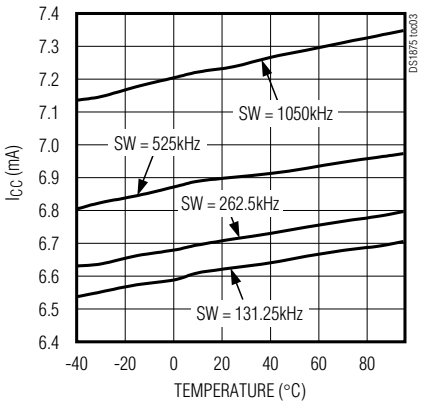
SUPPLY CURRENT vs. SUPPLY VOLTAGE



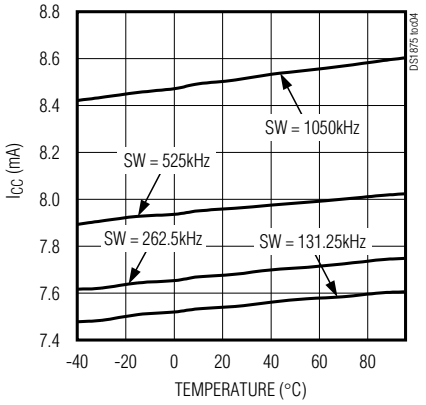
SUPPLY CURRENT vs. TEMPERATURE



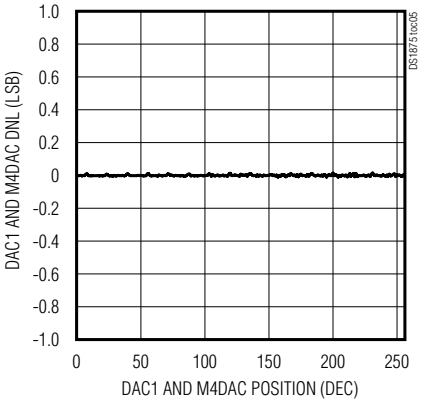
SUPPLY CURRENT vs. TEMPERATURE VCC = 3.3V, NO BIAS CURRENT



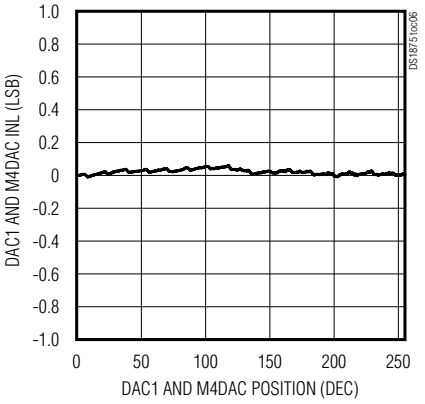
SUPPLY CURRENT vs. TEMPERATURE VCC = 5V, NO BIAS CURRENT



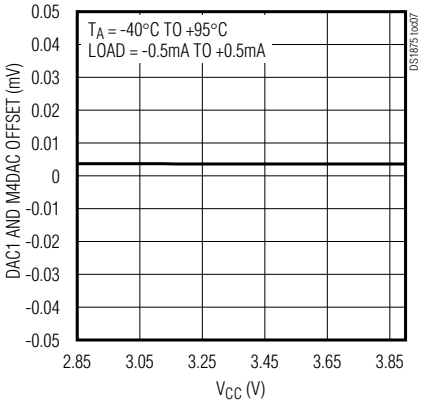
DAC1 AND M4DAC DNL



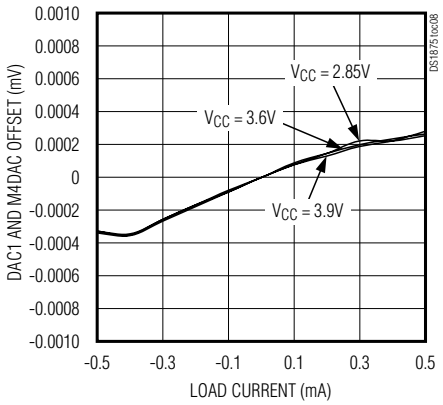
DAC1 AND M4DAC INL



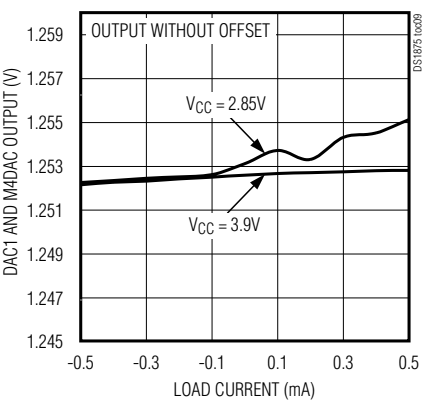
DAC1 AND M4DAC OFFSET vs. VCC



DAC1 AND M4DAC OFFSET VARIATION vs. LOAD CURRENT



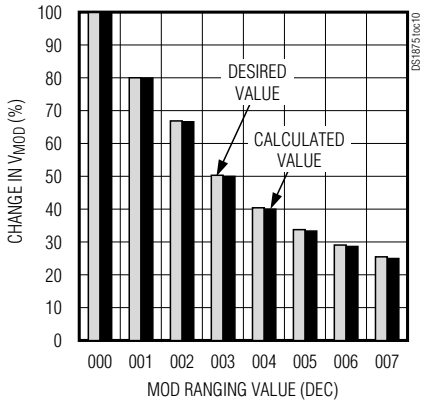
DAC1 AND M4DAC OUTPUT vs. LOAD CURRENT



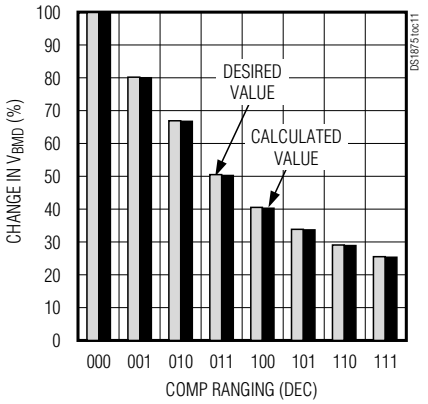
Typical Operating Characteristics (continued)

(V_{CC} = +2.85V to +3.9V, T_A = +25°C, unless otherwise noted.)

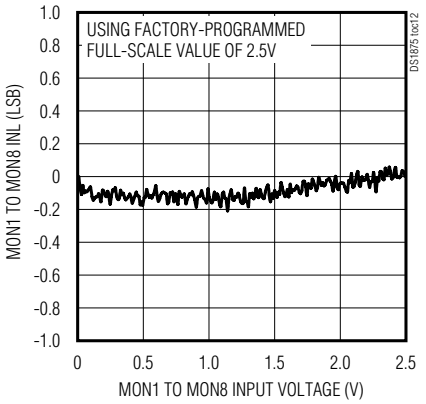
CALCULATED AND DESIRED % CHANGE IN V_{MOD} vs. MOD RANGING



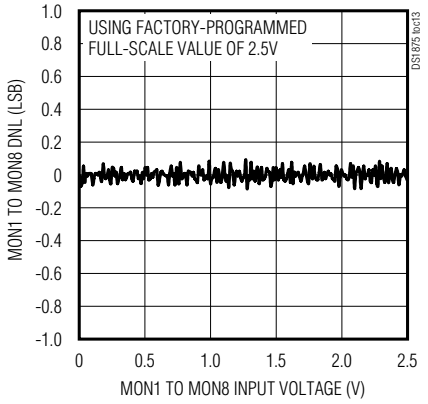
DESIRED AND CALCULATED CHANGE IN V_{BMD} vs. COMP RANGING



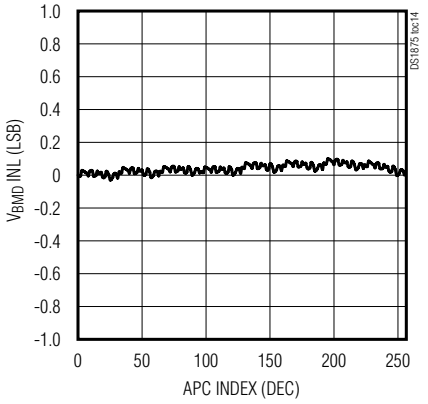
MON1 TO MON8 INL



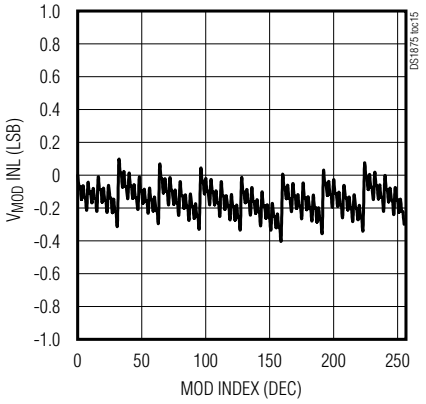
MON1 TO MON8 DNL



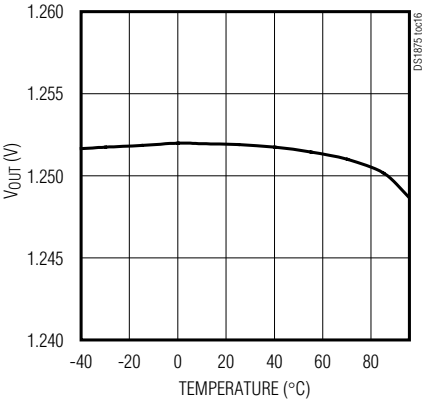
V_{BMD} INL vs. APC INDEX



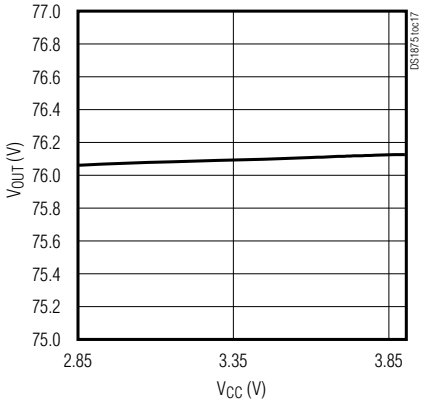
V_{MOD} INL vs. MOD INDEX



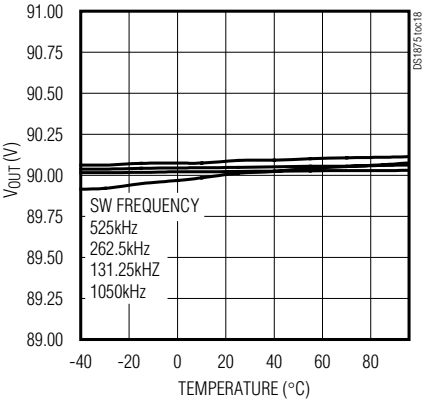
FB VOLTAGE vs. TEMPERATURE PWM DAC = FFh



V_{OUT} vs. V_{CC} V_{IN} = 3.3V



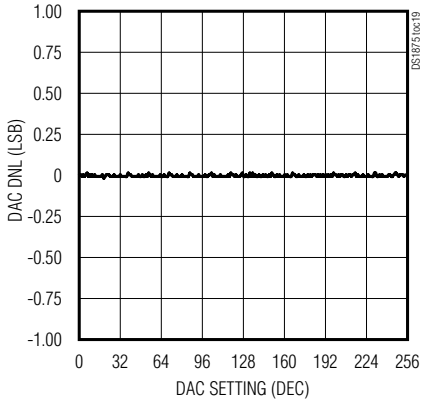
DUTY-CYCLE LIMIT vs. TEMPERATURE



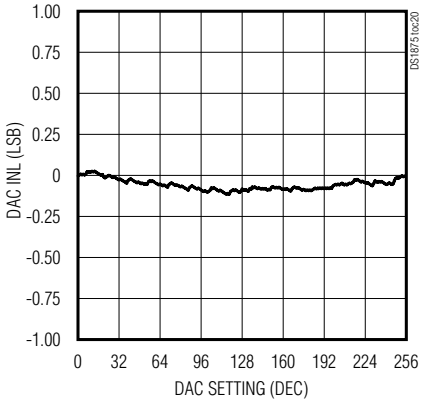
Typical Operating Characteristics (continued)

(V_{CC} = +2.85V to +3.9V, T_A = +25°C, unless otherwise noted.)

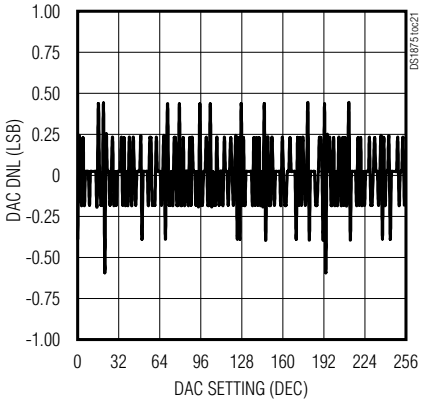
PWM DAC DNL



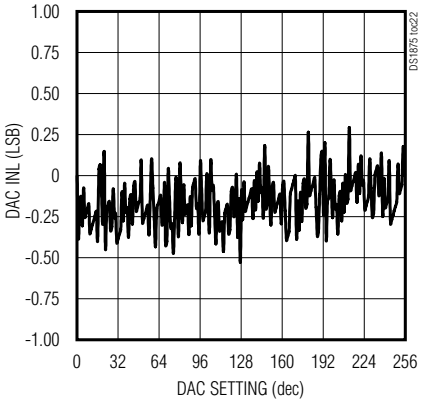
PWM DAC INL



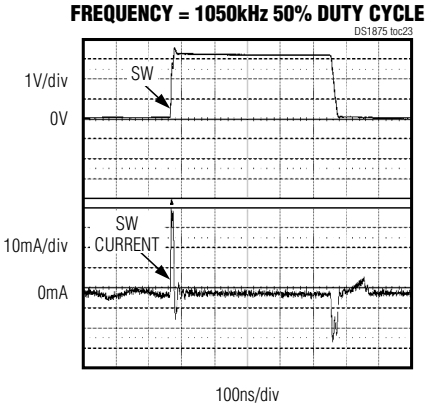
M3QT DAC DNL



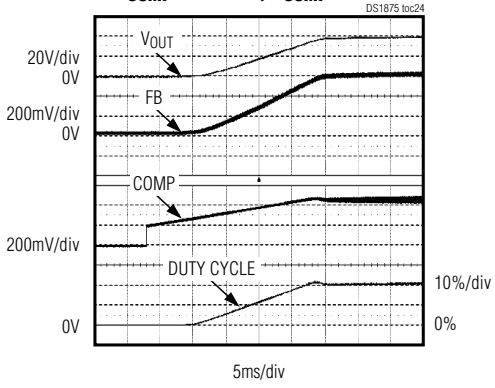
M3QT DAC INL



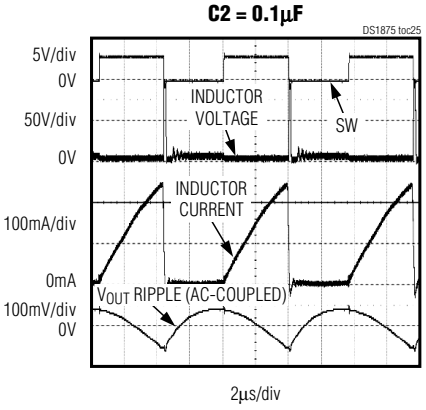
SW CURRENT INTO BSS123 FET
FREQUENCY = 1050kHz 50% DUTY CYCLE



PWM DAC CHANGING FROM 00h TO 80h
R_{COMP} = 24.3kΩ, C_{COMP} = 220nF



SWITCHING WAVEFORMS
V_{IN} = 3.3V, V_{OUT} ~ 90V, I_{OUT} ~ 1.25mA,
C2 = 0.1µF

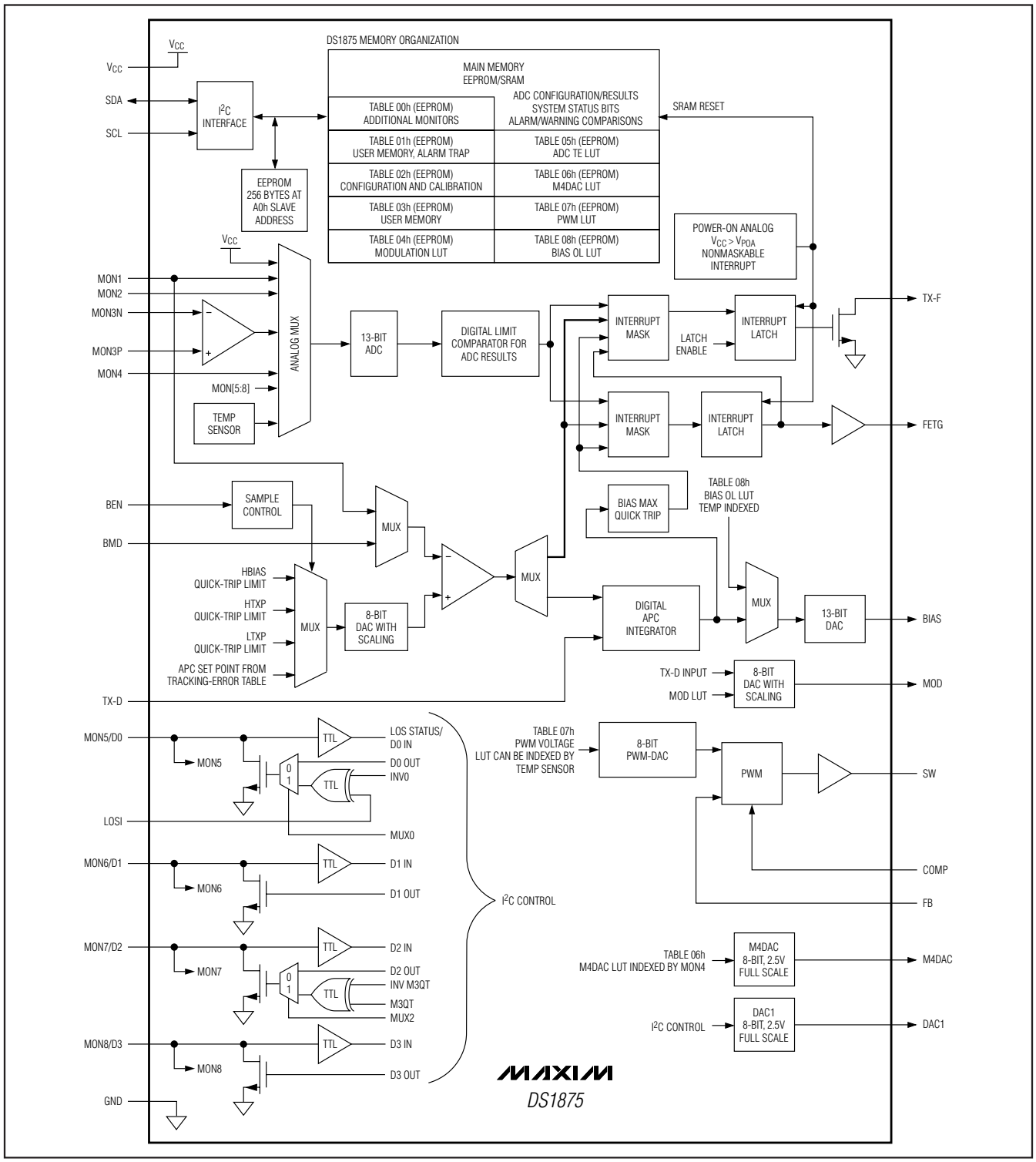


Pin Description

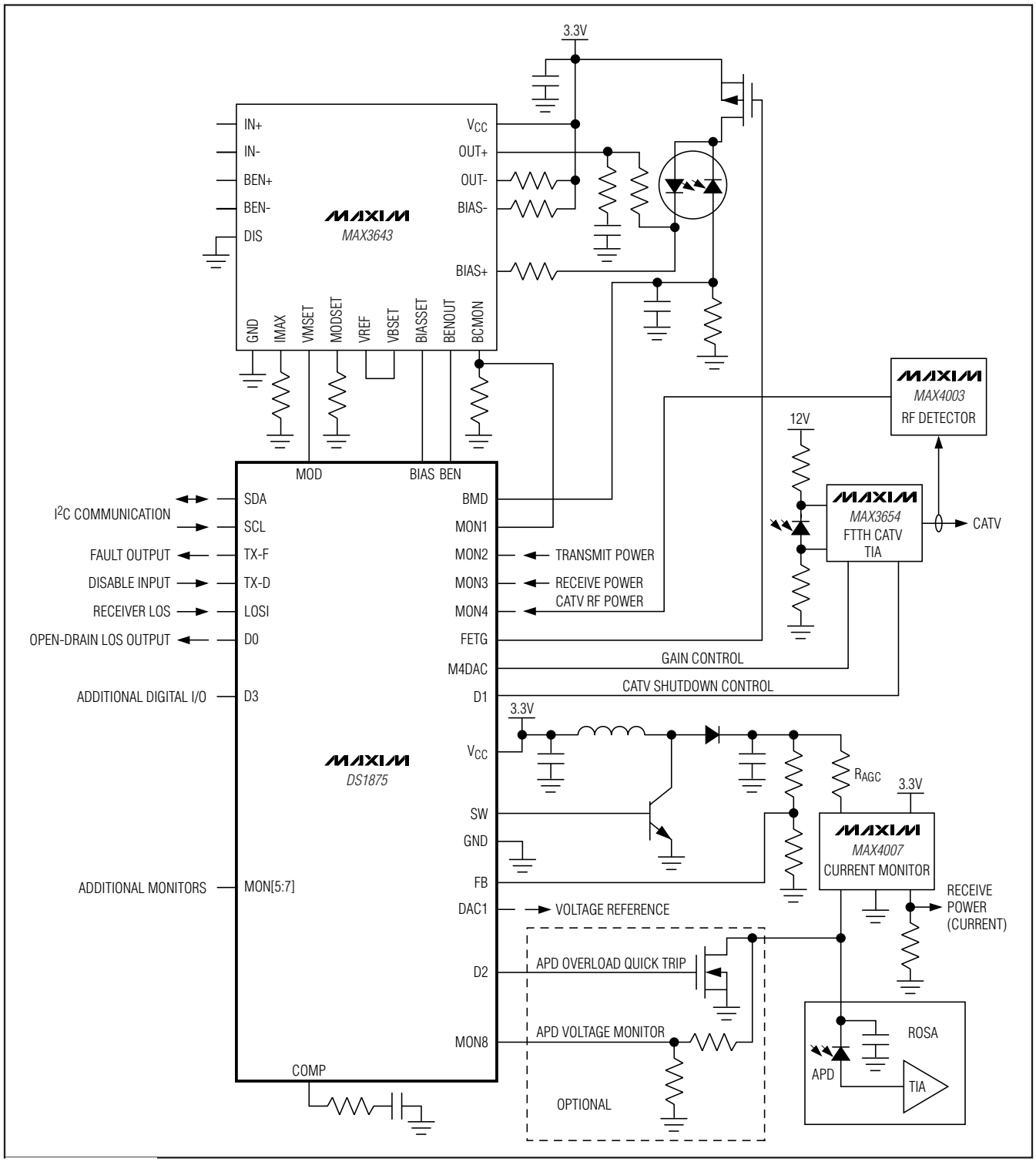
PIN	NAME	FUNCTION
1	BEN	Burst-Enable Input. Triggers the samples for the APC and quick-trip monitors.
2	SDA	I^2C Serial-Data Input/Output
3	SCL	I^2C Serial-Clock Input
4	TX-F	Transmit-Fault Output
5, 7, 11, 20, 36, 37, 38	N.C.	No Connection
6	FETG	FET Gate Output. Signals an external n-channel or p-channel MOSFET to enable/disable the laser's current.
8	TX-D	Transmit-Disable Input. Disables analog outputs.
9, 31, 35	V_{CC}	Power-Supply Input (2.85V to 3.9V)
10, 24, 32, 33	GND	Ground Connection
12	LOSI	Loss-of-Signal Input. Open-collector buffer for external loss-of-signal input. This input is accessible in the status register through the I^2C interface.
13	MON5/D0	External Monitor Input 5 or Digital I/O 0. This signal is the open-collector output driver for IN. It can also be controlled by the MUX0 and OUT0 bits. The voltage level of this pin can be read at IN0. In analog input mode, the voltage at this pin is digitized by the internal 13-bit analog-to-digital converter and can be read through the I^2C interface. Alarm and warning values can be assigned to interrupt the processor based on the ADC result.
14, 15, 16	MON6/D1, MON7/D2, MON8/D3	External Monitor Inputs 6, 7, and 8 or Digital I/O 1, 2, and 3. In digital mode, these open-collector outputs are controlled by the OUTx bits, and their voltage levels can be read at the INx bits. In analog input mode, the voltages at these pins are digitized by the internal 13-bit analog-to-digital converter and can be read through the I^2C interface. Alarm and warning values can be assigned to interrupt the processor based on the ADC result. D2 is configurable as a quick-trip output for MON3.
17, 18, 19	MON1, MON2, MON4	External Monitor Input 1, 2, and 4. The voltage at these pins is digitized by the internal 13-bit analog-to-digital converter and can be read through the I^2C interface. Alarm and warning values can be assigned to interrupt the processor based on the ADC result.
21, 22	MON3N, MON3P	External Monitor Input 3. This is a differential input that is digitized by the internal 13-bit ADC and can be read through the I^2C interface. Alarm and warning values can be assigned to interrupt the processor based on the ADC result. When used as a single-ended input, connect MON3N to ground.
23	DAC1	8-Bit DAC Output. Driven either by I^2C interface or temperature-indexed LUT.
25	M4DAC	8-Bit DAC Output for Generating Analog Voltage. Can be controlled by a LUT indexed by the voltage applied to MON4.
26	FB	Converter Feedback. Input to error amplifier. The other input to the error amplifier is an 8-bit DAC. The DAC can be driven by a temperature-indexed LUT. The output of the error amplifier is the input of the comparator used to create the PWM signal.
27	BIAS	Bias-Current Output. This 13-bit current output generates the bias current reference for the MAX3643.
28	MOD	Modulation Output Voltage. This 8-bit voltage output has eight full-scale ranges from 1.25V to 0.3125V. This pin is connected to the MAX3643's VMSET input to control the modulation current.
29	COMP	Compensation for Error Amplifier in PWM Controller
30	BMD	Back Monitor Diode Input (Feedback Voltage, Transmit Power Monitor)
34	SW	PWM Output. This is typically the switching node of a PWM converter. In conjunction with FB, a boost converter, buck converter, or analog 8-bit output can be created.
—	EP	Exposed Pad

PON Triplexer and SFP Controller

Block Diagram



Typical Operating Circuit



PON Triplexer and SFP Controller

Detailed Description

The DS1875 integrates the control and monitoring functionality required to implement a PON system using Maxim's MAX3643 compact burst-mode laser driver. The compact laser-driver solution offers a considerable cost benefit by integrating control and monitoring features in the low-power CMOS process, while leaving only the high-speed portions to the laser driver. Key components of the DS1875 are shown in the *Block Diagram* and described in subsequent sections. Table 1 contains a list of acronyms used in this data sheet.

Table 1. DS1875 Acronyms

ACRONYM	DEFINITION
10GEPON	10-Gigabit Ethernet PON
ADC	Analog-to-Digital Converter
AGC	Automatic Gain Control
APC	Automatic Power Control
APD	Avalanche Photodiode
BM	Burst Mode
BPON	Broadband PON
CATV	Cable Television
EPON	Ethernet PON
ER	Extinction Ratio
DAC	Digital-to-Analog Converter
FTTH	Fiber-to-the-Home
FTTX	Fiber-to-the-X
GEPON	Gigabit Ethernet PON
GPON	Gigabit PON
LOS	Loss of Signal
LUT	Lookup Table
TE	Tracking Error
TIA	Transimpedance Amplifier
ROSA	Receiver Optical Subassembly
RSSI	Receive Signal Strength Indicator
PON	Passive Optical Network
PWM	Pulse-Width Modulation
SFF	Small Form Factor
SFF-8472	Document Defining Register Map of SFPs and SFFs
SFP	Small Form Factor Pluggable
SFP+	Enhanced SFP
TOSA	Transmit Optical Subassembly

Bias Control

Bias current is controlled by an APC loop. The APC loop uses digital techniques to overcome the difficulties associated with controlling burst-mode systems.

Autodetect Bias Control

This is the default mode of operation. In autodetect bias control, transmit burst length is monitored. A "short burst" is declared when the burst is shorter than expected based on the sample rate setting in Table 02h, Register 88h. In the case that 32 consecutive short bursts are transmitted, the integrator is disabled and the BIAS DAC is loaded from the BIAS LUT (Table 08h). Any single burst of adequate burst length re-enables the APC integrator.

Open-Loop Bias Control

Open-loop control is configured by setting FBOL in Table 02h, Register C7h. In this mode, the BIAS LUT (Table 08h) is directly loaded to the BIAS DAC output. The BIAS LUT can be programmed in 2°C increments over the 40°C to +102°C range. It is left-shifted so that the LUT value is loaded to either the DAC MSB or the DAC MSB-1 (Bit BOLFS, Table 02h, Register 89h).

Closed-Loop Bias Control

The closed-loop control requires a burst length long enough to satisfy the sample rate settings in Table 02h, Register 88h (APC_SR[3:0]). Closed-loop control is configured by setting FBCL in Table 02h, Register C7h. In this mode, the APC integrator is enabled, which controls the BIAS DAC.

The APC loop begins by loading the value from the BIAS LUT (Table 08h) indexed by the present temperature conversion. The feedback for the APC loop is the monitor diode (BMD) current, which is converted to a voltage using an external resistor. The feedback voltage is compared to an 8-bit scaleable voltage reference, which determines the APC set point of the system. Scaling of the reference voltage accommodates the wide range in photodiode sensitivities. This allows the application to take full advantage of the APC reference's resolution.

The DS1875 has an LUT to allow the APC set point to change as a function of temperature to compensate for TE. The TE LUT (Table 05h) has 36 entries that determine the APC setting in 4°C windows between -40°C to +100°C. Ranging of the APC DAC is possible by programming a single byte in Table 02h, Register 8Dh.

DC Operation

When using autodetect mode or closed-loop mode, BEN should be equal to V_{CC} or long burst. In open-loop mode, BEN should be ground or any burst length.

Modulation Control

The MOD output is an 8-bit scaleable voltage output that interfaces with the MAX3643's VMSET input. An external resistor to ground from the MAX3643's MODSET pin sets the maximum current that the voltage at the VMSET input can produce for a given output range. This resistor value should be chosen to produce the maximum modulation current the laser type requires over temperature. Then the MOD output's scaling is used to calibrate the full-scale (FS) modulation output to a particular laser's requirements. This allows the application to take full advantage of the MOD output's resolution. The modulation LUT can be programmed in 2°C increments over the -40°C to +102°C range. Ranging of the MOD DAC is possible by programming a single byte in Table 02h, Register 8Bh.

BIAS and MOD Output During Power-Up

On power-up the modulation and bias outputs remain off until V_{CC} is above V_{POA}, a temperature conversion has been completed, and, if the V_{CC} ADC alarm is enabled, a V_{CC} conversion above the customer-defined V_{CC} low alarm level must clear the V_{CC} low alarm (t_{INIT}). Once all these conditions (t_{INIT}) are satisfied, the MOD output is enabled with the value determined by the temperature conversion and the modulation LUT (Table 04h).

When the MOD output is enabled, the BIAS output is turned on to a value equal to the temperature-indexed value in the BIAS LUT (Table 08h). Next, the APC integrator is enabled, and single LSB steps are taken to tightly control the average power.

If a fault is detected and TX-D is toggled to re-enable the outputs, the DS1875 powers up following a similar sequence to an initial power-up. The only difference is that the DS1875 already determined the present temperature, so the t_{INIT} time is not required for the DS1875 to recall the APC and MOD set points from EEPROM.

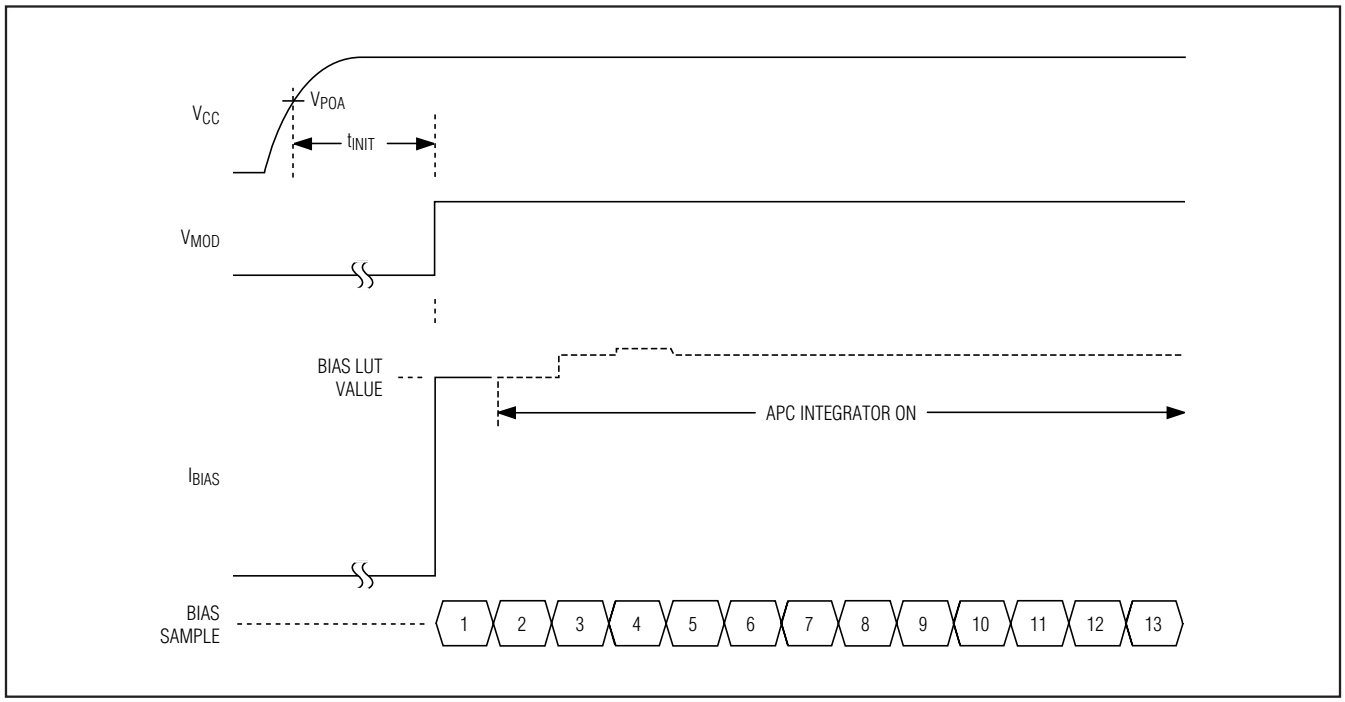


Figure 1. Power-Up Timing (BEN is a Long Burst)

BIAS and MOD Output as a Function of Transmit Disable (TX-D)

If the TX-D pin is asserted (logic 1) during normal operation, the outputs are disabled within t_{OFF}. When TX-D is deasserted (logic 0), the DS1875 turns on the MOD output with the value associated with the present temperature and initializes the BIAS using the same search algorithm used at startup. When asserted, the SOFT TX-D bit (Lower Memory, Register 6Eh) offers a software control identical to the TX-D pin (see Figure 2).

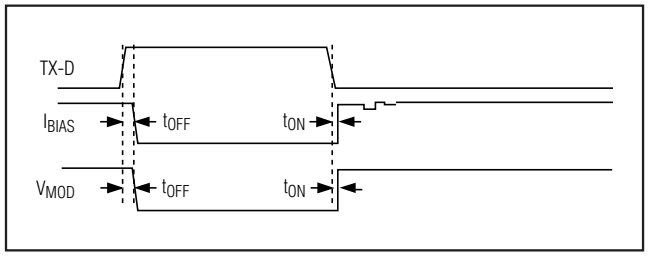


Figure 2. TX-D Timing

APC and Quick-Trip Shared Comparator Timing

As shown in Figure 3, the DS1875's input comparator is shared between the APC control loop and the three quick-trip alarms (TXP HI, TXP LO, and BIAS HI). The comparator polls the alarms in a multiplexed sequence. Six of every eight comparator readings are used for APC loop-bias current control. The other two updates are used to check the HTXP/LTXP (monitor diode voltage) and the HBIAS (MON1) signals against the internal APC and BIAS reference. If the last APC comparison was higher than the APC set point, it makes an HTXP comparison, and if it is lower, it makes an LTXP comparison. Depending on the results of the comparison, the corresponding alarms and warnings (TXP HI, TXP LO) are asserted or deasserted.

The DS1875 has a programmable comparator sample time based on an internally generated clock to facilitate a wide variety of external filtering options suitable for burst-mode transmitters. The rising edge of BEN triggers the sample to occur, and the Update Rate register (Table 02h, Register 88h) determines the sampling time. The first sample occurs (t_{FIRST}) after the rising edge of BEN. The internal clock is asynchronous to BEN, causing a ±50ns uncertainty regarding when the first sample will occur following BEN. After the first sample occurs, subsequent samples occur on a regular interval, t_{REP}. Table 2 shows the sample rate options available.

Updates to the TXP HI and TXP LO quick-trip alarms do not occur during the BEN low time. The BIAS HI quick trip can be sampled during the burst-low time. Any

Table 2. Update Rate Timing

APC_SR[3:0]	MINIMUM TIME FROM BEN TO FIRST SAMPLE (t_{FIRST}) ±50ns (ns)	REPEATED SAMPLE PERIOD FOLLOWING FIRST SAMPLE (t_{REP}) (ns)
0000b	350	800
0001b	550	1200
0010b	750	1600
0011b	950	2000
0100b	1350	2800
0101b	1550	3200
0110b	1750	3600
0111b	2150	4400
1000b	2950	6000
1001b*	3150	6400

**All codes greater than 1001b (1010b to 1111b) use the maximum sample time of code 1001b.*

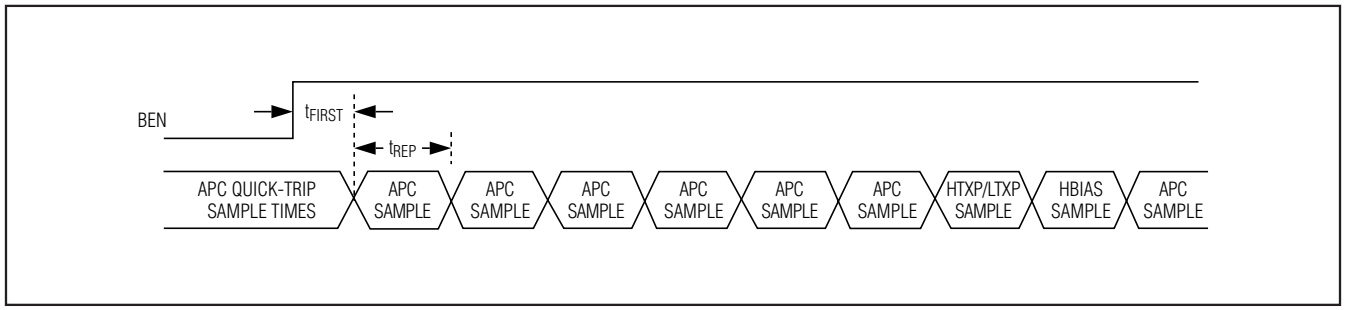


Figure 3. APC Loop and Quick-Trip Sample Timing

quick-trip alarm that is detected by default remains active until a subsequent comparator sample shows the condition no longer exists. A second bias-current monitor (BIAS MAX) compares the DS1875's BIAS DAC's code to a digital value stored in the MAX BIAS register. This comparison is made at every bias-current update to ensure that a high bias current is quickly detected.

Monitors and Fault Detection

Monitors

Monitoring functions on the DS1875 include a power-on analog (POA) V_{CC} comparison, five quick-trip comparators, and ADC channels. This monitoring combined with the interrupt masks determine if the DS1875 shuts down its outputs and triggers the TX-F and FETG outputs. All the monitoring levels and interrupt masks are user programmable with the exception of POA, which trips at a fixed range and is nonmaskable for safety reasons.

Power-On Analog (POA)

POA holds the DS1875 in reset until V_{CC} is at a suitable level ($V_{CC} > V_{POA}$) for the part to accurately measure with its ADC and compare analog signals with its quick-trip monitors. Because V_{CC} cannot be measured by the ADC when V_{CC} is less than V_{POA}, POA also asserts the V_{CC} low alarm, which is cleared by a V_{CC} ADC conversion greater than the customer-programmable V_{CC} low ADC limit. This allows a programmable limit to ensure that the head room requirements of the transceiver are satisfied during slow power-up. The TX-F and FETG outputs do not latch until there is a conversion above the V_{CC} low limit. The POA alarm is nonmaskable. The TX-F and FETG outputs are asserted when V_{CC} is below V_{POA}. See the *Low-Voltage Operation* section for more information.

Five Quick-Trip Monitors and Alarms

Five quick-trip monitors are provided to detect potential laser safety issues. These monitor:

1) High Bias Current (HBIAS)

2) Low Transmit Power (LTXP)

3) High Transmit Power (HTXP)

4) Max Output Current (BIAS MAX)

5) MON3 Quick Trip (M3QT)

The high- and low-transmit power quick-trip registers (HTXP and LTXP) set the thresholds used to compare against the BMD voltage to determine if the transmit power is within specification. The HBIAS quick trip compares the MON1 input (generally from the MAX3643 bias monitor output) against its threshold setting to determine if the present bias current is above specification. The BIAS MAX quick trip is a digital comparison that determines if the BIAS DAC indicates that the bias current is above specification. I_{BIAS} is not allowed to exceed the value set in the MAX BIAS register. When the DS1875 detects that the bias is at the limit, it sets the BIAS MAX status bit and clamps the bias current at the MAX BIAS level. In the closed-loop mode, if the recalled value from the BIAS LUT is greater than MAX BIAS then, the update is not done and I_{BIAS} reverts to the previous I_{BIAS} value. The quick trips are routed to the TX-F and FETG outputs through interrupt masks to allow combinations of these alarms to be used to trigger these outputs. When FETG is triggered, the DS1875 also disables the MOD and BIAS outputs. See the *BIAS and MOD Output During Power-Up* section for details.

MON3 Quick Trip

One additional quick trip is used to protect the APD from overcurrent. MON3P is used to monitor the current through the APD. When MON3P exceeds a threshold set by the M3QT DAC register (Table 02h, Register C3h), the PWM is shut down by blocking SW pulses. The MON3 comparison is single-ended referenced to ground. In the case where MON3 is used differentially and not referenced to ground, this must be considered when setting the MON3 quick-trip threshold. Additionally, the D2 pin can be driven either high or low as determined by INV M3QT and MUX M3QT bits in Lower Memory, Register 79h. An external switch controlled by pin D2 may be used to clamp the converter's output when MON3 quick trip occurs. This external switch discharges the output voltage much faster than allowing the load to discharge the rail. The MON3 quick-trip alarm can be latched by enabling M3QT LEN in Table 02h, Register 89h. The latch is reset by setting M3QT RESET in Lower Memory, Register 78h. A soft quick trip is performed by setting SOFT M3QT in Lower Memory, Register 78h (see Figure 4).

ADC Monitors and Alarms

The ADC monitors six channels that measure temperature (internal temp sensor), V_{CC}, and MON1–MON4 using an analog multiplexer to measure them round robin with a single ADC. Each channel has a customer-programmable full-scale range and offset value that is factory programmed to default value (see Table 3). Additionally, MON1–MON4 can right-shift results by up to 7 bits before the results are compared to alarm thresholds or read over the I^2C bus. This allows customers with specified ADC ranges to calibrate the ADC full scale to a factor of $1/2^n$ their specified range to measure small signals. The DS1875 can then right-shift the results by n bits to maintain the bit weight of their specification.

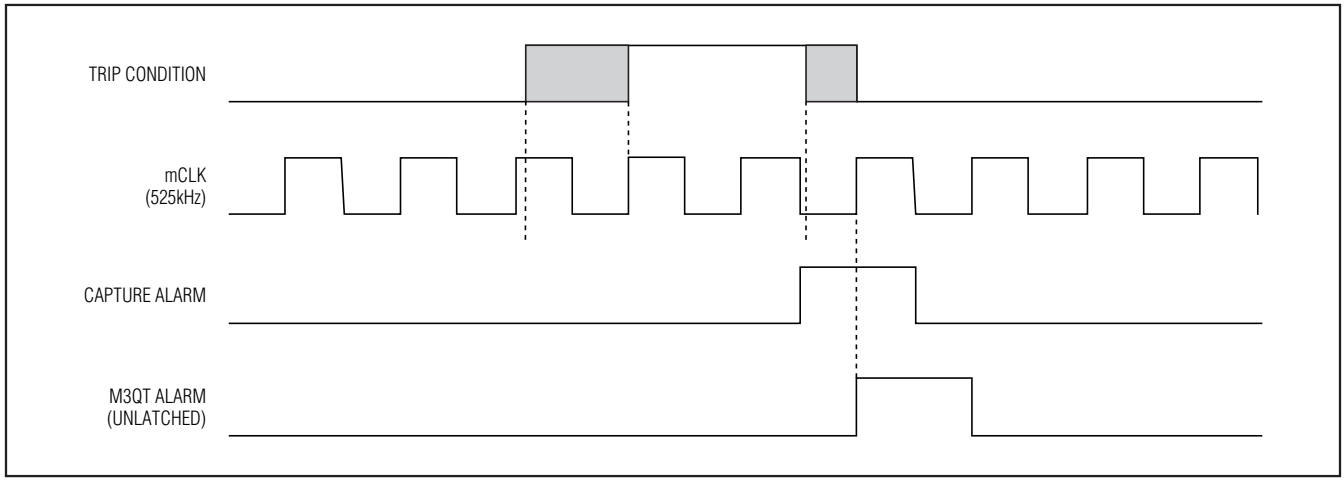


Figure 4. M3QT Timing

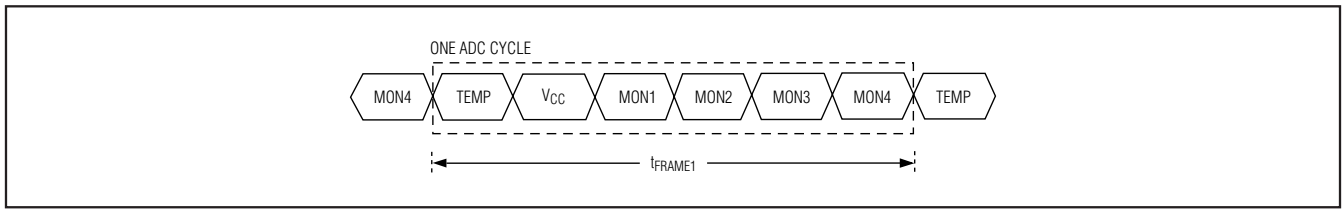


Figure 5. ADC Timing with EN5TO8B = 0

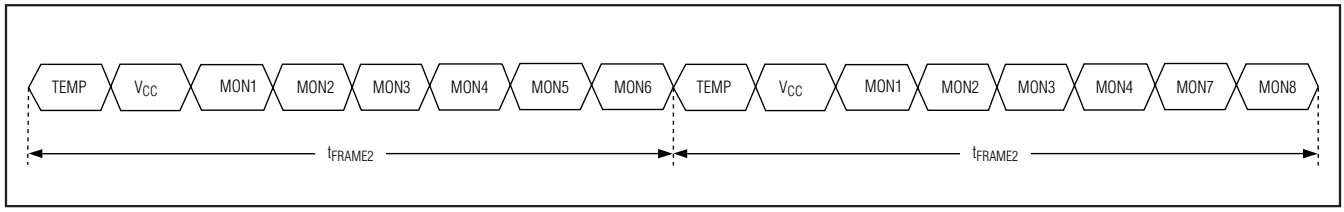


Figure 6. ADC Timing with EN5TO8B = 1

The ADC results (after right-shifting, if used) are compared to high and low alarm and warning thresholds after each conversion. The alarm values can be used to trigger the TX-F or FETG outputs. These ADC thresholds are user programmable through the I^2C interface, as well as masking registers that can be used to prevent the alarms from triggering the TX-F and FETG outputs.

Table 3. ADC Default Monitor Ranges

SIGNAL	+FS SIGNAL	+FS HEX	-FS SIGNAL	-FS HEX
Temperature (°C)	127.996	7FFF	-128	8000
V_{CC} (V)	6.5528	FFF8	0	0000
MON1–MON8 (V)	2.4997	FFF8	0	0000

ADC Timing

There are 10 analog channels that are digitized in a sequential fashion. The MON5–MON8 channels are sampled depending on the state of the EN5TO8B bit in Table 02h, Register 89h. If the bit is programmed to logic 0, the ADC cycles through temperature, V_{CC}, and MON1–MON4 (Figure 5). If the bit is programmed to logic 1, all 10 channels are digitized, including channels MON5–MON8 (Figure 6). In this mode (EN5TO8B = 0), each of MON5–MON8 is sampled on alternate cycles, as shown in Figure 5. The total time required to convert one set of channels is the sequential ADC cycle time, t_{FRAME1} or t_{FRAME2} (see Figure 6).

Right-Shifting ADC Result

If the weighting of the ADC digital reading must conform to a predetermined full-scale value defined by a standard's specification, then right-shifting can be used to adjust the predetermined full-scale analog measurement range while maintaining the weighting of the ADC results. The DS1875's range is wide enough to cover all requirements; when the maximum input value is ≤ 1/2 the FS value, right-shifting can be used to obtain greater accuracy. For instance, the maximum voltage might be 1/8th the specified predetermined full-scale value, so only 1/8th the converter's range is used. An alternative is to calibrate the ADC's full-scale range to 1/8th the readable predetermined full-scale value and use a right-shift value of 3. With this implementation, the resolution of the measurement is increased by a factor of 8, and because the result is digitally divided by 8 by right-shifting, the bit weight of the measurement still meets the standard's specification (i.e., SFF-8472).

The right-shift operation on the ADC result is carried out based on the contents of RIGHT SHIFT1/0 registers (Table 02h, Registers 8Eh–8Fh). Four analog channels, MON1–MON4, have 3 bits each allocated to set the number of right-shifts. Up to seven right-shift operations are allowed and are executed as a part of every conversion before the results are compared to the high and low alarm levels, or loaded into their corresponding measurement registers (Table 01h, Registers 62h–6Bh). This is true during the setup of internal calibration as well as during subsequent data conversions.

Transmit Fault (TX-F) Output

The TX-F output has masking registers for the ADC alarms and the QT alarms to select which comparisons cause it to assert. In addition, the FETG alarm is selectable through the TX-F mask to cause TX-F to assert. All alarms, with the exception of FETG, only cause TX-F to remain active while the alarm condition persists. However, the TX-F latch bit can enable the TX-F output to remain active until it is cleared by the TX-F reset bit, TX-D, SOFT TX-D, or by power cycling the part. If the FETG output is configured to trigger TX-F, it indicates that the DS1875 is in shutdown and requires TX-D, SOFT TX-D, or cycling power to reset. Only enabled alarms activate TX-F (see Figure 7). Table 4 shows TX-F as a function of TX-D and the alarm sources.

Table 4. TX-F as a Function of TX-D and Alarm Sources

$V_{CC} > V_{POA}$	TX-D	NONMASKED TX-F ALARM	TX-F
No	X	X	1
Yes	0	0	0
Yes	0	1	1
Yes	1	X	0

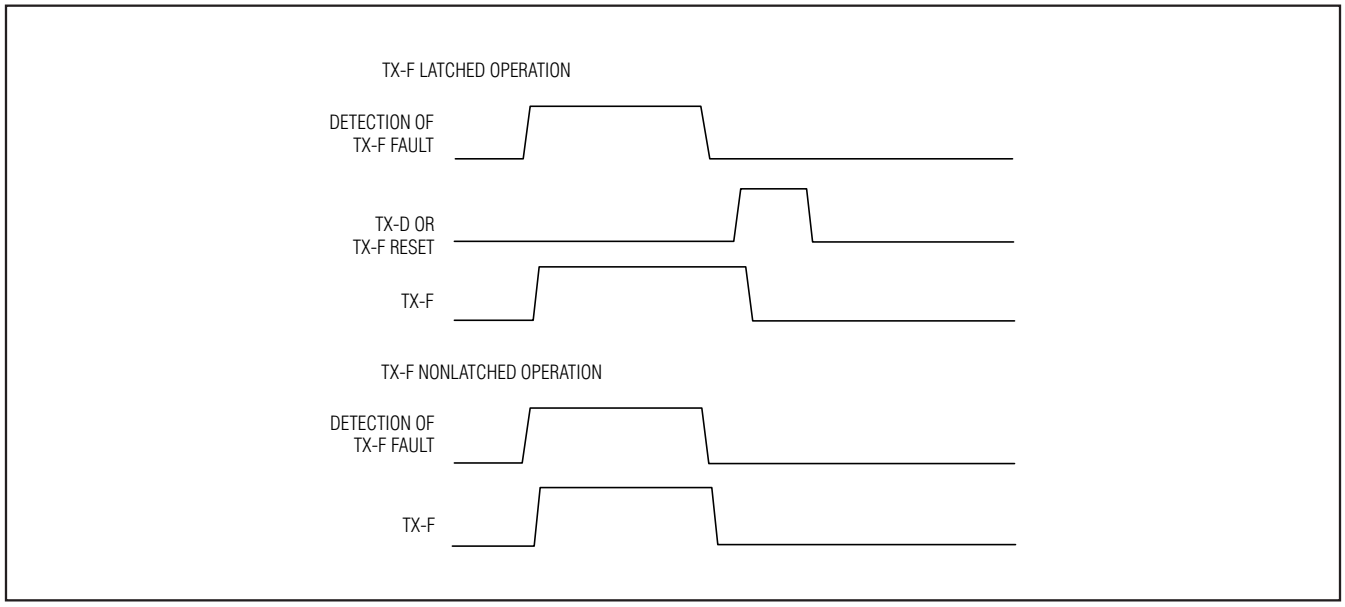


Figure 7. TX-F Timing

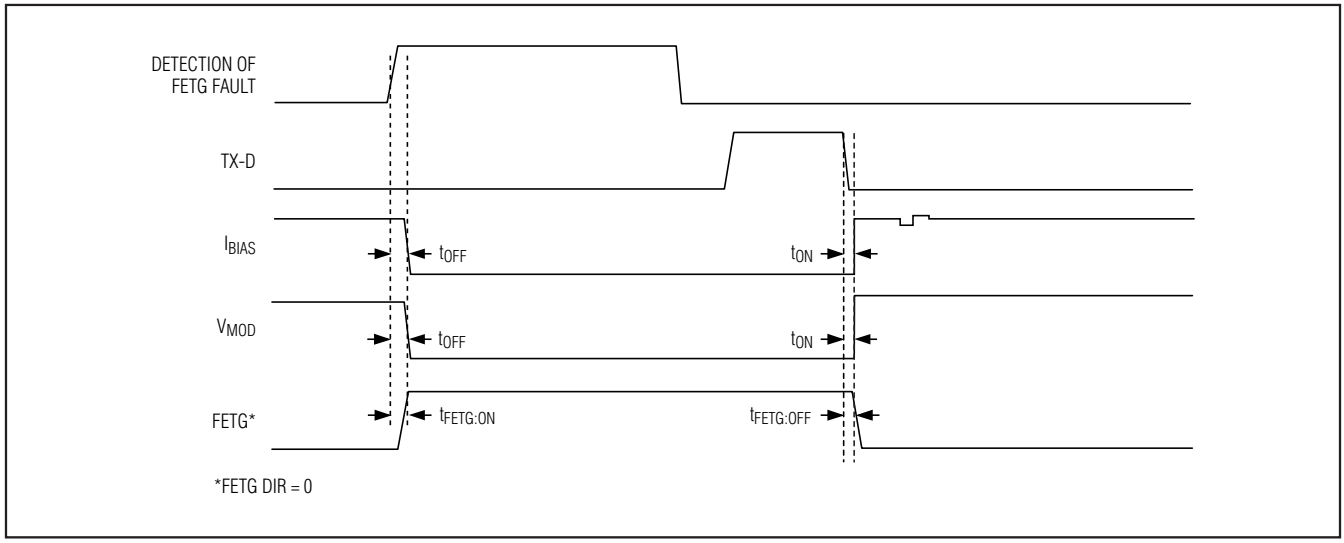


Figure 8. FETG/Output Disable Timing (Fault Condition Detected)

Safety Shutdown (FETG) Output

The FETG output has masking registers (separate from TX-F) for the ADC alarms and the QT alarms to select which comparisons cause it to assert. Unlike TX-F, the FETG output is always latched. Its output polarity is programmable to allow an external nMOS or pMOS to open during alarms to shut off the laser-diode current. If the FETG output triggers, indicating that the DS1875 is in shutdown, it requires TX-D, SOFT TX-D, or cycling power to be reset. Under all conditions, when the analog outputs are reinitialized after being disabled, all the alarms with the exception of the V_{CC} low ADC alarm are cleared. The V_{CC} low alarm must remain active to prevent the output from attempting to operate when inadequate V_{CC} exists to operate the laser driver. Once adequate V_{CC} is present to clear the V_{CC} low alarm, the outputs are enabled following the same sequence as the power-up sequence.

As previously mentioned, the FETG is an output used to disable the laser current through a series nMOS or pMOS. This requires that the FETG output can sink or source current. Because the DS1875 does not know if it should sink or source current before V_{CC} exceeds V_{POA}, which triggers the EE recall, this output is high impedance when V_{CC} is below V_{POA} (see the *Low-Voltage Operation* section for details and diagram). The application circuit should use a pullup or pulldown resistor on this pin that pulls FETG to the alarm/shutdown state (high for a pMOS, low for a nMOS). Once V_{CC} is above V_{POA}, the DS1875 pulls the FETG output to the state determined by the FETG DIR bit (Table 02h, Register 89h). Set FETG DIR to 0 if an nMOS is used and 1 if a pMOS is used.

Table 5. FETG, MOD, and BIAS Outputs as a Function of TX-D and Alarm Sources

$V_{CC} > V_{POA}$	TX-D	NONMASKED FETG ALARM	FETG	MOD AND BIAS OUTPUTS
Yes	0	0	FETG DIR	Enabled
Yes	0	1	FETG DIR	Disabled
Yes	1	X	FETG DIR	Disabled

Determining Alarm Causes Using the I²C Interface

To determine the cause of the TX-F or FETG alarm, the system processor can read the DS1875's alarm trap bytes (ATB) through the I²C interface (Table 01h, Registers F8h–FBh). The ATB has a bit for each alarm. Any time an alarm occurs, regardless of the mask bit's state, the DS1875 sets the corresponding bit in the ATB. Active ATB bits remain set until written to 0s through the I²C interface. On power-up, the ATB is 0s until alarms dictate otherwise. FETG causes additional alarms that make it difficult to determine the root cause of the problem. Therefore, no updates are made to the ATB when FETG occurs.

Die Identification

The DS1875 has an ID hard-coded to its die. Two registers (Table 02h, Registers 86h–87h) are assigned for this feature. Byte 86h reads 75h to identify the part as the DS1875; byte 87h reads the die revision.

Low-Voltage Operation

The DS1875 contains two power-on reset (POR) levels. The lower level is a digital POR (V_{POD}) and the higher level is an analog POR (V_{POA}). At startup, before the supply voltage rises above V_{POA}, the outputs are disabled (FETG and BIAS outputs are high impedance, MOD is low), all SRAM locations are low (including shadowed EEPROM (SEE)), and all analog circuitry is disabled. When V_{CC} reaches V_{POA}, the SEE is recalled, and the analog circuitry is enabled. While V_{CC} remains above V_{POA}, the device is in its normal operating state, and it responds based on its nonvolatile configuration. If during operation V_{CC} falls below V_{POA} but is still above V_{POD}, the SRAM retains the SEE settings from the first SEE recall, but the device analog is shut down and the outputs are disabled. FETG is driven to its alarm state defined by the FETG DIR bit (Table 02h, Register 89h). If the supply voltage recovers back above V_{POA}, the device immediately resumes normal functioning. When the supply voltage falls below V_{POD}, the device SRAM is placed in its default state and another SEE recall is required to reload the nonvolatile settings. The EEPROM recall occurs the next time V_{CC} exceeds V_{POA}. Figure 9 shows the sequence of events as the voltage varies.

Any time V_{CC} is above V_{POD}, the I^2C interface can be used to determine if V_{CC} is below the V_{POA} level. This is accomplished by checking the RDYB bit in the status (Lower Memory, Register 6Eh) byte. RDYB is set when V_{CC} is below V_{POA}. When V_{CC} rises above V_{POA}, RDYB is timed (within 500µs) to go to 0, at which point the part is fully functional.

For all device addresses sourced from EEPROM (Table 02h, Register 8Ch), the default device address is A2h until V_{CC} exceeds V_{POA}, allowing the device address to be recalled from the EEPROM.

Enhanced RSSI Monitoring (Dual Range Functionality)

The DS1875 offers a new feature to improve the accuracy and range of MON3, which is most commonly used for monitoring RSSI. This feature enables right-shifting (along with its gain and offset settings) when the input signal is below a set threshold (within the range that benefits using right-shifting) and then automatically disables right-shifting (recalling different gain and offset settings) when the input signal exceeds the threshold. Also, to prevent “chattering,” hysteresis prevents excessive switching between modes in addition to ensuring that continuity is maintained. Dual range operation is enabled by default (factory programmed in EEPROM). However, it can easily be disabled through the RSSI_FF and RSSI_FC bits. When dual range operation is disabled, MON3 operates identically to the other MON channels, although featuring a differential input.

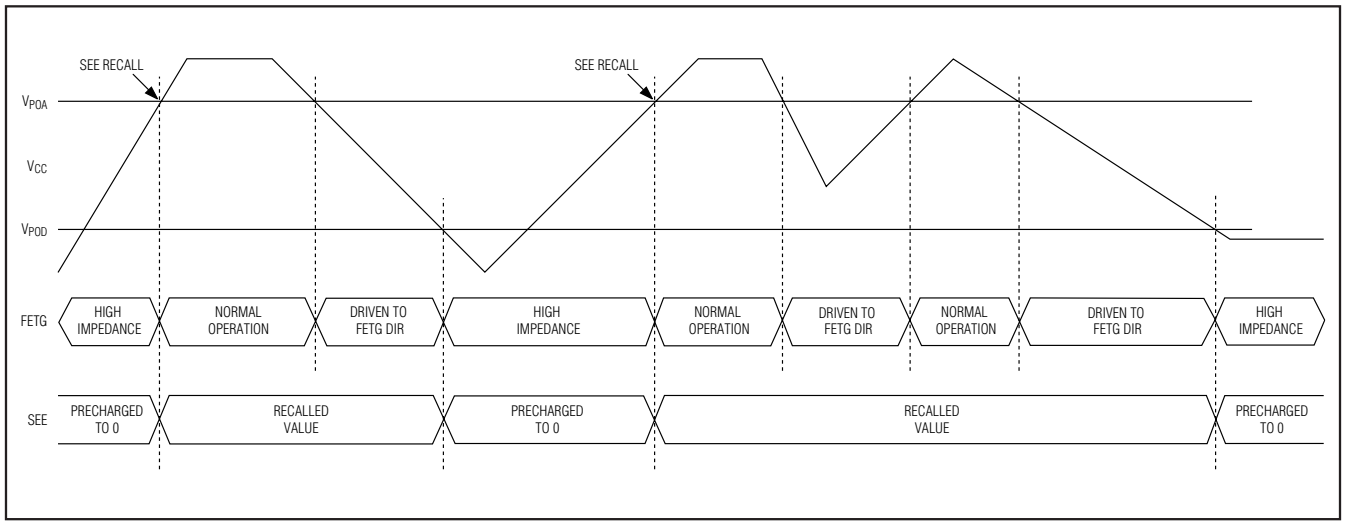


Figure 9. SEE Timing

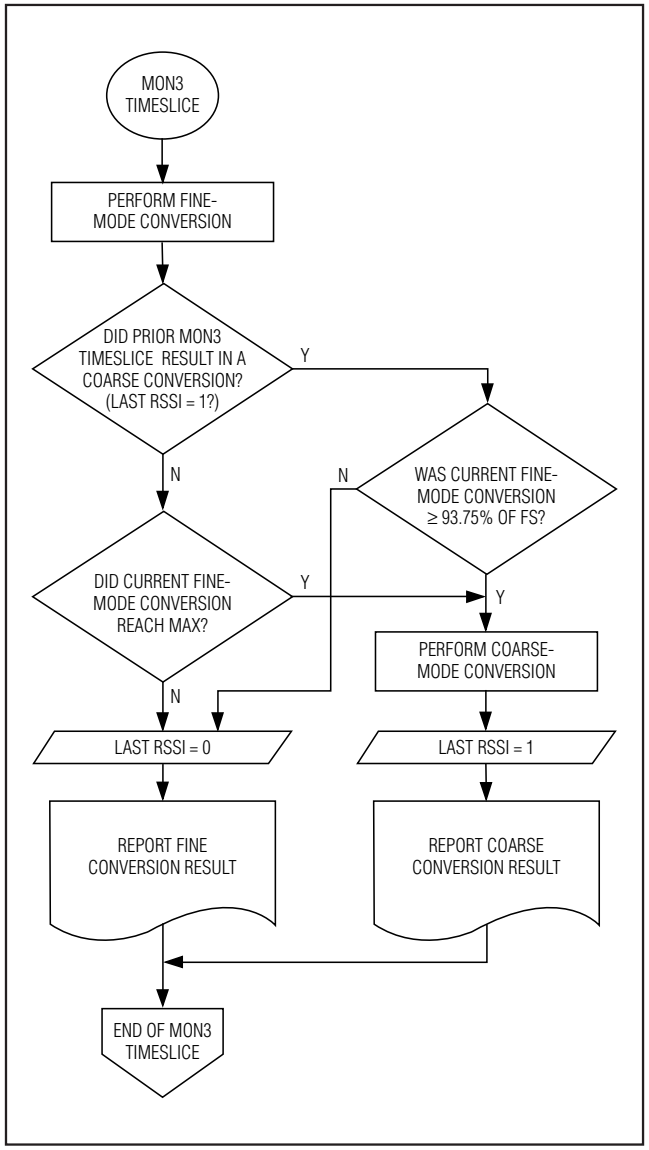


Figure 10. RSSI Flowchart

Dual-range functionality consists of two modes of operation: fine mode and coarse mode. Each mode is calibrated for a unique transfer function, hence the term, dual range. Table 6 highlights the registers related to MON3. Fine mode is equivalent to the other MON channels. Fine mode is calibrated using the gain, offset, and right-shifting registers at locations shown in Table 6 and is ideal for relatively small analog input voltages. Coarse mode is automatically switched to when the input exceeds the threshold (to be discussed in a subsequent paragraph). Coarse mode is calibrated using different gain and offset registers, but lacks right-shifting (since coarse mode is only used on large input signals). The gain and offset registers for coarse mode are also shown in Table 6. With the use of right-shifting, the fine mode full scale is programmed to (1/2N)th the coarse mode full scale. The DS1875 will now autorange to choose the range that gives the best resolution for the measurement. To eliminate chatter, 6.25% of hysteresis is applied when the input resides at the boundary of the two ranges. See Figure 10. Additional information for each of the registers can be found in the *Memory Map* section.

Dual range operation is transparent to the end user. The results of MON3 analog-to-digital conversions are still stored/reported in the same memory locations (68–69h, Lower Memory) regardless of whether the conversion was performed in fine mode or coarse mode.

When the DS1875 is powered up, analog-to-digital conversions begin in a round-robin fashion. Every MON3 timeslice begins with a fine mode analog-to-digital conversion (using fine mode's gain, offset, and right-shifting settings). See the flowchart in Figure 10. Then, depending on whether the last MON3 timeslice resulted in a coarse-mode conversion and also depending on the value of the current fine conversion, decisions are made whether to use the current fine-mode conversion result or to make an additional conversion (within the same MON3 timeslice), using coarse mode (using coarse mode's gain and offset settings, and no right-shifting) and reporting the coarse-mode result. The flowchart also illustrates how hysteresis is implemented. The fine-mode conversion is compared to one of

Table 6. MON3 Configuration Registers

REGISTER	FINE MODE	COARSE MODE
MON3 FINE SCALE	98h–99h, Table 02h	9Ch–9Dh, Table 02h
MON3 FINE OFFSET	A8h–A9h, Table 02h	ACh–ADh, Table 02h
RIGHT SHIFT0/1	8Eh–8Fh, Table 02h	—
CONFIG (RSSI_FC, RSSI_FF bits)	89h, Table 02h	
MON3 VALUE	68h–69h, Lower Memory	

Table 7. MON3 Hysteresis Threshold Values

NO. OF RIGHT-SHIFTS	FINE MODE (MAX)	COARSE MODE (MIN*)
0	FFF8h	F000h
1	7FFCh	7800h
2	3FFEh	3C00h
3	1FFFh	1E00h
4	0FFFh	0F00h
5	07FFh	0780h
6	03FFh	03C0h
7	01FFh	01E0h

**This is the minimum reported coarse-mode conversion.*

two thresholds. The actual threshold values are a function of the number of right-shifts being used. Table 7 shows the threshold values for each possible number of right-shifts.

The RSSI_FF and RSSI_FC (Table 02h, Register 89h) bits are used to force fine-mode or coarse-mode conversions, or to disable the dual-range functionality. Dual-range functionality is enabled by default (both RSSI_FC and RSSI_FF are factory programmed to 0 in EEPROM). It can be disabled by setting RSSI_FC to 0 and RSSI_FF to 1. These bits are also useful when calibrating MON3. For additional information, see the *Memory Map* section.

PWM Controller

The DS1875 has a PWM controller that, when used with external components, generates a low-noise, high-voltage output to bias APDs in optical receivers. The achievable boost voltage is determined by the external component selection. Figure 12 shows a typical schematic. Selection of switching frequency, external inductor, capacitors, resistor network, switching FET, and switch diode determine the performance of the DC-DC converter. The PWM controller can be configured in boost or buck mode. Both modes require an external nMOS or npn transistor.

The DS1875 PWM controller consists of several sections used to create a PWM signal to drive a DC-DC converter. Figure 11 is a block diagram of the DS1875 PWM controller. Following is a description of each block in the PWM controller and some guidelines for selecting components for the DC-DC converter.

The PWM DAC is used to set the desired output voltage of the DC-DC converter section. The feedback from the DC-DC converter is compared to the output from the PWM DAC by an error amplifier. If the FB level is less

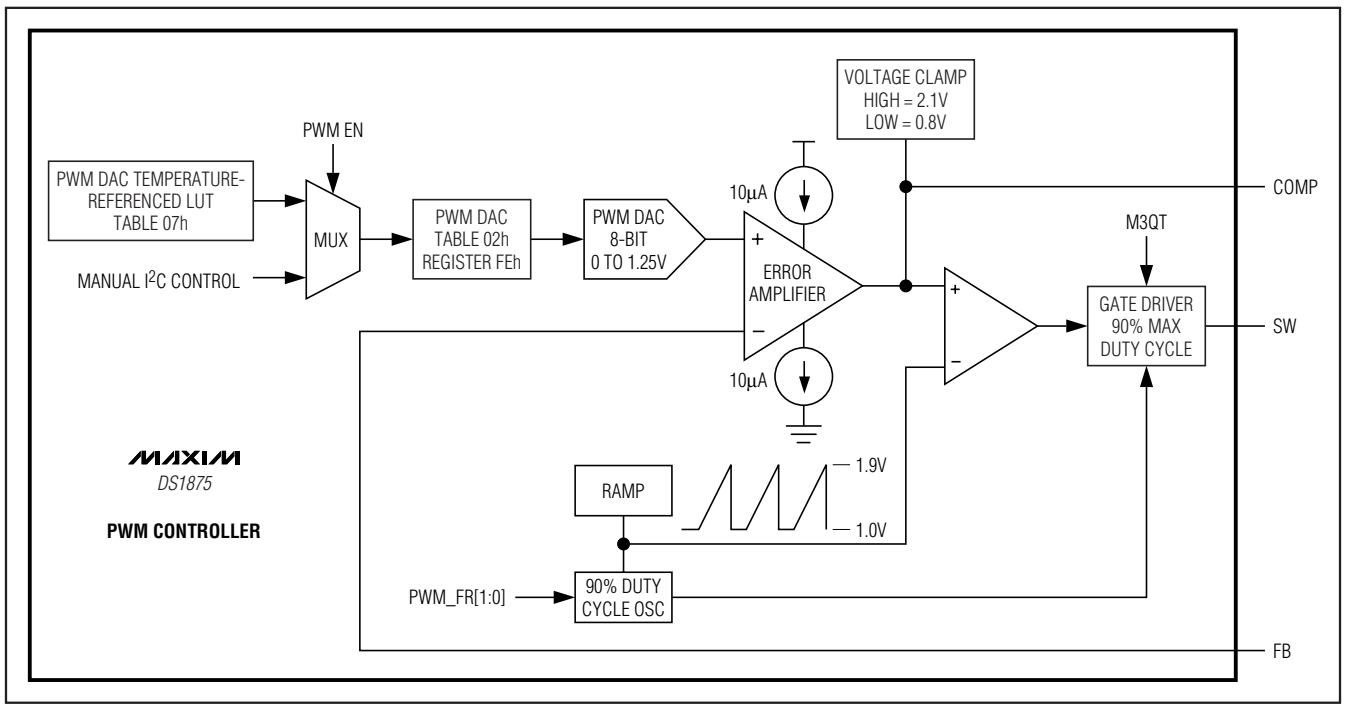


Figure 11. PWM Controller Diagram

than the PWM DAC level, the error amplifier increases the level on the COMP pin. The level on the COMP pin is compared to the signal from the oscillator and ramp generator to set the duty cycle that is input to the gate driver and maximum duty-cycle limiting block. An increase on the COMP pin increases the duty cycle. Conversely, if FB is greater than the PWM DAC, the level on COMP is decreased, decreasing the duty cycle. The gate driver and maximum duty-cycle block is used to limit the maximum duty cycle of the PWM controller to 90%. This block also disables the PWM driver if an M3QT has resulted from the APD current exceeding a desired limit.

The output from the PWM DAC is used to control the output voltage of the DC-DC converter. The values for the PWM DAC are recalled from the Table 07h, which is a temperature-indexed LUT. The temperature-indexed value from the LUT is written to the PWM DAC register (Table 02h, Register FEh), which updates the setting of the PWM DAC. The PWM DAC can also be operated in a manual mode by disabling the automatic updating from the LUT. This is done by clearing the PWM EN bit (Table 02h, Register 80h, Bit 5). The PWM DAC full-scale output is 1.25V with 8 bits of resolution. When designing the feedback for the DC-DC converter section, the user needs to make sure that the desired level applied to the FB pin is in this range.

The COMP pin is driven by the error amplifier comparing the PWM DAC to the DC-DC converter feedback signal at the FB pin. The error amplifier can sink and source 10µA. An external resistor and capacitor connected to the COMP pin determine the rate of change the COMP pin. The resistor provides an initial step when the current from the error amplifier changes. The capacitor determines how quickly the COMP pin charges to the desired level. The COMP pin has internal voltage clamps that limit the voltage level to a minimum of 0.8V and a maximum of 2.1V.

The oscillator and ramp generator create a ramped signal. The frequency of this signal can be 131.25kHz, 262.5kHz, 525kHz, or 1050kHz and is set by the PWM_FR[1:0] bits (Table 02h, Register 88h, Bits 5:4). The low level and high level for the ramped signal are approximately 1.0V and 1.9V, respectively.

The ramped signal is compared to the voltage level on the COMP pin to determine the duty cycle that is input to the gate driver and duty-cycle limiting block. When COMP is clamped low at 0.8V, below the level of the ramped signal, the comparator outputs a 0% duty-cycle signal to the gate driver block. When COMP is clamped at 2.1V, above the level of the ramped signal, the comparator outputs a 100% duty-cycle signal to the gate driver and duty-cycle limiting block. The duty-cycle liming block is used to limit the duty cycle of the PWM signal from the SW pin to 90%.

The PWM controller is designed to protect expensive APDs against adverse operating conditions while providing optimal bias. The PWM controller monitors photodiode current to protect APDs under avalanche conditions using the MON3 quick trip. A voltage level that is proportional to the APD current can be input to the MON3 pin. When this voltage exceeds the level set by the M3QT DAC (Table 02h, Register C3h), pulses from the PWM controller are blocked until the fault is cleared. The quick trip can also toggle the digital output D2. D2 can be connected to an external FET to quickly discharge the DC-DC converter filter capacitors.

Inductor Selection

Optimum inductor selection depends on input voltage, output voltage, maximum output current, switching frequency, and inductor size. Inductors are typically specified by their inductance (L), peak current (IPK), and resistance (LR).

The inductance value is given by:

$$L = \frac{V_{IN}^2 \times D^2 \times T \times \eta}{2I_{OUT(MAX)} \times V_{OUT}}$$

Where:

V_{IN} = DC-DC converter input voltage

V_{OUT} = Output of DC-DC converter

$I_{OUT(MAX)}$ = Maximum output current delivered

T = Time period of switching frequency (seconds)

D = Duty cycle

η = Estimated power conversion efficiency

The equation for inductance factors in conversion efficiency. For inductor calculation purposes, an η of 0.5 to 0.75 is usually suitable.

For example, to obtain an output of 80V with a load current of 1.0mA from an input voltage of 5.0V using the maximum 90% duty cycle and frequency of 1050kHz (T = 952ns), and assuming an efficiency of 0.5, the previous equation yields an L of 120µH, so a 100µH inductor would be a suitable value.

The peak inductor current is given by:

$$I_{PK} = \frac{V_{IN} \times D \times T}{L}$$

Stability and Compensation Component Selection

The components connected to the COMP pin (R_{COMP} and C_{COMP}) introduce a pole and zero that are necessary for stable operation of the PWM controller (Figure 12).

The dominant pole, POLE1, is formed by the output impedance of the error amplifier (R_{EA}) and C_{COMP}. The zero formed by the components on COMP, ZERO1, is selected to cancel POLE2 formed by the output filter cap C3 and output load R_{LOAD}. The additional pole, POLE3, formed by R1 and C3 should be at least a decade past the crossover frequency to not affect stability. The following formulas can be used to calculate the poles and zero for the application shown in Figure 12.

$$\text{POLE1 (dominant pole)} = 1/(2\pi \times R_{EA} \times C_{COMP})$$

$$\text{ZERO1 (compensation zero)} = 1/(2\pi \times R_{COMP} \times C_{COMP})$$

$$\text{POLE2 (output load pole)} = \frac{2 \times V_{OUT} - V_{IN}}{V_{OUT} - V_{IN}} \times \frac{1}{2\pi \times R_{LOAD} \times (C2 + C3)}$$

$$\text{POLE3 (output filter pole)} = 1/(2\pi \times R1 \times C3)$$

The DC open-loop gain is given by:

$$AOL = G_M \times R_{EA} \times \frac{V_{FB}}{0.85} \times \frac{2 \times V_{IN}}{2 \times V_{OUT} - V_{IN}} \times \sqrt{\left(\frac{V_{OUT} - V_{IN}}{V_{OUT}} \times \frac{R_{LOAD} \times T}{2 \times L}\right)}$$

Where:

R_{EA} = 260MΩ

G_M = 425µS

R_{LOAD} = Parallel combination of feedback network and load resistance

V_{OUT} = Output of DC-DC converter

V_{IN} = DC-DC converter input voltage

V_{FB} = Feedback voltage at the FB pin

T = Time period of switching frequency (seconds)

L = Inductor value (henries)

DAC1 Output

The DAC1 output has a full-scale 2.5V range with 8 bits of resolution, and is programmed through the I^2C interface. The DAC1 setting is nonvolatile and password-2 (PW2) protected.

M4DAC Output

The M4DAC output has a full-scale 2.5V range with 8 bits of resolution, and is controlled by an LUT indexed by the MON4 voltage. The M4DAC LUT (Table 06h) is nonvolatile and PW2 protected. See the *Memory Organization* section for details. The recalled value is either 16-bit or 32-bit depending on bits DBL_SB and UP_LOWB in Table 02h, Register C7h.

Digital I/O Pins

Five digital I/O pins are provided for additional monitoring and control. By default the LOSI pin is used to convert a standard comparator output for loss of signal (LOSI) to an open-collector output. This means the mux shown on the block diagram by default selects the LOSI pin as the source for the D0 output transistor. The level of the D0 pin can be read in the STATUS byte (Lower Memory, Register 6Eh) as the LOS STATUS bit. The LOS STATUS bit reports back the logic level of the D0 pin, so an external pullup resistor must be provided for this pin to output a high level. The LOSI signal can be inverted before driving the open-drain output transistor using the XOR gate provided. The MUX LOS allows the D0 pin to be used identically to the D1, D2, and D3 pins. However, the mux setting (stored in the EEPROM) does not take effect until $V_{CC} > V_{POA}$, allowing the EEPROM to recall. This requires the LOSI pin to be grounded for D0 to act identical to the D1, D2, and D3 pins.

Digital pins D1, D2, and D3 can be used as inputs or outputs. External pullup resistors must be provided to realize high-logic levels. The DIN byte indicates the logic levels of these input pins (Lower Memory, Register 79h), and the open-drain outputs can be controlled using the DOUT byte (Lower Memory, Register 78h). When $V_{CC} < V_{POA}$, these outputs are high impedance. Once $V_{CC} \geq V_{POA}$, the outputs go to the power-on default state stored in the DPU byte (Table 02h, Register C0h). The EEPROM-determined default state of the pin can be modified with PW2 access. After the default state has been recalled, the SRAM registers controlling outputs can be modified without password access. This allows the outputs to be used to control serial interfaces without wearing out the default EEPROM setting.

D2 can be configured as the output of a quick-trip monitor for MON3. The main application is to quickly shut down the PWM converter and discharge the voltage created by the converter. This is shown in the typical application circuit.

PON Triplexer and SFP Controller

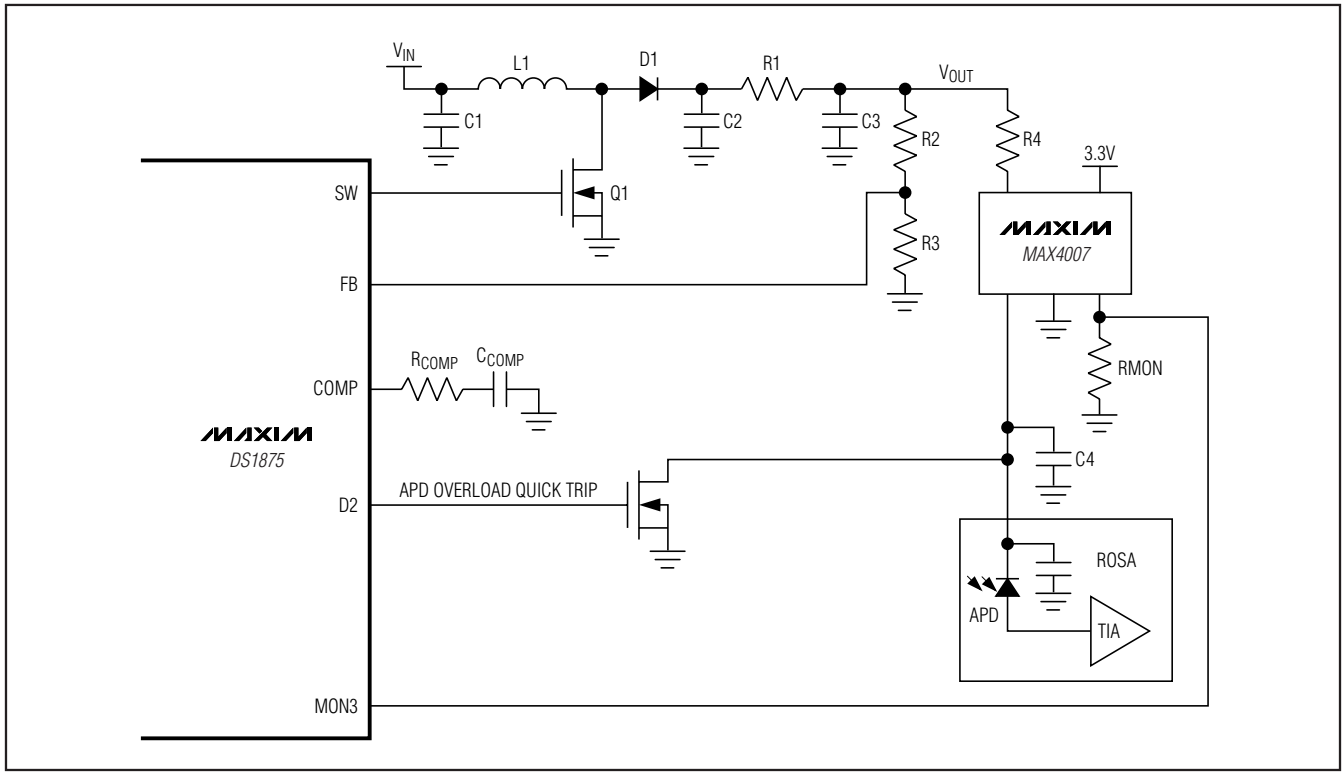


Figure 12. PWM Controller Typical APD Bias Circuit

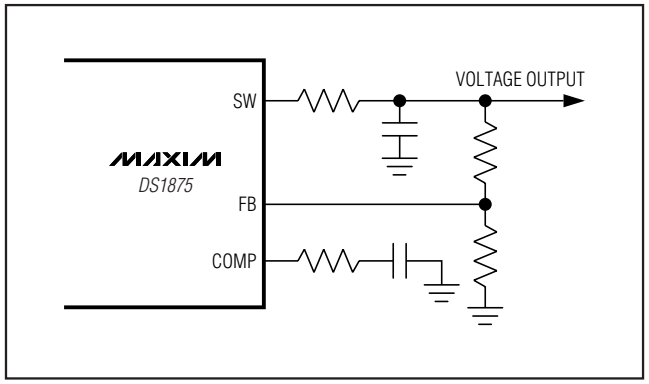


Figure 13. PWM Controller Voltage Output Configuration

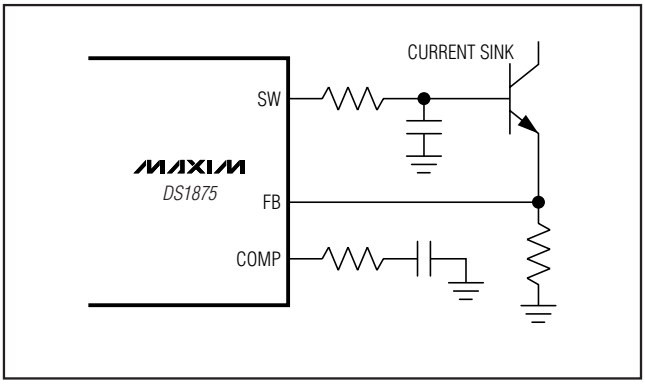


Figure 14. PWM Controller Current-Sink Output Configuration

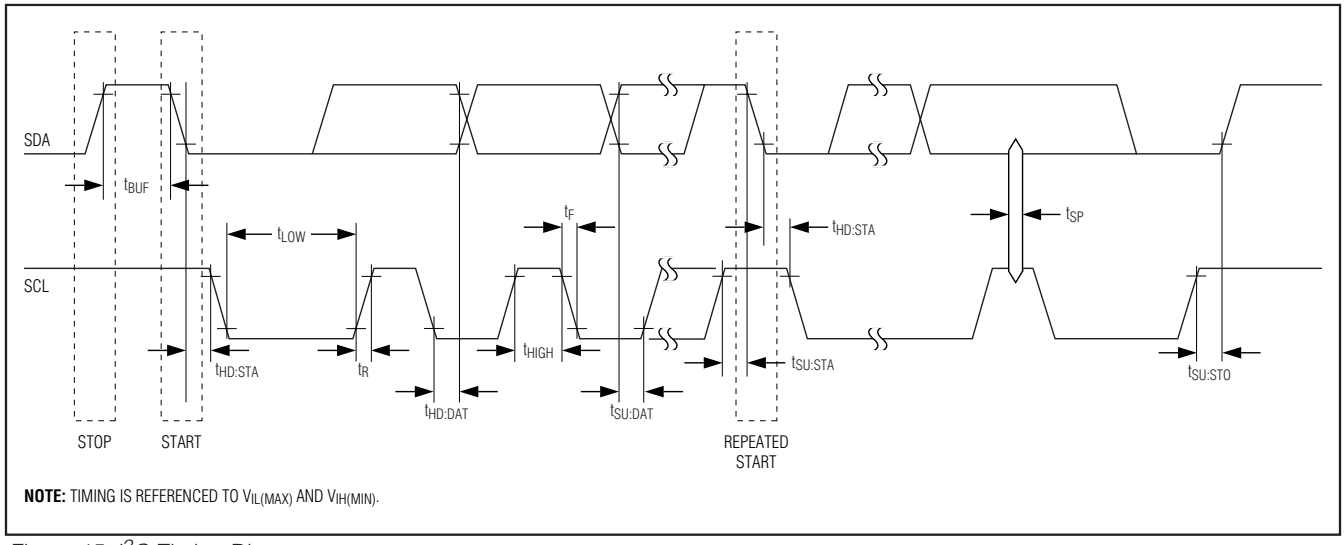


Figure 15. I²C Timing Diagram

I²C Communication

I²C Definitions

The following terminology is commonly used to describe I²C data transfers.

Master Device: The master device controls the slave devices on the bus. The master device generates SCL clock pulses and START and STOP conditions.

Slave Devices: Slave devices send and receive data at the master's request.

Bus Idle or Not Busy: Time between STOP and START conditions when both SDA and SCL are inactive and in their logic-high states.

START Condition: A START condition is generated by the master to initiate a new data transfer with a slave. Transitioning SDA from high to low while SCL remains high generates a START condition. See Figure 15 for applicable timing.

STOP Condition: A STOP condition is generated by the master to end a data transfer with a slave. Transitioning SDA from low to high while SCL remains high generates a STOP condition. See Figure 15 for applicable timing.

Repeated START Condition: The master can use a repeated START condition at the end of one data transfer to indicate that it will immediately initiate a new data transfer following the current one. Repeated START conditions are commonly used during read operations to identify a specific memory address to begin a data transfer. A repeated START condition is issued identically to a normal START condition. See Figure 15 for applicable timing.

Bit Write: Transitions of SDA must occur during the low state of SCL. The data on SDA must remain valid and unchanged during the entire high pulse of SCL plus the setup and hold-time requirements (Figure 15). Data is shifted into the device during the rising edge of the SCL.

Bit Read: At the end of a write operation, the master must release the SDA bus line for the proper amount of setup time before the next rising edge of SCL during a bit read (Figure 15). The device shifts out each bit of data on SDA at the falling edge of the previous SCL pulse and the data bit is valid at the rising edge of the current SCL pulse. Remember that the master generates all SCL clock pulses including when it is reading bits from the slave.

Acknowledgement (ACK and NACK): An acknowledge-ment (ACK) or not acknowledge (NACK) is always the 9th bit transmitted during a byte transfer. The device receiving data (the master during a read or the slave during a write operation) performs an ACK by transmitting a zero during the 9th bit. A device performs a NACK by transmitting a one during the 9th bit. Timing for the ACK and NACK is identical to all other bit writes (Figure 15). An ACK is the acknowledgment that the device is properly receiving data. A NACK is used to terminate a read sequence or as an indication that the device is not receiving data.

Byte Write: A byte write consists of 8 bits of information transferred from the master to the slave (most significant bit first) plus a 1-bit acknowledgement from the slave to the master. The 8 bits transmitted by the master are done according to the bit write definition and the acknowledgement is read using the bit read definition.

Byte Read: A byte read is an 8-bit information transfer from the slave to the master plus a 1-bit ACK or NACK from the master to the slave. The 8 bits of information that are transferred (most significant bit first) from the slave to the master are read by the master using the bit read definition, and the master transmits an ACK using the bit write definition to receive additional data bytes. The master must NACK the last byte read to terminate communication so the slave returns control of SDA to the master.

Slave Address Byte: Each slave on the I²C bus responds to a slave addressing byte sent immediately following a START condition. The slave address byte contains the slave address in the most significant 7 bits and the R/$\overline{W}$ bit in the least significant bit.

The DS1875 responds to two slave addresses. The auxiliary memory always responds to a fixed I²C slave address, A0h. The Lower Memory and tables 00h–08h respond to I²C slave addresses that can be configured to any value between 00h–FEh using the Device Address byte (Table 02h, Register 8Ch). The user also must set the ASEL bit (Table 02h, Register 89h) for this address to be active. By writing the correct slave address with R/$\overline{W}$ = 0, the master indicates it will write data to the slave. If R/$\overline{W}$ = 1, the master reads data from the slave. If an incorrect slave address is written, the DS1875 assumes the master is communicating with another I²C device and ignores the communications until the next START condition is sent. If the main device's slave address is programmed to be A0h, access to the auxiliary memory is disabled.

Memory Address: During an I²C write operation to the DS1875, the master must transmit a memory address to identify the memory location where the slave is to store the data. The memory address is always the second byte transmitted during a write operation following the slave address byte.

I²C Protocol

Writing a Single Byte to a Slave: The master must generate a START condition, write the slave address byte (R/W = 0), write the memory address, write the byte of data, and generate a STOP condition. The master must read the slave's acknowledgement during all byte write operations.

Writing Multiple Bytes to a Slave: To write multiple bytes to a slave, the master generates a START condition, writes the slave address byte (R/$\overline{W}$ = 0), writes the memory address, writes up to 8 data bytes, and generates a STOP condition. The DS1875 writes 1 to 8 bytes (one page or row) with a single write transaction. This is internally controlled by an address counter that allows data to be written to consecutive addresses without transmitting a memory address before each data byte is sent. The address counter limits the write to one 8-byte page (one row of the memory map). Attempts to write to additional pages of memory without sending a STOP condition between pages result in the address counter wrapping around to the beginning of the present row.

Example: A 3-byte write starts at address 06h and writes three data bytes (11h, 22h, and 33h) to three "consecutive" addresses. The result is that addresses 06h and 07h contain 11h and 22h, respectively, and the third data byte, 33h, is written to address 00h.

To prevent address wrapping from occurring, the master must send a STOP condition at the end of the page, then wait for the bus-free or EEPROM write time to elapse. Then the master can generate a new START condition and write the slave address byte (R/$\overline{W}$ = 0) and the first memory address of the next memory row before continuing to write data.

Acknowledge Polling: Any time a EEPROM location is written, the DS1875 requires the EEPROM write time (t_W) after the STOP condition to write the contents of the page to EEPROM. During the EEPROM write time, the device does not acknowledge its slave address because it is busy. It is possible to take advantage of that phenomenon by repeatedly addressing the DS1875, which allows the next page to be written as soon as the DS1875 is ready to receive the data. The alternative to acknowledge polling is to wait for a maximum period of t_W to elapse before attempting to write again to the DS1875.

EEPROM Write Cycles: When EEPROM writes occur to the memory, the DS1875 writes the whole EEPROM memory page, even if only a single byte on the page was modified. Writes that do not modify all 8 bytes on the page are allowed and do not corrupt the remaining bytes of memory on the same page. Because the whole page is written, bytes that

were not modified during the transaction are still subject to a write cycle. This can result in a whole page being worn out over time by writing a single byte repeatedly. Writing a page one byte at a time wears the EEPROM out eight times faster than writing the entire page at once. The DS1875's EEPROM write cycles are specified in the *Nonvolatile Memory Characteristics* table. The specification shown is at the worst-case temperature. It can handle approximately 10 times that many writes at room temperature. Writing to SRAM-shadowed EEPROM memory with SEEB = 1 does not count as a EEPROM write cycle when evaluating the EEPROM's estimated lifetime.

Reading a Single Byte from a Slave: Unlike the write operation that uses the memory address byte to define where the data is to be written, the read operation occurs at the present value of the memory address counter. To read a single byte from the slave, the master generates a START condition, writes the slave address byte with R/$\overline{W}$ = 1, reads the data byte with a NACK to indicate the end of the transfer, and generates a STOP condition.

Manipulating the Address Counter for Reads: A dummy write cycle can be used to force the address pointer to a particular value. To do this, the master generates a START condition, writes the slave address byte (R/$\overline{W}$ = 0), writes the memory address where it desires to read, generates a repeated START condition, writes the slave address byte (R/$\overline{W}$ = 1), reads data with ACK or NACK as applicable, and generates a STOP condition.

Memory Map

Memory Organization

The DS1875 features 10 separate memory tables that are internally organized into 8-byte rows.

The **Lower Memory** is addressed from 00h to 7Fh and contains alarm and warning thresholds, flags, masks, several control registers, password entry area (PWE), and the table select byte.

Table 00h contains conversion results for MON5 through MON8.

Table 01h primarily contains user EEPROM (with PW1 level access) as well as some alarm and warning status bytes.

Table 02h is a multifunction space that contains configuration registers, scaling and offset values, passwords, interrupt registers, as well as other miscellaneous control bytes.

Table 03h is strictly user EEPROM that is protected by a PW2-level password.

Table 04h contains a temperature-indexed LUT for control of the modulation voltage. The modulation LUT can be programmed in 2°C increments over the -40°C to +102°C range. Access to this register is protected by a PW2-level password.

Table 05h contains a temperature-indexed LUT that allows the APC set point to change as a function of temperature to compensate for Tracking Error (TE). The APC LUT has 36 entries that determine the APC setting in 4°C windows between -40°C to 100°C. Access to this register is protected by a PW2-level password.

Table 06h contains a MON4-indexed LUT for control of the M4DAC voltage. The MON4 LUT has 32 entries that are configurable to act as one 32-entry LUT of two 16-byte LUTs. When configured as one 32-byte LUT, each entry corresponds to an increment of 1/32 the full scale. When configured as two 16-byte LUTs, the first 16 bytes and the last 16 bytes each correspond to 1/16 full scale. Either of the two sections is selected with a separate configuration bit. Access to this register is protected by a PW2-level password.

Table 07h contains a temperature-indexed LUT for control of the PWM reference voltage (integration of FB input). The PWM LUT has 36 entries that determine the APC setting in 4°C windows between -40°C to +100°C. Access to this register is protected by a PW2-level password.

Table 08h contains a temperature-indexed LUT for control of the BIAS current. The BIAS LUT can be programmed in 2°C increments over the 40°C to +102°C range. Access to this register is protected by a PW2-level password.

Auxiliary Memory (Device A0h) contains 256 bytes of EE memory accessible from address 00h–FFh. It is selected with the device address of A0h.

See the *Register Descriptions* section for a more complete detail of each byte's function, as well as for read/write permissions for each byte.

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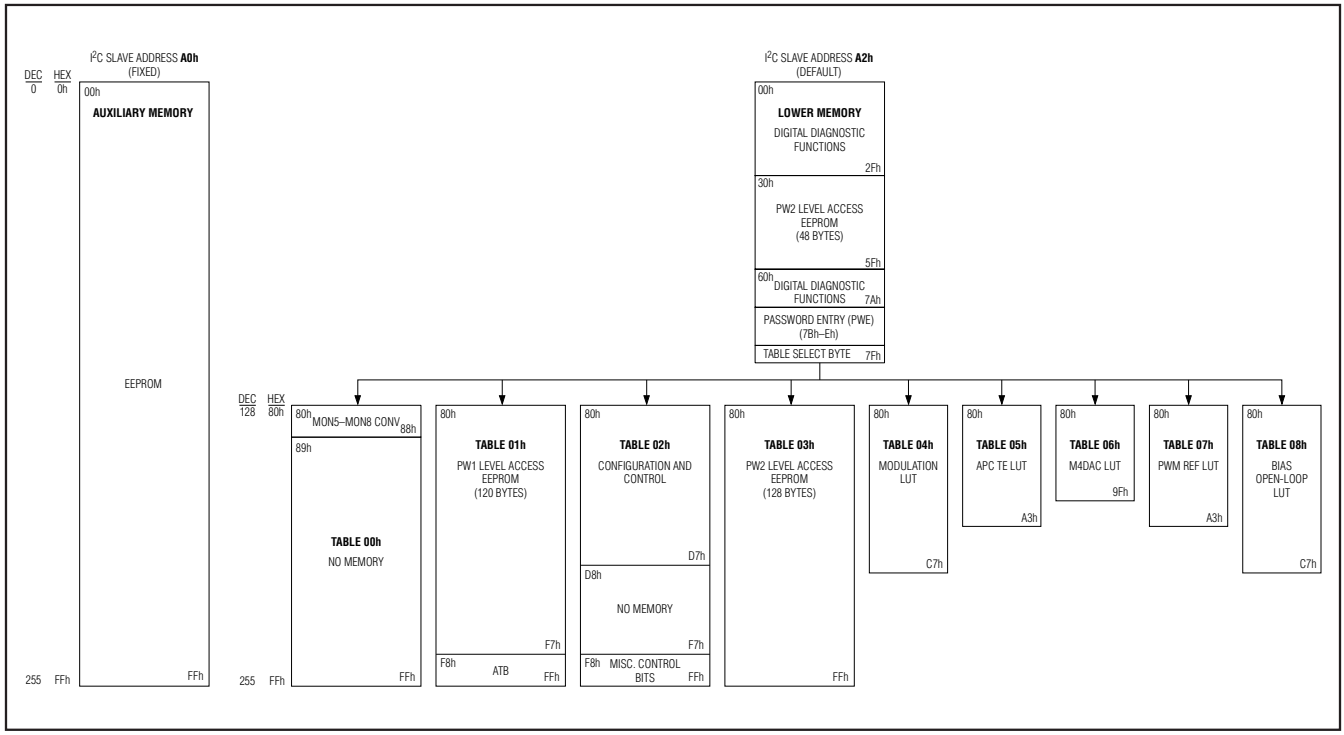


Figure 16. Memory Map

Shadowed EEPROM

Many NV memory locations (listed within the *Register Descriptions* section) are actually shadowed EEPROM that are controlled by the SEEB bit in Table 02h, Byte 80h.

The DS1875 incorporates shadowed-EEPROM memory locations for key memory addresses that can be written many times. By default the shadowed-EEPROM bit, SEEB, is not set and these locations act as ordinary EEPROM. By setting SEEB, these locations function like SRAM cells, which allow an infinite number of write cycles without concern of wearing out the EEPROM. This also eliminates the requirement for the EEPROM write time, t_{WR}. Because changes made with SEEB disabled do not affect the EEPROM, these changes are not retained through power cycles. The power-on value is the last value written with SEEB enabled. This function can be used to limit the number of EEPROM writes during calibration or to change the monitor thresholds periodically during normal operation helping to reduce the number of times EEPROM is written. The *Memory Map* description indicates which locations are shadowed EEPROM.

Register Descriptions

Lower Memory Register Map

This register map shows each byte/word (2 bytes) in terms of the row it is on in the memory. The first byte in the row is located in memory at the row address (hexadecimal) in the leftmost column. Each subsequent byte on the row is one/two memory locations beyond the previous byte/word's address. A total of 8 bytes are present on each row. For more information about each of these bytes, see the corresponding register description.

LOWER MEMORY									
ROW (HEX)	ROW NAME	WORD 0		WORD 1		WORD 2		WORD 3	
		BYTE 0/8	BYTE 1/9	BYTE 2/A	BYTE 3/B	BYTE 4/C	BYTE 5/D	BYTE 6/E	BYTE 7/F
00	<1>THRESHOLD$_0$	TEMP ALARM HI		TEMP ALARM LO		TEMP WARN HI		TEMP WARN LO	
08	<1>THRESHOLD$_1$	V_{CC} ALARM HI		V_{CC} ALARM LO		V_{CC} WARN HI		V_{CC} WARN LO	
10	<1>THRESHOLD$_2$	MON1 ALARM HI		MON1 ALARM LO		MON1 WARN HI		MON1 WARN LO	
18	<1>THRESHOLD$_3$	MON2 ALARM HI		MON2 ALARM LO		MON2 WARN HI		MON2 WARN LO	
20	<1>THRESHOLD$_4$	MON3 ALARM HI		MON3 ALARM LO		MON3 WARN HI		MON3 WARN LO	
28	<1>THRESHOLD$_5$	MON4 ALARM HI		MON4 ALARM LO		MON4 WARN HI		MON4 WARN LO	
30	<1>PW2 EE	EE	EE	EE	EE	EE	EE	EE	EE
38	<1>PW2 EE	EE	EE	EE	EE	EE	EE	EE	EE
40	<1>PW2 EE	EE	EE	EE	EE	EE	EE	EE	EE
48	<1>PW2 EE	EE	EE	EE	EE	EE	EE	EE	EE
50	<1>PW2 EE	EE	EE	EE	EE	EE	EE	EE	EE
58	<1>PW2 EE	EE	EE	EE	EE	EE	EE	EE	EE
60	<2>ADC VALUES$_0$	TEMP VALUE		V_{CC} VALUE		MON1 VALUE		MON2 VALUE	
68	<0>ADC VALUES$_1$	<2>MON3 VALUE		<2>MON4 VALUE		<2>RESERVED		<0>STATUS	<3>UPDATE
70	<2>ALARM/ WARN	ALARM$_3$	ALARM$_2$	ALARM$_1$	ALARM$_0$	WARN$_3$	WARN$_2$	RESERVED	RESERVED
78	<0>TABLE SELECT	<5>DOUT	<2>DIN	<6> RESERVED	<6>PWE MSB		<6>PWE LSB		<5>TBL SEL

ACCESS CODE	<0>	<1>	<2>	<3>	<4>	<5>	<6>	<7>	<8>	<9>	<10>	<11>
Read Access	See each bit/byte separately	All	All	All	PW2	All	N/A	PW1	PW2	N/A	PW2	All
Write Access		PW2	N/A	All and DS1875 hardware	PW2 + mode bit	All	All	PW1	PW2	PW2	N/A	PW1

Table 00h Register Map

TABLE 00h									
ROW (HEX)	ROW NAME	WORD 0		WORD 1		WORD 2		WORD 3	
		BYTE 0/8	BYTE 1/9	BYTE 2/A	BYTE 3/B	BYTE 4/C	BYTE 5/D	BYTE 6/E	BYTE 7/F
80	ADC VALUES	MON5 VALUE		MON6 VALUE		MON7 VALUE		MON8 VALUE	
88–FF	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY

ACCESS CODE	<0>	<1>	<2>	<3>	<4>	<5>	<6>	<7>	<8>	<9>	<10>	<11>
Read Access	See each bit/byte separately	All	All	All	PW2	All	N/A	PW1	PW2	N/A	PW2	All
Write Access		PW2	N/A	All and DS1875 hardware	PW2 + mode bit	All	All	PW1	PW2	PW2	N/A	PW1

Table 01h Register Map

TABLE 01h (PW1)									
ROW (HEX)	ROW NAME	WORD 0		WORD 1		WORD 2		WORD 3	
		BYTE 0/8	BYTE 1/9	BYTE 2/A	BYTE 3/B	BYTE 4/C	BYTE 5/D	BYTE 6/E	BYTE 7/F
80	<7>PW1 EE	EE	EE	EE	EE	EE	EE	EE	EE
88	<7>PW1 EE	EE	EE	EE	EE	EE	EE	EE	EE
90	<7>PW1 EE	EE	EE	EE	EE	EE	EE	EE	EE
98	<7>PW1 EE	EE	EE	EE	EE	EE	EE	EE	EE
A0	<7>PW1 EE	EE	EE	EE	EE	EE	EE	EE	EE
A8	<7>PW1 EE	EE	EE	EE	EE	EE	EE	EE	EE
B0	<7>PW1 EE	EE	EE	EE	EE	EE	EE	EE	EE
B8	<7>PW1 EE	EE	EE	EE	EE	EE	EE	EE	EE
C0	<7>PW1 EE	EE	EE	EE	EE	EE	EE	EE	EE
C8	<7>PW1 EE	EE	EE	EE	EE	EE	EE	EE	EE
D0	<7>PW1 EE	EE	EE	EE	EE	EE	EE	EE	EE
D8	<7>PW1 EE	EE	EE	EE	EE	EE	EE	EE	EE
E0	<7>PW1 EE	EE	EE	EE	EE	EE	EE	EE	EE
E8	<7>PW1 EE	EE	EE	EE	EE	EE	EE	EE	EE
F0	<7>PW1 EE	EE	EE	EE	EE	EE	EE	EE	EE
F8	<11>ALARM TRAP	$ALARM_3$	$ALARM_2$	$ALARM_1$	$ALARM_0$	$WARN_3$	$WARN_2$	RESERVED	RESERVED

ACCESS CODE	<0>	<1>	<2>	<3>	<4>	<5>	<6>	<7>	<8>	<9>	<10>	<11>
Read Access	See each bit/byte separately	All	All	All	PW2	All	N/A	PW1	PW2	N/A	PW2	All
Write Access		PW2	N/A	All and DS1875 hardware	PW2 + mode bit	All	All	PW1	PW2	PW2	N/A	PW1

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Table 02h Register Map

TABLE 02h (PW2)									
ROW (HEX)	ROW NAME	WORD 0		WORD 1		WORD 2		WORD 3	
		BYTE 0/8	BYTE 1/9	BYTE 2/A	BYTE 3/B	BYTE 4/C	BYTE 5/D	BYTE 6/E	BYTE 7/F
80	<0>CONFIG$_0$	<8>MODE	<4>TINDEX	<4>MOD DAC	<4>APC DAC	<4>VINDEX	<4>M4DAC	<10>DEVICE ID	<10>DEVICE VER
88	<8>CONFIG$_1$	SAMPLE RATE	CONFIG	RESERVED	MOD RANGING	DEVICE ADDRESS	COMP RANGING	RSHIFT$_1$	RSHIFT$_0$
90	<8>SCALE$_0$	RESERVED		V_{CC} SCALE		MON1 SCALE		MON2 SCALE	
98	<8>SCALE$_1$	MON3 FINE SCALE		MON4 SCALE		MON3 COARSE SCALE		RESERVED	
A0	<8>OFFSET$_0$	RESERVED		V_{CC} OFFSET		MON1 OFFSET		MON2 OFFSET	
A8	<8>OFFSET$_1$	MON3 FINE OFFSET		MON4 OFFSET		MON3 COARSE OFFSET		INTERNAL TEMP OFFSET*	
B0	<9>PWD VALUE	PW1 MSW		PW1 LSW		PW2 MSW		PW2 LSW	
B8	<8>INTERRUPT	FETG ENABLE$_1$	FETG ENABLE$_0$	TX-F ENABLE$_1$	TX-F ENABLE$_0$	HTXP	LTXP	HBIAS	MAX BIAS
C0	<8>CNTL OUT	DPU	RESERVED	RESERVED	M3QT DAC	DAC1	RESERVED	RESERVED	M4 LUT CNTL
C8	<8>SCALE$_2$	MON5 SCALE		MON6 SCALE		MON7 SCALE		MON8 SCALE	
D0	<8>OFFSET$_1$	MON5 OFFSET		MON6 OFFSET		MON7 OFFSET		MON8 OFFSET	
D8–F7	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY
F8	<0>MAN BIAS	<4>MAN BIAS$_1$	<4>MAN BIAS$_0$	<4>MAN_ CNTL	<10>BIAS DAC$_1$	<10>BIAS DAC$_0$	BIAS OL	PWM DAC	RESERVED

**The final result must be XORed with BB40h before writing to this register.*

ACCESS CODE	<0>	<1>	<2>	<3>	<4>	<5>	<6>	<7>	<8>	<9>	<10>	<11>
Read Access	See each bit/byte separately	All	All	All	PW2	All	N/A	PW1	PW2	N/A	PW2	All
Write Access		PW2	N/A	All and DS1875 hardware	PW2 + mode bit	All	All	PW1	PW2	PW2	N/A	PW1

Table 03h Register Map

TABLE 03h (PW2)									
ROW (HEX)	ROW NAME	WORD 0		WORD 1		WORD 2		WORD 3	
		BYTE 0/8	BYTE 1/9	BYTE 2/A	BYTE 3/B	BYTE 4/C	BYTE 5/D	BYTE 6/E	BYTE 7/F
80	<8>PW2 EE	EE	EE	EE	EE	EE	EE	EE	EE
88	<8>PW2 EE	EE	EE	EE	EE	EE	EE	EE	EE
90	<8>PW2 EE	EE	EE	EE	EE	EE	EE	EE	EE
98	<8>PW2 EE	EE	EE	EE	EE	EE	EE	EE	EE
A0	<8>PW2 EE	EE	EE	EE	EE	EE	EE	EE	EE
A8	<8>PW2 EE	EE	EE	EE	EE	EE	EE	EE	EE
B0	<8>PW2 EE	EE	EE	EE	EE	EE	EE	EE	EE
B8	<8>PW2 EE	EE	EE	EE	EE	EE	EE	EE	EE
C0	<8>PW2 EE	EE	EE	EE	EE	EE	EE	EE	EE
C8	<8>PW2 EE	EE	EE	EE	EE	EE	EE	EE	EE
D0	<8>PW2 EE	EE	EE	EE	EE	EE	EE	EE	EE
D8	<8>PW2 EE	EE	EE	EE	EE	EE	EE	EE	EE
E0	<8>PW2 EE	EE	EE	EE	EE	EE	EE	EE	EE
E8	<8>PW2 EE	EE	EE	EE	EE	EE	EE	EE	EE
F0	<8>PW2 EE	EE	EE	EE	EE	EE	EE	EE	EE
F8	<8>PW2 EE	EE	EE	EE	EE	EE	EE	EE	EE

ACCESS CODE	<0>	<1>	<2>	<3>	<4>	<5>	<6>	<7>	<8>	<9>	<10>	<11>
Read Access	See each bit/byte separately	All	All	All	PW2	All	N/A	PW1	PW2	N/A	PW2	All
Write Access		PW2	N/A	All and DS1875 hardware	PW2 + mode bit	All	All	PW1	PW2	PW2	N/A	PW1

Table 04h Register Map

TABLE 04h (MODULATION LUT)									
ROW (HEX)	ROW NAME	WORD 0		WORD 1		WORD 2		WORD 3	
		BYTE 0/8	BYTE 1/9	BYTE 2/A	BYTE 3/B	BYTE 4/C	BYTE 5/D	BYTE 6/E	BYTE 7/F
80	<8>LUT4	MOD	MOD	MOD	MOD	MOD	MOD	MOD	MOD
88	<8>LUT4	MOD	MOD	MOD	MOD	MOD	MOD	MOD	MOD
90	<8>LUT4	MOD	MOD	MOD	MOD	MOD	MOD	MOD	MOD
98	<8>LUT4	MOD	MOD	MOD	MOD	MOD	MOD	MOD	MOD
A0	<8>LUT4	MOD	MOD	MOD	MOD	MOD	MOD	MOD	MOD
A8	<8>LUT4	MOD	MOD	MOD	MOD	MOD	MOD	MOD	MOD
B0	<8>LUT4	MOD	MOD	MOD	MOD	MOD	MOD	MOD	MOD
B8	<8>LUT4	MOD	MOD	MOD	MOD	MOD	MOD	MOD	MOD
C0	<8>LUT4	MOD	MOD	MOD	MOD	MOD	MOD	MOD	MOD

ACCESS CODE	<0>	<1>	<2>	<3>	<4>	<5>	<6>	<7>	<8>	<9>	<10>	<11>
Read Access	See each bit/byte separately	All	All	All	PW2	All	N/A	PW1	PW2	N/A	PW2	All
Write Access		PW2	N/A	All and DS1875 hardware	PW2 + mode bit	All	All	PW1	PW2	PW2	N/A	PW1

Table 05h Register Map

TABLE 05h (APC TE LUT)									
ROW (HEX)	ROW NAME	WORD 0		WORD 1		WORD 2		WORD 3	
		BYTE 0/8	BYTE 1/9	BYTE 2/A	BYTE 3/B	BYTE 4/C	BYTE 5/D	BYTE 6/E	BYTE 7/F
80	<8>LUT5	APC REF	APC REF	APC REF	APC REF	APC REF	APC REF	APC REF	APC REF
88	<8>LUT5	APC REF	APC REF	APC REF	APC REF	APC REF	APC REF	APC REF	APC REF
90	<8>LUT5	APC REF	APC REF	APC REF	APC REF	APC REF	APC REF	APC REF	APC REF
98	<8>LUT5	APC REF	APC REF	APC REF	APC REF	APC REF	APC REF	APC REF	APC REF
A0	<8>LUT5	APC REF	APC REF	APC REF	APC REF	RESERVED	RESERVED	RESERVED	RESERVED

ACCESS CODE	<0>	<1>	<2>	<3>	<4>	<5>	<6>	<7>	<8>	<9>	<10>	<11>
Read Access	See each bit/byte separately	All	All	All	PW2	All	N/A	PW1	PW2	N/A	PW2	All
Write Access		PW2	N/A	All and DS1875 hardware	PW2 + mode bit	All	All	PW1	PW2	PW2	N/A	PW1

Table 06h Register Map

TABLE 06h (M4DAC LUT)									
ROW (HEX)	ROW NAME	WORD 0		WORD 1		WORD 2		WORD 3	
		BYTE 0/8	BYTE 1/9	BYTE 2/A	BYTE 3/B	BYTE 4/C	BYTE 5/D	BYTE 6/E	BYTE 7/F
80	<8>LUT6	M4DAC	M4DAC	M4DAC	M4DAC	M4DAC	M4DAC	M4DAC	M4DAC
88	<8>LUT6	M4DAC	M4DAC	M4DAC	M4DAC	M4DAC	M4DAC	M4DAC	M4DAC
90	<8>LUT6	M4DAC	M4DAC	M4DAC	M4DAC	M4DAC	M4DAC	M4DAC	M4DAC
98	<8>LUT6	M4DAC	M4DAC	M4DAC	M4DAC	M4DAC	M4DAC	M4DAC	M4DAC

ACCESS CODE	<0>	<1>	<2>	<3>	<4>	<5>	<6>	<7>	<8>	<9>	<10>	<11>
Read Access	See each bit/byte separately	All	All	All	PW2	All	N/A	PW1	PW2	N/A	PW2	All
Write Access		PW2	N/A	All and DS1875 hardware	PW2 + mode bit	All	All	PW1	PW2	PW2	N/A	PW1

Table 07h Register Map

TABLE 07h (PWM REFERENCE LUT)									
ROW (HEX)	ROW NAME	WORD 0		WORD 1		WORD 2		WORD 3	
		BYTE 0/8	BYTE 1/9	BYTE 2/A	BYTE 3/B	BYTE 4/C	BYTE 5/D	BYTE 6/E	BYTE 7/F
80	<8>LUT7	PWM REF	PWM REF	PWM REF	PWM REF	PWM REF	PWM REF	PWM REF	PWM REF
88	<8>LUT7	PWM REF	PWM REF	PWM REF	PWM REF	PWM REF	PWM REF	PWM REF	PWM REF
90	<8>LUT7	PWM REF	PWM REF	PWM REF	PWM REF	PWM REF	PWM REF	PWM REF	PWM REF
98	<8>LUT7	PWM REF	PWM REF	PWM REF	PWM REF	PWM REF	PWM REF	PWM REF	PWM REF
A0	<8>LUT7	PWM REF	PWM REF	PWM REF	PWM REF	RESERVED	RESERVED	RESERVED	RESERVED

ACCESS CODE	<0>	<1>	<2>	<3>	<4>	<5>	<6>	<7>	<8>	<9>	<10>	<11>
Read Access	See each bit/byte separately	All	All	All	PW2	All	N/A	PW1	PW2	N/A	PW2	All
Write Access		PW2	N/A	All and DS1875 hardware	PW2 + mode bit	All	All	PW1	PW2	PW2	N/A	PW1

Table 08h Register Map

TABLE 08h (BIAS OPEN-LOOP LUT)									
ROW (HEX)	ROW NAME	WORD 0		WORD 1		WORD 2		WORD 3	
		BYTE 0/8	BYTE 1/9	BYTE 2/A	BYTE 3/B	BYTE 4/C	BYTE 5/D	BYTE 6/E	BYTE 7/F
80	<8>LUT8	BIAS_OL	BIAS_OL	BIAS_OL	BIAS_OL	BIAS_OL	BIAS_OL	BIAS_OL	BIAS_OL
88	<8>LUT8	BIAS_OL	BIAS_OL	BIAS_OL	BIAS_OL	BIAS_OL	BIAS_OL	BIAS_OL	BIAS_OL
90	<8>LUT8	BIAS_OL	BIAS_OL	BIAS_OL	BIAS_OL	BIAS_OL	BIAS_OL	BIAS_OL	BIAS_OL
98	<8>LUT8	BIAS_OL	BIAS_OL	BIAS_OL	BIAS_OL	BIAS_OL	BIAS_OL	BIAS_OL	BIAS_OL
A0	<8>LUT8	BIAS_OL	BIAS_OL	BIAS_OL	BIAS_OL	BIAS_OL	BIAS_OL	BIAS_OL	BIAS_OL
A8	<8>LUT8	BIAS_OL	BIAS_OL	BIAS_OL	BIAS_OL	BIAS_OL	BIAS_OL	BIAS_OL	BIAS_OL
B0	<8>LUT8	BIAS_OL	BIAS_OL	BIAS_OL	BIAS_OL	BIAS_OL	BIAS_OL	BIAS_OL	BIAS_OL
B8	<8>LUT8	BIAS_OL	BIAS_OL	BIAS_OL	BIAS_OL	BIAS_OL	BIAS_OL	BIAS_OL	BIAS_OL
C0	<8>LUT8	BIAS_OL	BIAS_OL	BIAS_OL	BIAS_OL	BIAS_OL	BIAS_OL	BIAS_OL	BIAS_OL

ACCESS CODE	<0>	<1>	<2>	<3>	<4>	<5>	<6>	<7>	<8>	<9>	<10>	<11>
Read Access	See each bit/byte separately	All	All	All	PW2	All	N/A	PW1	PW2	N/A	PW2	All
Write Access		PW2	N/A	All and DS1875 hardware	PW2 + mode bit	All	All	PW1	PW2	PW2	N/A	PW1

Auxiliary A0h Memory Register Map

AUXILIARY MEMORY (A0h)									
ROW (HEX)	ROW NAME	WORD 0		WORD 1		WORD 2		WORD 3	
		BYTE 0/8	BYTE 1/9	BYTE 2/A	BYTE 3/B	BYTE 4/C	BYTE 5/D	BYTE 6/E	BYTE 7/F
00	<5>AUX EE	EE	EE	EE	EE	EE	EE	EE	EE
08	<5>AUX EE	EE	EE	EE	EE	EE	EE	EE	EE
10	<5>AUX EE	EE	EE	EE	EE	EE	EE	EE	EE
18	<5>AUX EE	EE	EE	EE	EE	EE	EE	EE	EE
20	<5>AUX EE	EE	EE	EE	EE	EE	EE	EE	EE
28	<5>AUX EE	EE	EE	EE	EE	EE	EE	EE	EE
30	<5>AUX EE	EE	EE	EE	EE	EE	EE	EE	EE
38	<5>AUX EE	EE	EE	EE	EE	EE	EE	EE	EE
40	<5>AUX EE	EE	EE	EE	EE	EE	EE	EE	EE
48	<5>AUX EE	EE	EE	EE	EE	EE	EE	EE	EE
50	<5>AUX EE	EE	EE	EE	EE	EE	EE	EE	EE
58	<5>AUX EE	EE	EE	EE	EE	EE	EE	EE	EE
60	<5>AUX EE	EE	EE	EE	EE	EE	EE	EE	EE
68	<5>AUX EE	EE	EE	EE	EE	EE	EE	EE	EE
70	<5>AUX EE	EE	EE	EE	EE	EE	EE	EE	EE
78	<5>AUX EE	EE	EE	EE	EE	EE	EE	EE	EE
80	<5>AUX EE	EE	EE	EE	EE	EE	EE	EE	EE
88	<5>AUX EE	EE	EE	EE	EE	EE	EE	EE	EE
90	<5>AUX EE	EE	EE	EE	EE	EE	EE	EE	EE
98	<5>AUX EE	EE	EE	EE	EE	EE	EE	EE	EE
A0	<5>AUX EE	EE	EE	EE	EE	EE	EE	EE	EE
A8	<5>AUX EE	EE	EE	EE	EE	EE	EE	EE	EE
B0	<5>AUX EE	EE	EE	EE	EE	EE	EE	EE	EE
B8	<5>AUX EE	EE	EE	EE	EE	EE	EE	EE	EE
C0	<5>AUX EE	EE	EE	EE	EE	EE	EE	EE	EE
C8	<5>AUX EE	EE	EE	EE	EE	EE	EE	EE	EE
D0	<5>AUX EE	EE	EE	EE	EE	EE	EE	EE	EE
D8	<5>AUX EE	EE	EE	EE	EE	EE	EE	EE	EE
E0	<5>AUX EE	EE	EE	EE	EE	EE	EE	EE	EE
E8	<5>AUX EE	EE	EE	EE	EE	EE	EE	EE	EE
F0	<5>AUX EE	EE	EE	EE	EE	EE	EE	EE	EE
F8	<5>AUX EE	EE	EE	EE	EE	EE	EE	EE	EE

ACCESS CODE	<0>	<1>	<2>	<3>	<4>	<5>	<6>	<7>	<8>	<9>	<10>	<11>
Read Access	See each bit/byte separately	All	All	All	PW2	All	N/A	PW1	PW2	N/A	PW2	All
Write Access		PW2	N/A	All and DS1875 hardware	PW2 + mode bit	All	All	PW1	PW2	PW2	N/A	PW1

Lower Memory Register Descriptions

Lower Memory, Register 00h to 01h: TEMP ALARM HI
Lower Memory, Register 04h to 05h: TEMP WARN HI

FACTORY DEFAULT	7FFFh
READ ACCESS	All
WRITE ACCESS	PW2
MEMORY TYPE	Nonvolatile (SEE)

00h, 04h	S	2^6	2^5	2^4	2^3	2^2	2^1	2^0
01h, 05h	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}
	BIT 7							BIT 0

Temperature measurement updates above this two's complement threshold set its corresponding alarm or warning bit. Temperature measurement updates equal to or below this threshold clear its alarm or warning bit.

Lower Memory, Register 02h to 03h: TEMP ALARM LO
Lower Memory, Register 06h to 07h: TEMP WARN LO

FACTORY DEFAULT	8000h
READ ACCESS	All
WRITE ACCESS	PW2
MEMORY TYPE	Nonvolatile (SEE)

02h, 06h	S	2^6	2^5	2^4	2^3	2^2	2^1	2^0
03h, 07h	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}
	BIT 7							BIT 0

Temperature measurement updates below this two's complement threshold set its corresponding alarm or warning bit. Temperature measurement updates equal to or above this threshold clear its alarm or warning bit.

Lower Memory, Register 08h to 09h: V_{CC} ALARM HI
Lower Memory, Register 0Ch to 0Dh: V_{CC} WARN HI
Lower Memory, Register 10h to 11h: MON1 ALARM HI
Lower Memory, Register 14h to 15h: MON1 WARN HI
Lower Memory, Register 18h to 19h: MON2 ALARM HI
Lower Memory, Register 1Ch to 1Dh: MON2 WARN HI
Lower Memory, Register 20h to 21h: MON3 ALARM HI
Lower Memory, Register 24h to 25h: MON3 WARN HI
Lower Memory, Register 28h to 29h: MON4 ALARM HI
Lower Memory, Register 2Ch to 2Dh: MON4 WARN HI

FACTORY DEFAULT	FFFFh
READ ACCESS	All
WRITE ACCESS	PW2
MEMORY TYPE	Nonvolatile (SEE)

	BIT 7							BIT 0
08h, 0Ch, 10h, 14h, 18h, 1Ch, 20h, 24h, 28h, 2Ch	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}
09h, 0Dh, 11h, 15h, 19h, 1Dh, 21h, 25h, 29h, 2Dh	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

Voltage measurement updates above this unsigned threshold set its corresponding alarm or warning bit. Voltage measurements equal to or below this threshold clear its alarm or warning bit.

Lower Memory, Register 0Ah to 0Bh: V_{CC} ALARM LO
Lower Memory, Register 0Eh to 0Fh: V_{CC} WARN LO
Lower Memory, Register 12h to 13h: MON1 ALARM LO
Lower Memory, Register 16h to 17h: MON1 WARN LO
Lower Memory, Register 1Ah to 1Bh: MON2 ALARM LO
Lower Memory, Register 1Eh to 1Fh: MON2 WARN LO
Lower Memory, Register 22h to 23h: MON3 ALARM LO
Lower Memory, Register 26h to 27h: MON3 WARN LO
Lower Memory, Register 2Ah to 2Bh: MON4 ALARM LO
Lower Memory, Register 2Eh to 2Fh: MON4 WARN LO

FACTORY DEFAULT	0000h
READ ACCESS	All
WRITE ACCESS	PW2
MEMORY TYPE	Nonvolatile (SEE)

0Ah, 0Eh, 12h, 16h, 1Ah, 1Eh, 22h, 26h, 2Ah, 2Eh	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}
0Bh, 0Fh, 13h, 17h, 1Bh, 1Fh, 23h, 27h, 2Bh, 2Fh	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
	BIT 7							BIT 0

Voltage measurement updates below this unsigned threshold set its corresponding alarm or warning bit. Voltage measurements equal to or above this threshold clear its alarm or warning bit.

Lower Memory, Register 30h to 5Fh: PW2 EE

FACTORY DEFAULT	00h
READ ACCESS	All
WRITE ACCESS	PW2
MEMORY TYPE	Nonvolatile (EE)

30h to 5Fh	EE	EE	EE	EE	EE	EE	EE	EE
	BIT 7							BIT 0

PW2 level access-controlled EEPROM.

Lower Memory, Register 60h to 61h: TEMP VALUE

FACTORY DEFAULT	0000h
READ ACCESS	All
WRITE ACCESS	N/A
MEMORY TYPE	Volatile

60h	S	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
61h	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}
	BIT 7							BIT 0

Signed two's complement direct-to-temperature measurement.

Lower Memory, Register 62h to 63h: V_{CC} VALUE
Lower Memory, Register 64h to 65h: MON1 VALUE
Lower Memory, Register 66h to 67h: MON2 VALUE
Lower Memory, Register 68h to 69h: MON3 VALUE
Lower Memory, Register 6Ah to 6Bh: MON4 VALUE

POWER-ON VALUE	0000h
READ ACCESS	All
WRITE ACCESS	N/A
MEMORY TYPE	Volatile

	BIT 7							BIT 0
62h, 64h, 66h, 68h, 6Ah	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}
63h, 65h, 67h, 69h, 6Bh	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

Left-justified unsigned voltage measurement.

Lower Memory, Register 6Ch to 6D: RESERVED

POWER-ON VALUE	00h
READ ACCESS	All
WRITE ACCESS	N/A
MEMORY TYPE	

	BIT 7							BIT 0
6Ch, 6Dh	0	0	0	0	0	0	0	0

These registers are reserved. The value when read is 00h.

Lower Memory, Register 6Eh: STATUS

POWER-ON VALUE	X000 0XXXb
READ ACCESS	All
WRITE ACCESS	See below
MEMORY TYPE	Volatile

Write Access		N/A	All	N/A	All	All	N/A	N/A	N/A
	6Eh	FETG STATUS	SOFT FETG	RESERVED	TX-F RESET	SOFT TX-D	TX-F STATUS	LOS STATUS	RDYB
		BIT 7							BIT 0

BIT 7	**FETG STATUS:** Reflects the active state of FETG. The FETG DIR bit in Table 02h, Register 89h defines the polarity of FETG. 0 = Normal operation. Bias and modulation outputs are enabled. 1 = The FETG output is active. Bias and modulation outputs are disabled.
BIT 6	**SOFT FETG:** 0 = (Default) 1 = Forces the bias and modulation outputs to their off state and assert the FETG output.
BIT 5	**RESERVED** (Default = 0)
BIT 4	**TX-F RESET:** 0 = (Default) 1 = Resets the latch for the TX-F output. This bit is self-clearing after resetting TX-F.
BIT 3	**SOFT TX-D:** This bit allows a software control that is identical to the TX-D pin. See the *BIAS and MOD Output as a Function of Transmit Disable (TX-D)* section for further information. Its value is wired-ORed with the logic value of the TX-D pin. 0 = Internal TX-D signal is equal to the external TX-D pin. 1 = Internal TX-D signal is high.
BIT 2	**TX-F STATUS:** Reflects the active state of the TX-F pin. 0 = TX-F pin is not active. 1 = TX-F pin is active.
BIT 1	**LOS STATUS:** Loss of Signal. Reflects the logic level of the LOSI input pin. 0 = LOSI is logic-low. 1 = LOSI is logic-high.
BIT 0	**RDBY:** Ready Bar. 0 = V_{CC} is above POA. 1 = V_{CC} is below POA and/or too low to communicate over the I^2C bus.

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Lower Memory, Register 6Fh: UPDATE

POWER-ON VALUE	00h
READ ACCESS	All
WRITE ACCESS	All + DS1875 Hardware
MEMORY TYPE	Volatile

	BIT 7							BIT 0
6Fh	TEMP RDY	VCC RDY	MON1 RDY	MON2 RDY	MON3 RDY	MON4 RDY	MON5/7 RDY	MON6/8 RDY

Update of completed conversions. At power-on, these bits are cleared and are set as each conversion is completed. These bits can be cleared so that a completion of a new conversion is verified.

Lower Memory, Register 70h: ALARM$_3$

POWER-ON VALUE	10h
READ ACCESS	All
WRITE ACCESS	N/A
MEMORY TYPE	Volatile

70h	TEMP HI	TEMP LO	VCC HI	VCC LO	MON1 HI	MON1 LO	MON2 HI	MON2 LO
	BIT 7							BIT 0

BIT 7	**TEMP HI:** High alarm status for temperature measurement. 0 = (Default) Last measurement was equal to or below threshold setting. 1 = Last measurement was above threshold setting.
BIT 6	**TEMP LO:** Low alarm status for temperature measurement. 0 = (Default) Last measurement was equal to or above threshold setting. 1 = Last measurement was below threshold setting.
BIT 5	**VCC HI:** High alarm status for V_{CC} measurement. 0 = (Default) Last measurement was equal to or below threshold setting. 1 = Last measurement was above threshold setting.
BIT 4	**VCC LO:** Low alarm status for V_{CC} measurement. This bit is set when the V_{CC} supply is below the POA trip point value. It clears itself when a V_{CC} measurement is completed and the value is above the low threshold. 0 = Last measurement was equal to or above threshold setting. 1 = (Default) Last measurement was below threshold setting.
BIT 3	**MON1 HI:** High alarm status for MON1 measurement. 0 = (Default) Last measurement was equal to or below threshold setting. 1 = Last measurement was above threshold setting.
BIT 2	**MON1 LO:** Low alarm status for MON1 measurement. 0 = (Default) Last measurement was equal to or above threshold setting. 1 = Last measurement was below threshold setting.
BIT 1	**MON2 HI:** High alarm status for MON2 measurement. 0 = (Default) Last measurement was equal to or below threshold setting. 1 = Last measurement was above threshold setting.
BIT 0	**MON2 LO:** Low alarm status for MON2 measurement. 0 = (Default) Last measurement was equal to or above threshold setting. 1 = Last measurement was below threshold setting.

Lower Memory, Register 71h: $ALARM_2$

POWER-ON VALUE	00h
READ ACCESS	All
WRITE ACCESS	N/A
MEMORY TYPE	Volatile

71h	MON3 HI	MON3 LO	MON4 HI	MON4 LO	RESERVED	RESERVED	RESERVED	RESERVED
	BIT 7							BIT 0

BIT 7	**MON3 HI:** High alarm status for MON3 measurement. 0 = (Default) Last measurement was equal to or below threshold setting. 1 = Last measurement was above threshold setting.
BIT 6	**MON3 LO:** Low alarm status for MON3 measurement. 0 = (Default) Last measurement was equal to or above threshold setting. 1 = Last measurement was below threshold setting.
BIT 5	**MON4 HI:** High alarm status for MON4 measurement. 0 = (Default) Last measurement was equal to or below threshold setting. 1 = Last measurement was above threshold setting.
BIT 4	**MON4 LO:** Low alarm status for MON4 measurement. 0 = (Default) Last measurement was equal to or above threshold setting. 1 = Last measurement was below threshold setting.
BITS 3:0	**RESERVED**

Lower Memory, Register 72h: ALARM$_1$

POWER-ON VALUE	00h
READ ACCESS	All
WRITE ACCESS	N/A
MEMORY TYPE	Volatile

72h	RESERVED	RESERVED	RESERVED	RESERVED	BIAS HI	RESERVED	TXP HI	TXP LO
	BIT 7							BIT 0

BITS 7:4	**RESERVED**
BIT 3	**BIAS HI:** High alarm status bias; fast comparison. 0 = (Default) Last comparison was below threshold setting. 1 = Last comparison was above threshold setting.
BIT 2	**RESERVED**
BIT 1	**TXP HI:** High alarm status TXP; fast comparison. 0 = (Default) Last comparison was below threshold setting. 1 = Last comparison was above threshold setting.
BIT 0	**TXP LO:** Low alarm status TXP; fast comparison. 0 = (Default) Last comparison was above threshold setting. 1 = Last comparison was below threshold setting.

Lower Memory, Register 73h: ALARM$_0$

POWER-ON VALUE	00h
READ ACCESS	All
WRITE ACCESS	N/A
MEMORY TYPE	Volatile

73h	M3QT HI	RESERVED	RESERVED	RESERVED	BIAS MAX	RESERVED	RESERVED	RESERVED
	BIT 7							BIT 0

BIT 7	**M3QT HI:** High alarm status for MON3; fast comparison. 0 = (Default) Last comparison was below threshold setting. 1 = Last comparison was above threshold setting.
BITS 6:4	**RESERVED**
BIT 3	**BIAS MAX:** Alarm status for maximum digital setting of BIAS. 0 = (Default) The value for BIAS is equal to or below the MAX BIAS register. 1 = Requested value for BIAS is greater than the MAX BIAS register.
BITS 2:0	**RESERVED**

Lower Memory, Register 74h: $WARN_3$

POWER-ON VALUE	10h
READ ACCESS	All
WRITE ACCESS	N/A
MEMORY TYPE	Volatile

74h	TEMP HI	TEMP LO	VCC HI	VCC LO	MON1 HI	MON1 LO	MON2 HI	MON2 LO
	BIT 7							BIT 0

BIT 7	**TEMP HI:** High warning status for temperature measurement. 0 = (Default) Last measurement was equal to or below threshold setting. 1 = Last measurement was above threshold setting.
BIT 6	**TEMP LO:** Low warning status for temperature measurement. 0 = (Default) Last measurement was equal to or above threshold setting. 1 = Last measurement was below threshold setting.
BIT 5	**VCC HI:** High warning status for V_{CC} measurement. 0 = (Default) Last measurement was equal to or below threshold setting. 1 = Last measurement was above threshold setting.
BIT 4	**VCC LO:** Low warning status for V_{CC} measurement. This bit is set when the V_{CC} supply is below the POA trip point value. It clears itself when a V_{CC} measurement is completed and the value is above the low threshold. 0 = Last measurement was equal to or above threshold setting. 1 = (Default) Last measurement was below threshold setting.
BIT 3	**MON1 HI:** High warning status for MON1 measurement. 0 = (Default) Last measurement was equal to or below threshold setting. 1 = Last measurement was above threshold setting.
BIT 2	**MON1 LO:** Low warning status for MON1 measurement. 0 = (Default) Last measurement was equal to or above threshold setting. 1 = Last measurement was below threshold setting.
BIT 1	**MON2 HI:** High warning status for MON2 measurement. 0 = (Default) Last measurement was equal to or below threshold setting. 1 = Last measurement was above threshold setting.
BIT 0	**MON2 LO:** Low warning status for MON2 measurement. 0 = (Default) Last measurement was equal to or above threshold setting. 1 = Last measurement was below threshold setting.

Lower Memory, Register 75h: $WARN_2$

POWER-ON VALUE	00h
READ ACCESS	All
WRITE ACCESS	N/A
MEMORY TYPE	Volatile

75h	MON3 HI	MON3 LO	MON4 HI	MON4 LO	RESERVED	RESERVED	RESERVED	RESERVED
	BIT 7							BIT 0

BIT 7	**MON3 HI:** High warning status for MON3 measurement. 0 = (Default) Last measurement was equal to or below threshold setting. 1 = Last measurement was above threshold setting.
BIT 6	**MON3 LO:** Low warning status for MON3 measurement. 0 = (Default) Last measurement was equal to or above threshold setting. 1 = Last measurement was below threshold setting.
BIT 5	**MON4 HI:** High warning status for MON4 measurement. 0 = (Default) Last measurement was equal to or below threshold setting. 1 = Last measurement was above threshold setting.
BIT 4	**MON4 LO:** Low warning status for MON4 measurement. 0 = (Default) Last measurement was equal to or above threshold setting. 1 = Last measurement was below threshold setting.
BITS 3:0	**RESERVED**

Lower Memory Register 76h to 77h: RESERVED MEMORY

POWER-ON VALUE	00h
READ ACCESS	All
WRITE ACCESS	N/A
MEMORY TYPE	

These registers are reserved. The value when read is 00h.

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Lower Memory, Register 78h: DOUT

POWER-ON VALUE	Recalled from Table 02h, Register C0h
READ ACCESS	All
WRITE ACCESS	All
MEMORY TYPE	Volatile

78h	M3QT RESET	SOFT M3QT	RESERVED	RESERVED	D3 OUT	D2 OUT	D1 OUT	D0 OUT
	BIT 7							BIT 0

BIT 7	**M3QT RESET:** Resets the latch for M3QT. The PWM does not begin normal operation until the MON3 voltage is below M3QT, regardless of resetting the latch. 0 = (default) 1 = M3QT alarm is reset.
BIT 6	**SOFT M3QT:** Software control for setting the M3QT alarm. The PWM output pulse SW is disabled. 0 = (Default) Internal signal is controlled by trip point comparison. 1 = M3QT alarm is set to 1.
BITS 5:4	**RESERVED**
BIT 3	**D3 OUT:** Controls the output of the open-drain pin D3. 0 = Output is held low. 1 = Output is high impedance.
BIT 2	**D2 OUT:** Controls the output of the open-drain pin D2. 0 = Output is held low. 1 = Output is high impedance.
BIT 1	**D1 OUT:** Controls the output of the open-drain pin D1. 0 = Output is held low. 1 = Output is high impedance.
BIT 0	**D0 OUT:** Controls the output of the open-drain pin D0. 0 = Output is held low. 1 = Output is high impedance.

At power-on, these bits are defined by the value stored in the DPU byte (Table 02h, Register C0h). These bits define the value of the logic states of their corresponding output pins.

Lower Memory, Register 79h: DIN

POWER-ON VALUE	See description
READ ACCESS	All
WRITE ACCESS	N/A
MEMORY TYPE	Volatile

79h	INV M3QT	MUX M3QT	INV LOS	MUX LOS	D3 IN	D2 IN	D1 IN	D0 IN
	BIT 7							BIT 0

BIT 7	**INV M3QT:** Status of inversion of M3QT (internal signal) to D2 pin. MUX M3QT bit must be set to 1 or this bit does not affect the output. The value is controlled (or set) by the DPU byte. 1 = M3QT buffered to D2 is inverted.
BIT 6	**MUX M3QT:** Determines control of D2 pin. The value is controlled (or set) by the DPU byte. 0 = Logic value of D2 is controlled by DOUT byte. 1 = Logic value of D2 is controlled by M3QT (internal signal) and INV M3QT bit.
BIT 5	**INV LOS:** Status of inversion of LOSI pin to D0 pin. MUX LOS bit must be set to 1 or this bit does not effect the output. The value is controlled (or set) by the DPU byte. 1 = LOSI buffered D0 is inverted.
BIT 4	**MUX LOS:** Determines control of D0 pin. The value is controlled (or set) by the DPU byte. 0 = Logic value of D0 is controlled by DOUT byte. 1 = Logic value of D0 is controlled by LOSI pin and INV LOS bit.
BIT 3	**D3 IN:** Reflects the logic value of D3 pin.
BIT 2	**D2 IN:** Reflects the logic value of D2 pin.
BIT 1	**D1 IN:** Reflects the logic value of D1 pin.
BIT 0	**D0 IN:** Reflects the logic value of D0 pin.

Lower Memory, Register 7Ah: RESERVED

POWER-ON VALUE	00h
READ ACCESS	All
WRITE ACCESS	N/A
MEMORY TYPE	N/A

This register is reserved. The value when read is 00h.

Lower Memory, Register 7Bh to 7Eh: Password Entry (PWE)

POWER-ON VALUE	FFFF FFFFh
READ ACCESS	N/A
WRITE ACCESS	All
MEMORY TYPE	Volatile

7Bh	2^{31}	2^{30}	2^{29}	2^{28}	2^{27}	2^{26}	2^{25}	2^{24}
7Ch	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}
7Dh	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}
7Eh	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
	BIT 7							BIT 0

There are two passwords for the DS1875. Each password is 4 bytes long. The lower level password (PW1) has all the access of a normal user plus those made available with PW1. The higher level password (PW2) has all the access of PW1 plus those made available with PW2. The values of the passwords reside in EEPROM inside PW2 memory. At power-up, all PWE bits are set to 1. All reads at this location are 0.

Lower Memory, Register 7Fh: Table Select (TBL SEL)

POWER-ON VALUE	00h
READ ACCESS	All
WRITE ACCESS	All
MEMORY TYPE	Volatile

7Fh	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
	BIT 7							BIT 0

The upper memory tables (Table 00h to 08h) of the DS1875 are accessible by writing the desired table value in this register.

Table 00h Register Descriptions

Table 00h, Register 80h to 81h: MON5 VALUE
Table 00h, Register 82h to 83h: MON6 VALUE
Table 00h, Register 84h to 85h: MON7 VALUE
Table 00h, Register 86h to 87h: MON8 VALUE

POWER-ON VALUE	0000h
READ ACCESS	All
WRITE ACCESS	N/A
MEMORY TYPE	Volatile

80h, 82h, 84h, 86h	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}
81h, 83h, 85h, 87h	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
	BIT 7							BIT 0

Left-justified unsigned voltage measurement.

Table 01h Register Descriptions

Table 01h, Register 80h to F7h: PW1 EEPROM

POWER-ON VALUE	00h
READ ACCESS	PW1
WRITE ACCESS	PW1
MEMORY TYPE	Nonvolatile (EE)

80h to F7h	EE	EE	EE	EE	EE	EE	EE	EE
	BIT 7							BIT 0

EEPROM for PW1-level access.

Table 01h, Register F8h: $ALARM_3$

POWER-ON VALUE	00h
READ ACCESS	All
WRITE ACCESS	PW1
MEMORY TYPE	Volatile

F8h	TEMP HI	TEMP LO	VCC HI	VCC LO	MON1 HI	MON1 LO	MON2 HI	MON2 LO
	BIT 7							BIT 0

Layout is identical to $ALARM_3$ in Lower Memory, Register 70h with two exceptions.
1. VCC LO alarm is not set at power-on.
2. These bits are latched. They are cleared by power-down or a write with PW1 access.

Table 01h, Register F9h: $ALARM_2$

POWER-ON VALUE	00h
READ ACCESS	All
WRITE ACCESS	PW1
MEMORY TYPE	Volatile

F9h	MON3 HI	MON3 LO	MON4 HI	MON4 LO	RESERVED	RESERVED	RESERVED	RESERVED
	BIT 7							BIT 0

Layout is identical to $ALARM_2$ in Lower Memory, Register 71h with one exception.
1. These bits are latched. They are cleared by power-down or a write with PW1 access.

Table 01h, Register FAh: $ALARM_1$

POWER-ON VALUE	00h
READ ACCESS	All
WRITE ACCESS	PW1
MEMORY TYPE	Volatile

FAh	RESERVED	RESERVED	RESERVED	RESERVED	BIAS HI	RESERVED	TXP HI	TXP LO
	BIT 7							BIT 0

Layout is identical to $ALARM_1$ in Lower Memory, Register 72h with one exception.
1. These bits are latched. They are cleared by power-down or a write with PW1 access.

Table 01h, Register FBh: $ALARM_0$

POWER-ON VALUE	00h
READ ACCESS	All
WRITE ACCESS	PW1
MEMORY TYPE	Volatile

FBh	M3QT HI	RESERVED	RESERVED	RESERVED	BIAS MAX	RESERVED	RESERVED	RESERVED
	BIT 7							BIT 0

Layout is identical to $ALARM_0$ in Lower Memory, Register 73h with one exception.
1. These bits are latched. They are cleared by power-down or a write with PW1 access

Table 01h, Register FCh: $WARN_3$

POWER-ON VALUE	00h
READ ACCESS	All
WRITE ACCESS	PW1
MEMORY TYPE	Volatile

FCh	TEMP HI	TEMP LO	VCC HI	VCC LO	MON1 HI	MON1 LO	MON2 HI	MON2 LO
	BIT 7							BIT 0

Layout is identical to $WARN_3$ in Lower Memory, Register 74h with two exceptions.
1. VCC LO warning is not set at power-on.
2. These bits are latched. They are cleared by power-down or a write with PW1 access.

Table 01h, Register FDh: $WARN_2$

POWER-ON VALUE	00h
READ ACCESS	All
WRITE ACCESS	PW1
MEMORY TYPE	Volatile

FDh	MON3 HI	MON3 LO	MON4 HI	MON4 LO	RESERVED	RESERVED	RESERVED	RESERVED
	BIT 7							BIT 0

Layout is identical to $WARN_2$ in Lower Memory, Register 75h with one exception.
1. These bits are latched. They are cleared by power-down or a write with PW1 access.

Table 01h, Register FEh to FFh: RESERVED

POWER-ON VALUE	00h
READ ACCESS	All
WRITE ACCESS	PW1
MEMORY TYPE	Volatile

These registers are reserved.

Table 02h, Register 80h: MODE

POWER-ON VALUE	3Fh
READ ACCESS	PW2
WRITE ACCESS	PW2
MEMORY TYPE	Volatile

80h	SEEB	RESERVED	PWM EN	M4DAC EN	AEN	MOD EN	APC EN	BIAS EN
	BIT 7							BIT 0

BIT 7	**SEEB:** 0 = (Default) Enables EEPROM writes to SEE bytes. 1 = Disables EEPROM writes to SEE bytes during configuration, so that the configuration of the part is not delayed by the EE cycle time. Once the values are known, write this bit to a 0 and write the SEE locations again for data to be written to the EEPROM.
BIT 6	**RESERVED**
BIT 5	**PWM EN:** 0 = PWM DAC is writable by the user and the LUT recalls are disabled. This allows users to interactively test their modules by writing the DAC value for the PWM DAC. The output is updated with the new value at the end of the write cycle. The I^2C STOP condition is the end of the write cycle. 1 = (Default) Enables auto control of the LUT for PWM DAC.
BIT 4	**M4DAC EN:** 0 = M4DAC is writable by the user and the LUT recalls are disabled. This allows users to interactively test their modules by writing the DAC value for M4DAC. The output is updated with the new value at the end of the write cycle. The I^2C STOP condition is the end of the write cycle. 1 = (Default) Enables auto control of the LUT for M4DAC.
BIT 3	**AEN:** 0 = The temperature-calculated index value TINDEX is writable by users and the updates of calculated indexes are disabled. This allows users to interactively test their modules by controlling the indexing for the LUTs. The recalled values from the LUTs appear in the DAC registers after the next completion of a temperature conversion.
BIT 2	**MOD EN:** 0 = MOD DAC is writable by the user and the LUT recalls are disabled. This allows users to interactively test their modules by writing the DAC value for modulation. The output is updated with the new value at the end of the write cycle. The I^2C STOP condition is the end of the write cycle. 1 = (Default) Enables auto control of the LUT for modulation.
BIT 1	**APC EN:** 0 = APC DAC is writable by the user and the LUT recalls are disabled. This allows users to interactively test their modules by writing the DAC value for APC reference. The output is updated with the new value at the end of the write cycle. The I^2C STOP condition is the end of the write cycle. 1 = (Default) Enables auto control of the LUT for APC reference.
BIT 0	**BIAS EN:** 0 = BIAS DAC is controlled by the user and the APC is in manual mode. The BIAS DAC value is written to the MAN BIAS register. All values that are written to MAN BIAS and are greater than the MAX BIAS register setting are not updated and set the BIAS MAX alarm bit. The BIAS DAC register continues to reflect the value of the BIAS DAC. This allows users to interactively test their modules by writing the DAC value for bias. The output is updated with the new value at the end of the write cycle to the MAN BIAS register. The I^2C STOP condition is the end of the write cycle. 1 = (Default) Enables auto control for the APC feedback.

Table 02h, Register 81h: Temperature Index (TINDEX)

FACTORY DEFAULT	00h
READ ACCESS	PW2
WRITE ACCESS	PW2 and AEN = 0
MEMORY TYPE	Volatile

81h	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	BIT 7							BIT 0

Holds the calculated index based on the temperature measurement. This index is used for the address during lookup of Tables 04h, 05h, 07h, and 08h. Temperature measurements below -40°C or above +102°C are clamped to 00h and C7h, respectively. The calculation of TINDEX is as follows:

$$TINDEX = \frac{Temp_Value + 40°C}{2°C} + 80h$$

For the temperature-indexed LUTs, the index used during the lookup function for each table is as follows:

Table 04h (MOD)	1	$TINDEX_6$	$TINDEX_5$	$TINDEX_4$	$TINDEX_3$	$TINDEX_2$	$TINDEX_1$	$TINDEX_0$
Table 05h (APC)	1	0	$TINDEX_6$	$TINDEX_5$	$TINDEX_4$	$TINDEX_3$	$TINDEX_2$	$TINDEX_1$
Table 07h (PWM)	1	0	$TINDEX_6$	$TINDEX_5$	$TINDEX_4$	$TINDEX_3$	$TINDEX_2$	$TINDEX_1$
Table 08h (BIAS)	1	$TINDEX_6$	$TINDEX_5$	$TINDEX_4$	$TINDEX_3$	$TINDEX_2$	$TINDEX_1$	$TINDEX_0$

Table 02h, Register 82h: MOD DAC

FACTORY DEFAULT	00h
READ ACCESS	PW2
WRITE ACCESS	PW2 and MOD EN = 0
MEMORY TYPE	Volatile

82h	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	BIT 7							BIT 0

The digital value used for MOD and recalled from Table 04h at the adjusted memory address found in TINDEX. This register is updated at the end of the temperature conversion.

$$V_{MOD} = \frac{Full\ Scale}{255} \times MOD\ DAC$$

Table 02h, Register 83h: APC DAC

FACTORY DEFAULT	00h
READ ACCESS	PW2
WRITE ACCESS	PW2 and APC EN = 0
MEMORY TYPE	Volatile

83h	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	BIT 7							BIT 0

The digital value used for APC reference and recalled from Table 05h at the adjusted memory address found in TINDEX. This register is updated at the end of the temperature conversion.

$$V_{BMD} = \frac{\text{Full Scale}}{255} \times \text{APC DAC}$$

Table 02h, Register 84h: Voltage Index (VINDEX)

FACTORY DEFAULT	00h
READ ACCESS	PW2
WRITE ACCESS	PW2 and AEN = 0
MEMORY TYPE	Volatile

84h	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	BIT 7							BIT 0

Holds the calculated index based on the MON4 voltage measurement. This index is used for the address during lookup of Table 06h. M4DAC LUT is 32 bytes from address 80h to 9Fh. The calculation of VINDEX is as follows:

$$\text{VINDEX} = \frac{\text{MON4}}{800\text{h}} + 80\text{h}$$

When configured as a single LUT, all 32 bytes are used for lookup.
When configured as a double LUT, the first 16 bytes (80h to 8Fh) form the lower LUT and the last 16 bytes (90h to 9Fh) form the upper LUT.
For the three different modes, the index used during the lookup function of Table 06h is as follows:

Single	1	0	0	$VINDEX_4$	$VINDEX_3$	$VINDEX_2$	$VINDEX_1$	$VINDEX_0$
Double/Lower	1	0	0	0	$VINDEX_4$	$VINDEX_3$	$VINDEX_2$	$VINDEX_1$
Double/Upper	1	0	0	1	$VINDEX_4$	$VINDEX_3$	$VINDEX_2$	$VINDEX_1$

Table 02h, Register 85h: M4DAC

FACTORY DEFAULT	00h
READ ACCESS	PW2
WRITE ACCESS	PW2 and M4DAC EN = 0
MEMORY TYPE	Volatile

85h	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	BIT 7							BIT 0

The digital value used for M4DAC and recalled from Table 06h at the adjusted memory address found in VINDEX. This register is updated at the end of the MON4 conversion.

$$V_{M4DAC} = \frac{2.5}{256} \times (M4DAC + 1)$$

Table 02h, Register 86h: DEVICE ID

FACTORY DEFAULT	75h
READ ACCESS	PW2
WRITE ACCESS	N/A
MEMORY TYPE	ROM

86h	0	1	1	1	0	1	0	1
	BIT 7							BIT 0

Hardwired connections to show the device ID.

Table 02h, Register 87h: DEVICE VER

FACTORY DEFAULT	DEVICE VERSION
READ ACCESS	PW2
WRITE ACCESS	N/A
MEMORY TYPE	ROM

87h	DEVICE VERSION	
	BIT 7	BIT 0

Hardwired connections to show device version.

Table 02h, Register 88h: SAMPLE RATE

FACTORY DEFAULT	30h
READ ACCESS	PW2
WRITE ACCESS	PW2
MEMORY TYPE	Nonvolatile (SEE)

88h	SEE	SEE	PWM_FR_1	PWM_FR_0	APC_SR_3	APC_SR_2	APC_SR_1	APC_SR_0
	BIT 7							BIT 0

BITS 7:6	**SEE**
BITS 5:4	**PWM_FR[1:0]:** 2-bit frequency rate for the SW pulsed output used with PWM. When switching a lower to a higher frequency, disable the SW output by setting SOFT M3QT (Byte 78h) to a 1 before changing PWM_FR. After changing PWM_FR, wait 200 periods of the new frequency before enabling the SW output. This delay allows for the internal signals to integrate and lock to the new frequency without creating a large duty cycle. 00b: 131.25kHz 01b: 262.5kHz 10b: 525kHz 11b: 1050kHz (Default)
BITS 3:0	**APC_SR[3:0]:** 4-bit sample rate for comparison of APC control.

Defines the sample rate for comparison of APC control.

APC_SR[3:0]	MINIMUM TIME FROM BEN TO FIRST SAMPLE (t_{FIRST}) ±50ns (ns)	REPEATED SAMPLE PERIOD FOLLOWING FIRST SAMPLE (t_{REP}) (ns)
0000b	350	800
0001b	550	1200
0010b	750	1600
0011b	950	2000
0100b	1350	2800
0101b	1550	3200
0110b	1750	3600
0111b	2150	4400
1000b	2950	6000
1001b*	3150	6400

**All codes greater than 1001b (1010b to 1111b) use the maximum sample time of code 1001b.*

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Table 02h, Register 89h: CONFIG

FACTORY DEFAULT	00h
READ ACCESS	PW2
WRITE ACCESS	PW2
MEMORY TYPE	Nonvolatile (SEE)

89h	FETG DIR	TX-F LEN	M3QT LEN	ASEL	BOLFS	RSSI_FC	RSSI_FF	EN5TO8B
	BIT 7							BIT 0

Configure the memory location and the polarity of the digital outputs.

BIT 7	**FETG DIR:** Chooses the direction or polarity of the FETG output for normal operation. 0 = (Default) Under normal operation, FETG is pulled low. 1 = Under normal operation, FETG is pulled high.
BIT 6	**TX-F LEN:** The TX-F output pin always reflects the wired-OR of all TX-F enabled alarm states. This bit enables the latching of the alarm state for the TX-F output pin. 0 = (Default) Not latched. 1 = The alarm bits are latched until cleared by a TX-D transition or power-down. If the V_{CC} alarm is enabled for either FETG or TX-F, then latching is disabled until after the first V_{CC} measurement is made above the V_{CC} ALARM LO set point to allow for proper operation during slow power-on cycles.
BIT 5	**M3QT LEN:** This bit enables the latching of the alarm for the M3QT. 0 = (Default) Not latched. 1 = The alarm bit is latched until cleared by setting the M3QT RESET bit (Byte 78h).
BIT 4	**ASEL:** Address select. 0 = (Default) Device address of A2h. 1 = Device address is equal to the value found in the DEVICE ADDRESS byte (Table 02h, 8Ch).
BIT 3	**BOLFS:** Bias open-loop full scale. 0 = (Default) Full scale is 600µA. 1 = Full scale is 1.2mA.
BITS 2:1	**RSSI_FC and RSSI_FF:** RSSI force coarse and RSSI force fine. Control bits for RSSI mode of operation on the MON3 conversion. 00b = (Default) Normal RSSI mode of operation. 01b = The fine settings of scale and offset are used for MON3 conversions. 10b = The coarse settings of scale and offset are used for MON3 conversions. 11b = Normal RSSI mode of operation.
BIT 0	**EN5TO8B:** This bit enables MON5–MON8 conversion (voltage of D0–D3 pins). 0 = (Default) Temperature, V_{CC}, and MON1–MON8 conversions are enabled. 1 = Temperature, V_{CC}, and MON1–MON4 conversions are enabled.

Table 02h, Register 8Ah: RESERVED

FACTORY DEFAULT	00h
READ ACCESS	PW2
WRITE ACCESS	PW2
MEMORY TYPE	Nonvolatile (SEE)

This register is reserved.

Table 02h, Register 8Bh: MOD RANGING

FACTORY DEFAULT	00h
READ ACCESS	PW2
WRITE ACCESS	PW2
MEMORY TYPE	Nonvolatile (SEE)

8Bh	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	MOD_2	MOD_1	MOD_0
	BIT 7							BIT 0

The lower nibble of this byte controls the full-scale range of the Modulation DAC

BITS 7:3	**RESERVED** (Default = 0)
BITS 2:0	**MOD[2:0]: MOD FS RANGING:** 3-bit value to select the FS output voltage for MOD. Default is 000b and creates a FS of 1.25V.

MOD[2:0]	% OF 1.25V	FS VOLTAGE (V)
000b	100.00	1.250
001b	80.05	1.001
010b	66.75	0.834
011b	50.13	0.627
100b	40.15	0.502
101b	33.50	0.419
110b	28.74	0.359
111b	25.17	0.315

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Table 02h, Register 8Ch: DEVICE ADDRESS

FACTORY DEFAULT	00h
READ ACCESS	PW2
WRITE ACCESS	PW2
MEMORY TYPE	Nonvolatile (SEE)

8Ch	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	BIT 7							BIT 0

This value becomes the I^2C slave address for the main memory when the ASEL (Table 02h, Register 89h) bit is set. If A0h is programmed to this register, the auxiliary memory is disabled.

Table 02h, Register 8Dh: COMP RANGING

FACTORY DEFAULT	00h
READ ACCESS	PW2
WRITE ACCESS	PW2
MEMORY TYPE	Nonvolatile (SEE)

8Dh	RESERVED	$BIAS_2$	$BIAS_1$	$BIAS_0$	RESERVED	APC_2	APC_1	APC_0
	BIT 7							BIT 0

The upper nibble of this byte controls the full-scale range of the quick-trip monitoring for BIAS. The lower nibble of this byte controls the full-scale range for the quick-trip monitoring of the APC reference as well as the closed-loop monitoring of APC.

<table>
<tr><td>BIT 7</td><td>RESERVED (Default = 0)</td></tr>
<tr><td>BITS 6:4</td><td>BIAS[2:0] BIAS Full-Scale Ranging. 3-bit value to select the FS comparison voltage for BIAS found on MON1. Default is 000b and creates a FS of 1.25V.
<table>
<tr><th>BIAS[2:0]</th><th>% OF 1.25V</th><th>FS VOLTAGE (V)</th></tr>
<tr><td>000b</td><td>100.00</td><td>1.250</td></tr>
<tr><td>001b</td><td>80.04</td><td>1.001</td></tr>
<tr><td>010b</td><td>66.73</td><td>0.834</td></tr>
<tr><td>011b</td><td>50.10</td><td>0.626</td></tr>
<tr><td>100b</td><td>40.11</td><td>0.501</td></tr>
<tr><td>101b</td><td>33.45</td><td>0.418</td></tr>
<tr><td>110b</td><td>28.69</td><td>0.359</td></tr>
<tr><td>111b</td><td>25.12</td><td>0.314</td></tr>
</table></td></tr>
<tr><td>BIT 3</td><td>RESERVED (Default = 0)</td></tr>
<tr><td>BITS 2:0</td><td>APC[2:0] APC Full-Scale Ranging. 3-bit value to select the FS comparison voltage for BMD with the APC. Default is 000b and creates a FS of 2.5V.
<table>
<tr><th>APC[2:0]</th><th>% OF 2.50V</th><th>FS VOLTAGE (V)</th></tr>
<tr><td>000b</td><td>100.00</td><td>1.250</td></tr>
<tr><td>001b</td><td>80.04</td><td>1.001</td></tr>
<tr><td>010b</td><td>66.73</td><td>0.834</td></tr>
<tr><td>011b</td><td>50.10</td><td>0.626</td></tr>
<tr><td>100b</td><td>40.11</td><td>0.501</td></tr>
<tr><td>101b</td><td>33.45</td><td>0.418</td></tr>
<tr><td>110b</td><td>28.69</td><td>0.359</td></tr>
<tr><td>111b</td><td>25.12</td><td>0.314</td></tr>
</table></td></tr>
</table>

Table 02h, Register 8Eh: RIGHT SHIFT$_1$ (RSHIFT$_1$)

FACTORY DEFAULT	00h
READ ACCESS	PW2
WRITE ACCESS	PW2
MEMORY TYPE	Nonvolatile (SEE)

8Eh	RESERVED	MON1$_2$	MON1$_1$	MON1$_0$	RESERVED	MON2$_2$	MON2$_1$	MON2$_0$
	BIT 7							BIT 0

Allows for right-shifting the final answer of MON1 and MON2 voltage measurements. This allows for scaling the measurements to the smallest full-scale voltage and then right-shifting the final result so the reading is weighted to the correct LSB.

Table 02h, Register 8Fh: RIGHT SHIFT$_0$ (RSHIFT$_0$)

FACTORY DEFAULT	30h
READ ACCESS	PW2
WRITE ACCESS	PW2
MEMORY TYPE	Nonvolatile (SEE)

8Fh	RESERVED	MON3$_2$	MON3$_1$	MON3$_0$	RESERVED	MON4$_2$	MON4$_1$	MON4$_0$
	BIT 7							BIT 0

Allows for right-shifting the final answer of MON3 and MON4 voltage measurements. This allows for scaling the measurements to the smallest full-scale voltage and then right-shifting the final result so the reading is weighted to the correct LSB.

Table 02h, Register 90h to 91h: RESERVED

FACTORY DEFAULT	0000h
READ ACCESS	PW2
WRITE ACCESS	PW2
MEMORY TYPE	Nonvolatile (SEE)

These registers are reserved.

Table 02h, Register 92h to 93h: V_{CC} SCALE
Table 02h, Register 94h to 95h: MON1 SCALE
Table 02h, Register 96h to 97h: MON2 SCALE
Table 02h, Register 98h to 99h: MON3 FINE SCALE
Table 02h, Register 9Ah to 9Bh: MON4 SCALE
Table 02h, Register 9Ch to 9Dh: MON3 COARSE SCALE

FACTORY CALIBRATED	
READ ACCESS	PW2
WRITE ACCESS	PW2
MEMORY TYPE	Nonvolatile (SEE)

92h, 94h, 96h, 98h, 9Ah, 9Ch	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}
93h, 95h, 97h, 99h, 9Bh, 9Dh	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
	BIT 7							BIT 0

Controls the scaling or gain of the FS voltage measurements. The factory-calibrated value produces an FS voltage of 6.5536V for V_{CC} and 2.5V for MON1, MON2, MON3, and MON4.

Table 02h, Register 9Eh to A1h: RESERVED

FACTORY DEFAULT	00h
READ ACCESS	PW2
WRITE ACCESS	PW2
MEMORY TYPE	Nonvolatile (SEE)

These registers are reserved.

Table 02h, Register A2h to A3h: V_{CC} OFFSET
Table 02h, Register A4h to A5h: MON1 OFFSET
Table 02h, Register A6h to A7h: MON2 OFFSET
Table 02h, Register A8h to A9h: MON3 FINE OFFSET
Table 02h, Register AAh to ABh: MON4 OFFSET
Table 02h, Register ACh to ADh: MON3 COARSE OFFSET

FACTORY DEFAULT	00h
READ ACCESS	PW2
WRITE ACCESS	PW2
MEMORY TYPE	Nonvolatile (SEE)

A2h, A4h, A6h, A8h, AAh, ACh	S	S	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}
A3h, A5h, A7h, A9h, ABh, ADh	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}
	BIT 7							BIT 0

Allows for offset control of these voltage measurements if desired.

Table 02h, Register AEh to AFh: INTERNAL TEMP OFFSET

FACTORY CALIBRATED	
READ ACCESS	PW2
WRITE ACCESS	PW2
MEMORY TYPE	Nonvolatile (SEE)

AEh	S	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}
AFh	2^{1}	2^{0}	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}
	BIT 7							BIT 0

Allows for offset control of temperature measurement if desired. The final result must be XORed with BB40h before writing to this register. Factory calibration contains the desired value for a reading in degrees Celsius.

Table 02h, Register B0h to B3h: PW1

FACTORY DEFAULT	FFFF FFFFh
READ ACCESS	N/A
WRITE ACCESS	PW2
MEMORY TYPE	Nonvolatile (SEE)

B0h	2^{31}	2^{30}	2^{29}	2^{28}	2^{27}	2^{26}	2^{25}	2^{24}
B1h	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}
B2h	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}
B3h	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
	BIT 7							BIT 0

The PWE value is compared against the value written to this location to enable PW1 access. At power-on, the PWE value is set to all 1s. Thus, writing these bytes to all 1s grants PW1 access on power-on without writing the password entry. All reads of this register are 00h.

Table 02h, Register B4h to B7h: PW2

FACTORY DEFAULT	FFFF FFFFh
READ ACCESS	N/A
WRITE ACCESS	PW2
MEMORY TYPE	Nonvolatile (SEE)

B4h	2^{31}	2^{30}	2^{29}	2^{28}	2^{27}	2^{26}	2^{25}	2^{24}
B5h	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}
B6h	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}
B7h	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
	BIT 7							BIT 0

The PWE value is compared against the value written to this location to enable PW2 access. At power-on, the PWE value is set to all 1s. Thus writing these bytes to all 1s grants PW2 access on power-on without writing the password entry. All reads of this register are 00h.

Table 02h, Register B8h: FETG ENABLE$_1$

FACTORY DEFAULT	00h
READ ACCESS	PW2
WRITE ACCESS	PW2
MEMORY TYPE	Nonvolatile (SEE)

B8h	TEMP EN	VCC EN	MON1 EN	MON2 EN	MON3 EN	MON4 EN	RESERVED	RESERVED
	BIT 7							BIT 0

Configures the maskable interrupt for the FETG pin.

BIT 7	**TEMP EN:** Enables/disables active interrupts on the FETG pin due to temperature measurements outside the threshold limits. 0 = Disable (Default) 1 = Enable
BIT 6	**VCC EN:** Enables/disables active interrupts on the FETG pin due to V_{CC} measurements outside the threshold limits. 0 = Disable (Default) 1 = Enable
BIT 5	**MON1 EN:** Enables/disables active interrupts on the FETG pin due to MON1 measurements outside the threshold limits. 0 = Disable (Default) 1 = Enable
BIT 4	**MON2 EN:** Enables/disables active interrupts on the FETG pin due to MON2 measurements outside the threshold limits. 0 = Disable (Default) 1 = Enable
BIT 3	**MON3 EN:** Enables/disables active interrupts on the FETG pin due to MON3 measurements outside the threshold limits. 0 = Disable (Default) 1 = Enable
BIT 2	**MON4 EN:** Enables/disables active interrupts on the FETG pin due to MON4 measurements outside the threshold limits. 0 = Disable (Default) 1 = Enable
BITS 1:0	**RESERVED** (Default = 0)

Table 02h, Register B9h: FETG ENABLE$_0$

FACTORY DEFAULT	00h
READ ACCESS	PW2
WRITE ACCESS	PW2
MEMORY TYPE	Nonvolatile (SEE)

B9h	TXP HI EN	TXP LO EN	BIAS HI EN	BIAS MAX EN	RESERVED	RESERVED	RESERVED	RESERVED
	BIT 7							BIT 0

Configures the maskable interrupt for the FETG pin.

BIT 7	**TXP HI EN:** Enables/disables active interrupts on the FETG pin due to TXP fast comparisons above the threshold limit. 0 = Disable (Default) 1 = Enable
BIT 6	**TXP LO EN:** Enables/disables active interrupts on the FETG pin due to TXP fast comparisons below the threshold limit. 0 = Disable (Default) 1 = Enable
BIT 5	**BIAS HI EN:** Enables/disables active interrupts on the FETG pin due to BIAS fast comparisons above the threshold limit. 0 = Disable. (Default) 1 = Enable
BIT 4	**BIAS MAX EN:** Enables/disables active interrupts on the FETG pin due to BIAS fast comparisons below the threshold limit. 0 = Disable (Default) 1 = Enable
BITS 3:0	**RESERVED** (Default = 0)

Table 02h, Register BAh: TX-F ENABLE$_1$

FACTORY DEFAULT	00h
READ ACCESS	PW2
WRITE ACCESS	PW2
MEMORY TYPE	Nonvolatile (SEE)

BAh	TEMP EN	VCC EN	MON1 EN	MON2 EN	MON3 EN	MON4 EN	RESERVED	RESERVED
	BIT 7							BIT 0

Configures the maskable interrupt for the TX-F pin.

BIT 7	**TEMP EN:** Enables/disables active interrupts on the TX-F pin due to temperature measurements outside the threshold limits. 0 = Disable (Default) 1 = Enable
BIT 6	**VCC EN:** Enables/disables active interrupts on the TX-F pin due to V_{CC} measurements outside the threshold limits. 0 = Disable (Default) 1 = Enable
BIT 5	**MON1 EN:** Enables/disables active interrupts on the TX-F pin due to MON1 measurements outside the threshold limits. 0 = Disable (Default) 1 = Enable
BIT 4	**MON2 EN:** Enables/disables active interrupts on the TX-F pin due to MON2 measurements outside the threshold limits. 0 = Disable (Default) 1 = Enable
BIT 3	**MON3 EN:** Enables/disables active interrupts on the TX-F pin due to MON3 measurements outside the threshold limits. 0 = Disable (Default) 1 = Enable
BIT 2	**MON4 EN:** Enables/disables active interrupts on the TX-F pin due to MON4 measurements outside the threshold limits. 0 = Disable (Default) 1 = Enable
BITS 2:0	**RESERVED** (Default = 0)

Table 02h, Register BBh: TX-F ENABLE$_0$

FACTORY DEFAULT	00h
READ ACCESS	PW2
WRITE ACCESS	PW2
MEMORY TYPE	Nonvolatile (SEE)

BBh	TXP HI EN	TXP LO EN	BIAS HI EN	BIAS MAX EN	RESERVED	RESERVED	RESERVED	FETG EN
	BIT 7							BIT 0

Configures the maskable interrupt for the TX-F pin.

BIT 7	**TXP HI EN:** Enables/disables active interrupts on the TX-F pin due to TXP fast comparisons above the threshold limit. 0 = Disable (Default) 1 = Enable
BIT 6	**TXP LO EN:** Enables/disables active interrupts on the TX-F pin due to TXP fast comparisons below the threshold limit. 0 = Disable (Default) 1 = Enable
BIT 5	**BIAS HI EN:** Enables/disables active interrupts on the TX-F pin due to BIAS fast comparisons above the threshold limit. 0 = Disable (Default) 1 = Enable
BIT 4	**BIAS MAX EN:** Enables/disables active interrupts on the TX-F pin due to BIAS fast comparisons above the threshold limit. 0 = Disable (Default) 1 = Enable
BITS 3:1	**RESERVED** (Default = 0)
BIT 0	**FETG EN:** 0 = Normal FETG operation (Default). 1 = Enables FETG to act as an input to TX-F output.

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Table 02h, Register BCh: HTXP

FACTORY DEFAULT	00h
READ ACCESS	PW2
WRITE ACCESS	PW2
MEMORY TYPE	Nonvolatile (SEE)

BCh	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	BIT 7							BIT 0

Fast comparison DAC threshold adjust for high TXP. This value is added to the APC DAC value recalled from Table 04h. If the sum is greater than 0xFF, 0xFF is used. Comparisons greater than V_{HTXP}, compared against V_{BMD}, create a TXP HI alarm. The same ranging applied to the APC DAC should be used here.

$$V_{HTXP} = \frac{\text{Full Scale}}{255} \times (\text{HTXP} + \text{APC DAC})$$

Table 02h, Register BDh: LTXP

FACTORY DEFAULT	00h
READ ACCESS	PW2
WRITE ACCESS	PW2
MEMORY TYPE	Nonvolatile (SEE)

BDh	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	BIT 7							BIT 0

Fast-comparison DAC threshold adjust for low TXP. This value is subtracted from the APC DAC value recalled from Table 04h. If the difference is less than 0x00, 0x00 is used. Comparisons less than V_{LTXP}, compared against V_{BMD}, create a TXP LO alarm. The same ranging applied to the APC DAC should be used here.

$$V_{LTXP} = \frac{\text{Full Scale}}{255} \times (\text{APC DAC} - \text{LTXP})$$

Table 02h, Register BEh: HBIAS

FACTORY DEFAULT	00h
READ ACCESS	PW2
WRITE ACCESS	PW2
MEMORY TYPE	Nonvolatile (SEE)

BEh	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	BIT 7							BIT 0

Fast-comparison DAC setting for high BIAS. Comparisons greater than V_{HBIAS}, found on the MON1 pin, create a BIAS HI alarm.

$$V_{HBIAS} = \frac{\text{Full Scale}}{255} \times \text{HBIAS}$$

Table 02h, Register BFh: MAX BIAS

FACTORY DEFAULT	00h
READ ACCESS	PW2
WRITE ACCESS	PW2
MEMORY TYPE	Nonvolatile (SEE)

BFh	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5
	BIT 7							BIT 0

This value defines the maximum DAC value allowed for the upper 8 bits of BIAS output during all operations.

Table 02h, Register C0h: DPU

FACTORY DEFAULT	00h
READ ACCESS	PW2
WRITE ACCESS	PW2
MEMORY TYPE	Nonvolatile (SEE)

C0h	INV M3QT	MUX M3QT	INV LOS	MUX LOS	D3 CNTL	D2 CNTL	D1 CNTL	D0 CNTL
	BIT 7							BIT 0

BIT 7	**INV M3QT:** Inverts the internal M3QT signal to output pin D2 if MUX M3QT is set. If MUX M3QT is not set, this bit's value is a don't care. 0 = (Default) Noninverted M3QT to D2 pin. 1 = Inverted M3QT to D2 pin.
BIT 6	**MUX M3QT:** Chooses the control for D2 output pin. 0 = (Default) D2 is controlled by bit D2 IN found in byte 79h. 1 = M3QT is buffered to D2 pin.
BIT 5	**INV LOS:** Inverts the buffered input pin LOSI to output pin D0 if MUX LOS is set. If MUX LOS is not set, this bit's value is a don't care. 0 = (Default) Noninverted LOSI to D0 pin. 1 = Inverted LOSI to D0 pin.
BIT 4	**MUX LOS:** Chooses the control for D0 output pin. 0 = (Default) DO is controlled by bit D0 IN found in byte 79h. 1 = LOSI is buffered to D0 pin.
BIT 3	**D3 CNTL:** At power-on, this bit's value is loaded into bit D3 OUT of byte 78h to control the output pin D3. 0 = (Default)
BIT 2	**D2 CNTL:** At power-on, this bit's value is loaded into bit D2 OUT of byte 78h to control the output pin D2. 0 = (Default)
BIT 1	**D1 CNTL:** At power-on, this bit's value is loaded into bit D1 OUT of byte 78h to control the output pin D1. 0 = (Default)
BIT 0	**D0 CNTL:** At power-on, this bit's value is loaded into bit D0 OUT of byte 78h to control the output pin D0. 0 = (Default)

Controls the power-on values for D3, D2, D1, and D0 output pins and mux and invertion of the LOSI pin.

Table 02h, Register C1h to C2h: RESERVED

FACTORY DEFAULT	00h
READ ACCESS	PW2
WRITE ACCESS	PW2
MEMORY TYPE	Nonvolatile (SEE)

These registers are reserved.

Table 02h, Register C3h: M3QT DAC

FACTORY DEFAULT	00h
READ ACCESS	PW2
WRITE ACCESS	PW2
MEMORY TYPE	Nonvolatile (SEE)

C3h	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	BIT 7							BIT 0

Register to control M3QT DAC.

$$V_{M3QT} = \frac{1.25}{256} \times (M3QT\ DAC + 1)$$

Table 02h, Register C4h: DAC1

FACTORY DEFAULT	00h
READ ACCESS	PW2
WRITE ACCESS	PW2
MEMORY TYPE	Nonvolatile (SEE)

C4h	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	BIT 7							BIT 0

Register to control DAC1.

$$V_{DACI} = \frac{2.5}{256} \times (DAC1 + 1)$$

Table 02h, Register C5h to C6h: RESERVED

FACTORY DEFAULT	00h
READ ACCESS	PW2
WRITE ACCESS	PW2
MEMORY TYPE	Nonvolatile (SEE)

These registers are reserved.

Table 02h, Register C7h: M4 LUT CNTL

FACTORY DEFAULT	00h
READ ACCESS	PW2
WRITE ACCESS	PW2
MEMORY TYPE	Nonvolatile (SEE)

C7h	RESERVED	RESERVED	RESERVED	RESERVED	FBOL	FBCL	DBL_SB	UP_LOWB
	BIT 7							BIT 0

BITS 7:4	**RESERVED** (Default = 000000b)
BITS 3:2	**FBOL and FBCL:** Force bias open loop and force bias closed loop. 00b = (Default) normal operation. 10b = Force control of I_{BIAS} to be open loop regardless of duration of BEN pulses. 01b = Force control of I_{BIAS} to be closed loop regardless of duration of BEN pulses. 11b = Same as 10b. When forcing open-loop mode, BEN should be ground or at any burst length.
BIT 1	**DBL_SB:** Chooses the size of LUT for Table 06h. 0 = (Default) Single LUT of 32 bytes. 1 = Double LUT of 16 bytes.
BIT 0	**UP_LOWB:** Determines which 16-byte LUT is used if DBL_SB = 1. If DBL_SB = 0, the value of this bit is a don't care. 0 = (Default) Chooses the lower 16 bytes of Table 06h (80h to 8Fh). 1 = Chooses the upper 16 bytes of Table 06h (90h to 9Fh).

Controls the size and location of LUT functions for the MON4 measurement.

Table 02h, Register C8h to C9h: MON5 SCALE
Table 02h, Register CAh to CBh: MON6 SCALE
Table 02h, Register CCh to CDh: MON7 SCALE
Table 02h, Register CEh to CFh: MON8 SCALE

FACTORY CALIBRATED	
READ ACCESS	PW2
WRITE ACCESS	PW2
MEMORY TYPE	Nonvolatile (SEE)

C8h, CAh, CCh, CEh	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}
C9h, CBh, CDh, CFh	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
	BIT 7							BIT 0

Controls the scaling or gain of the FS voltage measurements. The factory-calibrated value produces an FS voltage of 2.5V for MON5, MON6, MON7, and MON8.

Table 02h, Register D0h to D1h: MON5 OFFSET
Table 02h, Register D2h to D3h: MON6 OFFSET
Table 02h, Register D4h to D5h: MON7 OFFSET
Table 02h, Register D6h to D7h: MON8 OFFSET

FACTORY DEFAULT	00h
READ ACCESS	PW2
WRITE ACCESS	PW2
MEMORY TYPE	Nonvolatile (SEE)

D0h, D2h, D4h, D6h	S	S	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}
D1h, D3h, D5h, D7h	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}
	BIT 7							BIT 0

Allows for offset control of these voltage measurements if desired.

Table 02h, Register D8h to F7h: EMPTY
Table 02h, Register F8h to F9h: MAN BIAS

FACTORY DEFAULT	00h
READ ACCESS	PW2
WRITE ACCESS	PW2 and BIAS EN = 1
MEMORY TYPE	Volatile

F8h	RESERVED	RESERVED	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}
F9h	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
	BIT 7							BIT 0

When BIAS EN (Table 02h, Register 80h) is written to 0, writes to these bytes control the BIAS DAC.

Table 02h, Register FAh: MAN_CNTL

FACTORY DEFAULT	00h
READ ACCESS	PW2
WRITE ACCESS	PW2 and BIAS EN = 1
MEMORY TYPE	Volatile

FAh	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	MAN_CLK
	BIT 7							BIT 0

When BIAS EN (Table 02h, Register 80h) is written to 0, bit 0 of this byte controls the updates of the MAN BIAS value to the BIAS output. The values of MAN BIAS should be written with a separate write command. Setting bit 0 to a 1 clocks the MAN BIAS value to the output DAC.

1. Write the MAN BIAS value with a write command.
2. Set the MAN_CLK bit to a 1 with a separate write command.
3. Clear the MAN_CLK bit to a 0 with a separate write command.

Table 02h, Register FBh to FCh: BIAS DAC

FACTORY DEFAULT	8000h
READ ACCESS	PW2
WRITE ACCESS	N/A
MEMORY TYPE	Volatile

FBh	BOL	0	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}
FCh	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
	BIT 7							BIT 0

The bias open-loop bit (BOL) reflects the status of the BIAS current-control loop. If it is 1, the loop is open and the DS1875 is controlling the BIAS output from the LUT. If it is 0, the loop is closed and the BIAS output is controlled by active feedback from the BMD pin. The remaining bits are the digital value used for the BIAS output regardless of the value of OL.

Table 02h, Register FDh: BIAS OL

FACTORY DEFAULT	00h
READ ACCESS	PW2
WRITE ACCESS	PW2 and APC EN = 1
MEMORY TYPE	Volatile

FDh	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
	BIT 7							BIT 0

The digital value used for BIAS at power-on and during open loop. It is recalled from Table 08h at the adjusted memory address found in TINDEX. This register is updated at the end of the temperature conversion. The correct value depends on the value of BOLFS (Table 02h, Register 89h, bit 3).
If BOLFS = 0, BIAS OL[7:0] = I_{BIAS}[11:4].
If BOLFS = 1, BIAS OL[7:0] = I_{BIAS} [12:5].

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Table 02h, Register FEh: PWM DAC

FACTORY DEFAULT	00h
READ ACCESS	PW2
WRITE ACCESS	PW2 and PWM EN = 0
MEMORY TYPE	Volatile

FEh	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	BIT 7							BIT 0

The digital value used for PWM integration of the FB pin. It is recalled from Table 07h at the adjusted memory address found in TINDEX. This register is updated at the end of the temperature conversion.

$$V_{PWM} = \frac{1.25}{256} \times (\text{PWM DAC} + 1)$$

Table 02h, Register FFh: RESERVED

FACTORY DEFAULT	00h
READ ACCESS	PW2
WRITE ACCESS	N/A
MEMORY TYPE	N/A

This register is reserved.

Table 03h Register Descriptions

Table 03h, Register 80h to FFh: PW2 EEPROM

FACTORY DEFAULT	00h
READ ACCESS	PW2
WRITE ACCESS	PW2
MEMORY TYPE	Nonvolatile (EE)

80h to FFh	EE	EE	EE	EE	EE	EE	EE	EE
	BIT 7							BIT 0

PW2-protected EEPROM.

Table 04h Register Descriptions

Table 04h, Register 80h to C7h: MODULATION LUT

FACTORY DEFAULT	00h
READ ACCESS	PW2
WRITE ACCESS	PW2
MEMORY TYPE	Nonvolatile (EE)

80h to C7h	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	BIT 7							BIT 0

The digital value for the modulation DAC output.

The MODULATION LUT is a set of registers assigned to hold the temperature profile for the modulation DAC. The values in this table combined with the MOD bits in the MOD RANGING register (Table 02h, Register 8Bh) determine the set point for the modulation voltage. The temperature measurement is used to index the LUT (TINDEX, Table 02h, Register 81h) in 2°C increments from -40°C to +102°C, starting at 80h in Table 04h. Register 80h defines the -40°C to -38°C MOD output, Register 81h defines the -38°C to -36°C MOD output, and so on. Values recalled from this EEPROM memory table are written into the MOD DAC (Table 02h, Register 82h) location that holds the value until the next temperature conversion. The DS1875 can be placed into a manual mode (MOD EN bit, Table 02h, Register 80h), where MOD DAC is directly controlled for calibration. If the temperature compensation functionality is not required, then program the entire Table 04h, to the desired modulation setting.

Table 05h Register Descriptions

Table 05h, Register 80h to A3h: APC TE LUT

FACTORY DEFAULT	00h
READ ACCESS	PW2
WRITE ACCESS	PW2
MEMORY TYPE	Nonvolatile (EE)

80h to A3h	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	BIT 7							BIT 0

The APC TE LUT is a set of registers assigned to hold the temperature profile for the APC reference DAC. The values in this table combined with the APC bits in the COMP RANGING register (Table 02h, Register 8Dh) determine the set point for the APC loop. The temperature measurement is used to index the LUT (TINDEX, Table 02h, Register 81h) in 4°C increments from -40°C to +100°C, starting at Register 80h in Table 05h. Register 80h defines the -40°C to -36°C APC reference value, Register 81h defines the -36°C to -32°C APC reference value, and so on. Values recalled from this EEPROM memory table are written into the APC DAC (Table 02h, Register 83h) location that holds the value until the next temperature conversion. The DS1875 can be placed into a manual mode (APC EN bit, Table 02h, Register 80h), where APC DAC can be directly controlled for calibration. If TE temperature compensation is not required by the application, program the entire LUT to the desired APC set point.

Table 05h, Register A4h to A7h: RESERVED

FACTORY DEFAULT	00h
READ ACCESS	PW2
WRITE ACCESS	PW2
MEMORY TYPE	Nonvolatile (EE)

These registers are reserved.

Table 06h, Register 80h to 9Fh: M4DAC LUT

FACTORY DEFAULT	00h
READ ACCESS	PW2
WRITE ACCESS	PW2
MEMORY TYPE	Nonvolatile (EE)

80h to 9Fh	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	BIT 7							BIT 0

The M4DAC LUT is set of registers assigned to hold the voltage profile for the M4DAC. The values in this table determine the set point for the M4DAC. The MON4 voltage measurement is used to index the LUT (VINDEX, Table 02h, Register 84h), starting at Register 80h in Table 06h. Values recalled from this EEPROM memory table are written into the M4DAC (Table 02h, Register 85h) location that holds the value until the next MON4 voltage conversion. The DS1875 can be placed into a manual mode (M4DAC EN bit, Table 02h, Register 80h), where M4DAC is directly controlled for calibration. If voltage compensation is not required by the application, program the entire LUT to the desired M4DAC set point.

Table 07h Register Descriptions

Table 07h, Register 80h to A3h: PWM REFERENCE LUT

FACTORY DEFAULT	00h
READ ACCESS	PW2
WRITE ACCESS	PW2
MEMORY TYPE	Nonvolatile (EE)

80h to A3h	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	BIT 7							BIT 0

The PWM REFERENCE LUT is a set of registers assigned to hold the temperature profile for the PWM feedback. The values in this table determine the set point for the PWM loop. The temperature measurement is used to index the LUT (TINDEX, Table 02h, Register 81h) in 4°C increments from -40°C to +100°C, starting at Register 80h in Table 07h. Register 80h defines the -40°C to -36°C PWM reference value, Register 81h defines the -36°C to -32°C PWM reference value, and so on. Values recalled from this EEPROM memory table are written into the PWM DAC (Table 02h, Register FEh) location that holds the value until the next temperature conversion. The DS1875 can be placed into a manual mode (PWM EN bit, Table 02h, Register 80h), where PWM DAC can be directly controlled for calibration. If temperature compensation is not required by the application, program the entire LUT to the desired PWM set point.

Table 07h, Register A4h to A7h: RESERVED

FACTORY DEFAULT	00h
READ ACCESS	PW2
WRITE ACCESS	PW2
MEMORY TYPE	Nonvolatile (SEE)

These registers are reserved.

Table 08h Register Descriptions

Table 08h, Register 80h to C7h: BIAS OPEN-LOOP LUT

FACTORY DEFAULT	00h
READ ACCESS	All
WRITE ACCESS	All
MEMORY TYPE	Nonvolatile (EE)

80h to C7h	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	BIT 7							BIT 0

The BIAS OPEN-LOOP LUT is a set of registers assigned to hold the temperature profile for the BIAS OL DAC. The values in this table determine the set point for the BIAS current. The temperature measurement is used to index the LUT (TINDEX, Table 02h, Register 81h) in 2°C increments from -40°C to +102°C, starting at 80h in Table 08h. Register 80h defines the -40°C to -38°C BIAS OL output, Register 81h defines the -38°C to -36°C BIAS OL output, and so on. Values recalled from this EEPROM memory table are written into the BIAS OL (Table 02h, Register FDh) location that holds the value until the next temperature conversion. The DS1875 can be placed into a manual mode (BIAS EN bit, Table 02h, Register 80h), where BIAS OL DAC is directly controlled for calibration. If the temperature compensation functionality is not required, then program the entire Table 08h to the desired BIAS OL setting.

Auxiliary Memory A0h Register Descriptions

Auxiliary Memory A0h, Register 00h to FFh: EEPROM

FACTORY DEFAULT	00h
READ ACCESS	ALL
WRITE ACCESS	ALL
MEMORY TYPE	Nonvolatile (EE)

80h to FFh	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	BIT 7							BIT 0

Accessible with the slave address A0h.

Package Information

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REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/08	Initial release.	—
1	10/08	Updated all instances of the operating voltage range from 5.5V to 3.9V on multiple pages.	1, 5–13

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