DS1848

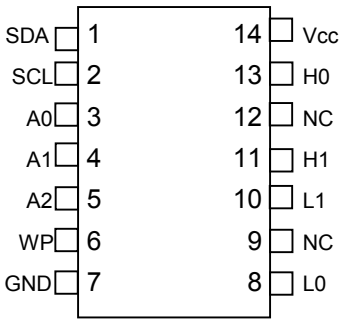
Dual Temperature-Controlled NV Variable Resistor & Memory

www.maxim-ic.com

FEATURES

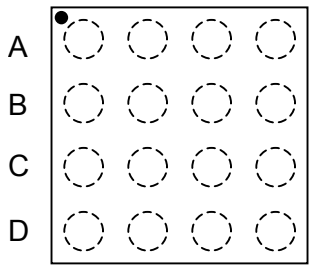
- Two linear taper, temperature-controlled variable resistors
- DS1848-050
  - One 50kΩ, 256 position
  - One 10kΩ, 256 position
- DS1848-010
  - Two 10kΩ, 256 position
- Resistor settings changeable every 2°C
- Access to temperature data and device control via a 2-wire interface
- Operates from 3V or 5V supplies
- Packaging: 14-pin TSSOP, 16-ball CSBGA
- Operating temperature: -40ºC to +95ºC
- Programming temperature: 0ºC to +70ºC
- 128 bytes of user EEPROM

PIN ASSIGNMENT



14-Pin TSSOP (173-mil)

Top View



16-Ball CSBGA (4mm x 4mm)

DESCRIPTION

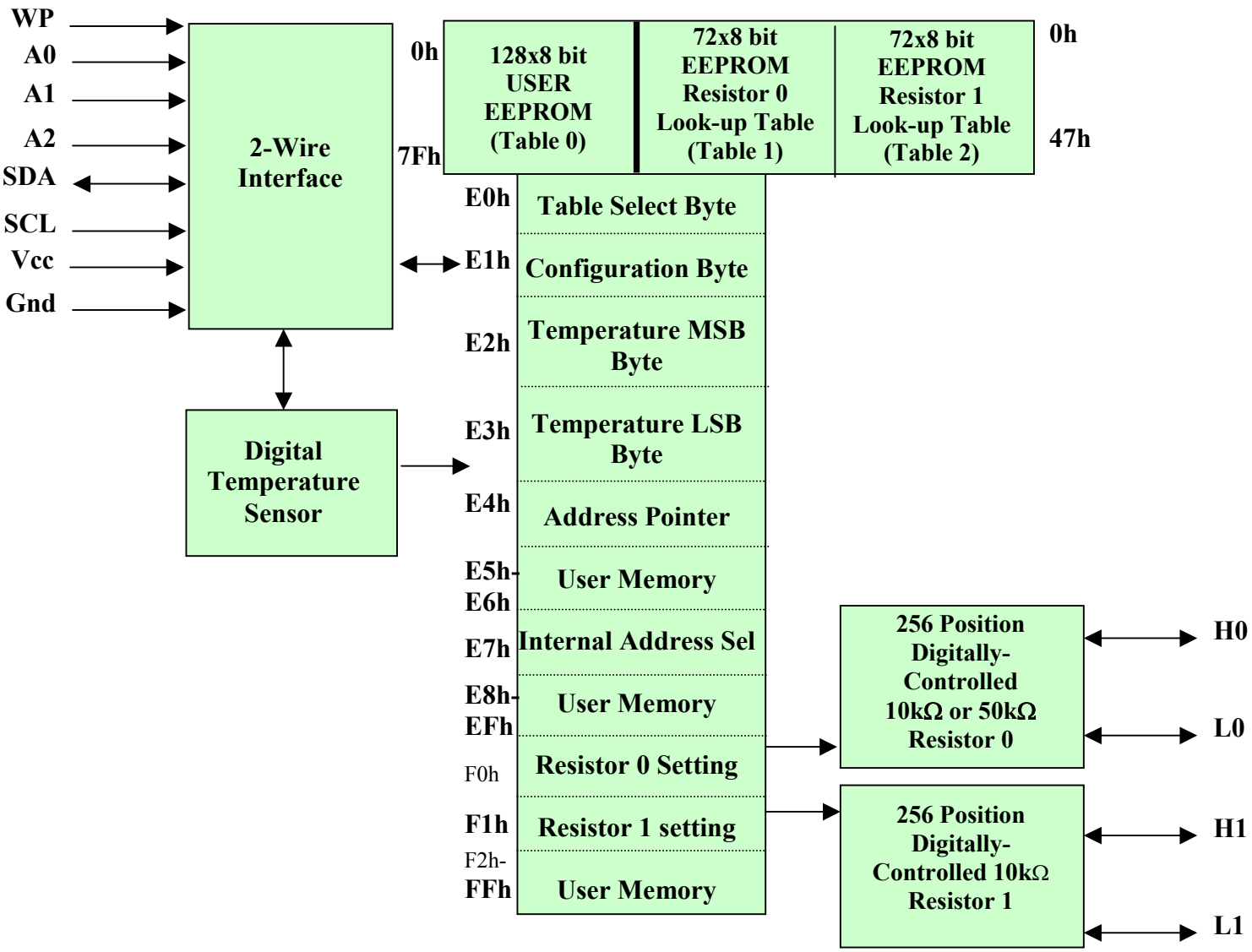
The DS1848 Dual Temperature-Controlled Nonvolatile (NV) Variable Resistor consists of two 256-position linear, variable resistors. The DS1848-050 consists of one 10kΩ and one 50kΩ, while the DS1848-010 consists of two 10kΩ resistors; both incorporate a direct-to-digital temperature sensor. The device provides an ideal method for setting and temperature-compensating bias voltages and currents in control applications using a minimum of circuitry.

The variable resistors settings are stored in EEPROM memory and can be accessed over the industry standard 2-wire serial bus. The value of each variable resistor is determined by a temperature-addressed look-up table, which can assign a unique value to each resistor for every 2°C increment over the -40°C to +95°C range. The output of the digital temperature sensor is also available as a 13-bit, 2's complement value over the serial bus. The interface I/O pins consist of SDA and SCL.

PIN DESCRIPTIONS

Name	TSSOP	BGA	Description
V_{CC}	14	A3	**Power Supply Terminal.** The DS1848 will support supply voltages ranging from +3.0V to +5.5V.
GND	7	D1	**Ground Terminal.**
SDA	1	B2	**2-Wire Serial Data Interface.** The serial data pin is for serial data transfer to and from the DS1848. The pin is open drain and may be wire-ORed with other open drain or open collector interfaces.
SCL	2	A2	**2-Wire Serial Clock Input.** The serial clock input is used to clock data into the DS1848 on rising edges and clock data out on falling edges.
WP	6	C1	**Write Protect Input.** If open or set to logic 1, all memory, control registers, and Look-up tables are write protected. If set to a logic 0, the device is not write protected and can be written to. The WP pin is pulled high internally.
A0	3	A1	**Address Input.** Pins A0, A1, and A2 are used to specify the address of each DS1848 when used in a multi-dropped configuration.
A1	4	B1	**Address Input.**
A2	5	C2	**Address Input.**
H0	13	A4	**High terminal of Resistor 0.** For both resistors, it is not required that the high terminal be connected to a potential greater than the low terminal. Voltage applied to the high terminal of each resistor cannot exceed V_{CC}, or go below ground.
H1	11	B3	**High terminal of Resistor 1.**
L0	8	D3	**Low terminal of Resistor 0.** For both resistors, it is not required that the low terminal be connected to a potential less than the high terminal. Voltage applied to the low terminal of each resistor cannot exceed V_{CC}, or go below ground.
L1	10	C4	**Low terminal of Resistor 1.**
NC	9	D4	**No Connect.**
NC	12	B4	**No Connect.**
NC		C3	**No Connect.**
NC		D2	**No Connect.**

DS1848 BLOCK DIAGRAM Figure 1



Memory Location	Name of Location	Function of Location
00h to 47h (the Table Select Byte, E0h, must be set to 01h or 02h to access the Look-Up Tables)	User Defined Look-Up Table (LUT)	This block contains the user-defined temperature settings of the resistors. Values between 00h and FFh can be written to either table to set the 256 position variable resistors. The first address location, 00h, is used to set the resistor at -40°C. Each successive memory location will contain the resistor setting for the previous temperature +2°C. For example, memory address 01h is the address that will set the resistor in a -38°C environment. For default memory settings and programming the look-up table, refer to the **Programming the Look-Up Table (LUT)** section of the datasheet.
00h to 7Fh (the Table Select Byte, E0h, must be set to 00h to access the User EEPROM Memory)	User Memory	This block is for general-purpose user memory. When shipped from the factory, memory locations 60h – 6Bh contain the same information as found in Look-Up Table 1, memory locations 28h – 33h. Memory locations 6Ch – 77h contain the same information as found in Look-Up Table 2, memory locations 28h – 33h.
E0h	Table Select Byte	Writing to this byte determines if one of the two 72x8 EEPROM look-up tables or the user EEPROM memory is selected for reading or writing. 00h (User EEPROM selected) 01h (Look-Up Table 1 selected) 02h (Look-Up Table 2 selected)
E1h	Configuration Byte	 TAU – Temperature/Address Update TEN – Temperature Update Enable AEN – Address Update Enable Default setting is 03h, TAU = 1, TEN = 1 and AEN = 1. TAU becomes a 1 after a temperature and address update has occurred as a result of a temperature conversion. The user can write this bit to 0 and check for a transition from 0 to 1 in order to verify that a conversion has occurred. If TEN = 0, the temperature conversion feature is disabled. The user sets the resistor in “manual mode” by writing to addresses F0h and F1h to control resistors 0 and 1, respectively.

Memory Location	Name of Location	Function of Location
		With AEN = 0 the user can operate in a test mode. Address updates made from the temperature sensor will cease. The user can load a memory location into E4h and verify that the values in locations F0h and F1h are the expected user-defined values.
E2h	Temperature MSB	This byte contains the MSB of the 13-bit 2s complement temperature output from the temperature sensor. S | 2^7 | 2^6 | 2^5 | 2^4 | 2^3 | 2^2 | 2^1
E3h	Temperature LSB	This byte contains the LSB of the 13-bit 2s complement temperature output from the temperature sensor. 2^0 | 2^{-1} | 2^{-2} | 2^{-3} | 2^{-4} | X | X | X For example temperature readings, refer to Table 2.
E4h	Address Pointer	Calculated, current resistor address (0h – 47h). The user-defined resistor setting at this location in the respective look-up table will be loaded into F0h and F1h to set the two resistors.
E5h to E6h	User Memory	General purpose user memory (SRAM)
E7h	Address Select	Internal or external device address select. This byte allows the user to use the external address pins or an internal register location to determine the device address. | A2 | A1 | A0 | $\overline{\text{ENB}}$ | ENB = 0 and external A2, A1, A0 grounded, device will use internal address bits (A2, A1, A0) in this register ENB = 1, external A2, A1, A0 = any setting, device will use external address pins Default setting is 01h. The device uses external pins to determine its address.
E8h to EFh	User Memory	General purpose user memory (SRAM)
F0h	Resistor 0 Setting	In the user-controlled setting mode, this block contains the resistor 0 setting.
F1h	Resistor 1 Setting	In the user-controlled setting mode, this block contains the resistor 1 setting.
F2h to FFh	User memory	General purpose user memory (SRAM)

PROGRAMMING THE LOOK-UP TABLE (LUT)

The following equation can be used to determine which resistor position setting, 00h – FFh, should be written in the LUT to achieve a given resistance at a specific temperature.

$$pos(\alpha, R, C) = \frac{R - u \bullet \left[1 + v \bullet (C - 25) + w \bullet (C - 25)^2\right]}{(x) \bullet \left[1 + y \bullet (C - 25) + z \bullet (C - 25)^2\right]} - \alpha$$

DS1848-050
α = 3.78964 for the 50kΩ resistor
α = 19.74866 for the 10kΩ resistor

DS1848-010
α = 8.394533 for both 10kΩ resistors

R = resistance desired at the output terminal
C = temperature in degrees Celsius
u, v, w, x, y, and z are calibration constants programmed into each of the corresponding look-up tables. Their addresses and LSB values are given in Table 1 below. Resistor 1 variables are found in Look-Up table 1 of the EEPROM, and Resistor 2 variables are found in Look-Up Table 2. After these values are read, they should be overwritten with the appropriate temperature specific resistance settings. Copies of these values can also be found in the User EEPROM memory.

LOOK-UP VARIABLE ADDRESSES Table1

Address in LUT (HEX)	Variable	LSB
28 – 29	u	2^{-8}
2A – 2B	v	10^{-6}
2C – 2D	w	10^{-9}
2E – 2F	x	2^{-8}
30 – 31	y	10^{-7}
32 – 33	z	10^{-10}

When shipped from the factory, all other memory locations in the LUTs are programmed to FFh (except bytes 00h-07h of Table 1 and 2 which may be factory programmed to values other than FFh).

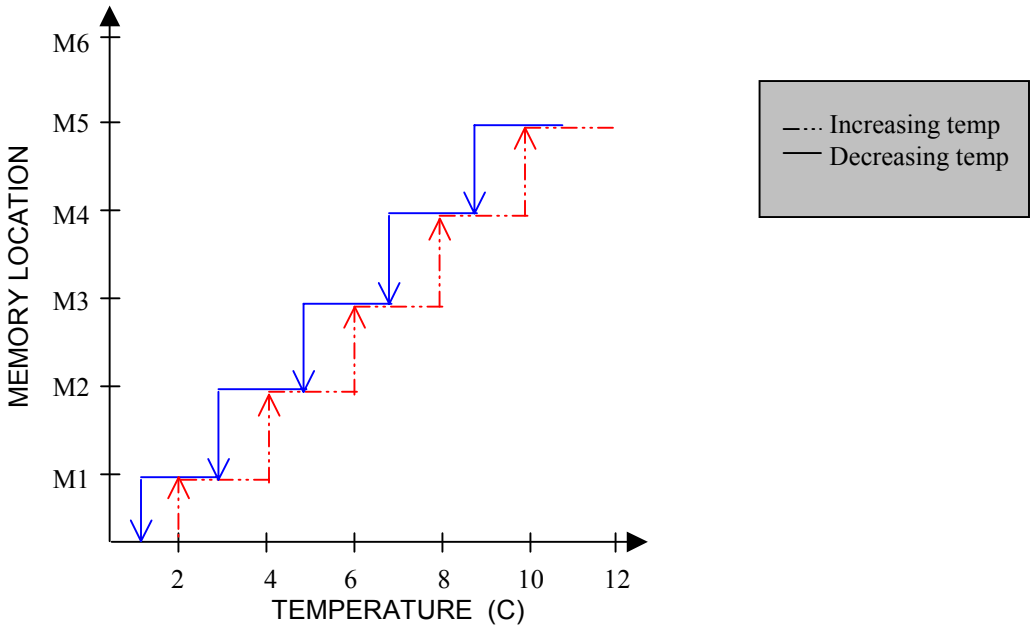
Note: Memory locations 44h – 47h, which cover the temperature range (+96ºC to +102ºC), are outside of the specified operating temperature range (-40ºC to +95ºC). However, the values stored in these locations will act as valid resistance settings if the temperature exceeds +95ºC. Therefore, Dallas Semiconductor recommends that the user program a resistance value into all LUT locations. Failure to do so will result in the part being set to the default value.

TEMPERATURE CONVERSION

The direct-to-digital temperature sensor measures temperature through the use of an on-chip temperature measurement technique with an operating range from -40°C to +95°C. Temperature conversions are initiated upon power-up, and the most recent result is stored in address locations E2h and E3h, which are updated every 10ms. Temperature conversion will not occur during an active read or write to memory.

The value of each resistor is determined by the temperature-addressed look-up table that assigns a unique value to each resistor for every 2°C increment with a 1°C hysteresis at a temperature transition over the operating temperature range. This can be seen in Figure 2.

TEMPERATURE CONVERSION HYSTERESIS Figure 2



EXAMPLE TEMPERATURE READINGS Table 2

TEMP	BINARY DATA	HEX DATA
+95ºC	0010 1111 1000 0000	2F80h
+25.0625ºC	0000 1100 1000 1000	0C88h
-10.125ºC	1111 1010 1111 0000	FAF0h
-40ºC	1110 1100 0000 0000	EC00h

2-WIRE OPERATION

Clock and Data Transitions: The SDA pin is normally pulled high with an external resistor or device. Data on the SDA pin may only change during SCL low time periods. Data changes during SCL high periods will indicate a start or stop conditions depending on the conditions discussed below. Refer to the timing diagram (Figure 4) for further details.

Start Condition: A high-to-low transition of SDA with SCL high is a start condition that must precede any other command. Refer to the timing diagram (Figure 4) for further details.

Stop Condition: A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command places the DS1848 into a low-power mode. Refer to the timing diagram (Figure 4) for further details.

Acknowledge: All address and data byte are transmitted via a serial protocol. The DS1848 pulls the SDA line low during the ninth clock pulse to acknowledge that it has received each word.

Standby Mode: The DS1848 features a low-power mode that is automatically enabled after power-on, after a stop command, and after the completion of all internal operations.

2-Wire Interface Reset: After any interruption in protocol, power loss, or system reset, the following steps reset the DS1848.

1. Clock up to nine cycles.
2. Look for SDA high in each cycle while SCL is high.
3. Create a START condition while SDA is high.

Device Addressing: The DS1848 must receive an 8-bit device address word following a START condition to enable a specific device for a read or write operation. The address word is clocked into the DS1848 MSB to LSB. The address word consists of Ah (10106) followed by A2, A1, and A0 then the R/W bit. If the R/W bit is high, a read operation is initiated. If the R/W is low, a write operation is initiated. For a device to become active, the values of A2, A1 and A0 must be the same as the hard-wired address pins on the DS1848. Upon a match of written and hard-wired addresses, the DS1848 will output a zero for one clock cycle as an acknowledge. If the address does not match, the DS1848 returns to a low-power mode.

Write Operations: After receiving a matching address byte with the R/W bit set low, the device goes into the write mode of operation. The master must transmit an 8-bit EEPROM memory address to the device to define the address where the data is to be written. After byte has been received, the DS1848 will transmit a zero for one clock cycle to acknowledge the receipt of the address. The master must then transmit an 8-bit data word to be written into this address. The DS1848 will again transmit a zero for one clock cycle to acknowledge the receipt of the data. At this point, the master must terminate the write operation with a STOP condition. The DS1848 then enters an internally timed write process t_w to the EEPROM memory. All inputs are disabled during this byte write cycle.

The DS1848 is capable of an 8-byte page write. A page write is initiated the same way as a byte write, but the master does not send a STOP condition after the first byte. Instead, after the slave acknowledges receipt of the data byte, the master can send up to seven more bytes using the same nine-clock sequence.

The master must terminate the write cycle with a STOP condition or the data clocked into the DS1848 will not be latched into permanent memory.

Acknowledge Polling: Once the internally-timed write has started and the DS1848 inputs are disabled, acknowledge polling can be initiated. The process involves transmitting a START condition followed by the device address. The R/W bit signifies the type of operation that is desired. The read or write sequence will only be allowed to proceed if the internal write cycle has completed and the DS1848 responds with a zero.

Read Operations: After receiving a matching address byte with the R/W bit set high, the device goes into the read mode of operation. There are three read operations: current address read, random read, and sequential address read.

CURRENT ADDRESS READ

The DS1848 has an internal address register that maintains the address used during the last read or write operation, incremented by one. This data is maintained as long as V_{CC} is valid. If the most recent address was the last byte in memory, then the register resets to the first address. This address stays valid between operations as long as power is available.

Once the device address is clocked in and acknowledged by the DS1848 with the R/W bit set to high, the current address data word is clocked out. The master does not respond with a zero, but does generate a STOP condition afterwards.

RANDOM READ

A random read requires a dummy byte write sequence to load in the data word address. Once the device and data address bytes are clocked in by the master and acknowledged by the DS1848, the master must generate another START condition. The master now initiates a current address read by sending the device address with the read/write bit set high. The DS1848 will acknowledge the device address and serially clocks out the data byte.

SEQUENTIAL ADDRESS READ

Sequential reads are initiated by either a current address read or a random address read. After the master receives the first data byte, the master responds with an acknowledge. As long as the DS1848 receives this acknowledge after a byte is read, the master may clock out additional data words from the DS1848. After reaching address FFh, it resets to address 00h.

The sequential read operation is terminated when the master initiates a stop condition. The master does not respond with a zero.

For a more detailed description of 2-wire theory of operation, refer to the next section.

2-WIRE SERIAL PORT OPERATION

The 2-wire serial port interface supports a bi-directional data transmission protocol with device addressing. A device that sends data on the bus is defined as a transmitter, and a device receiving data as a receiver. The device that controls the message is called a "master." The devices that are controlled by the master are "slaves." The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions. The DS1848 operates as a slave on the 2-wire bus. Connections to the bus are made via the open-drain I/O lines SDA and SCL. The following I/O terminals control the 2-wire serial port: SDA, SCL, A0, A1, A2. Timing diagrams for the 2-wire serial port can be found in Figures 3 and 4. Timing information for the 2-wire serial port is provided in the AC Electrical Characteristics Table for 2-wire serial communications.

The following bus protocol has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus not busy: Both data and clock lines remain HIGH.

Start data transfer: A change in the state of the data line from HIGH to LOW while the clock is HIGH defines a START condition.

Stop data transfer: A change in the state of the data line from LOW to HIGH while the clock line is HIGH defines the STOP condition.

Data valid: The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line can be changed during the LOW period of the clock signal. There is one clock pulse per bit of data. Figures 3 and 4 detail how data transfer is accomplished on the two-wire bus. Depending upon the state of the R/W bit, two types of data transfer are possible.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions is not limited and is determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth bit.

Within the bus specifications a regular mode (100kHz clock rate) and a fast mode (400kHz clock rate) are defined. The DS1848 works in both modes.

Acknowledge: Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse that is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is a stable LOW during the HIGH period of the acknowledge-related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the

slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

1. Data transfer from a master transmitter to a slave receiver. The first byte transmitted by the master is the command/control byte. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte.

2. Data transfer from a slave transmitter to a master receiver. The master transmits the first byte (the command/control byte) to the slave. The slave then returns an acknowledge bit. Next follows a number of data bytes transmitted by the slave to the master. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a 'not acknowledge' can be returned.

The master device generates all serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus will not be released.

The DS1848 may operate in the following two modes:

1. Slave receiver mode: Serial data and clock are received through SDA and SCL respectively. After each byte is received, an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave (device) address and direction bit.

2. Slave transmitter mode: The first byte is received and handled as in the slave receiver mode. However, in this mode the direction bit will indicate that the transfer direction is reversed. Serial data is transmitted on SDA by the DS1848, while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer.

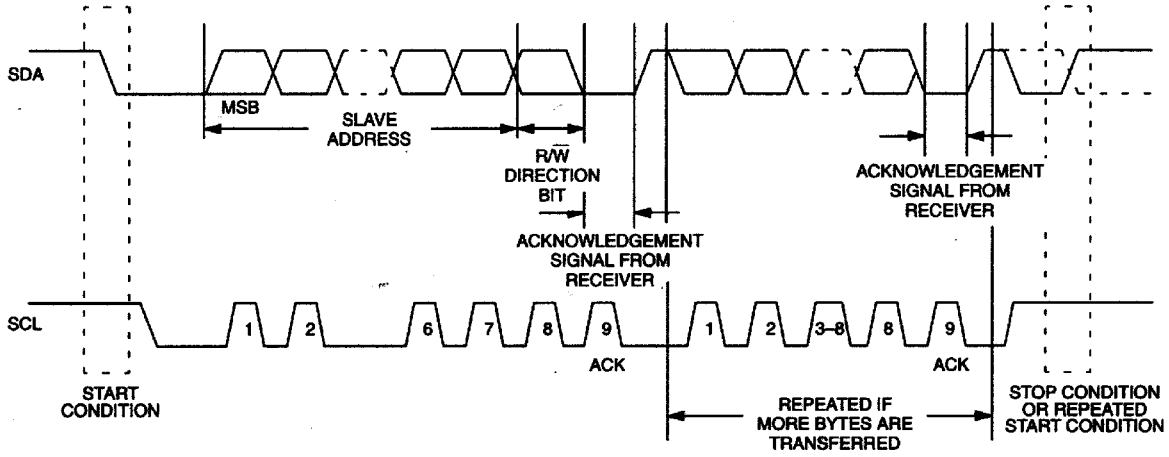
3. Slave Address: Command/control byte is the first byte received following the START condition from the master device. The command/control byte consists of a 4-bit control code. For the DS1848, this is set as *1010* binary for read/write operations. The next 3 bits of the command/ control byte are the device select bits or slave address (A2, A1, A0). They are used by the master device to select which of eight devices is to be accessed. When reading or writing the DS1848, the device-select bits must match the device-select pins (A2, A1, A0). The last bit of the command/control byte (R/W) defines the operation to be performed. When set to a 1, a read operation is selected, and when set to a 0, a write operation is selected.

Following the START condition, the DS1848 monitors the SDA bus checking the device type identifier being transmitted. Upon receiving the *1010* control code, the appropriate device address bits, and the read/write bit, the slave device outputs an acknowledge signal on the SDA line.

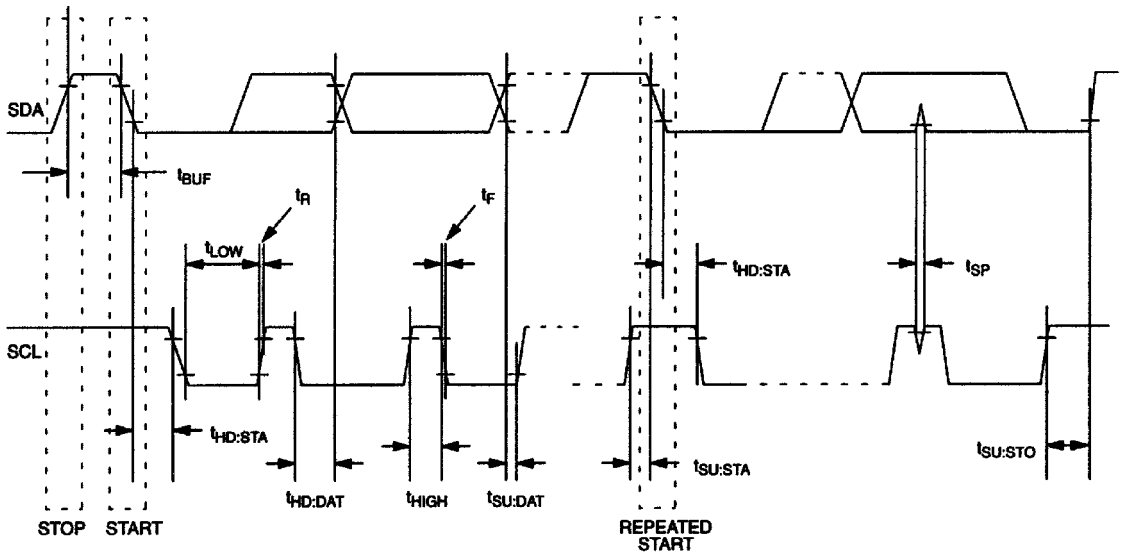
WRITE PROTECT

The write-protect input pin (WP) protects all memory (including EEPROM), control registers, and look-up tables from alteration in an application. However, this does not interfere with internal temperature/resistor updates. If set to a logic 0, the device is not write protected and can be written to via the 2-wire interface. This pin has an internal pull-up resistor.

2-WIRE DATA TRANSFER PROTOCOL Figure 3



2-WIRE AC CHARACTERISTICS Figure 4



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-0.3V to +6.0V
Operating Temperature	-40°C to +95°C
Programming Temperature	0°C to +70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	See J-STD-020A specification

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (-40°C to +95°C)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	Vcc		+3.0		5.5	V	1
Resistor Inputs	L0, L1, H0, H1		GND-0.3		V_{CC}+0.3	V	
Resistor Current	$I_{RESISTOR}$	DS1848-050 DS1848-010	-1 -3		1 3	mA	

DC ELECTRICAL CHARACTERISTICS (-40°C to +95°C; V_{CC} = 3.0V to 5.5V)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{CC}			0.5	1	mA	2
Input Leakage (digital inputs)	I_L		-1		+1	µA	
Input Leakage (H0, H1, L0, and L1)	I_L		-100		+100	nA	
Input Logic 1	V_{IH}		$0.7V_{CC}$		V_{CC}+0.3	V	15
Input Logic 0	V_{IL}		GND-0.3		$0.3V_{CC}$	V	
Input Current each I/O pin		$0.4<V_{I/O}<0.9V_{CC}$	-10		+10	µA	13
Low Level Output Voltage (SDA)	V_{OL1}	3mA sink current	0.0		0.4	V	
	V_{OL2}	6mA sink current	0.0		0.6	V	
I/O Capacitance	$C_{I/O}$				10	pF	
WP Internal Pull Up Resistance, R_{wp}	R_{wp}		40	65	100	kΩ	

ANALOG RESISTOR CHARACTERISTICS (-40°C to +95°C; V_{CC}=3.0V to 5.5V)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Absolute Error		using cal. values	-4		+4	LSB	14
Position FFh Resistance DS1848-050 DS1848-050 DS1848-010		 (50k resistor) (10k resistor) (10k resistor)	 44.6 9.0 8.0	 55.8 11.3 10.0	 67.0 13.6 12.0	kΩ	3
Position 00h Resistance DS1848-050 DS1848-050 DS1848-010		 (50k resistor) (10k resistor) (10k resistor)	 500 500 250	 850 850 425	 1200 1200 600	Ω	3
Absolute Linearity			-2		+2	LSB	4
Relative Linearity			-1		+1	LSB	5
Compensated Tempco Error		using calibration values	-4		+4	LSB	14
Uncompensated Tempco				850		ppm/°C	12

DIGITAL THERMOMETER

PARAMETER	SYMBOL	CONDITION	TYP	MAX	UNITS	NOTES
Thermometer Error	T_{ERR}	-40°C to 95°C		±3.0	°C	
Conversion Time	t_{CONVT}	12-bit conversion		10	ms	

AC ELECTRICAL CHARACTERISTICS (-40°C to +95°C, V_{CC} = 3.0V to 5.5V)

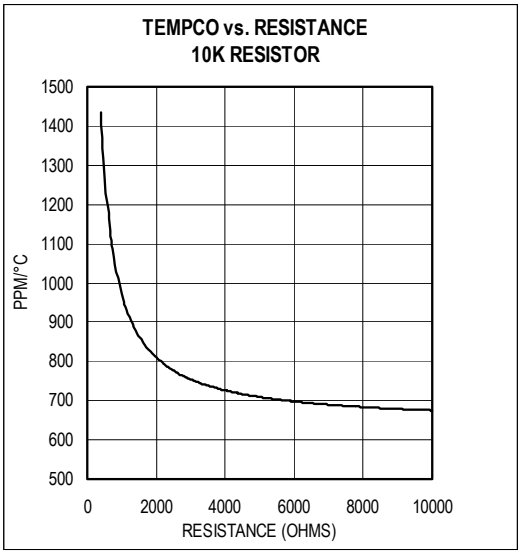
PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
SCL clock frequency	f_{SCL}	Fast Mode Standard Mode	0 0		400 100	kHz	6
Bus free time between STOP and START	t_{BUF}	Fast Mode Standard Mode	1.3 4.7			µs	6
Hold time (repeated) START condition	$t_{HD:STA}$	Fast Mode Standard Mode	0.6 4.0			µs	7,6
Low period of SCL clock	t_{LOW}	Fast Mode Standard Mode	1.3 4.7			µs	6
High period of SCL clock	t_{HIGH}	Fast Mode Standard Mode	0.6 4.0			µs	6
Data hold time	$t_{HD:DAT}$	Fast Mode Standard Mode	0 0		0.9	µs	6,8,9
Data set-up time	$t_{SU:DAT}$	Fast Mode Standard Mode	100 250			ns	6
Start set-up time	$t_{SU:STA}$	Fast Mode Standard Mode	0.6 4.7			µs	6
Rise time of both SDA and SCL signals	t_R	Fast Mode Standard Mode	$20+0.1C_B$		300 1000	ns	10
Fall time of both SDA and SCL signals	t_F	Fast Mode Standard Mode	$20+0.1C_B$		300 300	ns	10
Set-up time for STOP condition	$t_{SU:STO}$	Fast Mode Standard Mode	0.6 4.0			µs	
Capacitive load for each bus line	C_B				400	pF	10
EEPROM write time	t_W			5	20	ms	11

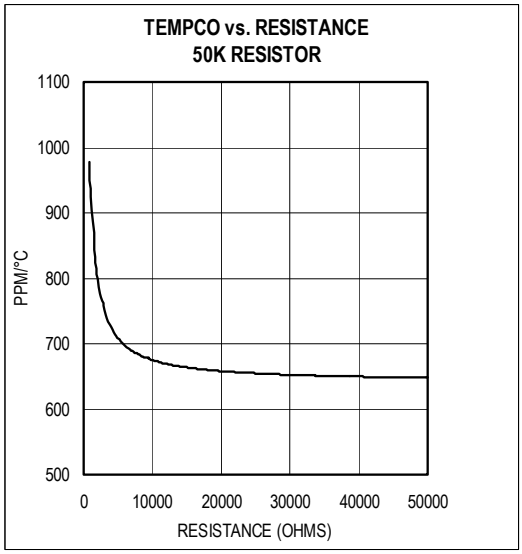
NONVOLATILE MEMORY CHARACTERISTICS

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Writes		85°C	50,000			

NOTES:

1) All voltages are referenced to ground.
2) Inputs SDA = SCL = WP = Vcc. A0, A1, and A2 must be tied to V_{CC} or GND.
3) Valid at 25°C only.
4) Absolute linearity is the difference of measured value from expected value at DAC position. Expected value is a straight line from measured minimum position to measured maximum position.
5) Relative linearity the deviation of an LSB DAC setting change vs. the expected LSB change. Expected LSB change is the slope of the straight line from measured minimum position to measured maximum position.
6) A fast mode device can be used in a standard mode system, but the requirement $t_{SU:DAT} > 250ns$ must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{RMAX} + t_{SU:DAT} = 1000ns + 250ns = 1250ns$ before the SCL line is released.
7) After this period, the first clock pulse is generated.
8) The maximum $t_{HD:DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
9) A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the $VI_{H\ MIN}$ of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.
10) C_B — total capacitance of one bus line in picofarads, timing referenced to $0.9V_{CC}$ and $0.1V_{CC}$.
11) EEPROM write begins after a stop condition occurs.
12) The temperature coefficient varies with resistor position from 650ppm/°C at position FFh to 1000ppm/°C at 00h (for the 50k resistor), or 1500ppm/°C at 00h (for the 10k resistor). See the graphs below. The tempco can be significantly reduced by using the resistor calibration values. When doing so, the average tempco over the entire temperature range is between 200ppm/°C (for the lower positions) and 10ppm/°C (higher positions). Refer to the *Programming the Look-Up Table* section of the data sheet.
13) I/O pins of fast mode devices must not obstruct the SDA and SCL lines if V_{CC} is switched off.
14) Refer to *Programming the Look-Up Table* section of the data sheet for calibration.
15) Address input A1 passes Latch-up per JEDEC 78 class I. All other pins pass class II.





ORDERING INFORMATION

ORDERING	PACKAGE	OPERATING	VERSION

NUMBER		TEMPERATURE	Resistor 0 /Resistor 1
DS1848E-010	14-PIN TSSOP (173-MIL)	-40ºC TO +95ºC	10kΩ/10kΩ
DS1848E-050	14-PIN TSSOP (173-MIL)	-40ºC TO +95ºC	50kΩ/10kΩ
DS1848E-010/T&R	14-PIN TSSOP/TAPE & REEL	-40ºC TO +95ºC	10kΩ/10kΩ
DS1848E-050/T&R	14-PIN TSSOP/TAPE & REEL	-40ºC TO +95ºC	50kΩ/10kΩ
DS1848B-010	16-BALL CSBGA	-40ºC TO +95ºC	10kΩ/10kΩ
DS1848B-050	16-BALL CSBGA	-40ºC TO +95ºC	50kΩ/10kΩ
DS1848B-010+	16-BALL CSBGA LF	-40ºC TO +95ºC	10kΩ/10kΩ
DS1848B-010+T&R	16-BALL CSBGA LF T&R	-40ºC TO +95ºC	10kΩ/10kΩ
DS1848B-010/T&R	16-BALL CSBGA T&R	-40ºC TO +95ºC	10kΩ/10kΩ
DS1848B-050+	16-BALL CSBGA LF	-40ºC TO +95ºC	50kΩ/10kΩ
DS1848B-050+T&R	16-BALL CSBGA LF T&R	-40ºC TO +95ºC	50kΩ/10kΩ
DS1848B-050/T&R	16-BALL CSBGA T&R	-40ºC TO +95ºC	50kΩ/10kΩ
DS1848E-010+	14-PIN TSSOP (173-MIL)	-40ºC TO +95ºC	10kΩ/10kΩ
DS1848E-010+T&R	14-PIN TSSOP LF T&R	-40ºC TO +95ºC	10kΩ/10kΩ
DS1848E-050+	14-PIN TSSOP (173-MIL)	-40ºC TO +95ºC	50kΩ/10kΩ
DS1848E-050+T&R	14-PIN TSSOP LF T&R	-40ºC TO +95ºC	50kΩ/10kΩ

+ Denotes lead-free package.