Rev 1; 9/06

Addressable Digital Potentiometer

DS1805

General Description

The DS1805 addressable digital potentiometer contains a single 256-position digitally controlled potentiometer. Device control is achieved through a 2-wire serial interface. Device addressing is provided through three address inputs that allow up to eight devices on a single 2-wire bus. The exact wiper position of the potentiometer can be written or read. The DS1805 is available in 16-pin SO and 14-pin TSSOP packages. The device is available in three standard resistance values: 10kΩ, 50kΩ, and 100kΩ. The DS1805 is specified over the industrial temperature range. The DS1805 provides a low-cost alternative for designs based on the DS1803, but require only a single potentiometer.

Applications

CCFL Inverters

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Portable Electronics

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Instrumentation and Industrial Controls

Features

- **3V or 5V Operation**
- **Low Power Consumption**
- **One Digitally Controlled, 256-Position Potentiometer**
- **Compatible with DS1803-Based Designs**
- **14-Pin TSSOP (173mil) and 16-Pin SO (150mil) Available for Surface-Mount Applications**
- **Three Address Inputs**
- **Serial 2-Wire Bus**
- **Operating Temperature Range**

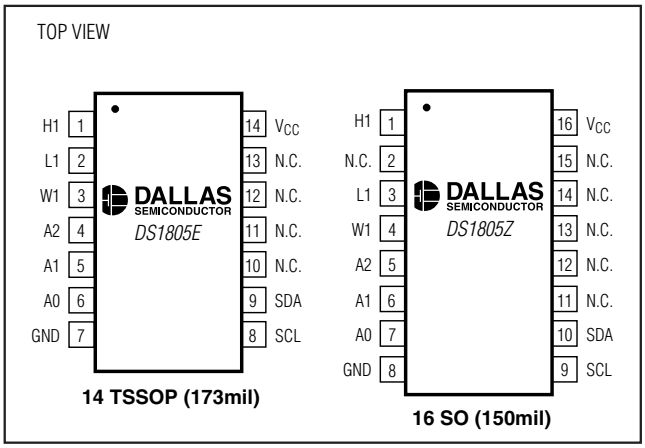
  Industrial: -40°C to +85°C
- **Standard Resistance Values**

  DS1805-010: 10kΩ

  DS1805-050*: 50kΩ

  DS1805-100*: 100kΩ

Pin Configurations



Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	RESISTANCE (KΩ)
DS1805E-010	-40°C to +85°C	14 TSSOP (173mil)	10
DS1805E-050*	-40°C to +85°C	14 TSSOP (173mil)	50
DS1805E-100*	-40°C to +85°C	14 TSSOP (173mil)	100
DS1805Z-010	-40°C to +85°C	16 SO (150mil)	10
DS1805Z-050*	-40°C to +85°C	16 SO (150mil)	50
DS1805Z-100*	-40°C to +85°C	16 SO (150mil)	100

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ABSOLUTE MAXIMUM RATINGS

Voltage on Any Pin Relative to Ground .....-0.5V to +6.0V
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-55°C to +125°C
Soldering Temperature.....See IPC/JEDEC J-STD-020A Specification

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A = -40°C to +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}	(Note 1)	2.7		5.5	V
Resistor Inputs	L, H, W	(Note 1)	-0.3		V_{CC} + 0.3	V

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.7V to 5.5V, T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current Active	I_{CC}	(Note 2)			200	µA
Input Leakage	I_{IL}		-1		+1	µA
Wiper Resistance	R_W			400	1000	Ω
Wiper Current	I_W				1	mA
Input Logic 1	V_{IH}		0.7V_{CC}		V_{CC} + 0.3	V
Input Logic 0	V_{IL}		GND - 0.3		0.3V_{CC}	V
Input Logic Levels A0, A1, A2 (Note 3)		Input logic 1	0.7V_{CC}		V_{CC} + 0.3	V
		Input logic 0	GND - 0.3		0.25V_{CC}	
Input Current each I/O Pin (Note 4)		0.4V < $V_{I/O}$ < 0.9V_{CC}	-10		+10	µA
Standby Current	I_{STBY}	(Note 5)		20	40	µA
Low-Level Output Voltage	V_{OL1}	3mA sink current	0		0.4	V
	V_{OL2}	6mA sink current	0		0.6	V
I/O Capacitance	$C_{I/O}$				10	pF
Pulse Width of Spikes that Must be Suppressed by the Input Filter	t_{SP}	Fast mode	0		50	ns

ANALOG RESISTOR CHARACTERISTICS

(V_{CC} = 2.7V to 5.5V, T_A = -40°C to +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
End-to-End Resistor Tolerance		(Note 6)	-20		+20	%
Absolute Linearity		(Note 7)	-0.75		+0.75	LSB
Relative Linearity		(Note 8)	-0.3		+0.3	LSB
-3dB Cutoff Frequency	f_{CUTOFF}	(Note 9)				Hz
Ratiometric Temperature Coefficient				8		ppm/°C
End-to-End Temperature Coefficient				550		ppm/°C
Capacitance	C_I				5	pF

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.7V to 5.5V, T_A = -40°C to +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency (Note 10)	f_{SCL}	Fast mode	0		400	kHz
		Standard mode	0		100	
Bus Free Time Between STOP and START Condition (Note 10)	t_{BUF}	Fast mode	1.3			µs
		Standard mode	4.7			
Hold Time (Repeated) START Condition (Notes 10, 11)	$t_{HD:STA}$	Fast mode	0.6			µs
		Standard mode	4.0			
Low Period of SCL Clock (Note 10)	t_{LOW}	Fast mode	1.3			µs
		Standard mode	4.7			
High Period of SCL Clock (Note 10)	t_{HIGH}	Fast mode	0.6			µs
		Standard mode	4.0			
Data Hold Time (Notes 10, 12, 13)	$t_{HD:DAT}$	Fast mode	0		0.9	µs
		Standard mode	0		0.9	
Data Setup Time (Note 10)	$t_{SU:DAT}$	Fast mode	100			ns
		Standard mode	250			
Rise Time of Both SDA and SCL Signals (Notes 10, 14)	t_R	Fast mode	$20 + 0.1C_B$		300	ns
		Standard mode	$20 + 0.1C_B$		1000	
Fall Time of Both SDA and SCL Signals (Notes 10, 14)	t_F	Fast mode	$20 + 0.1C_B$		300	ns
		Standard mode	$20 + 0.1C_B$		300	
Setup Time for STOP Condition (Note 10)	$t_{SU:STO}$	Fast mode	0.6			µs
		Standard mode	4.0			
Capacitive Load for Each Bus Line (Note 14)	C_B				400	pF

AC ELECTRICAL CHARACTERISTICS

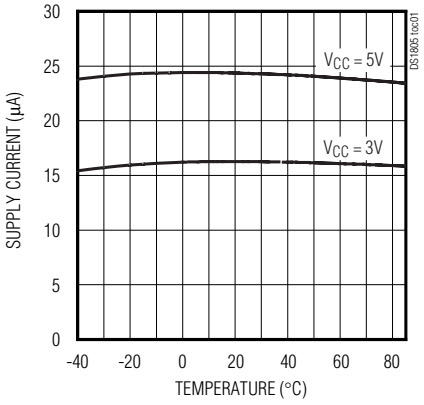
(V_{CC} = 2.7V to 5.5V, T_A = -40°C to +85°C)

Note 1: All voltages are referenced to ground.
Note 2: I_{CC} specified with SDA pin open. SCL = 400kHz clock rate.
Note 3: Address inputs A0, A1, and A2 should be connected to either V_{CC} or GND, depending on the desired address selections.
Note 4: I/O pins of fast mode devices must not obstruct the SDA and SCL lines if V_{CC} is switched off.
Note 5: I_{STBY} specified with SDA = SCL = V_{CC} = 5.0V.
Note 6: Valid at +25°C only.
Note 7: Absolute linearity is used to determine wiper voltage versus expected voltage as determined by wiper position.
Note 8: Relative linearity is used to determine the change in voltage between successive tap positions.
Note 9: -3dB cutoff frequency characteristics for the DS1805 depend on potentiometer total resistance: DS1805-010, 1MHz; DS1805-50, 200kHz; DS1805-100, 100kHz.
Note 10: A fast mode device can be used in a standard mode system, but the requirement $t_{SU:DAT}$ > 250ns must then be met. This will automatically be the case if the device does not stretch the low period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{RMAX} + t_{SU:DAT}$ = 1000ns + 250ns = 1250ns before the SCL line is released.
Note 11: After this period, the first clock pulse is generated.
Note 12: The maximum $t_{HD:DAT}$ has only to be met if the device does not stretch the low period (t_{LOW}) of the SCL signal.
Note 13: A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the V_{IHMIN} of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.
Note 14: C_B—total capacitance of one bus line in picofarads, timing referenced to (0.9)(V_{CC}) and (0.1)(V_{CC}).

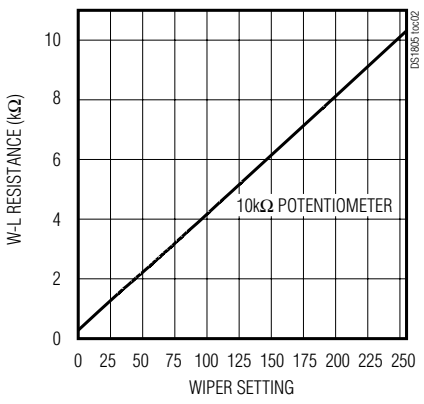
Typical Operating Characteristics

(V_{CC} = 5.0V, T_A = +25°C, unless otherwise noted.)

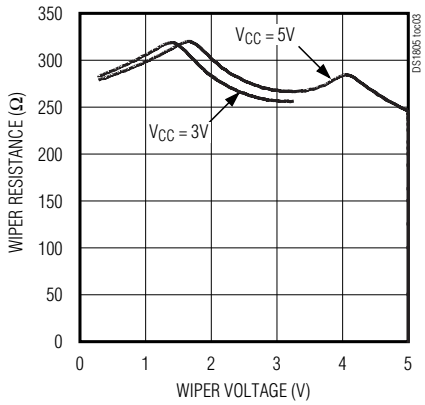
SUPPLY CURRENT vs. TEMPERATURE



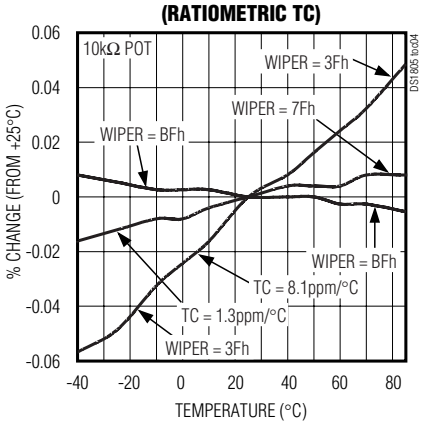
W-L RESISTANCE vs. WIPER SETTING



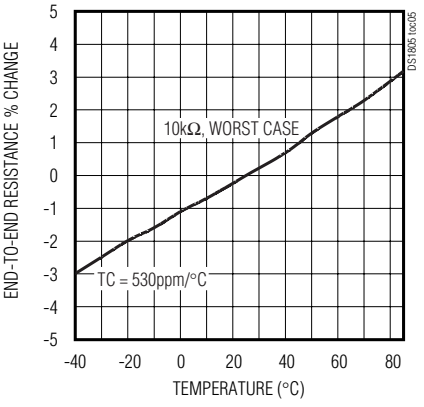
WIPER RESISTANCE vs. WIPER VOLTAGE (10kΩ)



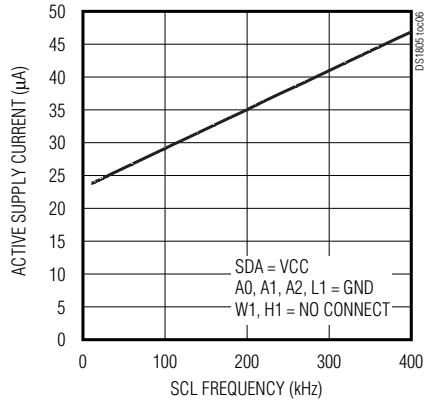
VOLTAGE DIVIDER PERCENT CHANGE (FROM +25°C) vs. TEMPERATURE (RATIOMETRIC TC)



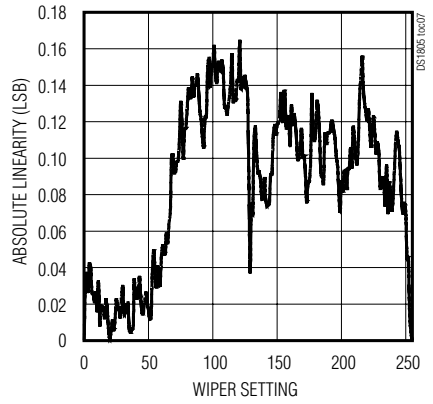
END-TO-END RESISTANCE TEMPERATURE CHANGE vs. TEMPERATURE



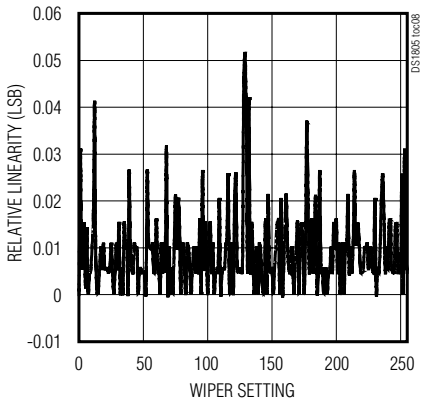
ACTIVE SUPPLY CURRENT vs. SCL FREQUENCY



VOLTAGE-DIVIDER ABSOLUTE LINEARITY vs. WIPER SETTING (10kΩ)



VOLTAGE-DIVIDER RELATIVE LINEARITY vs. WIPER SETTING (10kΩ)



Addressable Digital Potentiometer

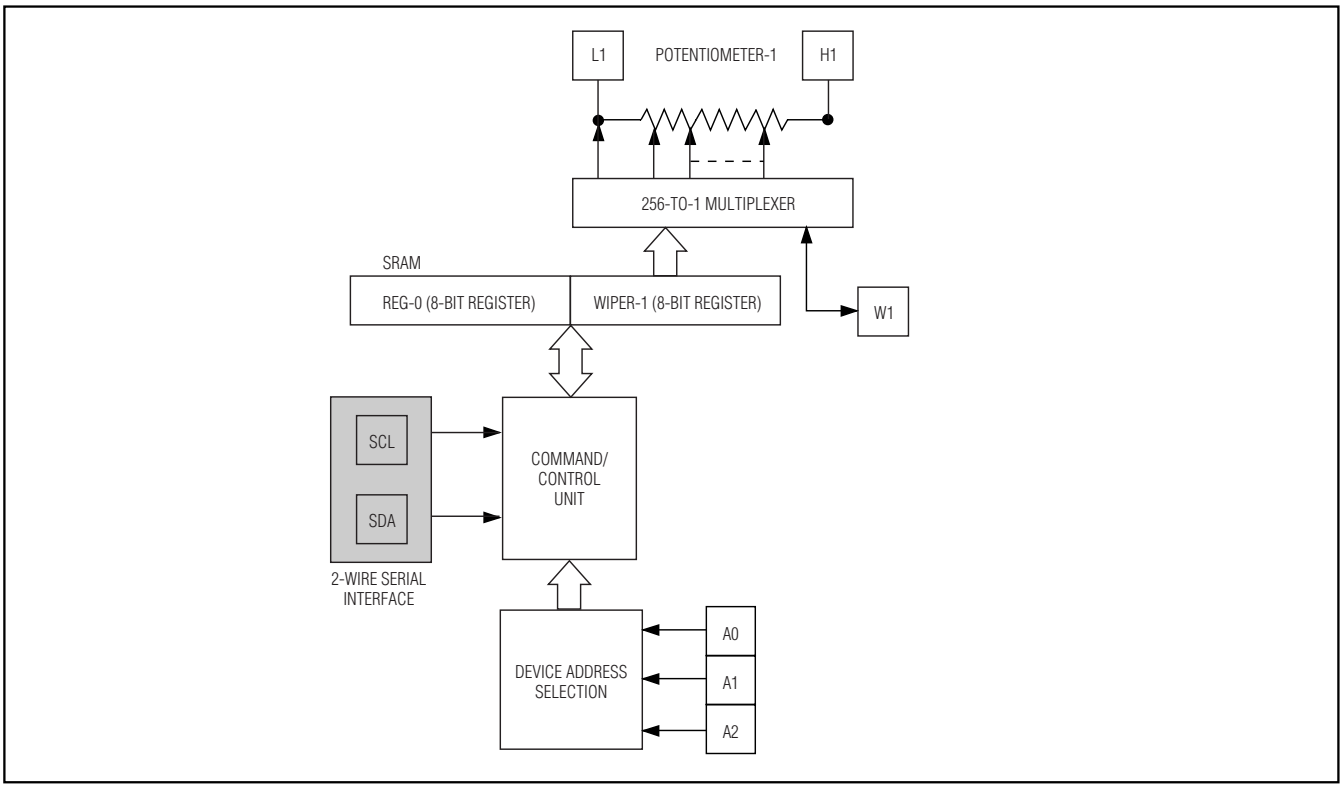


Figure 1. Functional Diagram

Pin Description

PIN		NAME	FUNCTION
TSSOP	SO		
1	1	H1	High End of Potentiometer
2	3	L1	Low End of Potentiometer
3	4	W1	Wiper Terminal of Potentiometer
6, 5, 4	7, 6, 5	A0, A1, A2	Address Select Inputs
7	8	GND	Ground
8	9	SCL	Serial Clock Input
9	10	SDA	Serial Data I/O
10–13	2, 11–15	N.C.	No Connection
14	16	V_{CC}	3V/5V Power-Supply Input

Detailed Description

The DS1805 addressable digital potentiometer contains a single 256-position digitally controlled potentiometer. Device control is achieved through a 2-wire serial interface. Device addressing is provided through three address inputs that allow up to eight devices on a single 2-wire bus. The exact wiper position of the potentiometer can be written or read. The DS1805 is available in 16-pin SO and 14-pin TSSOP packages. The device is available in three standard resistance values: 10kΩ, 50kΩ, and 100kΩ. The DS1805 specified over the industrial temperature range. The DS1805 is provides a low-cost alternative for designs based on the DS1803, but require only a single potentiometer.

Device Operation

The DS1805 is an addressable, digitally controlled device that has a single 256-position potentiometer. Figure 1 shows a block diagram of the part. Communication and control of the device is accomplished through a 2-wire serial interface that has SDA and SDL signals. Device addressing is attained using the device chip-select inputs A0, A1, and A2.

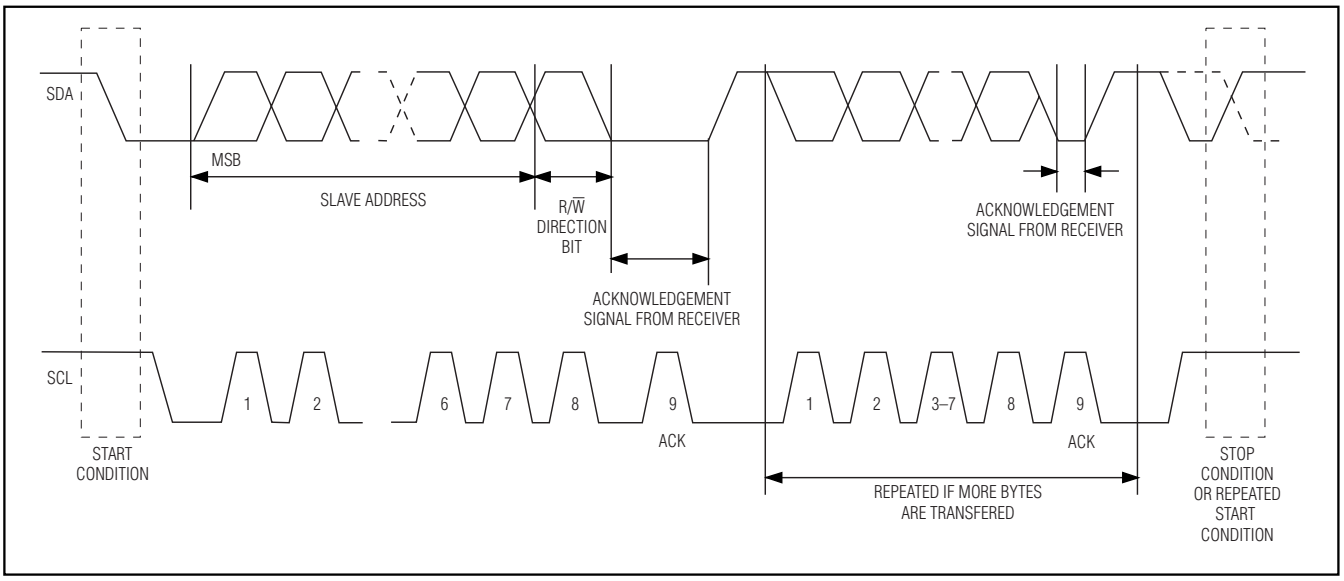


Figure 2. 2-Wire Data Transfer Overview

The potentiometer is composed of a 256-position resistor array. Two 8-bit registers are provided to ensure compatibility with DS1803-based designs. Register-0 is a general-purpose SRAM byte, while register-1 is assigned to the potentiometer and is used to set the wiper position on the resistor array. The wiper terminal is multiplexed to one of 256 positions on the resistor array based on its corresponding 8-bit register value. The highest wiper setting, FFh, is 1 LSB away from H1 (resistor 255), while the lowest setting, 00h, connects to L1.

The DS1805 is a volatile device that does not maintain the position of the wiper during power-down or loss of power. On power-up, the wiper position is set to 00h (the low-end terminal). The user can then set the wiper value to a desired position.

Communication with the DS1805 takes place over the 2-wire serial interface consisting of the bidirectional data terminal, SDA, and the serial clock input, SCL. Complete details of the 2-wire interface are discussed in the *2-Wire Serial Data Bus* section.

The 2-wire interface and address inputs A0, A1, and A2 allow operation of up to eight devices in a bus topology, with A0, A1, and A2 being the address of the device.

Application Considerations

The DS1805 is offered in three standard resistor values: 10kΩ, 50kΩ, and 100kΩ. The resolution of the potentiometer is defined as $R_{TOT}/256$, where R_{TOT} is the total resistor value of the potentiometer. The DS1805 is designed to operate using 3V or 5V power supplies over the industrial (-40°C to +85°C) temperature range. Maximum input signal levels across the potentiometer cannot exceed the operating power supply of the device.

2-Wire Serial Data Bus

The DS1805 supports a bidirectional 2-wire bus and data transmission protocol. A device that sends data on the bus is called a transmitter, and a device receiving data is called a receiver. The device that controls the message is called a master. The devices that are controlled by the master are slaves. The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions. The DS1805 operates as a slave on the 2-wire bus. Connections to the bus are made through the open-drain I/O lines, SDA and SCL.

The following bus protocol has been defined (Figure 2):

- Data transfer can be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high. Changes in the data line while the clock line is high will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus not busy: Both data and clock lines remain high.

Start data transfer: A change in the state of the data line from high to low while the clock is high defines a START condition.

Stop data transfer: A change in the state of the data line from low to high while the clock line is high defines the STOP condition.

Data valid: The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the high period of the clock signal. The data on the line must be changed during the low period of the clock signal. There is one clock pulse per bit of data. Figure 2 details how data transfer is accomplished on the 2-wire bus. Depending upon the state of the R/$\overline{W}$ bit, two types of data transfer are possible.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions is not limited and is determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth bit.

Within the bus specifications a regular mode (100kHz clock rate) and a fast mode (400kHz clock rate) are defined. The DS1805 works in both modes.

Acknowledge: Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse that is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable low during the high period of the acknowledge-related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line high to enable the master to generate the STOP condition.

Data transfer from a master transmitter to a slave receiver: The first byte transmitted by the master is the control byte (slave address). Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte.

Data transfer from a slave transmitter to a master receiver: The first byte (the slave address) is transmitted by the master. The slave then returns an acknowledge bit. Next follows a number of data bytes transmitted by the slave to the master. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a 'not acknowledge' is returned.

The master device generates all of the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus will not be released.

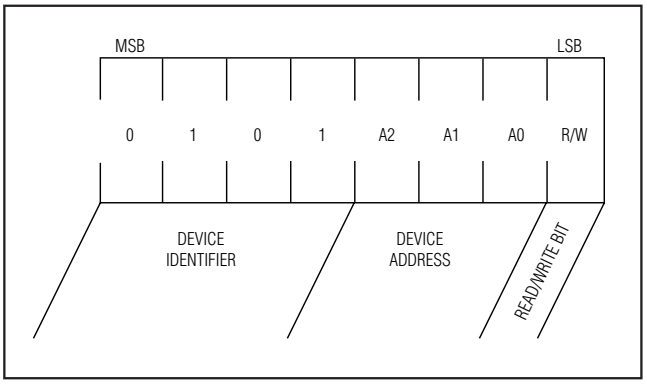


Figure 3. Control Byte

The DS1805 can operate in the following two modes:

Slave receiver mode: Serial data and clock are received through SDA and SCL. After each byte is received, an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit.

Slave transmitter mode: The first byte is received and handled as in the slave receiver mode. However, in this mode the direction bit will indicate that the transfer direction is reversed. Serial data is transmitted on SDA by the DS1805 while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer.

Slave Address

A control byte is the first byte received following the START condition from the master device. The control byte consists of a four-bit control code; for the DS1805, this is set as 0101 binary for read/write operations. The next three bits of the control byte are the device select bits (A2, A1, A0). They are used by the master device to select which of eight devices are to be accessed. The select bits are the three least significant bits (LSB) of the slave address. Additionally, A2, A1, and A0 can be changed any time during a powered condition of the part. The last bit of the control byte (R/$\overline{W}$) defines the operation to be performed. When set to a one, a read operation is selected; when set to a zero a write operation is selected. Figure 3 shows the control byte structure for the DS1805.

Following the START condition, the DS1805 monitors the SDA bus checking the device type identifier being transmitted. Upon receiving the 0101 address code and appropriate device select bits, the slave device outputs an acknowledge signal on the SDA line.

Command and Protocol

The DS1805's command and protocol structure of the DS1805 allows the user to read or write to both the scratchpad and potentiometer registers. Figures 4 and 5 show the command structures for the part. Potentiometer data values and control and command values are always transmitted most significant bit (MSB) first. During communications, the receiving unit always generates the acknowledge.

Reading the DS1805

As shown in Figure 4, the DS1805 provides one read-command operation. This operation allows the user to read both potentiometers. Specifically, the R/$\overline{W}$ bit of the control byte is set equal to a one for a read operation. Communication to read the DS1805 begins with a START condition that is issued by the master device. The control byte from the master device follows the START condition. Once the control byte has been received by the DS1805, the part responds with an acknowledge. The read/write bit of the control byte as stated should be set equal to one for reading the DS1805.

When the master has received the acknowledge from the DS1805, the master can then begin to receive potentiometer wiper data. The value of the register-0 wiper position will be the first returned from the DS1805. Once the eight bits of the register-0 wiper position have been transmitted, the master needs to issue an acknowledge, unless it is the only byte to be read, in which case the master issues a not acknowledge. If desired, the master can stop the communication transfer at this point by issuing the STOP condition. However, if the value of the potentiometer-1 wiper position value is needed, communication transfer can continue by clocking the remaining eight bits of the potentiometer-1 value, followed by a not acknowledge. Final communication transfer is terminated by issuing the STOP command. Figure 4 shows the flow of the read operation.

Table 1. 2-Wire Command Words

COMMAND	COMMAND VALUE
Write Register-0	101010 01
Write Potentiometer-1 Register	101010 10
Write Both Registers	101011 11

Writing to the DS1805

Figure 5 shows a data flow diagram for writing the DS1805. The DS1805 has three write-command operations. These include write reg-0, write pot-1, and write reg-0/pot-1. The write reg-0 command allows the user to write the value of scratchpad register-0 and as an option the value of potentiometer-1. The write-1 command allows the user to write the value of potentiometer-1 only. The last write command, write-0/1, allows the user to write both registers to the same value with one command and one data value being issued.

All the write operations begin with a START condition. Following the START condition, the master device issues the control byte. The read/write bit of the control byte is set to zero for writing the DS1805. Once the control byte has been issued and the master receives the acknowledgment from the DS1805, the command byte is transmitted to the DS1805. As mentioned above, there exist three write operations that can be used with the DS1805. Figure 5 and Table 1 show the binary value of each write command.

Package Information

For the latest package outline information, go to **www.maxim-ic.com/packages**.

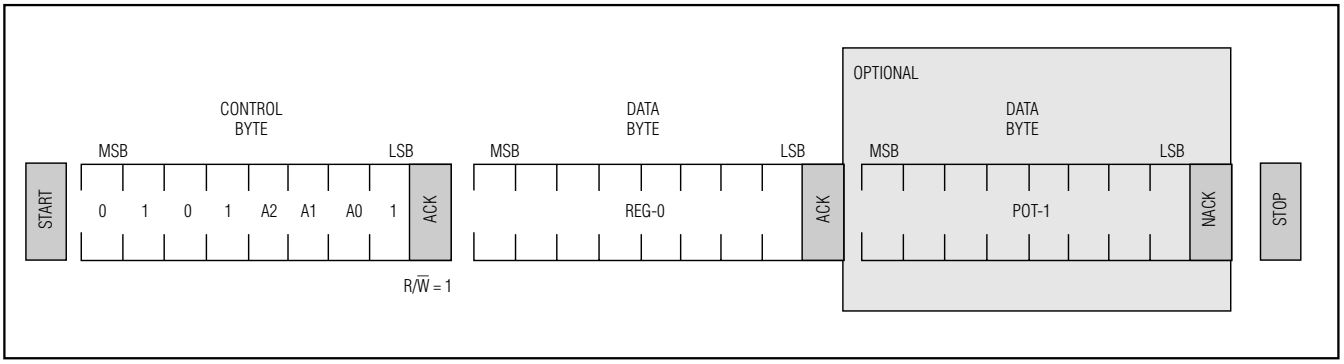


Figure 4. 2-Wire Read Protocols

Addressable Digital Potentiometer

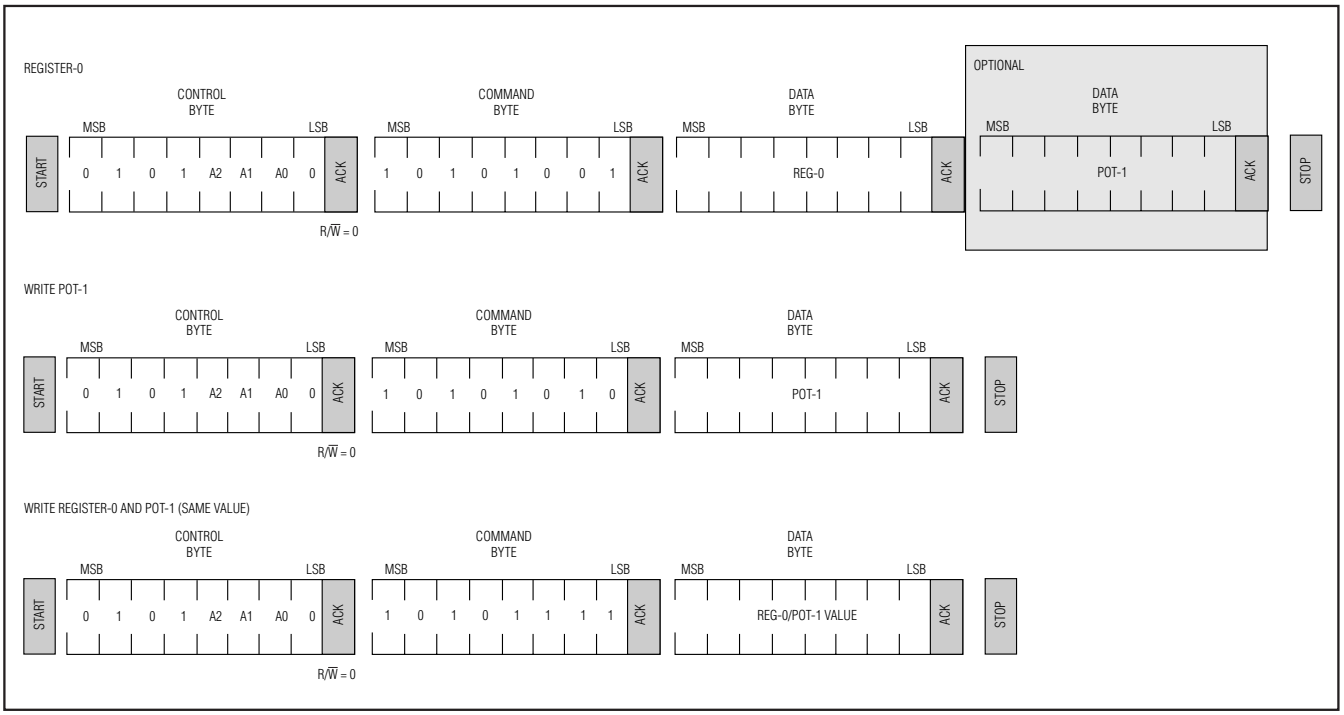


Figure 5. 2-Wire Write Protocols

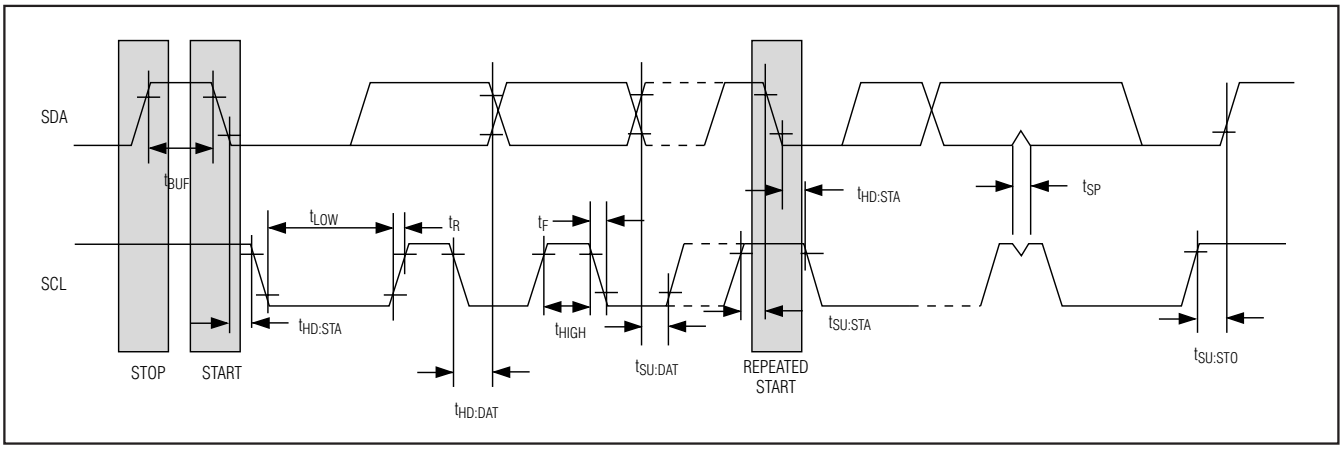


Figure 6. Timing Diagram

Revision History

Pages changed at Rev1: 9, 10

Package Information

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