DS1683

Total-Elapsed-Time and Event Recorder with Alarm

General Description

The DS1683 is an integrated elapsed-time recorder containing a factory-calibrated, low-temperature-coefficient RC time base that eliminates the need for an external crystal. Using EEPROM technology to maintain data in the absence of power, the DS1683 requires no backup power source. The DS1683 detects and records the number of falling edge transitions on the EVENT pin as well as the total cumulative time that the EVENT pin is held high. The ALARM pin alerts the user when the total time accumulated equals or exceeds the user-programmed alarm value, or when the total number of events equals or exceeds the user-programmed alarm value. The polarity of the open-drain ALARM pin can be programmed to either drive low or become high impedance upon an alarm condition. The DS1683 is ideal for applications that monitor the total amount of time that a device has been in operation and/or the number of uses since inception service, repair, or last calibration.

Applications

High-Temp, Rugged, Industrial Applications Where Vibration or Shock Could Damage a Quartz Crystal

Any System Where Time-of-Use is Important to Track

Power-on-Time Recorder

Benefits and Features

- **Records the Total Time the EVENT Input Has Been Active High and Number of Events (Falling Edges of EVENT) That Have Occurred**
- **32-Bit, Nonvolatile, Elapsed Time Counter (ETC) Monitors Event Duration with Quarter Seconds Resolution and Provides 34 Years of Total Time Accumulation**
- **Nonvolatile 16-Bit Event Counter Records the Number of Falling Edges Seen by the EVENT Pin**
- **Calibrated, Low-Temperature-Coefficient RC Time Base**
- **16 Bytes of User EEPROM**
- **Password Protection Scheme (4 Bytes)**
- **I^2C-Compatible Interface**
- **+2.5V to +5.5V Operating Voltage Range**

***Ordering Information* appears at end of data sheet.**

*For related parts and recommended products to use with this part, refer to **www.maximintegrated.com/DS1683.related**.*

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at www.maximintegrated.com.

19-6388; Rev 0; 6/12

ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND.)
Voltage Range on V_{CC}, ALARM, SDA, SCL .....-0.5V to +6.0V
Voltage Range on EVENT ..... -0.5V to (V_{CC} + 0.5V), not to exceed +6.0V
Continuous Power Dissipation (T_A = +70°C)
SO (derate 5.9mW/°C above +70°C).....470.6mW
Maximum Junction Temperature.....+150°C
Operating Temperature Range..... -40°C to +85°C
Programming Temperature Range ..... 0°C to +70°C
Storage Temperature Range..... -55°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(T_A = -40°C to +85°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}	(Note 1)	2.5		5.5	V
Input Logic 1 (SCL, SDA)	V_{IH}		0.7 x V_{CC}		V_{CC} + 0.3	V
Input Logic 0 (SCL, SDA)	V_{IL}		-0.3		0.3 x V_{CC}	V
EVENT Input Trip Point	V_{ETP}		0.3 x V_{CC}	0.5 x V_{CC}	0.7 x V_{CC}	V
EVENT Trip Point Hysteresis	V_{HYS}		1% of V_{CC}			
Power-On Reset	V_{POR}			2.4		V

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.5V to 5.5V, T_A = -40°C to +85°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Leakage	I_{LI}		-1		+1	µA
ALARM Output (I_{OL} = 10mA)	V_{OL}				0.8	V
SDA Output (I_{OL} = 4mA)	V_{OL}				0.4	V
Active Supply Current	I_{CCA}	(Note 1)		180	300	µA
EEPROM Write Current	I_{EE}	(Note 1)		250	350	µA

EVENT TIMING

(V_{CC} = 2.5V to 5.5V, T_A = -40°C to +85°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Time Event Minimum	t_G	(Note 1)	10	35	70	ms
Time Event Increment	t_{EI}	(Note 1)	237.5	250	262.5	ms
Time Event Max	t_{EM}	(Note 2)			34	Years
CLR ALM to Alarm Set		(Note 2)	10		150	µs

I²C AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.5V to 5.5V, T_A = -40°C to +85°C, timing referenced to $V_{IL(MAX)}$ and $V_{IH(MIN)}$, unless otherwise noted.) (Figure 7)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}				400	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		1.3			µs
Hold Time (Repeated) START Condition	$t_{HD:STA}$		0.6			µs
Low Period of SCL	t_{LOW}		1.3			µs
High Period of SCL	t_{HIGH}		0.6			µs
Data Hold Time	$t_{HD:DAT}$		0		0.9	µs
Data Setup Time	$t_{SU:DAT}$		100			ns
START Setup Time	$t_{SU:STA}$		0.6			µs
SDA and SCL Rise Time	t_R	(Note 3)	20 + 0.1C_B		300	ns
SDA and SCL Fall Time	t_F	(Note 3)	20 + 0.1C_B		300	ns
STOP Setup Time	$t_{SU:STO}$		0.6			µs
SDA and SCL Capacitive Loading	C_B	(Note 3)			400	pF
EEPROM Write Time	t_W	(Notes 4, 5, 6)		10	20	ms

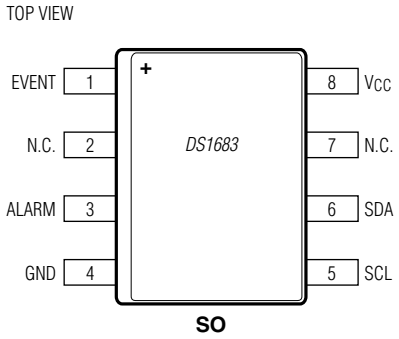
NONVOLATILE MEMORY CHARACTERISTICS

(V_{CC} = 2.5V to 5.5V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
EEPROM Write Cycles		T_A = +70°C (Note 7)	50,000		Writes
EEPROM Write Cycles (4 Banks)		T_A = +70°C (Note 8)	200,000		Writes

Note 1: All voltages are referenced to ground. Currents entering the IC are specified as positive; currents exiting the IC are specified as negative.
Note 2: Guaranteed by design.
Note 3: C_B: Total capacitance of one bus line in pF.
Note 4: EEPROM write time begins after a STOP condition occurs.
Note 5: A decoupling capacitor to supply high instantaneous currents during EEPROM writes is recommended. A typical value is 0.01µF. V_{CC} must be maintained above $V_{CC(MIN)}$, including transients, during EEPROM writes.
Note 6: V_{CC} must be at or above 2.5V for t_W after the end of an event to ensure data transfer to the EEPROM.
Note 7: Memory locations to which this specification applies: User Memory, ETC Alarm Limit, Event Counter Alarm Limit, Configuration, Password Value.
Note 8: Memory locations to which this specification applies: Event Counter register, ETC register.

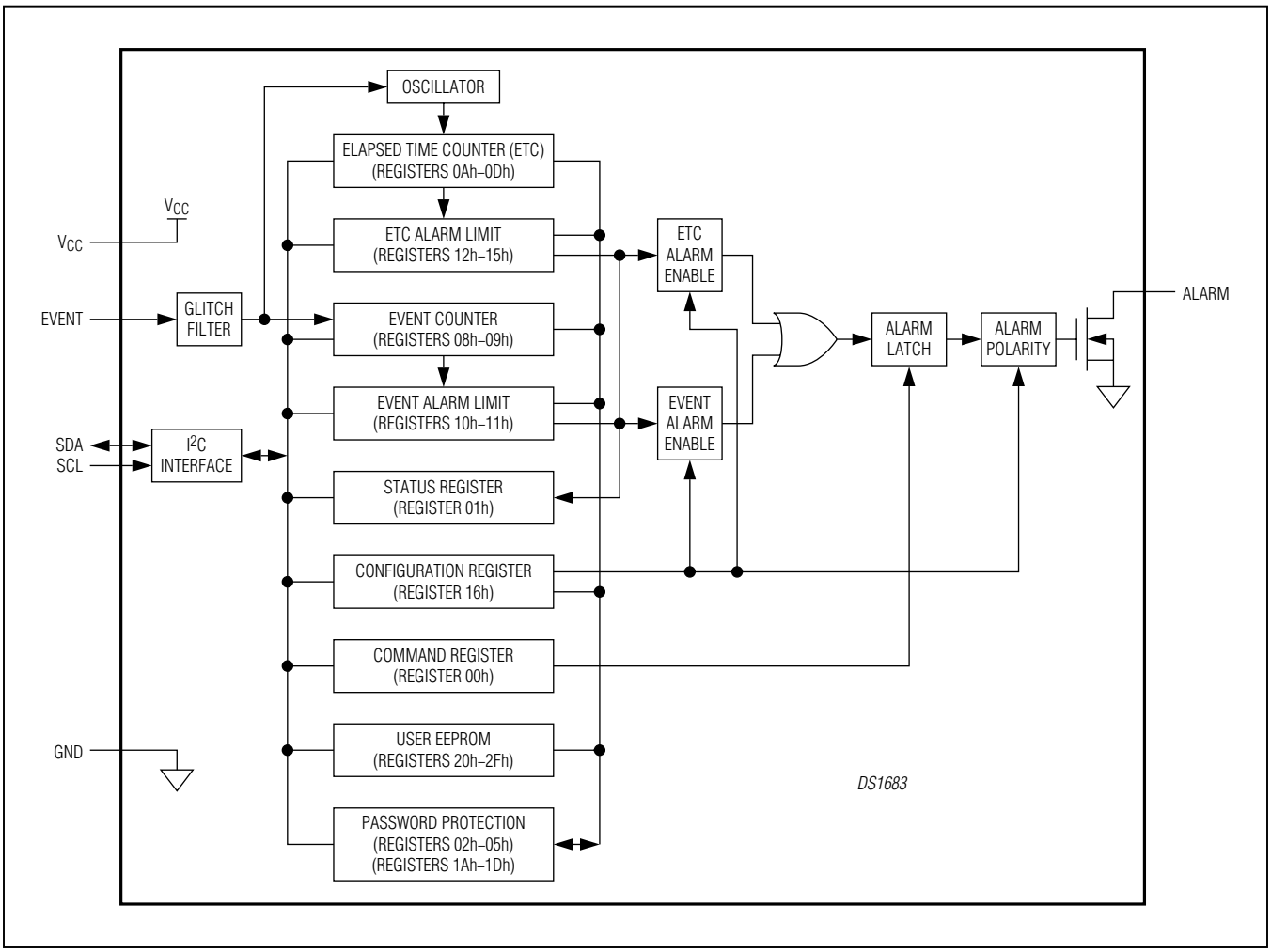
Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1	EVENT	Event Input. The EVENT pin controls when the values in the Elapsed Time Counter (ETC) register and the Event Counter register are incremented. The EVENT pin also determines when the data in these registers is stored to EEPROM.
2, 7	N.C.	No Connection. These pins are not connected internally.
3	ALARM	Alarm Output. The ALARM pin is an open drain structure, and is set active when an alarm condition is met. The active state of this pin is controlled by the ALRM POL bit located in the Configuration register. Once the ALARM pin is active, it will remain active until the alarm condition is cleared and the CLR ALM bit in the Command register is set.
4	GND	Ground
5	SCL	I^2C Serial-Clock Input. The SCL pin is the serial-clock input for the I^2C synchronous communications channel. The SCL pin is an input that requires an external pull-up resistor.
6	SDA	I^2C Serial-Data Input/Output. The SDA pin is the data input/output signal for the I^2C synchronous communications channel. The SDA pin is an open-drain I/O, which requires an external pullup resistor.
8	V_{CC}	+2.5V to +5.5V Input Supply

Block Diagram



Detailed Description

The DS1683 is an elapsed-time recorder that tracks the accumulated time the EVENT pin has been held high as well as the number of falling edge transitions seen by the EVENT pin. The main application is to track the accumulated on-time and number of power cycles of a device or system. Programmable alarm limits for both the accumulated on-time and number of falling edges of the EVENT pin are available so that the user can be alerted when these conditions are met. The accumulated elapsed time that the EVENT pin has been held high is stored in the 4-byte Elapsed Time Counter (ETC) register. The number of times the EVENT pin sees a falling transition is stored in the 2-byte Event Counter register. The DS1683 includes password protection to prevent tampering with accumulated values, alarm limits, configuration settings, and user memory values.

The ETC, ETC Alarm Limit, Event Counter, Event Counter Alarm Limit, Configuration, Password, and User Memory values are stored in shadowed EEPROM. On power-up, the values in the ETC and Event Counter are loaded into SRAM locations. When the state of the EVENT pin causes changes to the accumulated time and number of events, it is these SRAM registers that are incremented.

When the contents of the ETC and Event Counter registers match or exceed their programmable alarm limits, the ALARM pin can be driven to its active state as set by the polarity bit, ALRM POL, located in the Configuration register. Each of the alarm limits has an enable bit that should be used to determine whether or not the ALARM pin should be activated when the alarm conditions are met.

The DS1683 has an internal, low-temperature-coefficient, RC-based oscillator that is started on power-up. The DS1683 uses this RC time base to increment the ETC register in 250ms increments while the EVENT pin is held high. When the EVENT pin is driven low, the ETC register ceases to increment.

EVENT Pin

The DS1683 monitors the state of the EVENT pin to determine when an event occurs. When the pin is pulled high, the ETC and Event Counter values are transferred from shadowed EEPROM to SRAM. While the EVENT pin is held high, the value of the ETC SRAM begins incrementing once every 250ms. Incrementing the ETC SRAM value while EVENT is high allows the device to increment the ETC value without contributing to EEPROM wear out. When the EVENT pin falls to a logic 0, the Event Counter SRAM value increments by a value of one. Also at this time the ETC stops accumulating time. The values of the EVENT and ETC Counter SRAM locations are then stored in the ETC and EVENT Shadowed EEPROM array. The EVENT input is deglitched (t_G) to prevent short noise spikes from triggering an event.

While the EVENT pin is high, the I^{2}C bus is unavailable for write commands, though read commands can still be executed. When the EVENT pin transitions low, I^{2}C communication is unavailable for t_W (EEPROM write time), after which I^{2}C writes are possible. However, if an I^{2}C write operation is underway, and the EVENT pin transitions low to high, this operation is interrupted so that the ETC and Event Counter registers can be updated. So it is important to terminate all I^{2}C write transactions before transitioning the level on the EVENT pin.

An I^{2}C read command can be performed regardless of the state of the EVENT pin. On a low-to-high transition of the EVENT pin, the I^{2}C read command is allowed to complete. However, it is strongly recommended that all I^{2}C communication be terminated before transitioning the level on the EVENT pin.

When the EVENT pin is high and the device detects a START signal on the I^{2}C bus, a snapshot of the data in the ETC and Event Counter SRAM is made available on the I^{2}C bus. When the EVENT pin is low and the device detects a START signal on the I^{2}C bus, data is transferred from the ETC and Event Counter shadowed EEPROM bank memory.

Elapsed Time Counter (ETC) Register

The Elapsed Time Counter (ETC) register is a 32-bit value that holds time in quarter-second resolution. The ETC register consists of 4 bytes of memory in the memory map. Once the counter reaches FFFFFFFFh, counting stops. The ETC register is backed by 4 banks of shadowed EEPROM, which allow for 200k+ write cycles to occur before a wearout condition. When an I^{2}C read occurs while the EVENT pin is high, a snapshot of the value from the ETC SRAM is made available for the I^{2}C bus. When the EVENT pin is logic 0, I^{2}C reads take data from the shadowed EEPROM ETC bank memory.

On power-on reset (POR), the ETC value stored in the shadowed EEPROM bank memory is loaded into the ETC SRAM location (Figure 1). This also happens when a low-to-high transition occurs on the EVENT pin, or when an I^{2}C write to the ETC register occurs. When data is written to the ETC register, the value is stored in the shadowed EEPROM bank memory and also in the corresponding ETC SRAM location. This data is transferred after the STOP of the I^{2}C command.

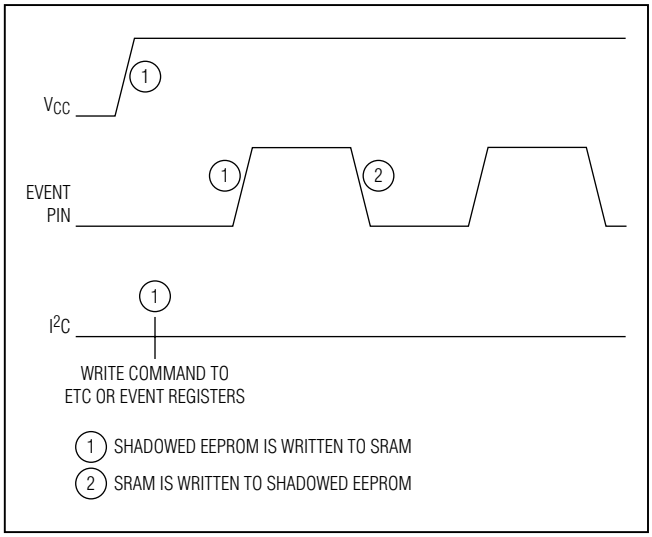


Figure 1. Data Transfer Between Nonvolatile and Volatile Memory Types

On the falling edge of the EVENT signal, the contents of the ETC SRAM counter are written to the ETC shadowed EEPROM registers.

When the EVENT pin is low, the ETC register can be written by the I2C bus. For example, when it comes time to reset the time stored in the ETC register, an I2C write command can be issued to set all the bits to 0.

ETC Alarm Register

The ETC Alarm register is a 32-bit value and contains the value that is compared to the accumulated ETC value. When a nonzero value is programmed into the ETC Alarm register, the ETC alarm function is enabled and the DS1683 compares the value in the ETC SRAM counter with the programmed value in the ETC Alarm register. When the ETC SRAM Counter matches or exceeds the alarm value, the ETC alarm flag (ETC AF) is set.

Note: To disable the ETC alarm function, program the ETC Alarm register to a value of all 0s. An alarm value of all 0s disables the ETC alarm function.

Event Counter Register

This 16-bit Event Counter stores the number of falling edges seen on the EVENT pin. Once the Event Counter reaches a value of FFFFh, event counting stops. The Event Counter register is backed by four banks of shadowed EEPROM, which allow for 200k+ write cycles occur before a wearout condition. When an I2C read occurs when the EVENT pin is high, a snapshot of the value from the Event Counter SRAM is made available for the I2C bus. When the EVENT pin is logic 0, I2C reads take data from the shadowed EEPROM Event Counter bank memory.

On POR, the Event Counter value stored in shadowed EEPROM bank memory is loaded into the Event Counter SRAM location. This also happens when a low-to-high transition occurs on the EVENT pin, or when an I2C write to the Event Counter register occurs. When data is written to the Event Counter register, the value is stored in the shadowed EEPROM bank memory, and also in the corresponding Event Counter SRAM location. This data is transferred after the STOP of the I2C command.

On the falling edge of the EVENT signal, the Event Counter SRAM register is incremented by a value of one, and the contents of the Event Counter SRAM are written to the Event Counter shadowed EEPROM.

When the EVENT pin is low, the Event Counter register can be written by the I2C bus. For example, when it comes time to reset the accumulated number of events in the Event Counter register, an I2C write command can be issued to set all of the bits to 0.

Event Counter Alarm Register

The Event Counter Alarm register is a 16-bit register, and contains the value that is compared to the accumulated Event Counter value. When a nonzero value is programmed into the Event Counter Alarm register, the Event Counter alarm function is enabled, and the DS1683 compares the value in the Event Counter SRAM with the programmed value in the EVENT Alarm register. When the Event Counter SRAM value matches or exceeds the alarm value, the Event Counter alarm flag (EVENT AF) is set.

Note: To disable the Event Counter alarm function, program the Event Counter Alarm register to a value of all 0s. An alarm value of all 0s disables the Event Counter alarm function.

Alarm Output

The ALARM pin is an open-drain structure, and setting the alarm polarity bit (ALRM POL) located in the Configuration register determines if the ALARM output is active high or active low (default is active low). The DS1683 monitors the values in the ETC and Event Counter registers and compares them to the values in the ETC and Event Counter Alarm registers. When the ETC and Event Counter values match or exceed their corresponding alarm values, their alarm flags (EVENT AF and ETC AF, located in the Status register) are set to a value of 1, indicating an alarm condition. If the corresponding Enable bits (ETC ALRM EN and EVENT ALRM EN, located in the Configuration register) are active, then the ALARM output is driven to its active state and is latched.

Once the alarm condition has been cleared, the corresponding alarm flag (EVENT AF and/or ETC AF) automatically clears. Once the actual alarm condition is cleared, the CLR ALM bit must be used to clear an active ALARM pin state. If the alarm condition is still present when the CLR ALM bit is toggled, the ALARM simply reactivates and latches.

Event Logging

When the DS1683 is powered up, the internal oscillator starts; the ETC and Event Counter values, which are recorded in the shadowed EEPROM bank memory, are transferred to the ETC and Event Counter SRAM locations; and the device waits for an event (rising edge of the EVENT signal). When an event triggers the input by transitioning the EVENT pin from a low to a high level, the following occur:

1) The ETC and Event Counter values are once again transferred from shadowed EEPROM bank memory to their SRAM counter locations.
2) After the glitch filtering and t_{EI}, the ETC SRAM counter value increments. See Figure 2 for timing. An event greater than time event minimum (t_G) but less than t_{EI} (i.e., a low-high-low transition on EVENT < t_{EI}) increments the Event Counter SRAM value but not the ETC SRAM value.
3) The ETC SRAM value increments every t_{EI}. The ETC SRAM counter holds time in quarter-second resolution.
4) When the EVENT pin goes low, the Event Counter SRAM value increments by one, the ETC SRAM counter stops incrementing, and the values from the ETC and Event Counter SRAM locations are transferred to their Shadowed EEPROM counterparts. The I²C bus is not available for t_W.

The ETC value does not roll over when FFFFFFFFh, or approximately 34 years, is reached. The Event Counter value does not roll over when reaching a value of FFFFh. While the EVENT pin is high, I²C write commands are ignored, though I²C read commands are still possible.

Password Protection

From the factory, the DS1683 powers up without password protection enabled. The intent is to provide a manufacturer an optional security feature to protect the Configuration register, Alarm registers, User EEPROM, ETC and Event Counter settings, and the Password Value (PWV). The customer is not able to alter the Configuration register, Alarm registers, ETC or Event Counter, User EEPROM or Password Value settings if the password conditions are not met.

The DS1683 password is stored in the 4-byte read-only Password Value register, located at 1Ah–1Dh. The default value for this register is FFFFFFFFh. To change this value, a 4-byte I²C write command must be issued. The 4 bytes of the new password must be issued with the same I²C write command. Once the STOP of the I²C write command is issued, the Password Value register is updated with the new 4-byte value.

The Password Entry bytes (PWE) are where the user enters the 4-byte password to unlock access to the DS1683's EEPROM locations. When writing the PWE value, the user must issue a 4-byte I²C write command starting at location 02h. This 4-byte value must match the 4-byte Password Value stored in registers 1Ah–1Dh.

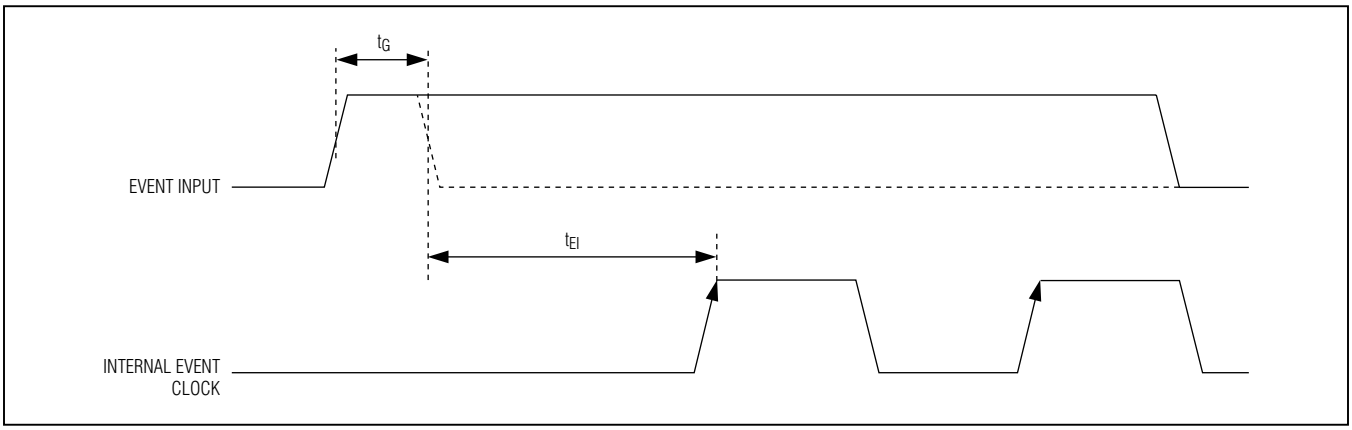


Figure 2. Event Input Timing

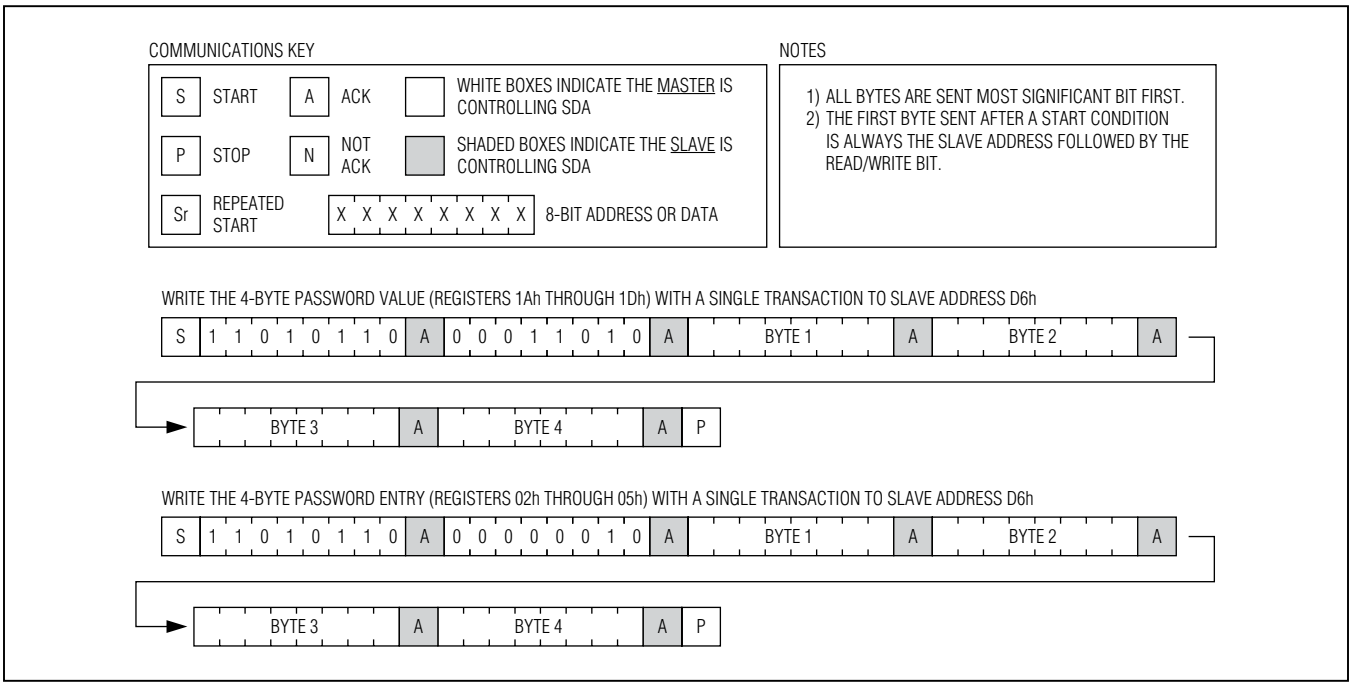


Figure 3. Password Value and Password Entry I²C Examples

If the Password Value has been changed from the factory default setting, the user has to enter this new password value into the PWE registers after a power cycle in order to unlock the memory again.

See Figure 3 for examples of writing the 4-byte Password Value and the 4-byte Password Entry value.

User Memory

The DS1683 has 16 bytes of user-programmable, EEPROM memory. User memory is set to read-only if the correct password is not entered into the Password Entry Bytes. If the correct password is entered into the Password Entry Bytes, the data can be written to the User Memory and stored in EEPROM with the correct I²C write command.

Table 1. Register Memory Map

ADDRESS	READ/WRITE	NAME	VOLATILE/ NONVOLATILE	FACTORY DEFAULT/POWER-UP DEFAULT	PASSWORD PROTECTION	FUNCTION
00h	Read/Write	COMMAND	V	00h	No	Command Register
01h	Read	STATUS	V	00h	No	Status Register
02h–05h	Read*/Write	PWE	V	FFh	No	Password Entry Registers
06h–07h	—	RSVD	—	—	—	Reserved
08h–09h	Read/Write	EVENT REG	NV	00h	Yes	Event Counter Registers
0Ah–0Dh	Read/Write	ETC REG	NV	00h	Yes	ETC Registers
0Eh–0Fh	—	RSVD	—	—	—	Reserved
10h–11h	Read/Write	EVENT COUNTER ALARM LIMIT	NV	00h	Yes	Event Counter Alarm Limit Registers
12h–15h	Read/Write	ETC ALARM LIMIT	NV	00h	Yes	ETC Alarm Limit Registers
16h	Read/Write	CONFIG	NV	00h	Yes	Configuration Register
17h–19h	—	RSVD	—	—	—	Reserved
1Ah–1Dh	Read*/Write	PWV	NV	FFh	Yes	Password Value
1Eh–1Fh	—	RSVD	—	—	—	Reserved
20h–2Fh	Read/Write	USER MEMORY	NV	00h	Yes	User EEPROM
30h–FFh	—	RSVD	—	—	—	Reserved

Note: *I^2C reads from memory locations that do not exist report a value of FFh.*

V: Volatile (SRAM); NV: Nonvolatile (EEPROM).

**The PWE and PWV bytes read back 0s.*

REGISTER 00h: COMMAND REGISTER

Factory Default/Power-On Value	00h
Read Access	All
Write Access	All
Memory Type	SRAM, Volatile

Memory Access	N/A	N/A	N/A	N/A	N/A	N/A	N/A	R/W
00h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CLR ALM
	BIT 7							BIT 0

7:1	Reserved	Reserved
0	CLR ALM	Clear Alarm Bit. This bit reads as a 0. Writing this bit to a 1 unlatches the active ALARM output, setting the ALARM pin to its inactive state if the alarm condition is no longer present. If the alarm condition persists, the ALARM pin once again asserts to its active state.

REGISTER 01h: STATUS REGISTER

Factory Default /Power-On Value	00h
Read Access	All
Write Access	N/A
Memory Type	SRAM, Volatile

Memory Access	N/A	N/A	N/A	R/W	R/W	R/W	R/W	R/W
01h	Reserved	Reserved	Reserved	Reserved	Reserved	EVENT	EVENT AF	ETC AF
	BIT 7							BIT 0

7:3	Reserved	Reserved
2	EVENT	This bit indicates the status of the EVENT pin's logic level, detected after the t_G glitch filter time.
1	EVENT AF	Default value = 0. If the value in the Event Counter SRAM value is greater than or equal to the Event Counter Alarm Limit value, then this bit is automatically set to a value of 1 to indicate an ALARM event. When the EVENT SRAM Counter value is less than the Event Counter Alarm Limit, this bit automatically set to a value of 0, indicating that there is no EVENT alarm.
0	ETC AF	Default value = 0. If the value in the ETC SRAM value is greater than or equal to the ETC Alarm Limit value, then this bit is automatically set to a value of 1 to indicate an ALARM event. When the ETC SRAM value is less than the ETC Alarm Limit, this bit automatically set to a value of 0, indicating that there is no ETC alarm.

REGISTERS 02h–05h: PASSWORD ENTRY (PWE)

Factory Default	FF FF FF FFh
Read Access	N/A; Reads as all 0s
Write Access	All
Memory Type	SRAM, Volatile

Memory Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
02h	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
03h	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8
04h	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}
05h	2^{31}	2^{30}	2^{29}	2^{28}	2^{27}	2^{26}	2^{25}	2^{24}
	BIT 7							BIT 0

There is one 4-byte password for the DS1683. Entering the correct password into the Password Entry (PWE) bytes allows write access to the Event, ETC, Event Counter Alarm Limit, ETC Alarm Limit, Configuration, Password Value, and User Memory registers. This value is write-only, and reads from this location result in all 0s. On power-up, the PWE bits are set to 1 to match the factory default Password Value of all 1s.

REGISTERS 08h–09h: EVENT COUNTER REGISTER

Factory Default	00 00h
Read Access	All
Write Access	PW
Memory Type	Shadowed EEPROM, Nonvolatile

Memory Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
08h	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
09h	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8
	BIT 7							BIT 0

The Event Counter register is a shadowed EEPROM register that contains the number of times a falling edge of the EVENT pin has occurred. On power-up, on every rising edge of the EVENT pin, and after an I^2C write to the Event Counter register, the value from the shadowed EEPROM is loaded up into the Event Counter memory (SRAM). It is this memory that is incremented on the falling edge of the EVENT pin. On the falling edge of the EVENT pin, this value in SRAM memory is then written to the shadowed EEPROM memory to store the number of times there has been a falling edge on the EVENT pin.

REGISTERS 0Ah–0Dh: ETC REGISTER

Factory Default	00 00 00 00h
Read Access	All
Write Access	PW
Memory Type	Shadowed EEPROM, Nonvolatile

Memory Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0Ah	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
0Bh	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8
0Ch	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}
0Dh	2^{31}	2^{30}	2^{29}	2^{28}	2^{27}	2^{26}	2^{25}	2^{24}
	BIT 7							BIT 0

The ETC register is a shadowed EEPROM register that contains the accumulated time in 250ms increments that the EVENT pin has been held high. On power-up, on every rising edge of the EVENT pin, and after an I^2C write to the ETC register, the value from the shadowed EEPROM location is loaded into the ETC counter memory (SRAM). When the EVENT pin is high, it is this SRAM memory that is incremented once every 250ms. On the falling edge of the EVENT pin, this value in SRAM memory is then written to the shadowed EEPROM memory to store the accumulated time in 250ms increments.

REGISTERS 10h–11h: EVENT COUNTER ALARM LIMIT REGISTER

Factory Default	00 00h
Read Access	All
Write Access	PW
Memory Type	Shadowed EEPROM, Nonvolatile

Memory Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
10h	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
11h	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8
	BIT 7							BIT 0

The Event Counter Alarm Limit is a shadowed EEPROM register, and when the Event Counter register value equals or exceeds the Event Counter Alarm Limit value, the EVENT flag bit (EVENT AF bit, Register 01h, bit 1) goes active high. When the Event Counter register value drops below the Event Counter Alarm Limit value, the EVENT AF bit automatically clears.

REGISTERS 12h–15h: ETC ALARM LIMIT REGISTER

Factory Default	00 00 00 00h
Read Access	All
Write Access	PW
Memory Type	Shadowed EEPROM, Nonvolatile

Memory Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
12h	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
13h	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8
14h	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}
15h	2^{31}	2^{30}	2^{29}	2^{28}	2^{27}	2^{26}	2^{25}	2^{24}
	BIT 7							BIT 0

The ETC Alarm Limit is a shadowed EEPROM, and when the ETC register value equals or exceeds the ETC Alarm Limit value, the ETC flag bit (ETC AF bit, Register 01h, bit 0) goes active high. When the ETC register value drops below the ETC Alarm Limit value, the EVENT AF bit automatically clears.

REGISTER 16h: CONFIGURATION REGISTER

Factory Default /Power-On Value	00h
Read Access	All
Write Access	PW
Memory Type	Shadowed EEPROM, Nonvolatile

Memory Access	N/A	N/A	N/A	R/W	R/W	R/W	R/W	R/W
01h	Reserved	Reserved	Reserved	Reserved	Reserved	ETC ALRM EN	EVENT ALRM EN	ALRM POL
	BIT 7							BIT 0

7:3	Reserved	Reserved
2	ETC ALRM EN	Default value = 0, which is disabled. When set to a 1, and if the ETC register is equal to or greater than the ETC Alarm limit, then this device triggers the ETC Alarm Flag (ETC AF), and the ALARM pin goes to its active state.
1	EVENT ALRM EN	Default value = 0, which is disabled. When set to a 1, and if the Event Counter register is equal to or greater than the Event Counter Alarm limit, then this device triggers the Event Counter Alarm Flag (EVENT AF), and the ALARM pin goes to its active state.
0	ALRM POL	Default value = 0, which sets the ALARM output active low. When set to a 1, the ALARM output is active high.

REGISTERS 1Ah–1Dh: PASSWORD VALUE (PWV)

Factory Default	FF FF FF FFh
Read Access	N/A; Reads as all 0s
Write Access	PW
Memory Type	Shadowed EEPROM, Nonvolatile

Memory Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1Ah	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
1Bh	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8
1Ch	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}
1Dh	2^{31}	2^{30}	2^{29}	2^{28}	2^{27}	2^{26}	2^{25}	2^{24}
	BIT 7							BIT 0

The default value for the four Password Value (PWV) is all 1s (FF FF FF FFh). The intent is to provide a manufacturer with a security feature to protect the Configuration register, Alarm registers, User EEPROM, ETC and Event Counter registers, and the Password Setting (PWV). The customer is not able to alter the Configuration register, Alarm registers, User EEPROM, ETC or Event Counter registers, or Password Setting if the password conditions are not met.

REGISTERS 20h–2Fh: USER MEMORY

Factory Default	00h for All Locations
Read Access	All
Write Access	PW
Memory Type	EEPROM, Nonvolatile

There are 16 bytes of user-programmable EEPROM memory. User memory is set to read-only if the correct password is not entered into the Password Entry bytes. If the correct password is entered into the Password Entry bytes, the data can be written to the User Memory and stored in EEPROM with the correct I^2C write command. The User Memory locations can be read regardless of the password protection.

Sample Applications

Figure 4 shows the DS1683 measuring total run time and operating from a battery with the ALARM pin connected to an LED. When the trigger switch is closed, the EVENT pin is pulled high and the ETC register begins incrementing. When the trigger switch is opened, the EVENT pin is pulled low by the resistor, the ETC register stops incrementing, the Event Counter register is incremented by one, and the values of both the ETC and Event Counter are stored in shadowed EEPROM. When the ETC or Event Counter alarm conditions are met, the ALARM pin pulls active low (the factory default setting), and current flows through the LED, indicating an alarm condition.

Figure 5 shows the DS1683 in a total time-of-use application where power may be removed at the same time as the end of the event. The V_{CC} slew rate at power-down is fast with respect to t_W. A capacitor maintains V_{CC} on the DS1683 above 2.5V until the EEPROM write completes. A Schottky diode blocks current from the capacitor to other devices connected to V_{CC}.

The V_{CC} holding capacitor value of 30µF is calculated using the maximum EEPROM write current and EEPROM write time. This assumes that the V_{CC} slew rate allows time from EVENT trip point to V_{CC} at 2.5V on the DS1683 is at least t_W.

Figure 6 shows the DS1683 in a total time-of-use application with power that can be removed at the same time as the end of the event. In this application, the V_{CC} slew rate at power-down is slow with respect to t_W. The external RST IC ends the event as V_{CC} begins to drop. V_{CC} must remain above 2.5V until the end of t_W.

Both circuits in Figure 5 and Figure 6 are read-only because the state of the EVENT pin is tied V_{CC}. Because the EVENT pin is a logic 1 while V_{CC} is applied, I^2C write commands are disabled, thus only I^2C read commands are possible in these configurations.

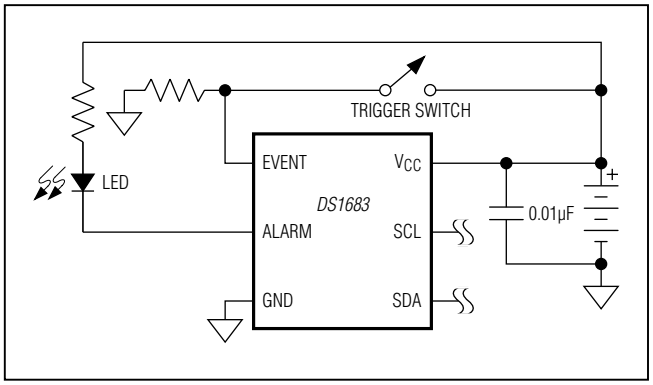


Figure 4. Total Run Time

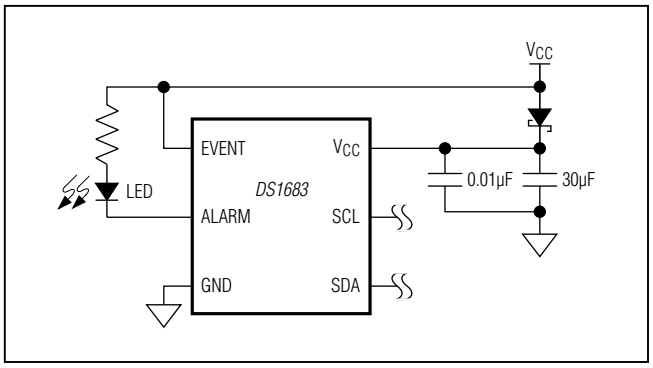


Figure 5. Total Time-of-Use Application with Fast V_{CC} Slew Rate (Read-Only)

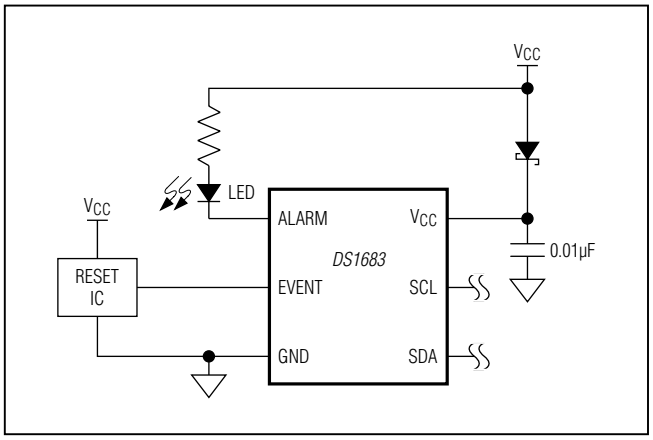


Figure 6. Total Time-of-Use Application with Slow V_{CC} Slew Rate (Read-Only)

I²C Serial Interface Description

I²C Definitions

The following terminology is commonly used to describe I²C data transfers. See Figure 7 and the *I²C AC Electrical Characteristics* table for additional information.

Master Device: The master device controls the slave devices on the bus. The master device generates SCL clock pulses and START and STOP conditions.

Slave Devices: Slave devices send and receive data at the master's request.

Bus Idle or Not Busy: Time between STOP and START conditions when both SDA and SCL are inactive and in their logic-high states. Depending on the device, when the bus is idle it initiates a low-power mode for slave devices.

START Condition: A START condition is generated by the master to initiate a new data transfer with a slave. Transitioning SDA from high to low while SCL remains high generates a START condition.

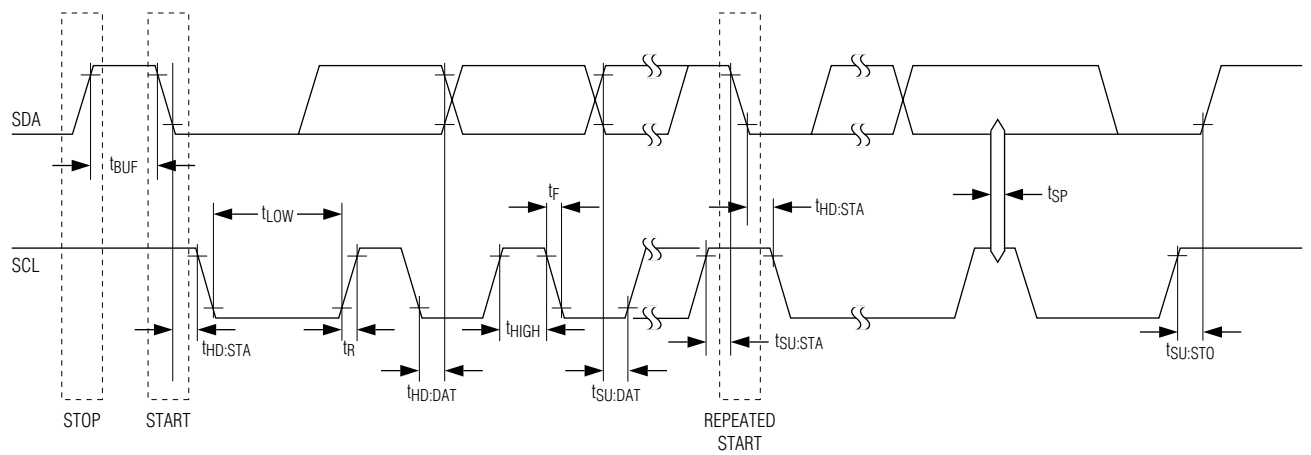
STOP Condition: A STOP condition is generated by the master to end a data transfer with a slave. Transitioning SDA from low to high while SCL remains high generates a STOP condition.

Repeated START Condition: The master can use a repeated START condition at the end of one data transfer to indicate that it will immediately initiate a new data transfer following the current one. Repeated STARTs are commonly used during read operations to identify a specific memory address to begin a data transfer. A repeated START condition is issued identically to a normal START condition.

Bit Write: Transitions of SDA must occur during the low state of SCL. The data on SDA must remain valid and unchanged during the entire high pulse of SCL plus the setup and hold time requirements. Data is shifted into the device during the rising edge of the SCL.

Bit Read: At the end of a write operation, the master must release the SDA bus line for the proper amount of setup time before the next rising edge of SCL during a bit read. The device shifts out each bit of data on SDA at the falling edge of the previous SCL pulse and the data bit is valid at the rising edge of the current SCL pulse. Remember that the master generates all SCL clock pulses including when it is reading bits from the slave.

Acknowledgement (ACK and NACK): An acknowledgement (ACK) or not-acknowledge (NACK) is always the 9th bit transmitted during a byte transfer. The device receiving data (the master during a read or the slave during a write operation) performs an ACK by transmitting a zero during the 9th bit. A device performs a NACK by transmitting a one (done by releasing SDA) during the 9th bit. Timing (Figure 7) for the ACK and NACK is identical to all other bit writes. An ACK is the acknowledgment that the device is properly receiving



NOTE: TIMING IS REFERENCED TO $V_{IL(MAX)}$ AND $V_{IH(MIN)}$.

Figure 7. I²C Timing Diagram

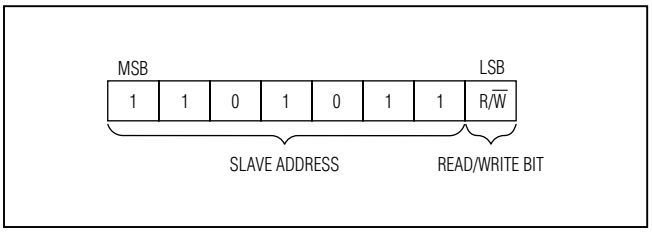


Figure 8. DS1683 I²C Slave Address

data. A NACK is used to terminate a read sequence or as an indication that the device is not receiving data.

Byte Write: A byte write consists of 8 bits of information transferred from the master to the slave (most significant bit first) plus a 1-bit acknowledgement from the slave to the master. The 8 bits transmitted by the master are done according to the bit write definition and the acknowledgement is read using the bit read definition.

Byte Read: A byte read is an 8-bit information transfer from the slave to the master plus a 1-bit ACK or NACK from the master to the slave. The 8 bits of information that are transferred (most significant bit first) from the slave to the master are read by the master using the bit read definition, and the master transmits an ACK using the bit write definition to receive additional data bytes. The master must NACK the last byte read to terminate communication so the slave returns control of SDA to the master.

Slave Address Byte: Each slave on the I²C bus responds to a slave address byte sent immediately following a START condition. The slave address byte contains the slave address in the most significant 7 bits and the R/$\overline{W}$ bit in the least significant bit.

The DS1683's slave address is D6h (1101 011R/$\overline{W}$, where R/$\overline{W}$ is 0). When the R/$\overline{W}$ bit is 0 (such as in D6h), the master is indicating it will write data to the slave. If R/$\overline{W}$ is set to a 1 (D7h in this case), the master is indicating it wants to read from the slave. See Figure 8.

If an incorrect (nonmatching) slave address is written, the DS1683 assumes the master is communicating with another I²C device and ignores the communication until the next START condition is sent.

Memory Address: During an I²C write operation to the DS1683, the master must transmit a memory address to identify the memory location where the slave is to store the data. The memory address is always the second byte transmitted during a write operation following the slave address byte.

I²C Communication

Writing a Single Byte to a Slave: The master must generate a START condition, write the slave address byte (R/$\overline{W}$ = 0), write the memory address, write the byte of data, and generate a STOP condition. The master must read the slave's acknowledgement during all byte write operations.

When writing to the DS1683, EEPROM is written following the STOP condition at the end of the write command. To change the setting without changing the EEPROM, terminate the write with a repeated START condition before the next STOP condition occurs. Using a repeated START condition prevents the t_W delay required for the EEPROM write cycle to finish.

For a write command, data is transferred after receiving a STOP.

Writing Multiple Bytes to a Slave: To write multiple bytes to a slave, the master generates a START condition, writes the slave address byte (R/$\overline{W}$ = 0), writes the memory address, writes up to 8 data bytes, and generates a STOP condition. The DS1683 writes 1 to 8 bytes (one page or row) with a single write transaction. This is internally controlled by an address counter that allows data to be written to consecutive addresses without transmitting a memory address before each data byte is sent. The address counter limits the write to one 8-byte page (one row of the memory map). Attempts to write to additional pages of memory without sending a STOP condition between pages result in the address counter wrapping around to the beginning of the present row. For example, a 3-byte write starts at address 06h and writes 3 data bytes (11h, 22h, and 33h) to three "consecutive" addresses. The result is that addresses 06h and 07h would contain 11h and 22h, respectively, and the third data byte, 33h, would be written to address 00h. To prevent address wrapping from occurring, the master must send a STOP condition at the end of the page, then wait for the bus-free or EEPROM write time to elapse. Then the master can generate a new START condition and write the slave address byte (R/$\overline{W}$ = 0) and the first memory address of the next memory row before continuing to write data.

Acknowledge Polling: Any time a EEPROM byte is written, the DS1683 requires the EEPROM write time (t_W) after the STOP condition to write the contents of the byte to EEPROM. During the EEPROM write time, the device does not acknowledge its slave address because it is busy. It is possible to take advantage

of this phenomenon by repeatedly addressing the DS1683, which allows communication to continue as soon as the DS1683 is ready. The alternative to acknowledge polling is to wait for a maximum period of t_W to elapse before attempting to access the device.

EEPROM Write Cycles: The DS1683's EEPROM write cycles are specified in the *Nonvolatile Memory Characteristics* table. The specification shown is at the worst-case temperature (hot). It can handle many additional writes at room temperature.

Reading a Single Byte from a Slave: Unlike the write operation that uses the specified memory address byte to define where the data is to be written, the read operation occurs at the present value of the memory address counter. To read a single byte from the slave, the master generates a START condition, writes the slave address byte with R/$\overline{W}$ = 1, reads the data byte with a NACK to indicate the end of the transfer, and generates a STOP condition. However, since requiring the master to keep track of the memory address counter is impractical, the following method should be used to perform reads from a specified memory location.

Manipulating the Address Counter for Reads: A dummy write cycle can be used to force the address counter (or pointer) to a particular value. To do this, the master generates a START condition, writes the slave address byte (R/$\overline{W}$ = 0), writes the memory address where it desires to read, generates a repeated START condition, writes the slave address byte (R/$\overline{W}$ = 1), reads data with ACK or NACK as applicable, and generates a STOP condition. Recall that the master must NACK the last byte to inform the slave that no additional bytes will be read. See Figure 9 for I^{2}C communication examples.

Reading Multiple Bytes from a Slave: The read operation can be used to read multiple bytes with a single transfer. When reading bytes from the slave, the master simply ACKs the data byte if it desires to read another byte before terminating the transaction. After the master reads the last byte it must NACK to indicate the end of the transfer and generates a STOP condition.

Applications Information

Power-Supply Decoupling

To achieve best results, it is recommended that the power supply is decoupled with a 0.01µF or a 0.1µF capacitor. Use high-quality, ceramic, surface-mount capacitors, and mount the capacitors as close as possible to the V_{CC} and GND pins to minimize lead inductance.

SDA and SCL Pullup Resistors

SDA is an open-collector output on the DS1683 that requires a pullup resistor to realize high-logic levels. An I^{2}C master using either an open-collector output with a pullup resistor or a push-pull output driver can be used for SCL. Pullup resistor values should be chosen to ensure that the rise and fall times listed in the *I^{2}C AC Electrical Characteristics* are within specification.

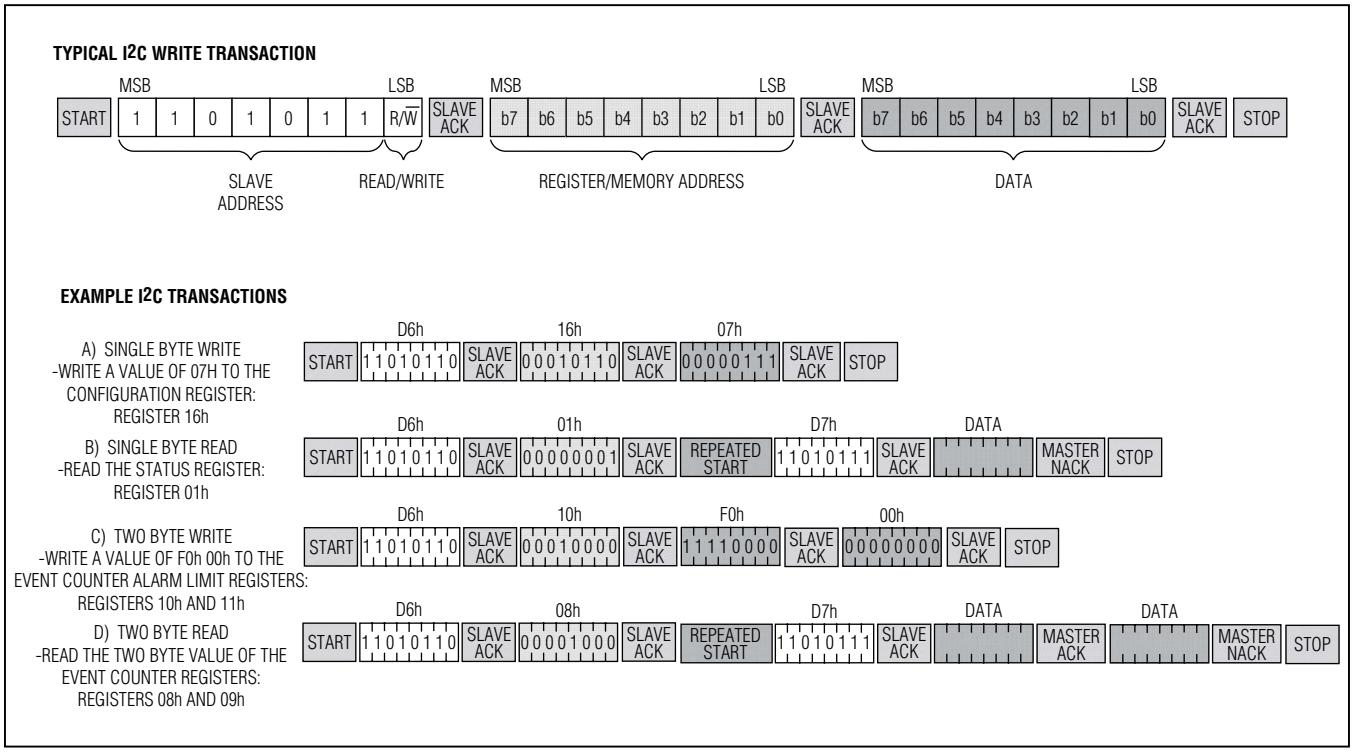


Figure 9. I2C Examples

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
DS1683S+	-40°C to +85°C	8 SO
DS1683S+T&R	-40°C to +85°C	8 SO

+Denotes a lead(Pb)-free/RoHS-compliant package.
T&R = Tape and reel.

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
8 SO	S8+4	21-0041	90-0096

Total-Elapsed-Time and Event Recorder with Alarm

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/12	Initial release	—

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