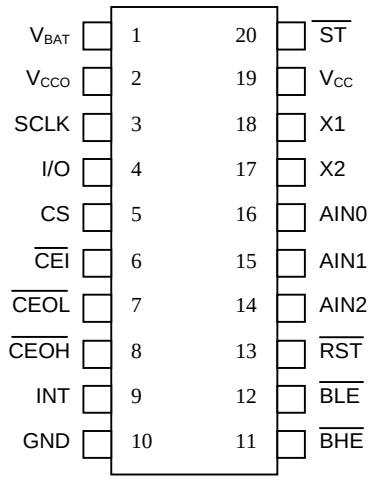
DS1673
Portable System Controller

www.dalsemi.com

FEATURES

- Provides Real Time Clock:
  - Counts seconds, minutes, hours, date of the month, month, day of the week, and year with leap year compensation valid up to 2100
  - Power control circuitry supports system power on from day/time alarm
- Microprocessor monitor:
  - Halts microprocessor during power-fail
  - Automatically restarts microprocessor after power failure
  - Monitors pushbutton for external override
  - Halts and resets an out of control microprocessor
- NV RAM control:
  - Automatic battery backup and write protection to external SRAM
- 3-channel, 8-bit analog-to-digital converter
- Simple 3-wire interface
- +3.0 or +5.0V operation

PIN ASSIGNMENT



20-Pin TSSOP
20-Pin SOIC

ORDERING INFORMATION

DS1673E - X	20-Pin TSSOP
DS1673S - X	20-Pin SOIC
	3 +3V operation
	5 +5V operation

DESCRIPTION

The Portable System Controller is a circuit which incorporates many of the functions necessary for low power portable products integrated into one chip. The DS1673 provides a Real Time Clock, NV RAM controller, microprocessor monitor, and a 3-channel, 8-bit analog-to-digital converter. Communication with the DS1673 is established through a simple 3-wire interface.

The Real Time Clock (RTC) provides seconds, minutes, hours, day, date, month, and year information with leap year compensation. The RTC also provides an alarm interrupt. This interrupt works when the DS1673 is powered by the system power supply or when in battery backup operation so the alarm can be used to wake up a system that is powered down.

Automatic backup and write protection of external SRAM is provided through the V_{CCO}, $\overline{CEOL}$, and $\overline{CEOH}$ pins. The backup energy source used to power the RTC is also used to retain RAM data in the absence of V_{CC} through the V_{CCO} pin. The chip enable outputs to RAM ($\overline{CEOL}$ and $\overline{CEOH}$) are controlled during power transients to prevent data corruption.

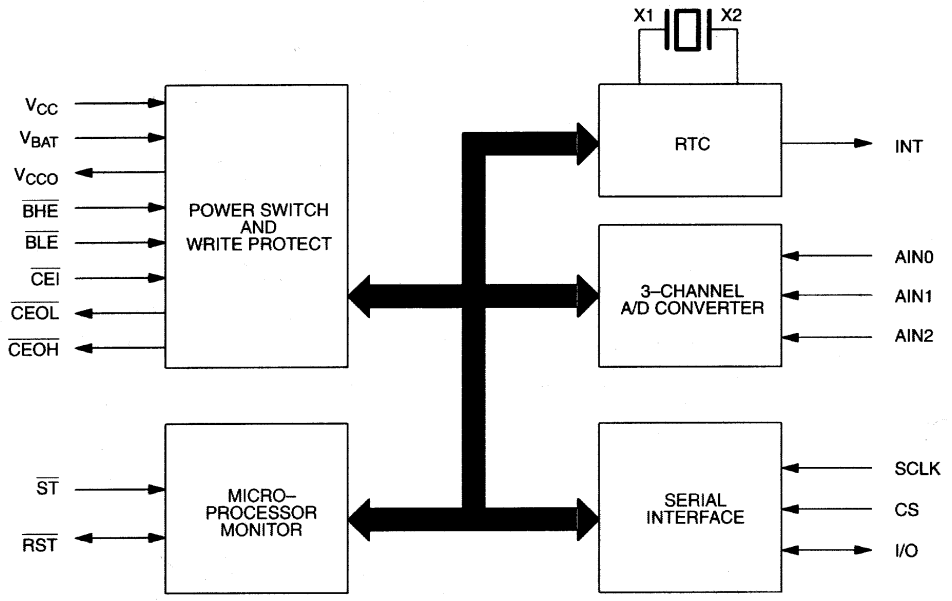
The microprocessor monitor circuitry of the DS1673 provides three basic functions. First, a precision temperature-compensated reference and comparator circuit monitors the status of V_{CC}. When an out-of-tolerance condition occurs, an internal power-fail signal is generated which forces the reset to the active state. When V_{CC} returns to an in-tolerance condition, the reset signals are kept in the active state for 250 ms to allow the power supply and processor to stabilize. The second microprocessor monitor function is pushbutton reset control. The DS1673 debounces a pushbutton input and guarantees an active reset pulse width of 250 ms. The third function is a watchdog timer. The DS1673 has an internal timer that forces the reset signals to the active state if the strobe input is not driven low prior to watchdog time-out.

The DS1673 also provides a 3-channel, 8-bit successive approximation analog-to-digital converter. The converter has an internal 2.55 volt (typical) reference voltage generated by an on-board band-gap circuit. The A/D converter is monotonic (no missing codes) and has an internal analog filter to reduce high frequency noise.

OPERATION

The block diagram in Figure 1 shows the main elements of the DS1673. The following paragraphs describe the function of each pin.

DS1673 BLOCK DIAGRAM Figure 1



SIGNAL DESCRIPTIONS

V_{CC}, GND - DC power is provided to the device on these pins. V_{CC} is the +3.0 volt or +5.0 volt input.

V_{BAT} (Backup Power Supply) - Battery input for standard 3-volt lithium cell or other energy source.

SCLK (Serial Clock Input) - SCLK is used to synchronize data movement on the serial interface.

I/O (Data Input/Output) - The I/O pin is the bi-directional data pin for the 3-wire interface.

CS (Chip Select) - The Chip Select signal must be asserted high during a read or a write for communication over the 3-wire serial interface.

V_{CCO} (External SRAM Power Supply Output) - This pin is internally connected to V_{CC} when V_{CC} is within nominal limits. However, during power-fail V_{CCO} is internally connected to the V_{BAT} pin. Switchover occurs when V_{CC} drops below V_{CCSW}.

INT (Interrupt Output) - The INT pin is an active high output of the DS1673 that can be used as an interrupt input to a microprocessor. The INT output remains high as long as the status bit causing the interrupt is present and the corresponding interrupt-enable bit is set. The INT pin operates when the DS1673 is powered by V_{CC} or V_{BAT}.

$\overline{\text{CEI}}$ (RAM Chip Enable In) - $\overline{\text{CEI}}$ must be driven low to enable the external RAM.

$\overline{\text{BLE}}$ (Byte Low Enable Input) - This pin when driven low activates the $\overline{\text{CEOL}}$ output if $\overline{\text{CEI}}$ is also driven low.

$\overline{\text{BHE}}$ (Byte High Enable Input) - This pin when driven low activates the $\overline{\text{CEOH}}$ output if $\overline{\text{CEI}}$ is also driven low.

$\overline{\text{CEOL}}$ (RAM Chip Enable Out Low) – Chip enable output for low order SRAM byte.

$\overline{\text{CEOH}}$ (RAM Chip Enable Out High) – Chip enable output for high order SRAM byte.

$\overline{\text{ST}}$ (Strobe Input) - The Strobe input pin is used in conjunction with the watchdog timer. If the $\overline{\text{ST}}$ pin is not driven low within the watchdog time period, the $\overline{\text{RST}}$ pin is driven low.

$\overline{\text{RST}}$ (Reset) - The $\overline{\text{RST}}$ pin functions as a microprocessor reset signal. This pin is driven low 1) when V_{CC} is outside of nominal limits; 2) when the watchdog timer has "timed out"; 3) during the power-up reset period; and 4) in response to a pushbutton reset. The $\overline{\text{RST}}$ pin also functions as a pushbutton reset input. When the $\overline{\text{RST}}$ pin is driven low, the signal is debounced and timed such that a $\overline{\text{RST}}$ signal of at least 250 ms is generated. This pin has an internal 47 kΩ pullup resistor.

AIN0, AIN1, AIN2 (Analog Inputs) - These pins are the three analog inputs for the 3-channel analog-to-digital converter.

X1, X2 - Connections for a standard 32.768 kHz quartz crystal. For greatest accuracy, the DS1673 must be used with a crystal that has a specified load capacitance of 6 pF. There is no need for external capacitors or resistors. Note: X1 and X2 are very high impedance nodes. It is recommended that they and the crystal be guard-ringed with ground and that high frequency signals be kept away from the crystal area. For more information on crystal selection and crystal layout considerations, please consult Application Note 58, "Crystal Considerations with Dallas Real Time Clocks."

The DS1673 will not function without a crystal.

POWER-UP/POWER-DOWN CONSIDERATIONS

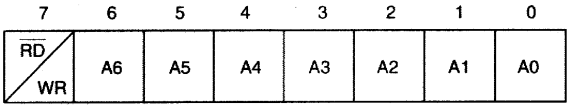
When V_{CC} is applied to the DS1673 and reaches a level greater than V_{CCTP} (power-fail trip point), the device becomes fully accessible after t_{RPU} (250 ms typical). Before t_{RPU} elapses, all inputs are disabled. When V_{CC} drops below V_{CCSW}, the device is switched over to the V_{BAT} supply.

During power-up, when V_{CC} returns to an in-tolerance condition, the $\overline{RST}$ pin is kept in the active state for 250 ms (typical) to allow the power supply and microprocessor to stabilize.

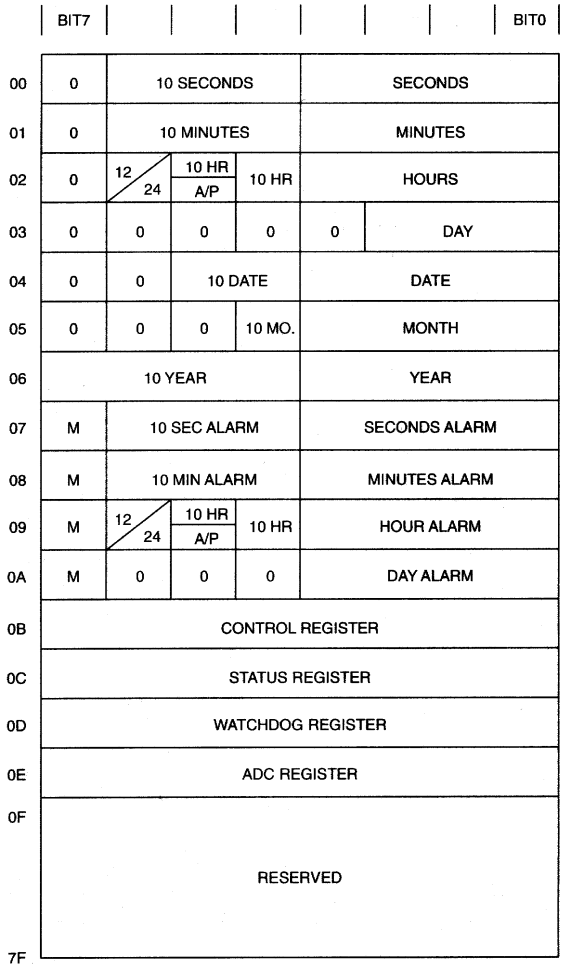
ADDRESS/COMMAND BYTE

The command byte for the DS1673 is shown in Figure 2. Each data transfer is initiated by a command byte. Bits 0 through 6 specify the address of the registers to be accessed. The MSB (bit 7) is the Read/Write bit. This bit specifies whether the accessed byte will be read or written. A read operation is selected if bit 7 is a 0 and a write operation is selected if bit 7 is a one. The address map for the DS1673 is shown in Figure 3.

ADDRESS/COMMAND BYTE Figure 2



DS1673 ADDRESS MAP Figure 3



CLOCK, CALENDAR AND ALARM

The time and calendar information is accessed by reading/writing the appropriate register bytes. Note that some bits are set to 0. These bits will always read 0 regardless of how they are written. Also note that registers 0Fh to 7Fh are reserved. These registers will always read 0 regardless of how they are written. The contents of the time, calendar, and alarm registers are in the Binary-Coded Decimal (BCD) format. The DS1673 can run in either 12-hour or 24-hour mode. Bit 6 of the hours register is defined as the 12- or 24-hour mode select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the AM/PM bit with logic 1 being PM. In the 24-hour mode, bit 5 is the second 10-hour bit (20-23 hours).

The DS1673 also contains a time of day alarm. The alarm registers are located in registers 07h to 0Ah. Bit 7 of each of the alarm registers are mask bits (see Table 1). When all of the mask bits are logic 0, an alarm will occur once per week when the values stored in timekeeping registers 00h to 03h match the values stored in the time of day alarm registers. An alarm will be generated every day when mask bit of the day alarm register is set to 1. An alarm will be generated every hour when the day and hour alarm mask bits are set to 1. Similarly, an alarm will be generated every minute when the day, hour, and minute alarm mask bits are set to 1. When day, hour, minute, and seconds alarm mask bits are set to 1, an alarm will occur every second.

TIME OF DAY ALARM BITS Table 1

ALARM REGISTER MASK BITS (BIT 7)				
SECONDS	**MINUTES**	**HOURS**	**DAYS**	
1	1	1	1	Alarm once per second.
0	1	1	1	Alarm when seconds match.
0	0	1	1	Alarm when minutes and seconds match.
0	0	0	1	Alarm when hours, minutes and seconds match.
0	0	0	0	Alarm when day, hours, minutes and seconds match.

SPECIAL PURPOSE REGISTERS

The DS1673 has two additional registers (control register and status register) that control the Real Time Clock and interrupts.

CONTROL REGISTER

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
$\overline{\text{EOSC}}$	WP	AIS1	AIS0	0	0	0	AIE

$\overline{\text{EOSC}}$ (Enable Oscillator) - This bit, when set to logic 0 will start the oscillator. When this bit is set to a logic 1, the oscillator is stopped and the DS1673 is placed into a low-power standby mode with a current drain of less than 200 nanoamps when in battery back-up mode. When the DS1673 is powered by V_{CC}, the oscillator is always on regardless of the status of the $\overline{\text{EOSC}}$ bit; however, the Real Time Clock is incremented only when $\overline{\text{EOSC}}$ is a logic 0.

WP (Write Protect) - Before any write operation to the Real Time Clock or any other registers, this bit must be logic 0. When high, the write protect bit prevents a write operation to any register.

AIS0-AIS1 (Analog Input Select) - These 2 bits are used to determine the analog input for the analog-to-digital conversion. Table 2 lists the specific analog input that is selected by these 2 bits.

AIE (Alarm Interrupt Enable) - When set to a logic 1, this bit permits the Interrupt Request Flag (IRQF) bit in the status register to assert INT. When the AIE bit is set to logic 0, the IRQF bit does not initiate the INT signal.

ANALOG INPUT SELECTION Table 2

AIS1	AIS0	ANALOG INPUT
0	0	NONE
0	1	AIN0
1	0	AIN1
1	1	AIN2

STATUS REGISTER

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CU	LOBAT	0	0	0	0	0	IRQF

CU (Conversion Update In Progress) - When this bit is a 1, an update to the ADC Register (register 0Eh) will occur within 488 µs. When this bit is a 0, an update to the ADC Register will not occur for at least 244 µs.

LOBAT (Low Battery Flag) - This bit reflects the status of the backup power source connected to the V_{BAT} pin. When V_{BAT} is greater than 2.5 volts, LOBAT is set to a logic 0. When V_{BAT} is less than 2.3 volts, LOBAT is set to a logic 1.

IRQF (Interrupt Request Flag) - A logic 1 in the Interrupt Request Flag bit indicates that the current time has matched the time of day Alarm registers. If the AIE bit is also a logic 1, the INT pin will go high. IRQF is cleared by reading or writing to any of the alarm registers.

NONVOLATILE SRAM CONTROLLER

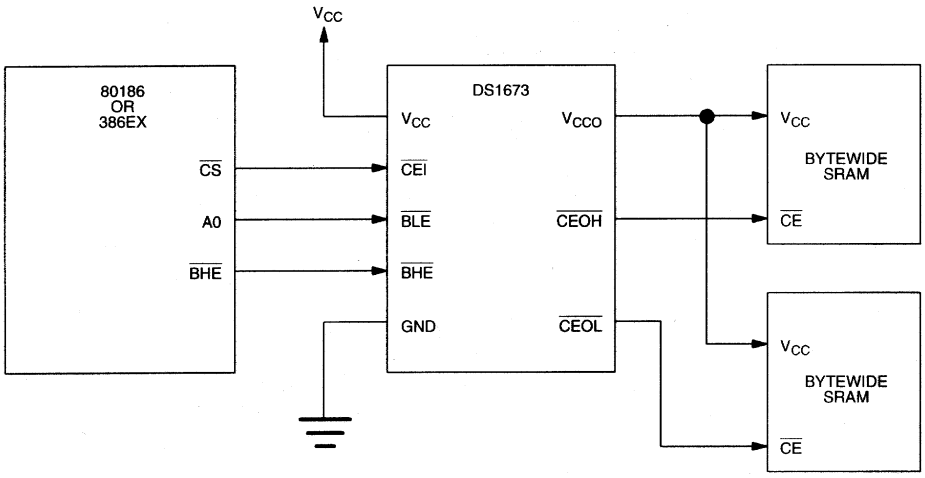
The DS1673 provides automatic backup and write protection for external SRAM. This function is provided by gating the chip enable signals and by providing a constant power supply through the V_{CCO} pin. The DS1673 was specifically designed with the Intel 80186 and 386EX microprocessors in mind. As such, the DS1673 has the capability to provide access to the external SRAM in either byte-wide or word-wide format. This capability is provided by the chip enable scheme. Three input signals and two output signals are used for enabling the external SRAM(s) (see Figure 4). $\overline{CEI}$ (chip enable in), $\overline{BHE}$ (byte high enable), and $\overline{BLE}$ (byte low enable) are used for enabling either one or two external SRAMs through the $\overline{CEOL}$ (chip enable low) and the $\overline{CEOH}$ (chip enable high) outputs. Table 3 illustrates the function of these pins.

The DS1673 nonvolatilizes the external SRAM(s) by write-protecting the SRAM(s) and by providing a back-up power supply in the absence of V_{CC}. When V_{CC} falls below V_{PF}, access to the external SRAM(s) are prohibited by forcing $\overline{CEOL}$ and $\overline{CEOH}$ high regardless of the level of $\overline{CEI}$, $\overline{BLE}$, and $\overline{BHE}$. Upon power-up, access is prohibited until the end of t_{RPU}.

EXTERNAL SRAM CHIP ENABLE Table 3

$\overline{CEI}$	$\overline{BHE}$	$\overline{BLE}$	$\overline{CEOL}$	$\overline{CEOH}$	FUNCTION
0	0	0	0	0	Word transfer
0	0	1	1	0	Byte transfer in upper half of data bus (D15-D8)
0	1	0	0	1	Byte transfer in lower half of data bus (D7-D0)
0	1	1	1	1	External SRAMs disabled
1	X	X	1	1	External SRAMs disabled

EXTERNAL SRAM INTERFACE (WORD-WIDE) TO THE DS1673 Figure 4



MICROPROCESSOR MONITOR

The DS1673 monitors three vital conditions for a microprocessor: power supply, software execution, and external override.

First, a precision temperature-compensated reference and comparator circuit monitors the status of V_{CC}. When an out-of-tolerance condition occurs, an internal power-fail signal is generated which forces the $\overline{RST}$ pin to the active state, thus warning a processor-based system of impending power failure. When V_{CC} returns to an in-tolerance condition upon power-up, the reset signal is kept in the active state for 250 ms (typical) to allow the power supply and microprocessor to stabilize. Note, however, that if the $\overline{EOSC}$ bit is set to a logic 1 (to disable the oscillator during battery back-up mode), the reset signal will be kept in an active state for 250 ms plus the start-up time of the oscillator.

The second monitoring function is push-button reset control. The DS1673 provides for a pushbutton switch to be connected to the $\overline{RST}$ output pin. When the DS1673 is not in a reset cycle, it continuously monitors the $\overline{RST}$ signal for a low going edge. If an edge is detected, the DS1673 will debounce the switch by pulling the $\overline{RST}$ line low. After the internal 250 ms timer has expired, the DS1673 will continue to monitor the $\overline{RST}$ line. If the line is still low, the DS1673 will continue to monitor the line looking for a rising edge. Upon detecting release, the DS1673 will force the $\overline{RST}$ line low and hold it low for 250 ms.

The third microprocessor monitoring function provided by the DS1673 is a watchdog timer. The watchdog timer function forces $\overline{RST}$ to the active state when the $\overline{ST}$ input is not stimulated within the predetermined time period. The time period is set by the Time Delay (TD) bits in the Watchdog Register. The time delay can be set to 250 ms, 500 ms, or 1000 ms (see Figure 5). If TD0 and TD1 are both set to zero, the watchdog timer is disabled. When enabled, the watchdog timer starts timing out from the set time period as soon as $\overline{RST}$ is inactive. The default setting is for the watchdog timer to be enabled with 1000 ms time delay. If a high-to-low transition occurs on the $\overline{ST}$ input pin prior to time-out, the watchdog timer is reset and begins to time-out again. If the watchdog timer is allowed to time-out, then the $\overline{RST}$ signal is driven to the active state for 250 ms (typical). The $\overline{ST}$ input can be derived from microprocessor address signals, data signals, and/or control signals. To guarantee that the watchdog timer does not time-out, a high-to-low transition must occur at or less than the minimum period.

WATCHDOG TIME-OUT CONTROL Figure 5

WATCHDOG REGISTER

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	0	0	0	0	0	TD1	TD0

WATCHDOG REGISTER

TD1	TD0	WATCHDOG TIME-OUT
0	0	WATCHDOG DISABLED
0	1	250 ms
1	0	500 ms
1	1	1000 ms

ANALOG-TO-DIGITAL CONVERTER

The DS1673 provides a 3-channel, 8-bit analog-to-digital converter. The A/D reference voltage (2.55V typical) is derived from an on-chip band-gap circuit. Three multiplexed analog inputs are provided through the AIN0, AIN1, and AIN2 pins. The A/D converter is monotonic (no missing codes) and uses a successive approximation technique to convert the analog signal into a digital code.

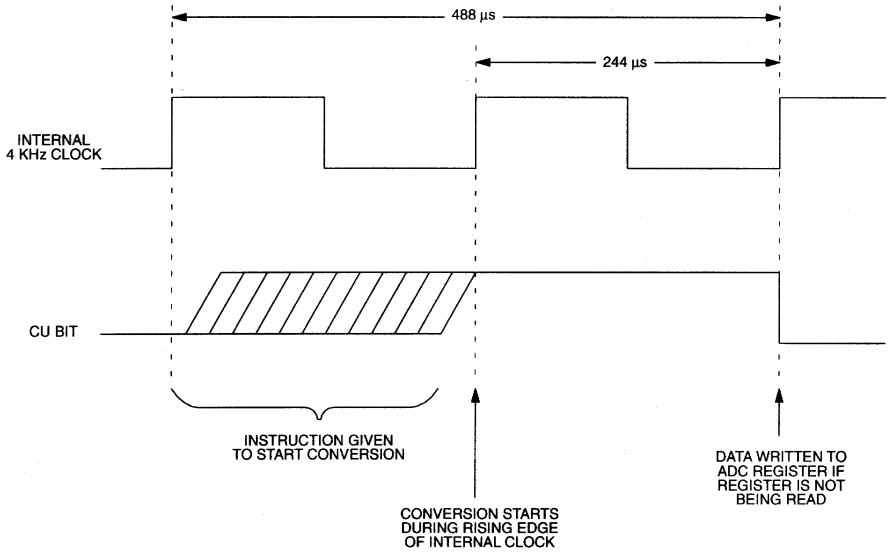
An A/D conversion is the process of assigning a digital code to an analog input voltage. This code represents the input value as a fraction of the full-scale voltage (FSV) range. Thus the FSV range is then divided by the A/D converter into 256 codes (8 bits). The FSV range is bounded by an upper limit equal to the reference voltage and the lower limit which is ground. The DS1673 has a FSV of 2.55V (typical) which provides a resolution of 10 mV. An input voltage equal to the reference voltage converts to FFh while an input voltage equal to ground converts to 00h. The relative linearity of the A/D converter is ±0.5 LSB.

The A/D converter selects from one of three different analog inputs (AIN0 - AIN2). The input that is selected is determined by the Analog Input Select (AIS) bits in the Control Register. Table 2 lists the specific analog input that is selected by these 2 bits. Note also that the converter can be turned off by these bits to reduce power. When the A/D is turned on by setting AIS0 and AIS1 to any value other than 0,0 the analog input voltage is converted and written to the ADC Register within 488 µs. An internal analog filter at the input reduces high frequency noise. Subsequent updates occur approximately every 10 ms. If AIS0 and/or AIS1 are changed, updates will occur at the next 10 ms conversion time.

The Conversion Update In Progress (CU) bit in the Status Register indicates when the ADC Register can be read. When this bit is a 1, an update to the ADC Register will occur within 488 µs maximum. However, when this bit is 0 an update will not occur for at least 244 µs. The CU bit should be polled before reading the ADC Register to insure that the contents are stable during a read cycle. Once a read cycle to the ADC Register has been started, the DS1673 will not update that register until the read cycle has been completed. It should also be mentioned that taking CS low will abort the read cycle and will allow the ADC Register to be updated.

Figure 6 illustrates the timing of the CU bit relative to an instruction to begin conversion and the completion of that conversion.

CU BIT TIMING Figure 6



3-WIRE SERIAL INTERFACE

Communication with the DS1673 is accomplished through a simple 3-wire interface consisting of the Chip Select (CS), Serial Clock (SCLK) and Input/Output (I/O) pins.

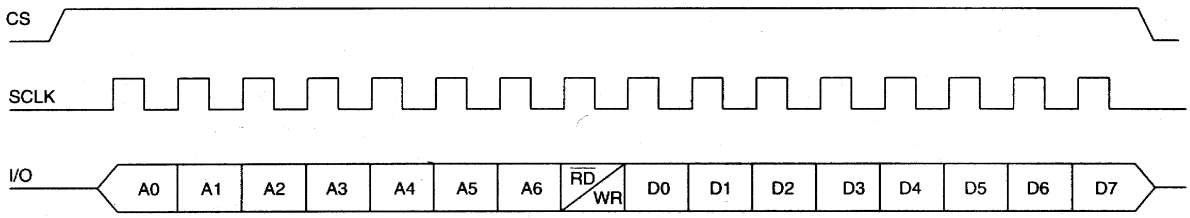
All data transfers are initiated by driving the CS input high. The CS input serves two functions. First, CS turns on the control logic which allows access to the shift register for the address/command sequence. Second, the CS signal provides a method of terminating either single byte or multiple byte (burst) data transfer. A clock cycle is a sequence of a rising edge followed by a falling edge. For data input, data must be valid during the rising edge of the clock and data bits are output on the falling edge of the clock. If the CS input goes low, all data transfer terminates and the I/O pin goes to a high impedance state.

Address and data bytes are always shifted LSB first into the I/O pin. Any transaction requires the address/command byte to specify a read or write to a specific register followed by 1 or more bytes of data. The address byte is always the first byte entered after CS is driven high. The most significant bit ($\overline{RD}$/WR) of this byte determines if a read or write will take place. If this bit is 0, one or more read cycles will occur. If this bit is 1, one or more write cycles will occur.

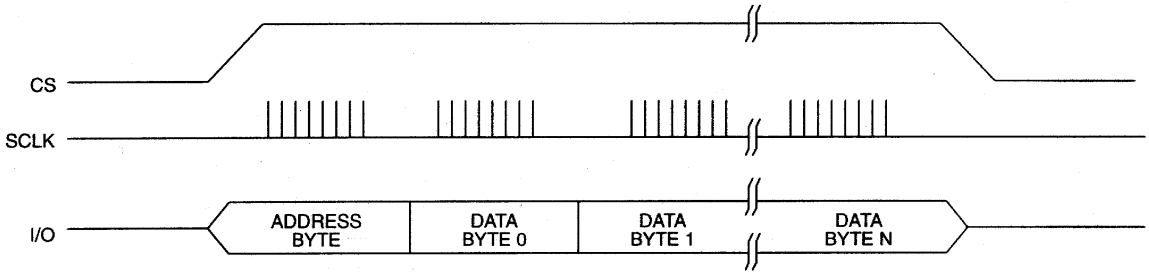
Data transfers can occur 1 byte at a time or in multiple byte burst mode. After CS is driven high an address is written to the DS1673. After the address, 1 or more data bytes can be read or written. For a single-byte transfer 1 byte is read or written and then CS is driven low. For a multiple-byte transfer, multiple bytes can be read or written to the DS1673 after the address has been written. Each read or write cycle causes the register address to automatically increment. Incrementing continues until the device is disabled. After accessing register 0Eh, the address wraps to 00h.

Data transfer for single-byte transfer and multiple-byte burst transfer is illustrated in Figures 7 and 8.

SINGLE-BYTE DATA TRANSFER Figure 7



MULTIPLE-BYTE BURST TRANSFER Figure 8



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	See J-STD-020A

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage 5 Volt Operation	V_{CC}	4.5	5.0	5.5	V	1
Power Supply Voltage 3 Volt Operation	V_{CC}	2.7	3.0	3.3	V	1
Input Logic 1	V_{IH}	2.0		V_{CC}+0.3	V	1
Input Logic 0	V_{IL}	-0.3		+0.8	V	1
Battery Voltage	V_{BAT}	2.5		3.7	V	1

DC ELECTRICAL CHARACTERISTICS (0°C to 70°C; V_{CC}=5.0V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I_{LI}	-1		+1	µA	
CS Leakage	I_{LO}			150	µA	7
Logic 1 Output	V_{OH}	2.4			V	2
Logic 0 Output	V_{OL}			0.4	V	3
Active Supply Current (CS=V_{CC} -0.2)	I_{CCA}		1.5	2.0	mA	4
A/D Converter Current	I_{ADC}			500	µA	5
Standby Current (CS=V_{IL})	I_{CCS}			300	µA	6
Oscillator Current	I_{OSC}		300	500	nA	
Battery Standby Current (Oscillator Off)	I_{BAT}			200	nA	
Internal $\overline{RST}$ Pullup Resistor	R_P	35	47	60	kΩ	
V_{CC} Trip Point	V_{CCTP}	4.25	4.35	4.50	V	
V_{CC} Switchover	V_{CCSW}	2.60	2.70	2.80	V	12
A/D Reference Voltage	V_{ADC}	2.47	2.55	2.63	V	
Pushbutton Detect	PB_{DV}	0.8		2.0	V	
Pushbutton Release	PB_{RD}		0.3	0.8	V	
Output Voltage	V_{CCO}	V_{CC}-0.3			V	11
V_{CCO} Output Current (Source=V_{CC})	I_{CCO1}			150	mA	13
V_{CCO} Output Current (Source=V_{BAT})	I_{CCO2}			150	µA	14

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC}=3.0V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I_{LI}	-1		+1	µA	
CS Leakage	I_{LO}			150	µA	7
Logic 1 Output	V_{OH}	2.4			V	2
Logic 0 Output	V_{OL}			0.4	V	3
Active Supply Current (CS=V_{CC} -0.2)	I_{CCA}		0.75	1.0	mA	4
A/D Converter Current	I_{ADC}			200	µA	5
Standby Current (CS=V_{IL})	I_{CCS}			100	µA	6
Oscillator Current	I_{OSC}		300	500	nA	
Battery Standby Current (Oscillator Off)	I_{BAT}			200	nA	
Internal $\overline{RST}$ Pullup Resistor	R_P	35	47	60	kΩ	
V_{CC} Trip Point	V_{CCTP}	2.5	2.6	2.7	V	
V_{CC} Switchover	V_{CCSW}	2.30	2.40	2.50	V	12
A/D Reference Voltage	V_{ADC}	2.47	2.55	2.63	V	
Pushbutton Detect	PB_{DV}	0.8		2.0	V	
Pushbutton Release	PB_{RD}		0.3	0.8	V	
Output Voltage	V_{CCO}	V_{CC}-0.3			V	11
V_{CCO} Output Current (Source=V_{CC})	I_{CCO1}			80	mA	13
V_{CCO} Output Current (Source=V_{BAT})	I_{CCO2}			100	µA	14

CAPACITANCE

(t_A=25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_I		10		pF	
I/O Capacitance	$C_{I/O}$		15		pF	
Crystal Capacitance	C_X		6		pF	

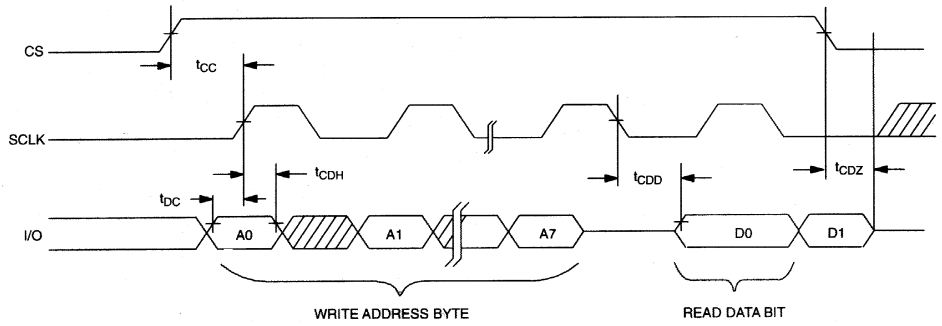
AC ELECTRICAL CHARACTERISTICS (0°C to 70°C; V_{CC}=5.0V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data to Clock Setup	t_{DC}	50			ns	8
CLK to Data Hold	t_{CDH}	70			ns	8
CLK to Data Delay	t_{CDD}			200	ns	8, 9, 10
CLK to Low Time	t_{CL}	250			ns	8
CLK to High Time	t_{CH}	250			ns	8
CLK Frequency	t_{CLK}			2.0	MHz	8
CLK Rise and Fall	t_R, t_F			500	ns	
CS to CLK Setup	t_{CC}	1			µs	8
CLK to CS Hold	t_{CCH}	60			ns	8
CS Inactive Time	t_{CWH}	1			µs	8
CS to I/O High-Z	t_{CDZ}			70	ns	8
V_{CC} Slew Rate (4.5V to 2.3V)	t_F	1			ms	
V_{CC} Slew Rate (2.3V to 4.5V)	t_R	0			ns	
V_{CC} Detect to $\overline{RST}$ (V_{CC} Falling)	t_{RPD}			100	ns	
Reset Active Time	t_{RST}		250		ms	15
Pushbutton Debounce	PB_{DB}		250		ms	15
V_{CC} Detect to $\overline{RST}$ (V_{CC} Rising)	t_{RPU}		250		ms	15, 16
$\overline{ST}$ Pulse Width	t_{ST}	20			ns	
Chip Enable Propagation Delay to External SRAM	t_{CED}		8	15	ns	
Nominal Voltage to V_{CC} Switchover Fall Time	t_{FB}	200			µs	

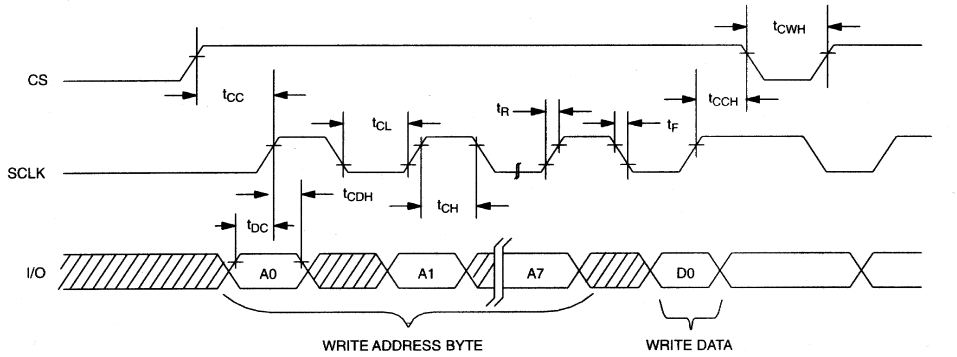
AC ELECTRICAL CHARACTERISTICS (0°C to 70°C; V_{CC}=3.0V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data to Clock Setup	t_{DC}	150			ns	8
CLK to Data Hold	t_{CDH}	210			ns	8
CLK to Data Delay	t_{CDD}			600	ns	8, 9, 10
CLK to Low Time	t_{CL}	750			ns	8
CLK to High Time	t_{CH}	750			ns	8
CLK Frequency	t_{CLK}			0.667	MHz	8
CLK Rise and Fall	t_R, t_F			1500	ns	
CS to CLK Setup	t_{CC}	3			µs	8
CLK to CS Hold	t_{CCH}	180			ns	8
CS Inactive Time	t_{CWH}	3			µs	8
CS to I/O High-Z	t_{CDZ}			210	ns	8
V_{CC} Slew Rate (2.7V to 2.3V)	t_F	300			µs	
V_{CC} Slew Rate (2.3V to 2.7V)	t_R	0			ns	
V_{CC} Detect to $\overline{RST}$ (V_{CC} Falling)	t_{RPD}			200	ns	
Reset Active Time	t_{RST}		250		ms	15
Pushbutton Debounce	PB_{DB}		250		ms	15
V_{CC} Detect to $\overline{RST}$ (V_{CC} Rising)	t_{RPU}		250		ms	15, 16
$\overline{ST}$ Pulse Width	t_{ST}	40			ns	
Chip Enable Propagation Delay to External SRAM	t_{CED}		8	25	ns	
Nominal Voltage to V_{CC} Switchover Fall Time	t_{FB}	300			µs	

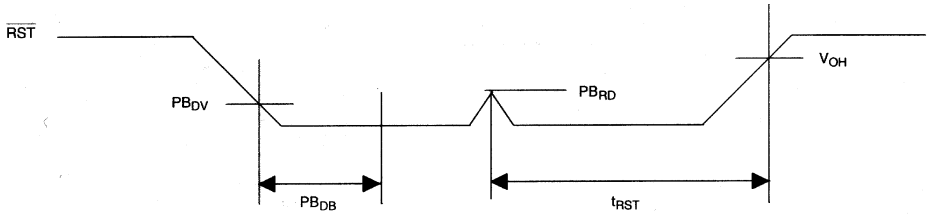
TIMING DIAGRAM: READ DATA Figure 9



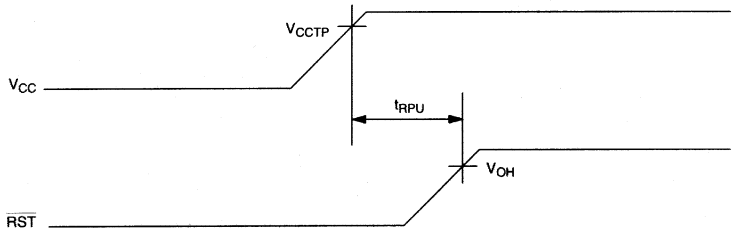
TIMING DIAGRAM: WRITE DATA Figure 10



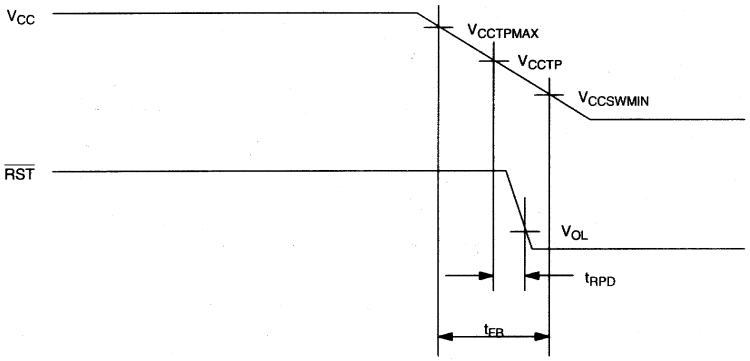
PUSHBUTTON RESET Figure 11



POWER-UP Figure 12



POWER-DOWN Figure 13



NOTES:

1. All voltages are referenced to ground.

2. Logic 1 voltages are specified at a source current of 0.4 mA at V_{CC}=3.0V, V_{OH}=V_{CC} for capacitive loads.

3. Logic 0 voltages are specified at a sink current of 1.5 mA at V_{CC}=3.0, V_{OL}=GND for capacitive loads.

4. I_{CCA} is specified with outputs open, CS set to a logic 1, SCLK=500 kHz, oscillator enabled, and D/A converter enabled.

5. I_{ADC} is specified with CS, V_{CCO} open and I/O, SCLK at logic zero. A/D converter is enabled.

6. I_{CCS} is specified with CS, V_{CCO} open and I/O, SCLK at logic zero. A/D converter is disabled.

7. CS has a 40 kΩ pull-down resistor to ground.

8. Measured at V_{IH}=2.0V or V_{IL}=0.8V and 10 ns maximum rise and fall time.

9. Measured at V_{OH}=2.4V or V_{OL}=0.4V.

10. Load capacitance= 25 pF.

11. I_{CCO}=100 mA, $V_{CC} > V_{CCTP}$.

12. V_{CCO} switchover from V_{CC} to V_{BAT} occurs when V_{CC} drops below the lower of V_{CCSW} and V_{BAT}.

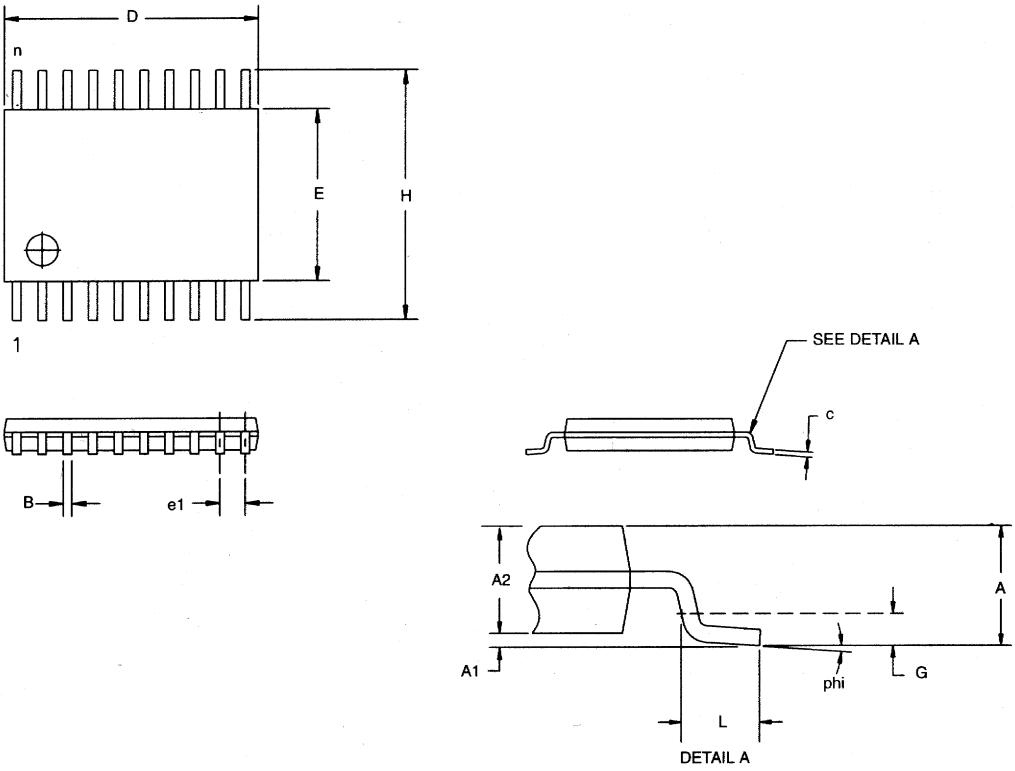
13. Current from V_{CC} input pin to V_{CCO} output pin.

14. Current from V_{BAT} input pin to V_{CCO} output pin.

15. Timebase is generated by very accurate crystal oscillator. Accuracy of this time period is based on the crystal that is used. A typical crystal with a specified load capacitance of 6 pF will provide an accuracy within ±100 ppm over the 0°C to 70°C temperature range.

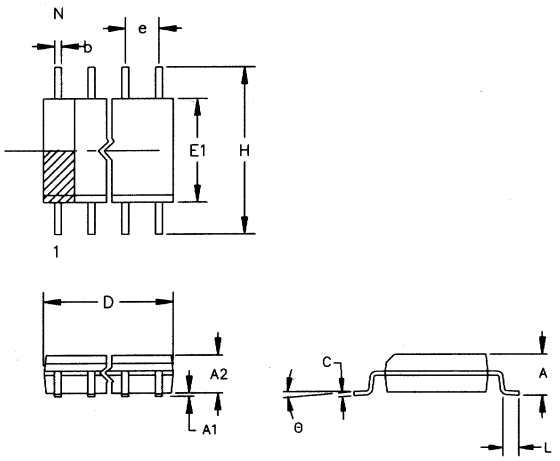
16. If the $\overline{\text{EOSC}}$ bit in the Control Register is set to a logic 1, t_{RPU} is equal to 250 ms plus the start-up time of the crystal oscillator.

20-PIN TSSOP (PRELIMINARY)



DIM	MIN	MAX
A MM	-	1.10
A1 MM	0.05	-
A2 MM	0.75	1.05
C MM	0.09	0.18
L MM	0.50	0.70
e1 MM	0.65 BSC	
B MM	0.18	0.30
D MM	6.40	6.90
E MM	4.40 NOM	
GMM	0.25 REF	
H MM	6.25	6.55
phi	0°	8°

20-PIN SOIC PACKAGE



The chamfer on the body is optional. If it is not present, a terminal 1 identifier must be positioned so that 1/2 or more of its area is contained in the hatched zone.

PKG	20-PIN	
DIM	**MIN**	**MAX**
A IN.	0.094	0.105
MM	2.38	2.68
A1 IN.	0.004	0.012
MM	0.102	0.30
A2 IN.	0.089	0.095
MM	2.26	2.41
b IN.	0.013	0.020
MM	0.33	0.51
C IN.	0.009	0.013
MM	0.229	0.33
D IN.	0.498	0.511
MM	12.65	12.99
e IN.	0.050 BSC	
MM	1.27 BSC	
E1 IN.	0.290	0.300
MM	7.37	7.62
H IN.	0.398	0.416
MM	10.11	10.57
L IN.	0.016	0.040
MM	0.406	1.20
Θ	0°	8°