DS1667
Digital Resistor with OP AMP

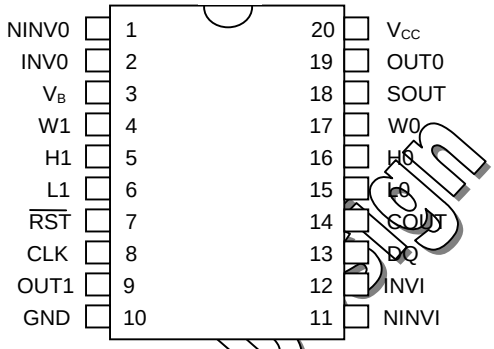
www.dalsemi.com

FEATURES

- Two digitally controlled 256-position potentiometers
- Serial port provides means for setting and reading both potentiometers
- Resistors can be connected in series to provide additional resolution
- Default wiper position on power up is 50%
- Resistive elements are temperature-compensated to +20% end to end
- Two high-gain, wide bandwidth operational amplifiers
- Low power CMOS design
- Applications include analog-to-digital and digital-to-analog converters, variable oscillators, and variable gain amplifiers
- 20-pin DIP package or optional 20-pin SOIC surface mount package
- Operating temperature range
  - Commercial: 0°C to 70°C
- Resistance values:

	RESOLUTION	-3 dB POINT
DS1667-10:	10k 39 ohms	1.1 MHz
DS1667-50:	50k 195 ohms	200 kHz
DS1667-100:	100k 390 ohms	100 kHz

PIN ASSIGNMENT



20-Pin DIP (300-mil) and 20-Pin SOIC
See Mech. Drawings Section

PIN DESCRIPTION

V_{CC}	- +5-Volt Supply
GND	- Ground
L0, L1	- Low End of Resistor
H0, H1	- High End of Resistor
W0, W1	- Wiper End of Resistor
V_B	- Substrate Bias and OP AMP Negative Supply
SOUT	- Wiper for Stacked Configuration
$\overline{RST}$	- Serial Port Reset Input
DQ	- Serial Port Input/Output
CLK	- Serial Port Clock Input
COUT	- Cascade Serial Port Output
NINV0, NINVI	- Noninverting OP AMP Input
INV0, INVI	- Inverting OP AMP Input
OUT0, OUT1	- OP AMP Outputs

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DESCRIPTION

The DS1667 is a dual-solid state potentiometer that is adjustable by digitally selected resistive elements. Each potentiometer is composed of 256 resistive elements. Between each resistive section of each potentiometer are tap points accessible to the wiper. The position of the wiper on the resistive array is set by an 8-bit register that controls which tap point is connected to the wiper output. Each 8-bit register can be read or written by sending or receiving data bits over a 3-wire serial port. In addition, the resistors can be stacked such that a single potentiometer of 512 sections results. When two separate potentiometers are used, the resolution of the DS1667 is equal to the resistance value divided by 256. When the potentiometers are stacked end to end, the resistance value is doubled while the resolution remains the

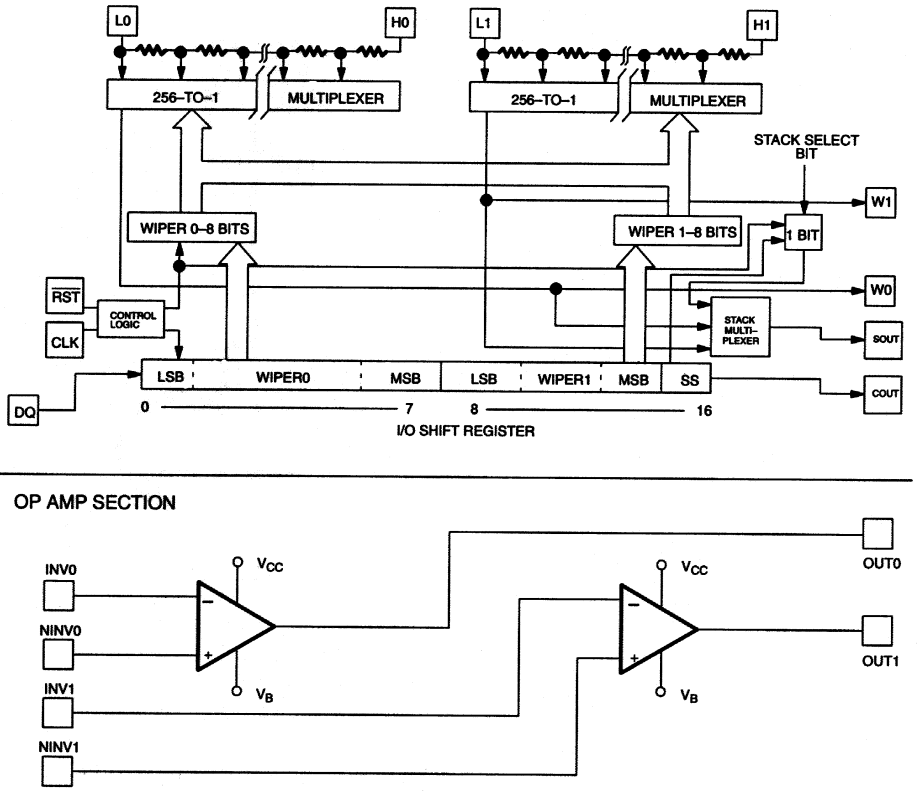
same. The DS1667 also contains two high gain wide bandwidth operational amplifiers. Each amplifier has both the inverting and non-inverting inputs and the output available for user configuration. The operational amplifiers can be paired with the resistive elements to perform such functions as analog to digital conversion, digital to analog conversion, variable gain amplifiers, and variable oscillators.

OPERATION - DIGITAL RESISTOR SECTION

The DS1667 contains two potentiometers, each of which has its wiper set by a value contained in an 8-bit register (see Figure 1). Each potentiometer consists of 256 resistors of equal value with tap points between each resistor and at the low end.

In addition, the potentiometer can be stacked by connecting them in series such that the high end of potentiometer 0 is connected to the low end of potentiometer 1. When stacking potentiometers, the stack select bit is used to select which potentiometer wiper will appear at the stack multiplexer output (SOUT). A zero written to the stack multiplexer will connect wiper 0 to the SOUT pin. This wiper will determine which of the 256 bottom taps of the stacked potentiometer is selected. When a 1 is written to the stack multiplexer, wiper 1 is selected and one of the upper 256 taps of the stacked potentiometer is presented at the SOUT pin.

BLOCK DIAGRAM Figure 1



Information is written to and read from the wiper 0 and wiper 1 registers and the stack select bit via the 17-bit I/O shift register. The I/O shift register is serially loaded by a 3-wire serial port consisting of $\overline{RST}$, DQ, and CLK. It is updated by transferring all 17 bits (Figure 2). Data can be entered into the 17-bit shift register only when the $\overline{RST}$ input is at a high level. While at a high level, the $\overline{RST}$ function allows serial entry of data via the D/Q pin. The potentiometers always maintain their previous value until $\overline{RST}$ is taken to a low level, which terminates data transfer. While $\overline{RST}$ input is low, the DQ and CLK inputs are ignored.

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Valid data is entered into the I/O shift register while $\overline{RST}$ is high on the low-to-high transition of the CLK input. Data input on the DQ pin can be changed while the clock input is high or low, but only data meeting the setup requirements will enter the shift register. Data is always entered starting with the value of the stack select bit. The next 8 bits to be entered are those specifying the wiper 1 setting. The MSB of these 8 bits is sent first. The next 8 bits to be entered are those specifying the wiper 0 setting, sent MSB first. The 17th bit to be entered, therefore, will be the least significant bit of the wiper 0 setting. If fewer than 17 bits are entered, the value of the potentiometer settings will result from the number of bits that were entered plus the remaining bits of the old value shifted over by the number of bits sent. If more than 17 bits are sent, only the last 17 bits are left in the shift register. Therefore, sending other than 17 bits can produce indeterminate potentiometer settings.

As bits are entered into the shift register, the previous value is shifted out bit by bit on the cascade serial port pin (COUT). By connecting the COUT pin to the DQ pin of a second DS1667, multiple devices can be daisy chained together as shown in Figure 3.

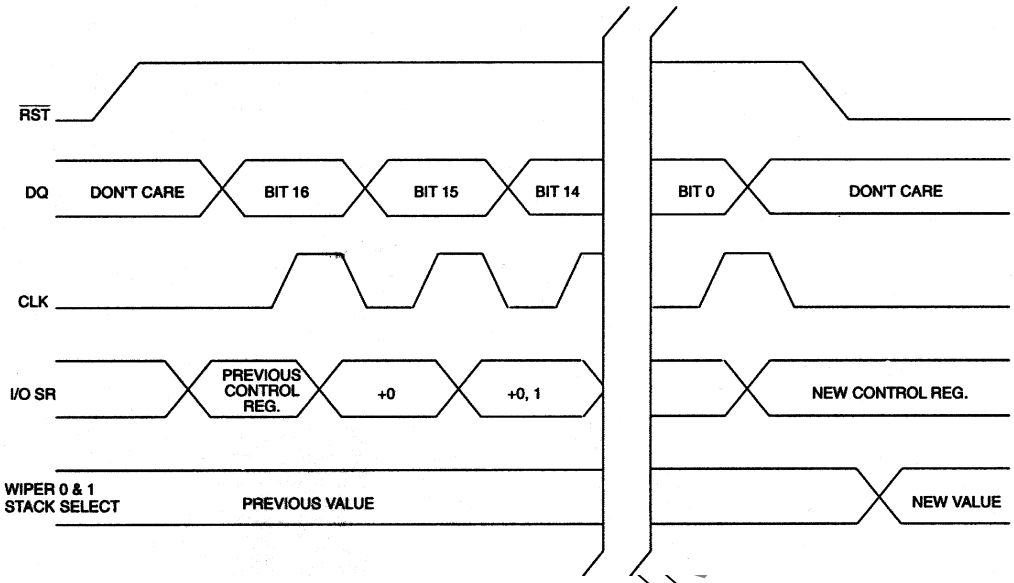
When connecting multiple devices, the total number of bits sent is always 17 times the number of DS1667s in the daisy chain. In applications where it is desirable to read the settings of potentiometers, the COUT pin of the last device connected in a daisy chain must be connected back to the DQ input of the first device through a resistor with a value of 1k to 10k. This resistor provides isolation between COUT and DQ when writing to the device (see Figure 3).

When reading data, the DQ line is left floating by the reading device. When $\overline{RST}$ is held low, bit 17 is always present on the COUT pin, which is fed back to the input DQ pin through the resistor (see Figure 4). This data bit can now be read by the reading device. The $\overline{RST}$ pin is then transitioned high to initiate a data transfer. When the CLK input transitions low to high, bit 17 is loaded into the first position of the I/O shift register and bit 16 becomes present on COUT and DQ. After 17 bits (or 17 times the number of devices for a daisy chain), the data has shifted completely around and back to its original position. When $\overline{RST}$ is transitioned back low to end data transfer, the value (the same as before the read occurred) is loaded into the wiper 0 and wiper 1 registers and the stack select bit.

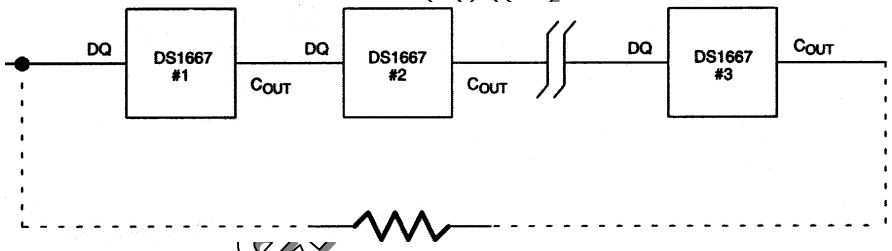
When power is applied to the DS1667, the device always has the wiper settings at half position and the stack select bit is at 0.

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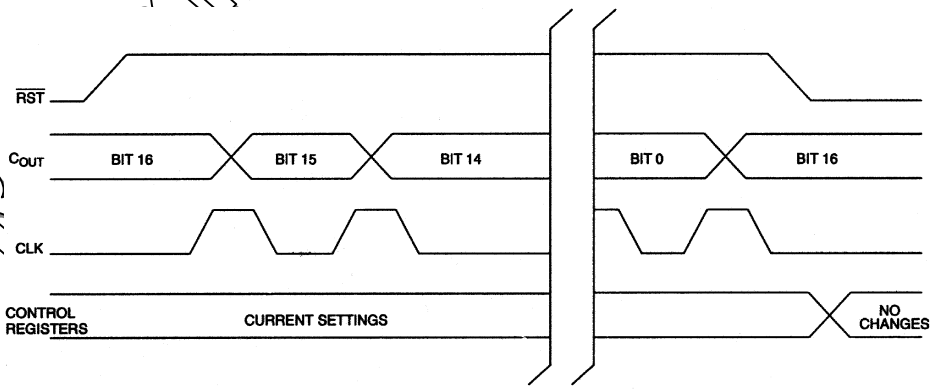
WRITING DATA Figure 2



CASCADING MULTIPLE DEVICES Figure 3



READING DATA Figure 4



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DS1667 LINEARITY MEASUREMENTS

An important specification for the DS1667 is linearity, that is, for a given digital input, how close the analog output is to that which is expected.

The test circuit used to measure the linearity of the DS1667 is shown in Figure 5. Note that to get an accurate output voltage it is necessary to assure that the output current is 0, in order to negate the effects of wiper impedance RW, which is typically 400 ohms. For any given setting N for the pot, the expected voltage output at SOUT is:

$$VO = -5 + [10 \text{ X } (N/256)] \text{ (in volts)}$$

Absolute linearity is a comparison of the actual measured output voltage versus the expected value given by the equation above and is given in terms of an LSB, which is the change in expected output when the digital input is incremented by 1. In this case the LSB is 10/256 or 0.03906 volts. The equation for the absolute linearity of the DS1667 is:

$$\frac{V_O \text{ (actual)} - V_O \text{ (expected)}}{\text{LSB}} = \text{AL (in LSBs)}$$

The specification for absolute linearity of the DS1667 is ± 1 LSB typical.

Relative linearity is a comparison of the difference of actual output voltages of two successive taps and the difference of the expected output voltages of two successive taps. The expected difference of output voltages is 1 LSB or 0.03906V for the measurement system of Figure 5. Relative linearity is expressed in terms of an LSB and is given by the equation:

$$\frac{\Delta V_O \text{ (actual)} - \text{LSB}}{\text{LSB}} = \text{RL}$$

The specification for relative linearity of the DS1667 is ± 0.5 LSB typical.

Figure 6 is a plot of absolute linearity (AL) and relative linearity (RL) versus wiper setting for a typical DS1667 at 25°C.

DESCRIPTION AND OPERATION - OP AMP SECTION

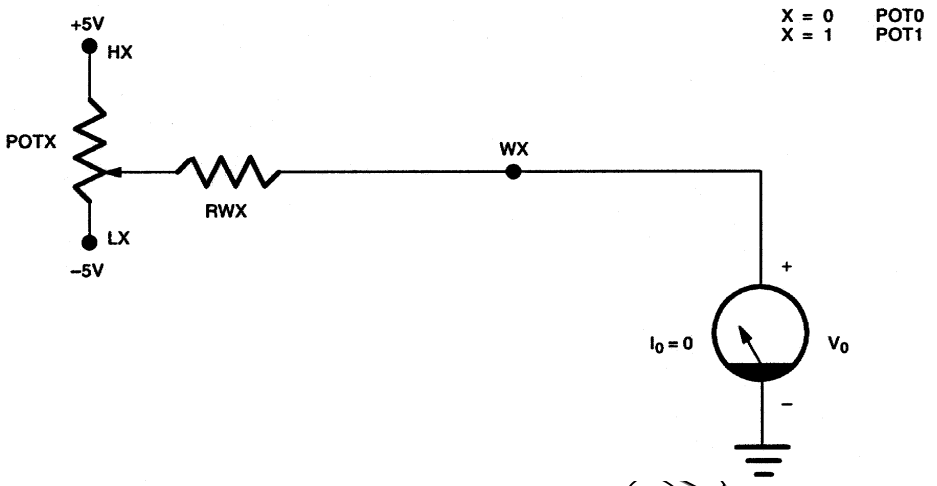
The DS1667 contains two operational amplifiers which are ideal for operation from a single 5V supply and ground or from +5V supplies (see Figure 1). An internal resistor divider defines the internal reference of the op amp to be halfway between the power supplies, i.e.:

$$\frac{V_{DD} + V_B}{2}$$

For optimal performance, choose analog ground to be this value. The operational amplifiers feature rail to rail output swing in addition to an input common mode range that includes the positive rail. Performance features include broad band noise immunity as well as voltage gain into realistic loads specified at both 600 ohms and 2k ohms. High voltage gain is produced with low input offset voltage and low offset voltage drift. Current consumption is less than 1.9 mA per amplifier and the device is virtually immune to latchup.

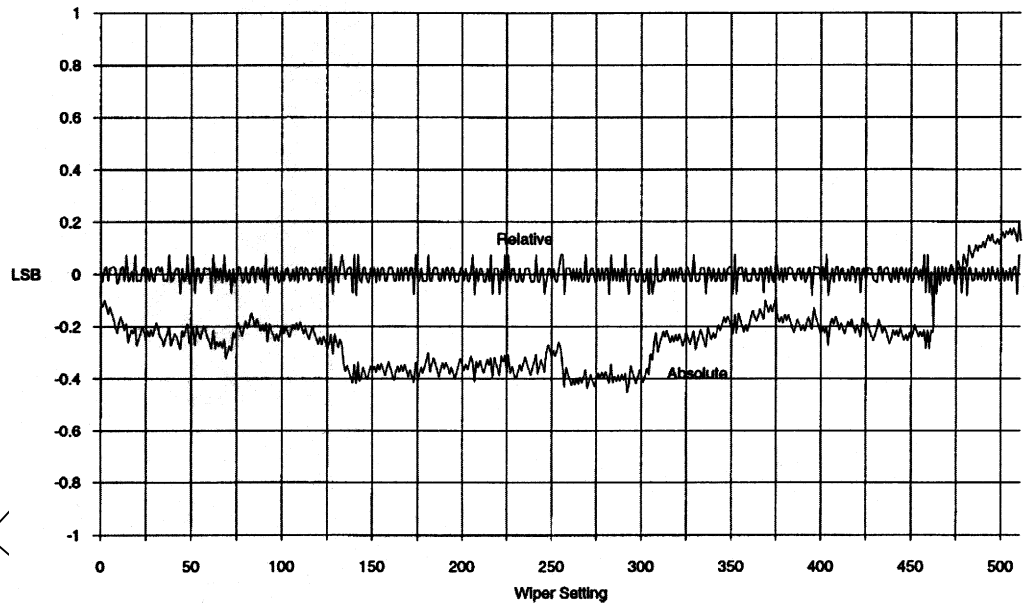
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LINEARITY MEASUREMENT CONFIGURATION Figure 5



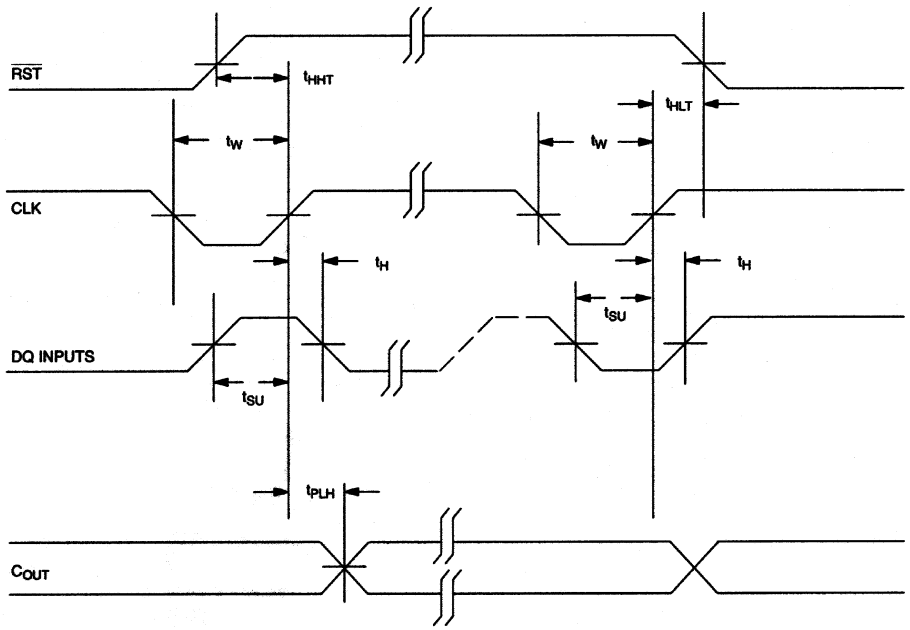
DS1667 ABSOLUTE AND RELATIVE LINEARITY Figure 6

Absolute and Relative Linearity
(Normalized to 1 LSB)



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TIMING DIAGRAM: RESISTOR SECTION Figure 7



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ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground (V_B = GND)	-0.5V to +7.0V
Voltage on Resistor Pins when V_B = -5.5V	-5.5V to +7.0V
Voltage on V_B	-5.5V to GND
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

RESISTOR SECTION (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Positive Supply Voltage	V_{CC}	+4.5	5.0	5.5	V	1
Input Logic 1	V_{IH}	2.0		V_{CC}+0.5	V	1
Input Logic 0	V_{IL}	-0.5		+0.8	V	1
Negative Supply Voltage	V_B	-5.5		GND	V	1
Resistor Inputs	L, H, W	V_B - 0.5		V_{CC}+0.5	V	2

DC ELECTRICAL CHARACTERISTICS

RESISTOR SECTION (0°C to 70°C; V_{CC} = 5.0V ± 10%, V_B = -5.0V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Positive Supply Current	I_{CC}		3	5	mA	
Negative Supply Current	I_B		3	5	mA	
Input Leakage	I_U	-1		+1	µA	
Wiper Resistance	R_W		400	1000	ohms	
Wiper Current	I_W			1	mA	
Output Leakage	I_{LO}	-1		+1	µA	
Logic 1 Output @ 2.4 Volts	I_{OH}	-1.0			mA	
Logic 0 Output @ 0.4 Volts	I_{OL}			4	mA	
End-to-End Resistor Tolerance	TOL_R	-20		+20	%	9
Noise (ref: 1V)	N		-120		$\frac{dB}{\sqrt{Hz}}$	
Absolute Linearity	AL		1.0		LSB	
Relative Linearity	RL		0.5		LSB	
Resistor Temperature Coefficient	TC_R		750		$\frac{ppm}{°C}$	

CAPACITANCE (T_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

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AC ELECTRICAL CHARACTERISTICS
RESISTOR SECTION

(0°C to 70°C, V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
CLK Frequency	f_{CLK}			10	MHz	
Width of CLK Pulse	t_W	50			ns	
Data Setup Time	t_{SU}	30			ns	
Data Hold Time	t_H	10			ns	
Propagation Delay Time Low to High Level Clock to Output	t_{PLH}			50	ns	3
$\overline{RST}$ High to Clock Input High	t_{HHT}	50			ns	
$\overline{RST}$ Low from Clock Input High	t_{HLT}	50			ns	

OPERATIONAL AMPLIFIER SECTION DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 5.0V ± 10%, V_B = -5.0V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Offset Voltage	V_{OS}		5	10	mV	
Input Offset Voltage Drift	V_{OSD}		10		uV/°C	
Common Mode Rejection	CM_R		62		dB	
Positive Power Supply Rejection	$+PS_R$		62		dB	
Negative Power Supply Rejection	$-PS_R$		62		dB	
Input Common Mode Voltage Range	V_{CCM}	V_B+1.5V		V_{CC}	V	
Large Signal Voltage Gain			106		dB	R_L=2kΩ
Large Signal Voltage Gain			96		dB	R_L=600kΩ
Output Swing	V_{SWGH}	4.6	4.7		V	R_L=2kΩ to GND V_B = -5V
Output Swing	V_{SWGL}		-4.7	-4.6	V	
Output Swing	V_{SWGH}	4.5	4.6		V	R_L=600kΩ to GND V_B = -5V
Output Swing	V_{SWGL}		-4.6	-4.5	V	
Output Current	$V_{O,SOURCE}$	13	58		mA	V_O = 0V
Output Current	$V_{O,SINK}$	13	63		mA	V_O = +5V

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OPERATIONAL AMPLIFIER SECTION
AC ELECTRICAL CHARACTERISTICS (0°C to 70°C; V_{CC} = 5.0V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Slew Rate	V_{SL}	0.7	2		V/µs	6
Gain Bandwidth Product	GBP		2.5		MHz	5
Phase Margin	PM		75		deg	5
Gain Margin	GM		20		dB	5
Amp-to-Amp Isolation	AAI		130		dB	
Input Referred Voltage Noise	IRVF		100		$nV/\sqrt{Hz}$	F=1 kHz
Input Referred Current Noise	IRV1		0.0002		$pA/\sqrt{Hz}$	F=1 kHz
Total Harmonic Distortion	HD		0.1		%	F=10 kHz AV=-10 RL=2kΩ $V_O = 1V_{PP}$

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NOTES:

1. All voltages are referenced to ground.
2. Resistor inputs cannot exceed the substrate bias voltage in the negative direction.
3. Measured with a load as shown in Figure 8.
4. Over a frequency range of 0 - 1 kHz.
5. Load is R_L = 600 ΩC_L = 10 pF.
6. V_{DD} = +5.0V V_B = -5.0V connected as voltage follower with 10V step input and $R_L = \infty$.
7. To achieve best op amp performance, V_{DD} = +5.0V V_B = -5.0V and analog ground = 0V. In general analog ground = $\frac{V_{DD} + V_B}{2}$
8. OP AMPS idle, no load.
9. Valid at 25°C only.

LOAD SCHEMATIC Figure 8

