DS15MB200 Dual 1.5 Gbps 2:1/1:2 LVDS Mux/Buffer with Pre-Emphasis

Check for Samples: DS15MB200

FEATURES

- **1.5 Gbps Data Rate Per Channel**
- **Configurable Off/On Pre-emphasis Drives Lossy Backplanes and Cables**
- **LVDS/BLVDS/CML/LVPECL Compatible Inputs, LVDS Compatible Outputs**
- **Low Output Skew and Jitter**
- **On-chip 100Ω Input and Output Termination**
- **15 kV ESD Protection on LVDS Inputs/Outputs**
- **Hot Plug Protection**
- **Single 3.3V Supply**
- **Industrial -40 to +85°C Temperature Range**
- **48-pin WQFN Package**

DESCRIPTION

The DS15MB200 is a dual-port 2 to 1 multiplexer and 1 to 2 repeater/buffer. High-speed data paths and flow-through pinout minimize internal device jitter and simplify board layout, while pre-emphasis overcomes ISI jitter effects from lossy backplanes and cables. The differential inputs and outputs interface to LVDS or Bus LVDS signals such as those on Texas Instrument's 10-, 16-, and 18-bit Bus LVDS SerDes, or to CML or LVPECL signals.

The 3.3V supply, CMOS process, and robust I/O ensure high performance at low power over the entire industrial -40 to +85°C temperature range.

Typical Application

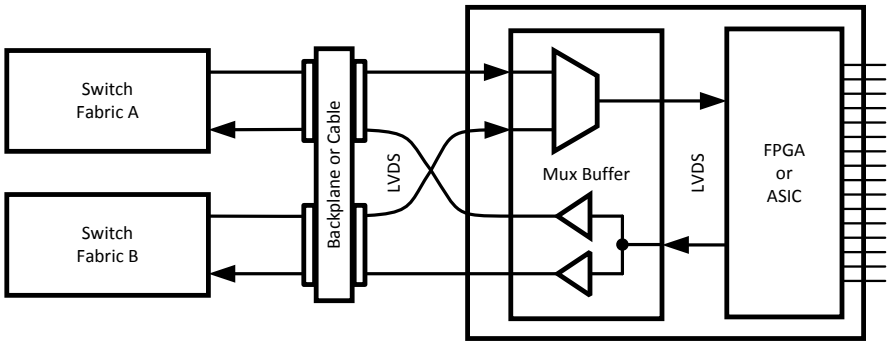


Figure 1.

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Block Diagram

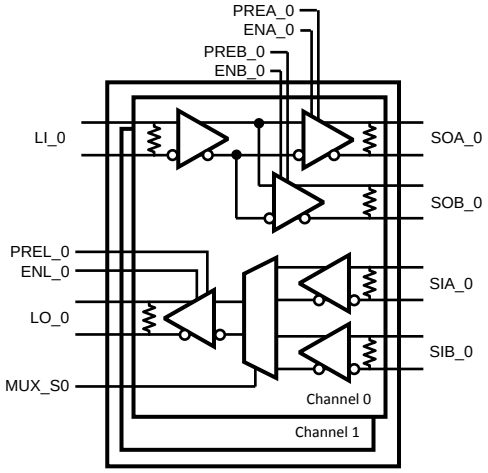


Figure 2.

PIN DESCRIPTIONS

Pin Name	WQFN Pin Number	I/O, Type	Description
SWITCH SIDE DIFFERENTIAL INPUTS			
SIA_0+ SIA_0−	30 29	I, LVDS	Switch A-side Channel 0 inverting and non-inverting differential inputs. LVDS, Bus LVDS, CML, or LVPECL compatible.
SIA_1+ SIA_1−	19 20	I, LVDS	Switch A-side Channel 1 inverting and non-inverting differential inputs. LVDS, Bus LVDS, CML, or LVPECL compatible.
SIB_0+ SIB_0−	28 27	I, LVDS	Switch B-side Channel 0 inverting and non-inverting differential inputs. LVDS, Bus LVDS, CML, or LVPECL compatible.
SIB_1+ SIB_1−	21 22	I, LVDS	Switch B-side Channel 1 inverting and non-inverting differential inputs. LVDS, Bus LVDS, CML, or LVPECL compatible.
LINE SIDE DIFFERENTIAL INPUTS			
LI_0+ LI_0−	40 39	I, LVDS	Line-side Channel 0 inverting and non-inverting differential inputs. LVDS, Bus LVDS, CML, or LVPECL compatible.
LI_1+ LI_1−	9 10	I, LVDS	Line-side Channel 1 inverting and non-inverting differential inputs. LVDS, Bus LVDS, CML, or LVPECL compatible.
SWITCH SIDE DIFFERENTIAL OUTPUTS			
SOA_0+ SOA_0−	34 33	O, LVDS	Switch A-side Channel 0 inverting and non-inverting differential outputs. LVDS compatible(1)(2).
SOA_1+ SOA_1−	15 16	O, LVDS	Switch A-side Channel 1 inverting and non-inverting differential outputs. LVDS compatible(1)(2).
SOB_0+ SOB_0−	32 31	O, LVDS	Switch B-side Channel 0 inverting and non-inverting differential outputs. LVDS compatible(1)(2).
SOB_1+ SOB_1−	17 18	O, LVDS	Switch B-side Channel 1 inverting and non-inverting differential outputs. LVDS compatible(1)(2).
LINE SIDE DIFFERENTIAL OUTPUTS			
LO_0+ LO_0−	42 41	O, LVDS	Line-side Channel 0 inverting and non-inverting differential outputs. LVDS compatible(1)(2).
LO_1+ LO_1−	7 8	O, LVDS	Line-side Channel 1 inverting and non-inverting differential outputs. LVDS compatible(1)(2).

(1) For interfacing LVDS outputs to CML or LVPECL compatible inputs, refer to the applications section of this datasheet (planned).
(2) The LVDS outputs do not support a multidrop (BLVDS) environment. The LVDS output characteristics of the DS15MB200 device have been optimized for point-to-point backplane and cable applications.

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PIN DESCRIPTIONS (continued)

Pin Name	WQFN Pin Number	I/O, Type	Description
DIGITAL CONTROL INTERFACE			
MUX_S0 MUX_S1	38 11	I, LVTTL	Mux Select Control Inputs (per channel) to select which Switch-side input, A or B, is passed through to the Line-side.
PREA_0 PREA_1 PREB_0 PREB_1	26 23 25 24	I, LVTTL	Output pre-emphasis control for Switch-side outputs. Each output driver on the Switch A-side and B-side has a separate pin to control the pre-emphasis on or off.
PREL_0 PREL_1	44 5	I, LVTTL	Output pre-emphasis control for Line-side outputs. Each output driver on the Line A-side and B-side has a separate pin to control the pre-emphasis on or off.
ENA_0 ENA_1 ENB_0 ENB_1	36 13 35 14	I, LVTTL	Output Enable Control for Switch A-side and B-side outputs. Each output driver on the A-side and B-side has a separate enable pin.
ENL_0 ENL_1	45 4	I, LVTTL	Output Enable Control for The Line-side outputs. Each output driver on the Line-side has a separate enable pin.
POWER			
V_{DD}	2, 6, 12, 37, 43, 46, 48	I, Power	V_{DD} = 3.3V ±0.3V.
GND	3, 47(3)	I, Power	Ground reference for LVDS and CMOS circuitry. For the WQFN package, the DAP is used as the primary GND connection to the device. The DAP is the exposed metal contact at the bottom of the WQFN-48 package. It should be connected to the ground plane with at least 4 vias for optimal AC and thermal performance.

(3) Note that the DAP on the backside of the WQFN package is the primary GND connection for the device when using the WQFN package.

Connection Diagrams

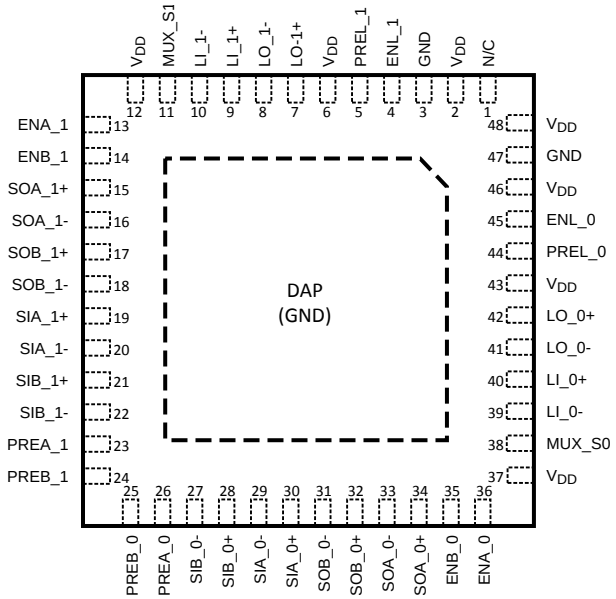


Figure 3. WQFN Top View
DAP = GND

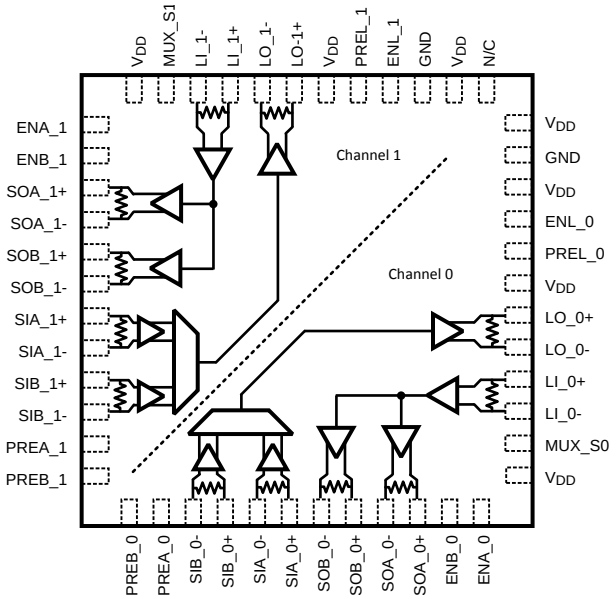


Figure 4. Directional Signal Paths Top View
(Refer to pin names for signal polarity)

Output Characteristics

The output characteristics of the DS15MB200 have been optimized for point-to-point backplane and cable applications, and are not intended for multipoint or multidrop signaling.

A 100Ω output (source) termination resistor is incorporated in the device to eliminate the need for an external resistor, providing excellent drive characteristics by locating the source termination as close to the output as physically possible.

Pre-Emphasis Controls

The pre-emphasis is used to compensate for long or lossy transmission media. Separate pins are provided for each output to minimize power consumption. Pre-emphasis is programmable to be off or on per the Pre-emphasis Control Table.

PREx_n(1)	Output Pre-Emphasis
0	0%
1	100%

(1) Applies to PREA_0, PREA_1, PREB_0, PREB_1, PREL_0, PREL_1

Multiplexer Truth Table(2)(3)

Data Inputs		Control Inputs		Output
SIA_0	SIB_0	MUX_S0	ENL_0	LO_0
X	valid	0	1	SIB_0
valid	X	1	1	SIA_0
X	X	X	0	Z

(2) Same functionality for channel 1
(3) X = Don't Care
Z = High Impedance (TRI-STATE)

Repeater/Buffer Truth Table(1)(2)

Data Input	Control Inputs		Outputs	
LI_0	ENA_0	ENB_0	SOA_0	SOB_0
X	0	0	Z	Z
valid	0	1	Z	LI_0
valid	1	0	LI_0	Z
valid	1	1	LI_0	LI_0

(1) Same functionality for channel 1
(2) X = Don't Care
Z = High Impedance (TRI-STATE)



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

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Absolute Maximum Ratings[1]

		Value	Unit
Supply Voltage (V_{DD})		−0.3 to +4.0	V
CMOS Input Voltage		-0.3 to (V_{DD}+0.3)	V
LVDS Receiver Input Voltage[2]		-0.3 to (V_{DD}+0.3)	V
LVDS Driver Output Voltage		-0.3 to (V_{DD}+0.3)	V
LVDS Output Short Circuit Current		+40	mA
Junction Temperature		+150	°C
Storage Temperature		−65 to +150	°C
Lead Temperature (Solder, 4sec)		260	°C
Max Pkg Power Capacity @ 25°C		5.2	W
Thermal Resistance (θ_{JA})		24	°C/W
Package Derating above +25°C		41.7	mW/°C
ESD Last Passing Voltage	HBM, 1.5kΩ, 100pF	8	kV
	LVDS pins to GND only	15	kV
	EIAJ, 0Ω, 200pF	250	V
	CDM	1000	V

(1) Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Texas Instruments does not recommend operation of products outside of recommended operation conditions.
(2) V_{ID} max < 2.4V

Recommended Operating Conditions

	Min	Max	Unit
Supply Voltage (V_{CC})	3.0	3.6	V
Input Voltage (V_I)[1]	0	V_{CC}	V
Output Voltage (V_O)	0	V_{CC}	V
Operating Temperature (T_A) Industrial	−40	+85	°C

(1) V_{ID} max < 2.4V

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Electrical Characteristics

Over recommended operating supply and temperature ranges unless other specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Units
LVTTL DC SPECIFICATIONS (MUX_Sn, PREA_n, PREB_n, PREL_n, ENA_n, ENB_n, ENL_n)						
V_{IH}	High Level Input Voltage		2.0		V_{DD}	V
V_{IL}	Low Level Input Voltage		GND		0.8	V
I_{IH}	High Level Input Current	$V_{IN} = V_{DD} = V_{DDMAX}$	−10		+10	µA
I_{IHR}	High Level Input Current	PREA_n, PREB_n, PREL_n	40		200	µA
I_{IL}	Low Level Input Current	$V_{IN} = V_{SS}$, $V_{DD} = V_{DDMAX}$	−10		+10	µA
C_{IN1}	Input Capacitance	Any Digital Input Pin to V_{SS}		2.0		pF
C_{OUT1}	Output Capacitance	Any Digital Output Pin to V_{SS}		4.0		pF
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA	−1.5	−0.8		V
LVDS INPUT DC SPECIFICATIONS (SIA±, SIB±, LI±)						
V_{TH}	Differential Input High Threshold[2]	V_{CM} = 0.8V or 1.2V or 3.55V, V_{DD} = 3.6V		0	100	mV
V_{TL}	Differential Input Low Threshold[2]	V_{CM} = 0.8V or 1.2V or 3.55V, V_{DD} = 3.6V	−100	0		mV
V_{ID}	Differential Input Voltage	V_{CM} = 0.8V to 3.55V, V_{DD} = 3.6V	100		2400	mV
V_{CMR}	Common Mode Voltage Range	V_{ID} = 150 mV, V_{DD} = 3.6V	0.05		3.55	V
C_{IN2}	Input Capacitance	IN+ or IN− to V_{SS}		2.0		pF
I_{IN}	Input Current	V_{IN} = 3.6V, $V_{DD} = V_{DDMAX}$ or 0V	−15		+15	µA
		V_{IN} = 0V, $V_{DD} = V_{DDMAX}$ or 0V	−15		+15	µA
LVDS OUTPUT DC SPECIFICATIONS (SOA_n±, SOB_n±, LO_n±)						
V_{OD}	Differential Output Voltage, 0% Pre-emphasis[2]	R_L is the internal 100Ω between OUT+ and OUT−	250	360	500	mV
ΔV_{OD}	Change in V_{OD} between Complementary States		-35		35	mV
V_{OS}	Offset Voltage[3]		1.05	1.22	1.475	V
ΔV_{OS}	Change in V_{OS} between Complementary States		-35		35	mV
I_{OS}	Output Short Circuit Current	OUT+ or OUT− Short to GND		−21	-40	mA
C_{OUT2}	Output Capacitance	OUT+ or OUT− to GND when TRI-STATE		4.0		pF
SUPPLY CURRENT (Static)						
I_{CC}	Supply Current	All inputs and outputs enabled and active, terminated with external load of 100Ω between OUT+ and OUT-.		225	275	mA
I_{CCZ}	Supply Current - Powerdown Mode	ENA_0 = ENB_0 = ENL_0 = ENA_1 = ENB_1 = ENL_1 = L		0.6	4.0	mA
SWITCHING CHARACTERISTICS—LVDS OUTPUTS						
t_{LHT}	Differential Low to High Transition Time	Use an alternating 1 and 0 pattern at 200 Mb/s, measure between 20% and 80% of V_{OD}.[4]		170	250	ps
t_{HLT}	Differential High to Low Transition Time			170	250	ps
t_{PLHD}	Differential Low to High Propagation Delay	Use an alternating 1 and 0 pattern at 200 Mb/s, measure at 50% V_{OD} between input to output.		1.0	2.5	ns
t_{PHLD}	Differential High to Low Propagation Delay			1.0	2.5	ns
t_{SKD1}	Pulse Skew	$\lvert t_{PLHD} - t_{PHLD} \rvert$[4]		25	75	ps
t_{SKCC}	Output Channel to Channel Skew	Difference in propagation delay (t_{PLHD} or t_{PHLD}) among all output channels.[4]		50	115	ps

(1) Typical parameters are measured at V_{DD} = 3.3V, T_A = 25°C. They are for reference purposes, and are not production-tested.
(2) Differential output voltage V_{OD} is defined as ABS(OUT+–OUT−). Differential input voltage V_{ID} is defined as ABS(IN+–IN−).
(3) Output offset voltage V_{OS} is defined as the average of the LVDS single-ended output voltages at logic high and logic low states.
(4) Not production tested. Guaranteed by statistical analysis on a sample basis at the time of characterization.

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Electrical Characteristics (continued)

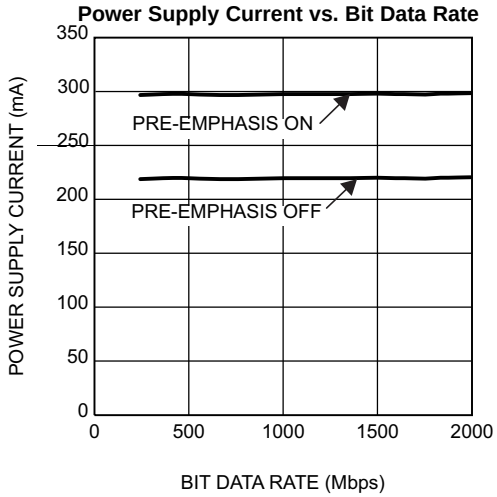
Over recommended operating supply and temperature ranges unless other specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Units
t_{JIT}	Jitter (0% Pre-emphasis)[5]	RJ - Alternating 1 and 0 at 750MHz[6]		1.1	1.5	psrms
		DJ - K28.5 Pattern, 1.5 Gbps[7]		20	34	psp-p
		TJ - PRBS 2^7-1 Pattern, 1.5 Gbps[8]		14	28	psp-p
t_{ON}	LVDS Output Enable Time	Time from ENA_n, ENB_n, or ENL_n to OUT± change from TRI-STATE to active.		0.5	1.5	µs
t_{ON2}	LVDS Output Enable Time from Powerdown Mode	Time from ENA_n, ENB_n, or ENL_n to OUT± change from Powerdown Mode to active.		10	20	µs
t_{OFF}	LVDS Output Disable Time	Time from ENA_n, ENB_n, or ENL_n to OUT± change from active to TRI-STATE or Powerdown mode.			12	ns

(5) Jitter is not production tested, but guaranteed through characterization on a sample basis.
(6) Random Jitter, or RJ, is measured RMS with a histogram including 1500 histogram window hits. The input voltage = V_{ID} = 500mV, 50% duty cycle at 750MHz, t_r = t_f = 50ps (20% to 80%).
(7) Deterministic Jitter, or D_J, is measured to a histogram mean with a sample size of 350 hits. Stimulus and fixture jitter have been subtracted. The input voltage = V_{ID} = 500mV, K28.5 pattern at 1.5 Gbps, t_r = t_f = 50ps (20% to 80%). The K28.5 pattern is repeating bit streams of (0011111010 1100000101).
(8) Total Jitter, or T_J, is measured peak to peak with a histogram including 3500 window hits. Stimulus and fixture jitter have been subtracted. The input voltage = V_{ID} = 500mV, 2^7-1 PRBS pattern at 1.5 Gbps, t_r = t_f = 50ps (20% to 80%).

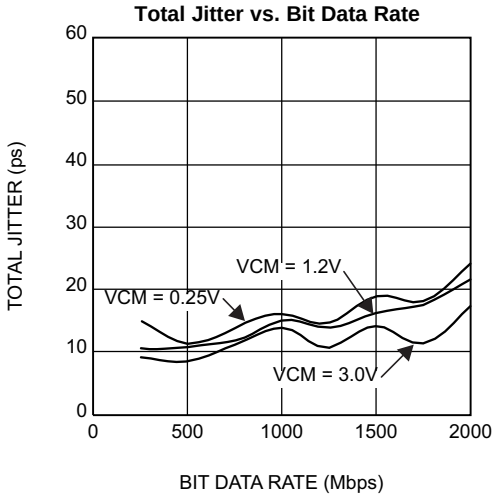
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WQFN Performance Characteristics



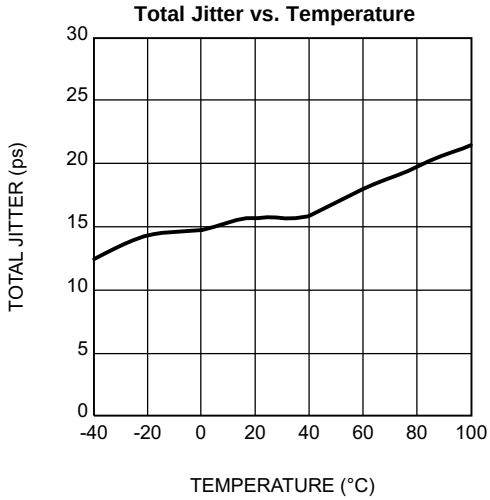
Dynamic power supply current was measured with all channels active and toggling at the bit data rate. Data pattern has no effect on the power consumption.
V_{DD} = 3.3V, T_A = +25°C, V_{ID} = 0.5V, V_{CM} = 1.2V

Figure 5.



Total Jitter measured at 0V differential while running a PRBS 2^{7-1} pattern with one channel active, all other channels are disabled.
V_{DD} = 3.3V, T_A = +25°C, V_{ID} = 0.5V, pre-emphasis off.

Figure 6.



Total Jitter measured at 0V differential while running a PRBS 2^7-1 pattern with one channel active, all other channels are disabled. V_{DD} = 3.3V, V_{ID} = 0.5V, V_{CM} = 1.2V, 1.5 Gbps data rate, pre-emphasis off.

Figure 7.

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TRI-STATE AND POWERDOWN MODES

The DS15MB200 has output enable control on each of the six onboard LVDS output drivers. This control allows each output individually to be placed in a low power TRI-STATE mode while the device remains active, and is useful to reduce power consumption on unused channels. In TRI-STATE mode, some outputs may remain active while some are in TRI-STATE.

When all six of the output enables (all drivers on both channels) are deasserted (LOW), then the device enters a Powerdown mode that consumes only 0.5mA (typical) of supply current. In this mode, the entire device is essentially powered off, including all receiver inputs, output drivers and internal bandgap reference generators. When returning to active mode from Powerdown mode, there is a delay until valid data is presented at the outputs because of the ramp to power up the internal bandgap reference generators.

Any single output enable that remains active will hold the device in active mode even if the other five outputs are in TRI-STATE.

When in Powerdown mode, any output enable that becomes active will wake up the device back into active mode, even if the other five outputs are in TRI-STATE.

Input Failsafe Biasing

External pull up and pull down resistors may be used to provide enough of an offset to enable an input failsafe under open-circuit conditions. This configuration ties the positive LVDS input pin to VDD thru a pull up resistor and the negative LVDS input pin is tied to GND by a pull down resistor. The pull up and pull down resistors should be in the 5kΩ to 15kΩ range to minimize loading and waveform distortion to the driver. The common-mode bias point ideally should be set to approximately 1.2V (less than 1.75V) to be compatible with the internal circuitry. Please refer to application note AN-1194, “Failsafe Biasing of LVDS Interfaces” (SNLA051) for more information.

Interfacing LVPECL to LVDS

An LVPECL driver consists of a differential pair with coupled emitters connected to GND via a current source. This drives a pair of emitter-followers that require a 50 ohm to V_{CC}-2.0 load. A modern LVPECL driver will typically include the termination scheme within the device for the emitter follower. If the driver does not include the load, then an external scheme must be used. The 1.3 V supply is usually not readily available on a PCB, therefore, a load scheme without a unique power supply requirement may be used.

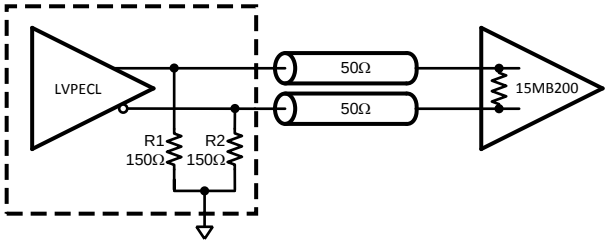


Figure 8. DC Coupled LVPECL to LVDS Interface

Figure 8 is a separated π termination scheme for a 3.3 V LVPECL driver. R1 and R2 provides proper DC load for the driver emitter followers, and may be included as part of the driver device(1). The DS15MB200 includes a 100 ohm input termination for the transmission line. The common mode voltage will be at the normal LVPECL levels – around 2 V. This scheme works well with LVDS receivers that have rail-to-rail common mode voltage, V_{CM}, range. Most Texas Instrument's LVDS receivers have wide V_{CM} range. The exceptions are noted in devices' respective datasheets. Those LVDS devices that do have a wide V_{CM} range do not vary in performance significantly when receiving a signal with a common mode other than standard LVDS V_{CM} of 1.2 V.

(1) The bias networks shown above for LVPECL drivers and receivers may or may not be present within the driver device. The LVPECL driver and receiver specification must be reviewed closely to ensure compatibility between the driver and receiver terminations and common mode operating ranges.

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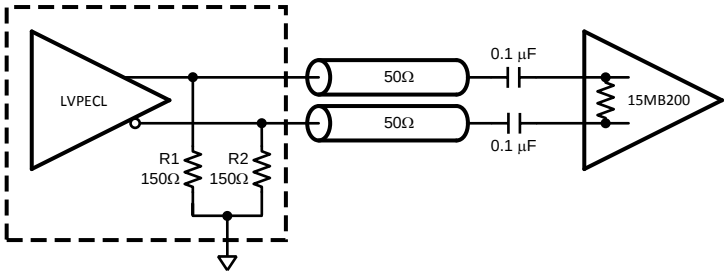


Figure 9. AC Coupled LVPECL to LVDS Interface

An AC coupled interface is preferred when transmitter and receiver ground references differ more than 1 V. This is a likely scenario when transmitter and receiver devices are on separate PCBs. Figure 9 illustrates an AC coupled interface between a LVPECL driver and LVDS receiver. R1 and R2, if not present in the driver device(2), provide DC load for the emitter followers and may range between 140-220 ohms for most LVPECL devices for this particular configuration. The DS15MB200 includes an internal 100 ohm resistor to terminate the transmission line for minimal reflections. The signal after AC coupling capacitors will swing around a level set by internal biasing resistors (i.e. fail-safe) which is either $V_{DD}/2$ or 0 V depending on the actual failsafe implementation. If internal biasing is not implemented, the signal common mode voltage will slowly wander to GND level.

Interfacing LVDS to LVPECL

An LVDS driver consists of a current source (nominal 3.5mA) which drives a CMOS differential pair. It needs a differential resistive load in the range of 70 to 130 ohms to generate LVDS levels. In a system, the load should be selected to match transmission line characteristic differential impedance so that the line is properly terminated. The termination resistor should be placed as close to the receiver inputs as possible. When interfacing an LVDS driver with a non-LVDS receiver, one only needs to bias the LVDS signal so that it is within the common mode range of the receiver. This may be done by using separate biasing voltage which demands another power supply. Some receivers have required biasing voltage available on-chip (V_T, V_{TT} or V_{BB}).

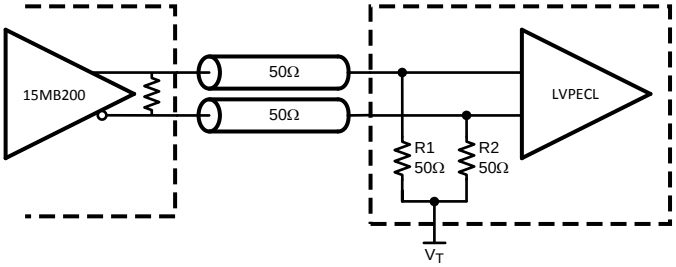


Figure 10. DC Coupled LVDS to LVPECL Interface

Figure 10 illustrates interface between an LVDS driver and a LVPECL with a V_T pin available. R1 and R2, if not present in the receiver(2), provide proper resistive load for the driver and termination for the transmission line, and V_T sets desired bias for the receiver.

(2) The bias networks shown above for LVPECL drivers and receivers may or may not be present within the driver device. The LVPECL driver and receiver specification must be reviewed closely to ensure compatibility between the driver and receiver terminations and common mode operating ranges.

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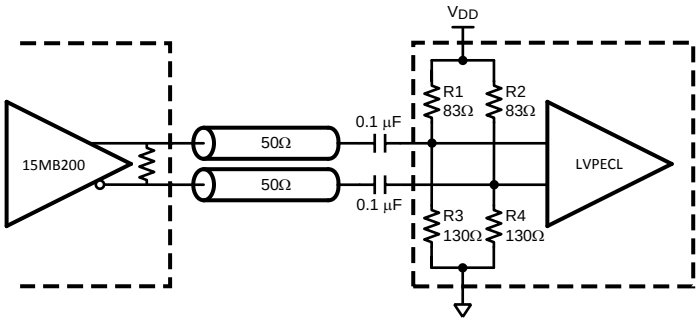


Figure 11. AC Coupled LVDS to LVPECL Interface

Figure 11 illustrates AC coupled interface between an LVDS driver and LVPECL receiver without a V_T pin available. The resistors R1, R2, R3, and R4, if not present in the receiver(2), provide a load for the driver, terminate the transmission line, and bias the signal for the receiver.

Packaging Information

The Leadless Leadframe Package (WQFN) is a leadframe based chip scale package (CSP) that may enhance chip speed, reduce thermal impedance, and reduce the printed circuit board area required for mounting. The small size and very low profile make this package ideal for high density PCBs used in small-scale electronic applications such as cellular phones, pagers, and handheld PDAs. The WQFN package is offered in the no Pullback configuration. In the no Pullback configuration the standard solder pads extend and terminate at the edge of the package. This feature offers a visible solder fillet after board mounting.

The WQFN has the following advantages:

- Low thermal resistance
- Reduced electrical parasitics
- Improved board space efficiency
- Reduced package height
- Reduced package mass

For more details about WQFN packaging technology, refer to applications note AN-1187, "Leadless Leadframe Package" (SNOA401).

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REVISION HISTORY

Changes from Revision D (March 2013) to Revision E	Page
• Changed layout of National Data Sheet to TI format	11

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS15MB200TSQ/NOPB	ACTIVE	WQFN	RHS	48	250	Green (RoHS & no Sb/Br)	SN	Level-3-260C-168 HR	-40 to 85	15M200	Samples
DS15MB200TSQX/NOPB	ACTIVE	WQFN	RHS	48	2500	Green (RoHS & no Sb/Br)	SN	Level-3-260C-168 HR	-40 to 85	15M200	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

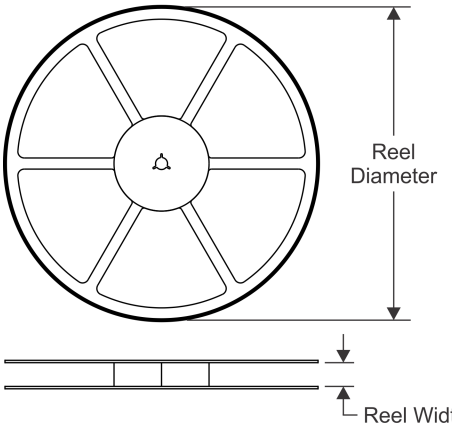
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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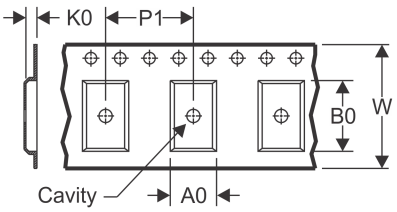
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

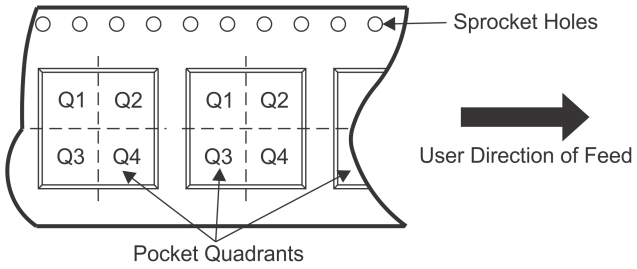


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

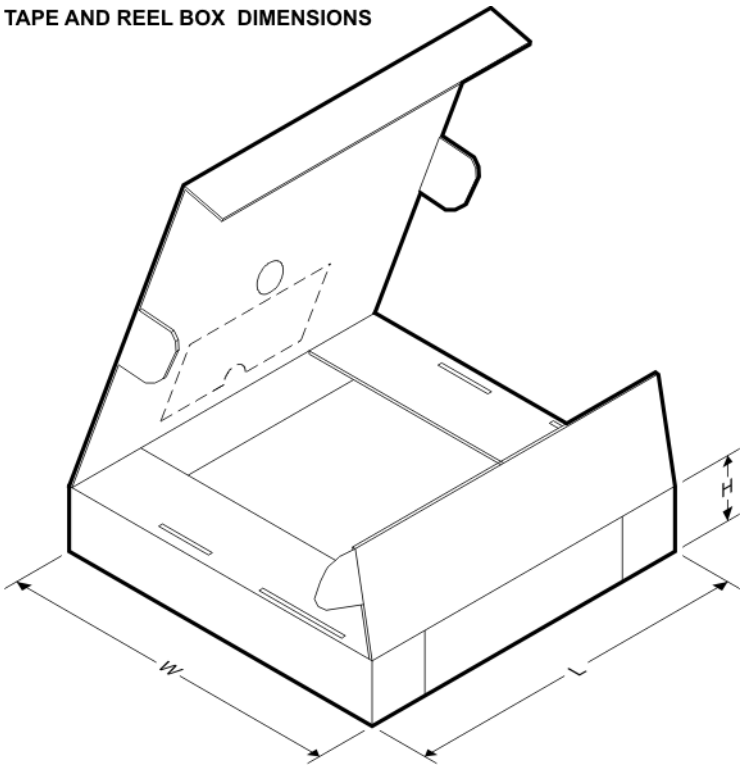
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS15MB200TSQ/NOPB	WQFN	RHS	48	250	178.0	16.4	7.3	7.3	1.3	12.0	16.0	Q1
DS15MB200TSQX/NOPB	WQFN	RHS	48	2500	330.0	16.4	7.3	7.3	1.3	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

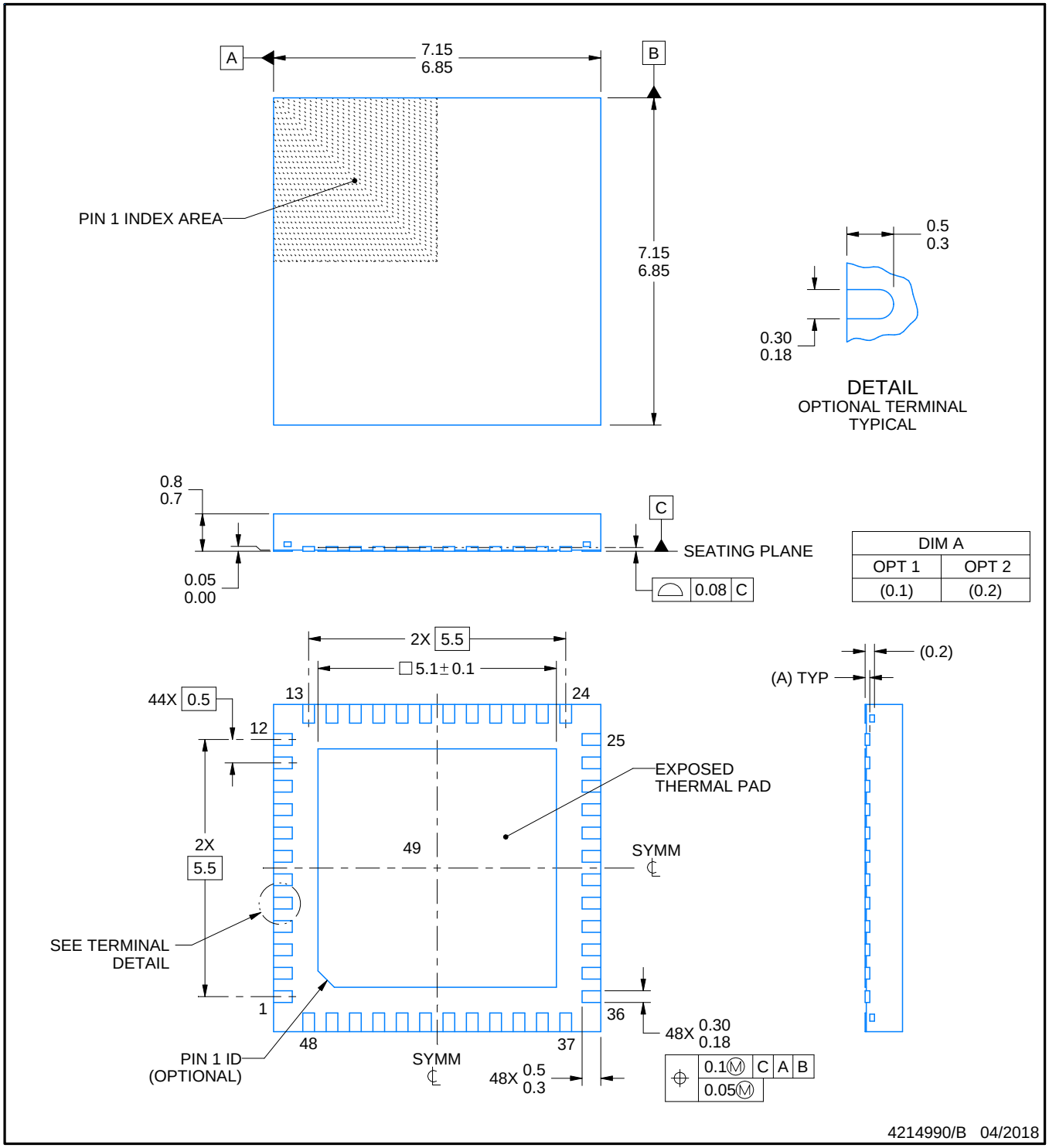
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS15MB200TSQ/NOPB	WQFN	RHS	48	250	210.0	185.0	35.0
DS15MB200TSQX/NOPB	WQFN	RHS	48	2500	367.0	367.0	38.0

PACKAGE OUTLINE

RHS0048A

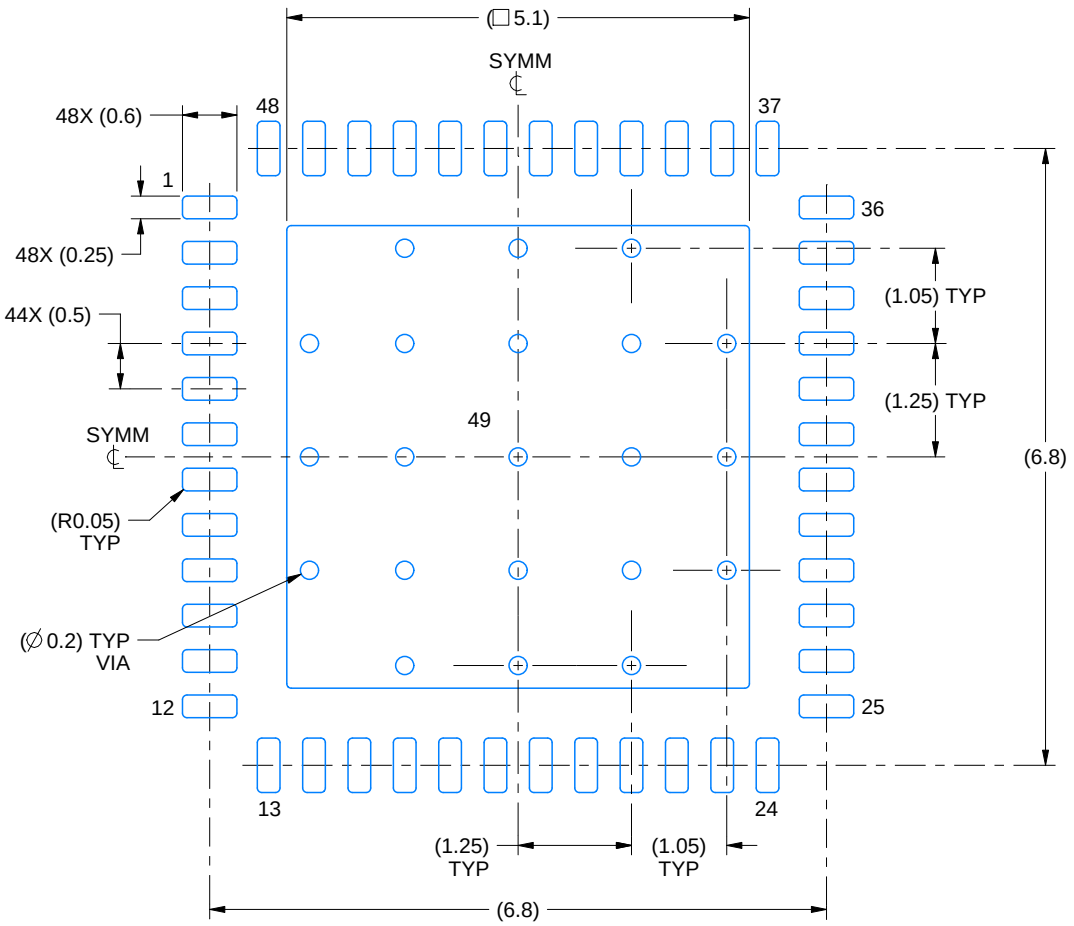
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

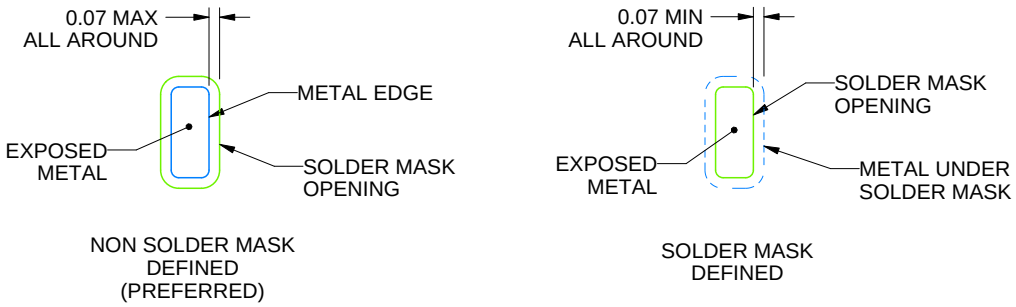


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:12X

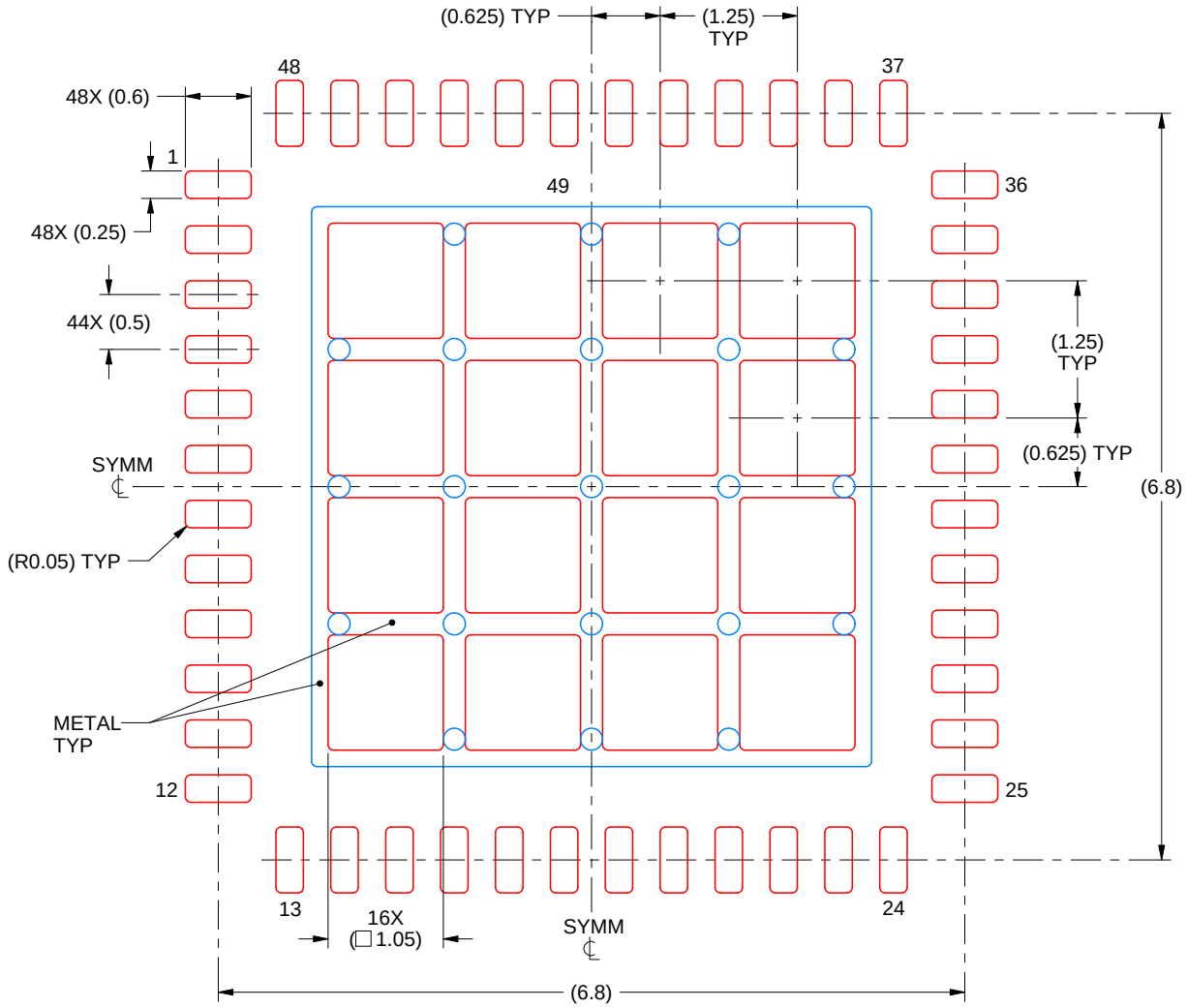


SOLDER MASK DETAILS

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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 49
68% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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