DS1371
I²C, 32-Bit Binary Counter Watchdog Clock

www.maxim-ic.com

General Description

The DS1371 is a 32-bit binary counter that is designed to continuously count time in seconds. An additional counter that can generate a periodic alarm or serve as a watchdog timer is also provided. If enabled as a watchdog timer, the watchdog strobe input pin provides a hardware reset of the counter. If disabled, this counter can be used as 3 Bytes of general-purpose RAM. A configurable output can be used as an interrupt or provide a square wave at one of four selectable frequencies. The device is programmed serially through a I²C bidirectional bus.

Applications

Servers
Point-of-Sale Equipment
Portable Instruments
Elapsed Time Measurements

Features

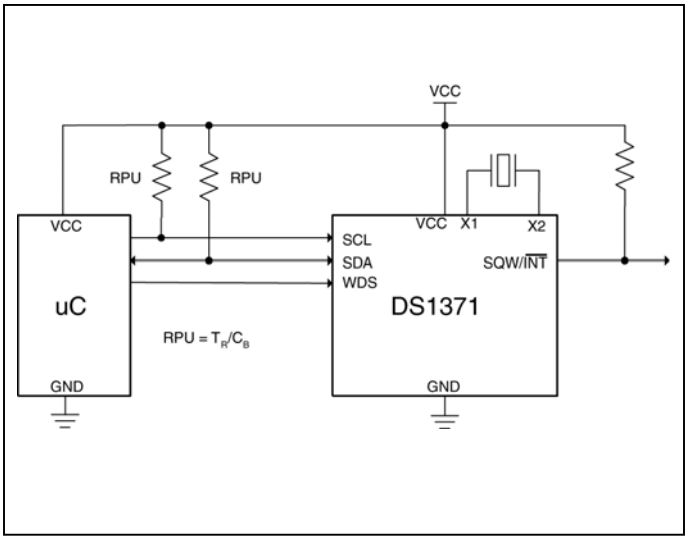
- 32-Bit Binary Counter
- 24-Bit Binary Counter Provides Periodic Alarm, Watchdog Timer, or RAM
- Strobe Input to Reset Watchdog Timer
- Single Output Configurable as Interrupt or Square Wave
- I²C Serial Interface
- Low-Voltage Operation
- Operating Temperature Range: -40°C to +85°C
- Available in 8-Pin µSOP

Ordering Information

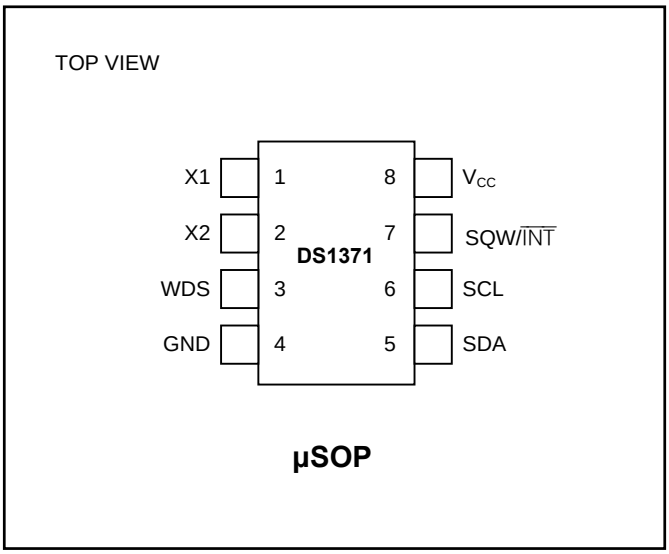
PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
DS1371U	-40°C to +85°C	8 µSOP	1371
DS1371U+	-40°C to +85°C	8 µSOP	1371

+Denotes a lead-free/RoHS-compliant package. A + appears on the top mark for lead-free packages.

Typical Operating Circuit



Pin Configuration



REV: 070607

ABSOLUTE MAXIMUM RATINGS

Voltage Range on V_{CC} Pin Relative to Ground……..-0.3V to +6.0V
Voltage Range on SDA, SCL, and WDS Relative to Ground……..-0.3V to (V_{CC} +0.5V)
Operating Temperature Range (noncondensing)……...-40°C to +85°C
Storage Temperature Range…….-55°C to +125°C
Soldering Temperature**……...**See IPC/JEDEC J-STD-020

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A = -40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Supply Voltage (Note 1)	V_{CC}	1.7	3.3	5.5	V
Input Logic 1 (Notes 2, 3)	V_{IH}	0.7 V_{CC}		V_{CC} + 0.3	V
Input Logic 0 (Notes 2, 3)	V_{IL}	-0.3		0.3V_{CC}	V

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 1.7V to 5.5V, T_A = -40°C to +85°C, unless otherwise noted.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage (Note 1)	V_{CC}		1.7		5.5	V
Oscillator Operating Voltage Range (Note 1)	V_{OSC}		1.3		5.5	V
Input Leakage	I_{LI}	(Note 2)			1	µA
I/O Leakage	I_{LO}	(Note 3)			1	µA
SDA Logic 0 Output (Note 1)	I_{OLSDA}	V_{CC} > 2V; V_{OL} = 0.4V			3	mA
		V_{CC} < 2V; V_{OL} = 0.2V_{CC}				
SQW/$\overline{INT}$ Logic 0 Output (Note 1)	I_{OLSQW}	V_{CC} > 2V; V_{OL} = 0.4V			3.0	mA
		1.7V < V_{CC} < 2V; V_{OL} = 0.2V_{CC}			3.0	
		1.3V < V_{CC} < 1.7V; V_{OL} = 0.2V_{CC}			250	µA
Active Supply Current	I_{CCA}	(Note 5)		100	150	µA
Timekeeping Current (Oscillator Enabled, INTCN = 1)	I_{OSC0}	(Notes 6, 7)			800	nA
Timekeeping Current (Oscillator Enabled, INTCN = 0)	I_{OSC1}	(Notes 6, 7)			1300	nA
Data Retention Current (Oscillator Disabled)	I_{DDR}	(Note 6)			100	nA

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 1.7V to 5.5V, T_A = -40°C to +85°C, unless otherwise noted.) (Note 8)

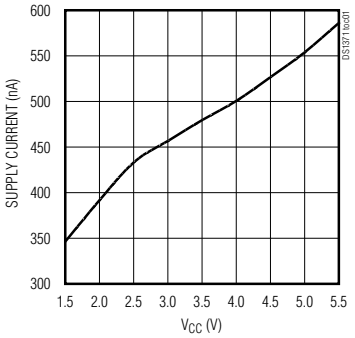
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency (Note 9)	f_{SCL}	Fast mode	100		400	kHz
		Standard mode	0		100	
Bus Free Time Between STOP and START Conditions	t_{BUF}	Fast mode	1.3			µs
		Standard mode	4.7			
Hold Time (repeated) START Condition (Note 10)	$t_{HD:STA}$	Fast mode	0.6			µs
		Standard mode	4.0			
Low Period of SCL Clock	t_{LOW}	Fast mode	1.3			µs
		Standard mode	4.7			
High Period of SCL Clock	t_{HIGH}	Fast mode	0.6			µs
		Standard mode	4.0			
Data Hold Time (Notes 11, 12)	$t_{HD:DAT}$	Fast mode	0		0.9	µs
		Standard mode	0		0.9	
Data Setup Time (Note 13)	$t_{SU:DAT}$	Fast mode	100			ns
		Standard mode	250			
Start Setup Time	$t_{SU:STA}$	Fast mode	0.6			µs
		Standard mode	4.7			
Rise Time of Both SDA and SCL Signals (Note 9)	t_R	Fast mode	$20 + 0.1C_B$		300	ns
		Standard mode	$20 + 0.1C_B$		1000	
Fall Time of Both SDA and SCL Signals (Note 9)	t_F	Fast mode	$20 + 0.1C_B$		300	ns
		Standard mode	$20 + 0.1C_B$		300	
Setup Time for STOP Condition	$t_{SU:STO}$	Fast mode	0.6			µs
		Standard mode	4.7			
Capacitive Load for Each Bus Line (Note 7)	C_B				400	pF
Pulse Width of Spikes that Must be Suppressed by the Input Filter (Note 14)	T_{SP}	Fast mode		30		ns
Watchdog Strobe (WDS) Pulse Width	t_{WDS}		100			ns
Oscillator Stop Flag (OSF) Delay (Note 8)	t_{OSF}		100			ms

Note 1: All voltages are referenced to ground.
Note 2: SCL and WDS only.
Note 3: SDA and SQW/$\overline{INT}$.
Note 4: Limits at -40°C are guaranteed by design and not production tested.
Note 5: I_{CCA}—SCL clocking at max frequency = 400kHz. WDS inactive.
Note 6: Specified with WDS input and I^2C bus inactive, SCL = SDA = V_{CC}.
Note 7: Measured with a 32.768kHz crystal attached to the X1 and X2 pins.
Note 8: The parameter t_{OSF} is the period of time the oscillator must be stopped in order for the OSF flag to be set over the voltage range of 1.3V ≤ V_{CC} ≤ V_{CCMAX}.
Note 9: A fast mode device can be used in a standard mode system, but the requirement $t_{SU:DAT}$ ≥ to 250ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{R\,MAX}$ + $t_{SU:DAT}$ = 1000 + 250 = 1250ns before the SCL line is released.
Note 10: After this period, the first clock pulse is generated.
Note 11: A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the V_{IHMIN} of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.
Note 12: The maximum $t_{HD:DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
Note 13: C_B—total capacitance of one bus line in pF.
Note 14: This parameter is not production tested.

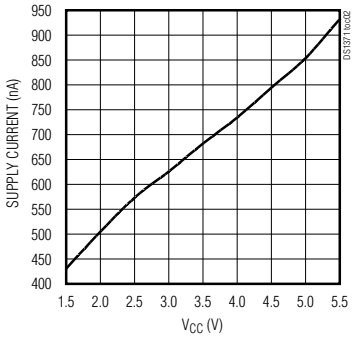
Typical Operating Characteristics

(V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.)

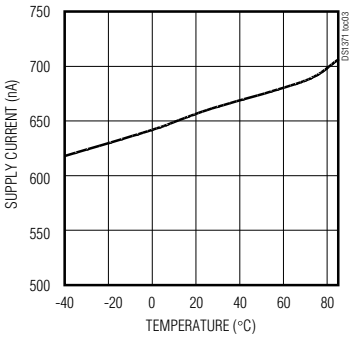
I_{OSCO} vs. V_{CC}
SQUARE-WAVE OFF



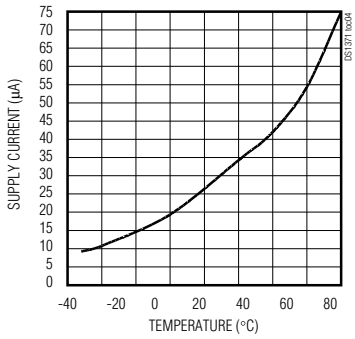
I_{OSC1} vs. V_{CC}
SQUARE-WAVE ON



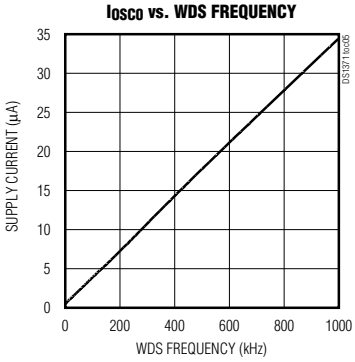
I_{OSCO} vs. TEMPERATURE
V_{CC} = 3.3V



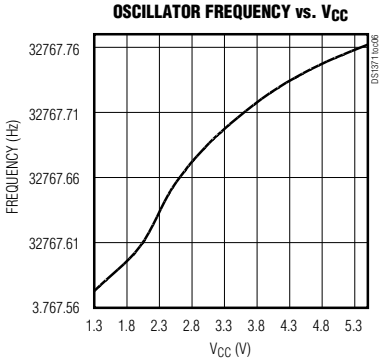
I_{CCA} vs. V_{CC}
SQUARE-WAVE ON



I_{OSCO} vs. WDS FREQUENCY



OSCILLATOR FREQUENCY vs. V_{CC}



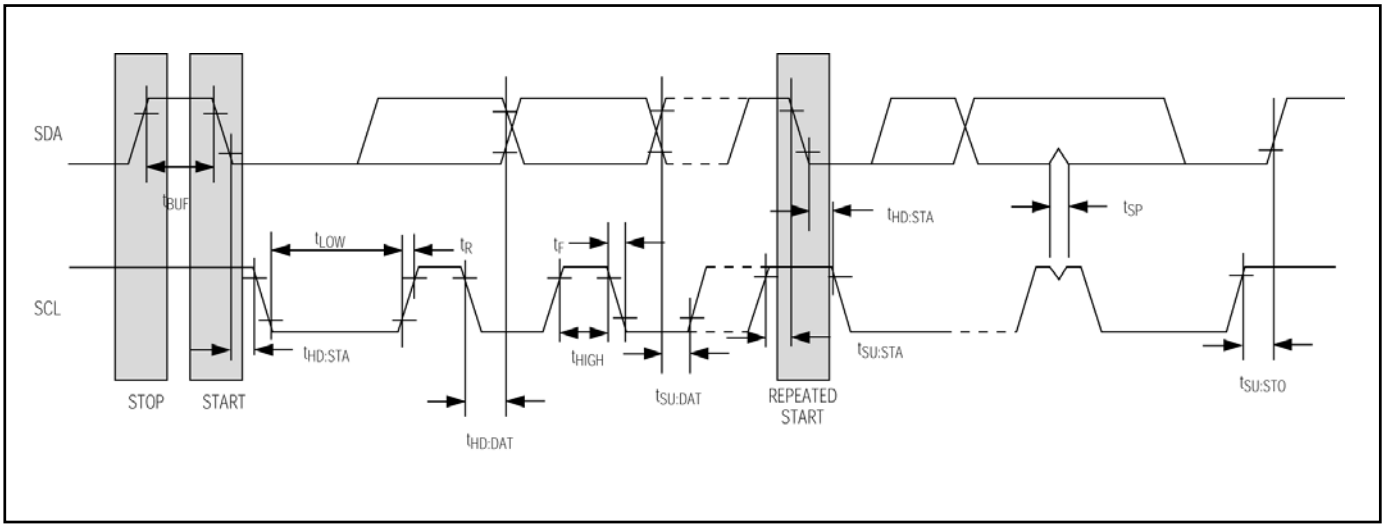


Figure 1. Timing Diagram

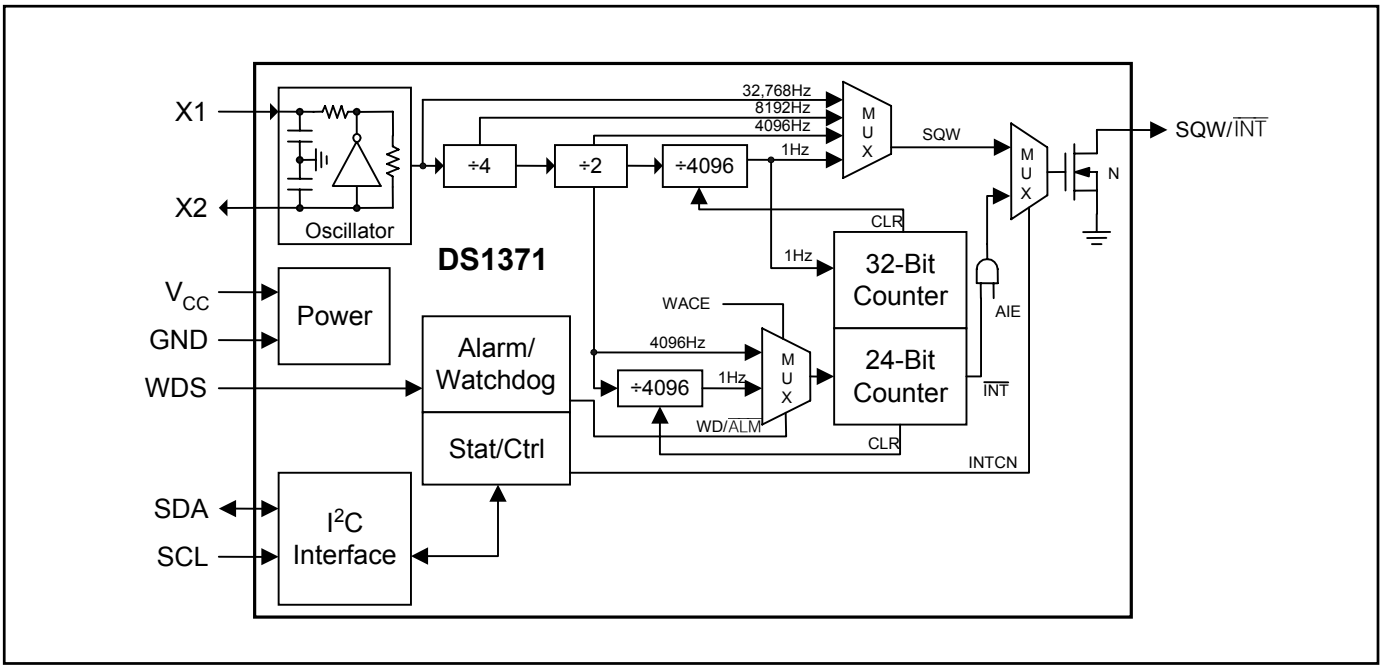


Figure 2. Functional Diagram

PIN DESCRIPTION

PIN	NAME	FUNCTION
1, 2	X1, X2	These signals are connections for a standard 32.768kHz quartz crystal. The internal oscillator circuitry is designed for operation with a crystal having a specified load capacitance (C_L) of 6pF. No external resistors or capacitors are required. For more information about crystal selection and crystal layout considerations, refer to *Application Note 58: Crystal Considerations with Dallas Real-Time Clocks*. The DS1371 can also be driven by an external 32.768kHz oscillator. In this configuration, the X1 pin is connected to the external oscillator signal and the X2 pin is floated.
3	WDS	Watchdog Input. A positive edge-triggered hardware interrupt input that restarts the watchdog counter when this signal transitions from a low to a high. While WDS remains at a static low or high, the watchdog counter continues to decrement.
4	GND	Ground
5	SDA	I^2C Serial Data. Input/output for I^2C data.
6	SCL	I^2C Serial Clock. Input for I^2C clock.
7	SQW/$\overline{INT}$	Square-Wave/Interrupt Output. This pin is used to output the programmable square-wave or alarm interrupt signal. It is open drain and requires an external pullup resistor.
8	V_{CC}	Supply Voltage Terminal

Detailed Description

The DS1371 is a real-time clock (RTC) with a I^2C serial interface that provides elapsed seconds from a user-defined starting point in a 32-bit counter (Figure 2). A 24-bit counter can be configured as either a watchdog counter or as an alarm counter. An on-chip oscillator circuit uses a customer-supplied 32.768kHz crystal to keep time.

Oscillator Circuit

The DS1371 uses an external 32.768kHz crystal. The oscillator circuit does not require any external resistors or capacitors to operate (Figure 2). Table 1 specifies several crystal parameters for the external crystal. Using a crystal with the specified characteristics, the startup time is usually less than one second.

Clock Accuracy

The accuracy of the clock is dependent upon the accuracy of the crystal and the accuracy of the match between the capacitive load of the oscillator circuit and the capacitive load for which the crystal was trimmed. Additional error is added by crystal frequency drift caused by temperature shifts. External circuit noise coupled into the oscillator circuit can result in the clock running fast. Figure 3 shows a typical PC board layout for isolation of the crystal and oscillator from noise. Refer to *Application Note 58: Crystal Considerations with Dallas Real-Time Clocks* for detailed information.

Table 1. Crystal Specifications*

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Nominal Frequency	f_O		32.768		kHz
Series Resistance	ESR			50	kΩ
Load Capacitance	C_L		6		pF

**The crystal, traces, and crystal input pins should be isolated from RF generating signals. Refer to* Application Note 58: Crystal Considerations for Dallas Real-Time Clocks *for additional specifications.*

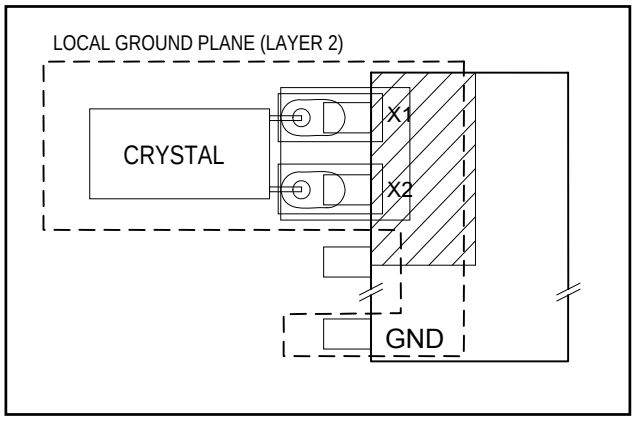


Figure 3. Layout Example

Address Map

Table 2 shows the address map for the registers of the DS1371. During a multibyte access, when the address pointer reaches the end of the register space (08h), it wraps around to location 00h. On an I^2C START, STOP, or address pointer incrementing to location 00h, the current time is transferred to a second set of registers. The time information is read from these secondary registers, while the clock may continue to run. This eliminates the need to reread the registers in case of an update of the main registers during a read.

Table 2. Address Map

ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	FUNCTION
00H	TOD COUNTER BYTE 0								Time-of-Day Counter
01H	TOD COUNTER BYTE 1								Time-of-Day Counter
02H	TOD COUNTER BYTE 2								Time-of-Day Counter
03H	TOD COUNTER BYTE 3								Time-of-Day Counter
04H	WD/$\overline{\text{ALM}}$ COUNTER BYTE 0								Watchdog/ Alarm Counter
05H	WD/$\overline{\text{ALM}}$ COUNTER BYTE 1								Watchdog/ Alarm Counter
06H	WD/$\overline{\text{ALM}}$ COUNTER BYTE 2								Watchdog/ Alarm Counter
07H	$\overline{\text{EOSC}}$	WACE	WD/$\overline{\text{ALM}}$	0	INTCN	RS2	RS1	AIE	Control
08H	OSF	0	0	0	0	0	0	AF	Status

Note: *Unless otherwise specified, the state of the registers are not defined when power is first applied.*

Time-of-Day Counter

The time-of-day counter is a 32-bit up counter. The contents can be read or written by accessing the address range 00h–03h. When the counter is read, the current time of day is latched into a register, which is output on the serial data line while the counter continues to increment. Writing to the counter resets the countdown chain for the time-of-day counter (Figure 2). The watchdog countdown chain is unaffected. If the square-wave output is enabled and is set to 1Hz, the output resets when the countdown chain is reset. Because the other square-wave frequencies are derived before the section of the countdown chain that is reset, the other frequencies are unaffected by a write to the time-of-day counter.

Watchdog/Alarm Counter

If the counter is not needed, it can be disabled and used as a 24-bit cache of NV RAM by setting the WACE bit in the control register to logic 0. If all 24 bits of the watchdog/alarm counter are written to zero, the counter is disabled, independent of the WACE bit setting. When the watchdog counter is written to a nonzero value, and WACE is written to logic 1, the function of the counter is determined by the WD/$\overline{\text{ALM}}$ bit.

Note: The WDS input must be low when writing to the watchdog counter registers.

When the WD/$\overline{\text{ALM}}$ bit in the control register is set to a logic 0, the WD/$\overline{\text{ALM}}$ counter decrements every second until it reaches zero. At this point, the AF bit in the status register is set to a 1 and the counter is reloaded and restarted. AF remains set until cleared by writing it to a 0. If INTCN = AIE = 1, the SQW/$\overline{\text{INT}}$ pin will go active whenever AF = 1.

Note: WACE must be set to a logic 1 after the alarm value is written.

When the WD/$\overline{\text{ALM}}$ bit is set to logic 1, the WD/$\overline{\text{ALM}}$ counter decrements every 1/4096 of a second (approximately every 244µs) until it reaches zero. When any of the watchdog counters bytes are read, the seed value is reloaded and the counter restarts. Writing to the watchdog counter updates the seed value and reloads the counter with the new seed value. A low to high transition on the WDS input reloads and restarts the counter with the seed value. When the counter reaches zero, the AF bit is set and the counter stops. The AF bit remains set until cleared by writing it to 0. If INTCN and AIE are both at logic 1 when the AF bit becomes set, the SQW/$\overline{\text{INT}}$ pin pulses low for 250ms. At the end of the 250ms pulse, the AF bit is cleared and SQW/$\overline{\text{INT}}$ becomes high impedance.

Note: WACE must be toggled from a logic 0 to a logic 1 after the watchdog counter is written from a zero to a nonzero value.

The 250ms pulse on SQW/$\overline{\text{INT}}$ cannot be truncated by writing either AF or AIE to zero during the low time. If the WD/$\overline{\text{ALM}}$ counter is written during the 250ms pulse, the counter starts decrementing upon the pulse completion.

Special Purpose Registers

The DS1371 has two additional registers (07h–08h) that control the WD/$\overline{\text{ALM}}$ counter, square-wave output, and interrupts.

Control Register (07h)

Bit #	7	6	5	4	3	2	1	0
Name	$\overline{\text{EOSC}}$	WACE	WD/$\overline{\text{ALM}}$	0	INTCN	RS2	RS1	AIE
Default	0	0	0	0	0	1	1	0

Bit 7: Enable Oscillator ($\overline{\text{EOSC}}$). When set to logic 0, the oscillator is started. When set to logic 1, the oscillator is stopped. When this bit is set to a logic 1, the oscillator is stopped and the DS1371 is placed into a low-power standby mode (I_{DDR}). This bit is clear (logic 0) when power is first applied.

Bit 6: WD/$\overline{\text{ALM}}$ Counter Enable (WACE). When set to logic 1, the WD/$\overline{\text{ALM}}$ counter is enabled. When set to logic 0, the WD/$\overline{\text{ALM}}$ counter is disabled, and the 24-bits can be used as general-purpose RAM. This bit is clear (logic 0) when power is first applied.

Bit 5: WD/$\overline{\text{ALM}}$ Counter Select (WD/$\overline{\text{ALM}}$). When set to logic 0, the counter decrements every second until it reaches 0 and is then reloaded and restarted. When set to logic 1, the WD/$\overline{\text{ALM}}$ counter decrements every 1/4096 of a second (approximately every 244µs) until it reaches 0, sets the AF bit in the status register, and stops. If any of the WD/$\overline{\text{ALM}}$ counter registers are read or written, or a rising edge on the WDS pin occurs before the counter reaches 0, the counter is reloaded and restarted. This bit is clear (logic 0) when power is first applied.

Bit 3: Interrupt Control (INTCN). This bit controls the SQW/$\overline{\text{INT}}$ signal. When the INTCN bit is set to logic 0, a square wave is output on the SQW/$\overline{\text{INT}}$ pin whose frequency is defined by bits RS2 and RS1. The oscillator must also be enabled for the square wave to be output. When the INTCN bit is set to logic 1, then this permits the alarm flag bit in the status register to assert SQW/$\overline{\text{INT}}$ (provided that the alarm is also enabled). The alarm flag is always set, regardless of the state of the INTCN bit. The INTCN bit is set to logic 0 when power is first applied.

Bits 2 and 1: Rate Select 1 and 2 (RS2 and RS1). These bits control the frequency of the square-wave output when the square wave has been enabled. Table 3 shows the square-wave frequencies that can be selected with the RS bits. These bits are both set (logic 1) when power is first applied.

Bit 0: Alarm Interrupt Enable (AIE). When set to logic 1, this bit permits the AF bit in the status register to assert SQW/$\overline{\text{INT}}$ (when INTCN = 1). When set to logic 0 or INTCN is set to logic 0, the AF bit does not initiate the SQW/$\overline{\text{INT}}$ signal. If the WD/$\overline{\text{ALM}}$ bit is set to a logic 1 and the AF flag is set, writing AIE to a 0 does not truncate the 250ms pulse on the SQW/$\overline{\text{INT}}$ pin. The AIE bit is at logic 0 when power is first applied.

Table 3. SQW/$\overline{\text{INT}}$ Operating Modes

WACE	WD/$\overline{\text{ALM}}$	INTCN	AIE	RS2	RS1	SQW/$\overline{\text{INT}}$ OUTPUT
X	X	0	X	0	0	1Hz
X	X	0	X	0	1	4.096kHz
X	X	0	X	1	0	8.192kHz
X	X	0	X	1	1	32.768kHz
1	0	1	1	X	X	Alarm
1	1	1	1	X	X	WD

Status Register (08h)

Bit #	7	6	5	4	3	2	1	0
Name	OSF	0	0	0	0	0	0	AF
Default	1	0	0	0	0	0	0	—

Bit 7: Oscillator Stop Flag (OSF). A logic 1 in this bit indicates that the oscillator either is stopped or was stopped for some period and can be used to judge the validity of the timekeeping data. This bit is set to logic 1 any time that the oscillator stops. The following are examples of conditions that can cause the OSF bit to be set:

- The first time power is applied.
- The voltage present on V_{CC} is insufficient to support oscillation.
- The $\overline{EOSC}$ bit is turned off.
- External influences on the crystal (e.g., noise, leakage, etc.)
- This bit remains at logic 1 until written to logic 0.

Bit 0: Alarm Flag (AF). A logic 1 in the AF bit indicates that the WD/$\overline{ALM}$ counter reached 0. If INTCN is set to a 1, and WD/$\overline{ALM}$ is set to 0 and AIE is set to 1, the SQW/$\overline{INT}$ pin goes low and stays low until AF is cleared. AF is cleared when written to logic 0. This bit can only be written to logic 0. Attempting to write logic 1 leaves the value unchanged. If INTCN and WD/$\overline{ALM}$ are set to 1 and the AIE is set to 1, the SQW/$\overline{INT}$ pin pulses low for 250ms when the WD/$\overline{ALM}$ counter reaches 0 and sets AF = 1. At the completion of the 250ms pulse, the DS1371 clears the AF bit to a 0. If the 250ms pulse is active, writing AF to a 0 does not truncate the pulse.

I²C Serial Interface

The DS1371 supports a bidirectional I^2C bus and data transmission protocol. A device that sends data onto the bus is defined as a transmitter and a device receiving data as a receiver. The device that controls the message is called a "master." The devices that are controlled by the master are "slaves." The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions. The DS1371 operates as a slave on the I^2C bus. Within the I^2C bus specifications a standard mode (100kHz clock rate) and a fast mode (400kHz clock rate) are defined. The DS1371 works in both modes. Connections to the bus are made through the open-drain I/O lines SDA and SCL.

The following bus protocol has been defined (Figure 4):

- Data transfer can be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is high are interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus not busy: Both data and clock lines remain HIGH.

Start data transfer: A change in the state of the data line from high to low, while the clock line is high, defines a START condition.

Stop data transfer: A change in the state of the data line from low to high, while the clock line is high, defines a STOP condition.

Data valid: The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the high period of the clock signal. The data on the line must be changed during the low period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between the START and the STOP conditions is not limited, and is determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth bit. Within the I^2C bus specifications a standard mode (100kHz clock rate) and a fast mode (400kHz clock rate) are defined.

Acknowledge: Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse, which is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse. Setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

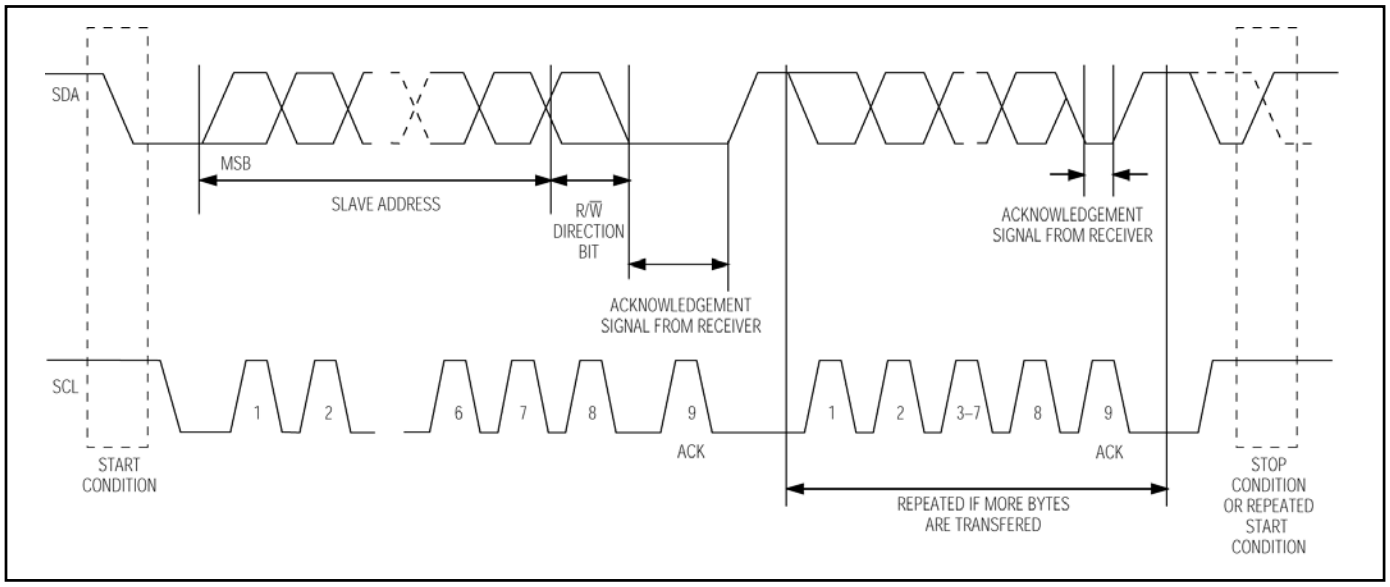


Figure 4. I^2C Data Transfer Overview

Figures 5 and 6 detail how data transfer is accomplished on the I^2C bus. Depending upon the state of the R/$\overline{W}$ bit, two types of data transfer are possible:

Data transfer from a master transmitter to a slave receiver. The first byte transmitted by the master is the slave address. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte.

Data transfer from a slave transmitter to a master receiver. The first byte (the slave address) is transmitted by the master. The slave then returns an acknowledge bit. Next follows a number of data bytes transmitted by the slave to the master. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a "not acknowledge" is returned.

The master device generates all of the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus is not released.

The DS1371 can operate in the following two modes:

Slave receiver mode (DS1371 write mode). Serial data and clock are received through SDA and SCL. After each byte is received, an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit. The slave address byte is the first byte received after the START condition is generated by the master. The slave address byte contains the 7-bit DS1371 address, which is 1101000, followed by the direction bit (R/$\overline{W}$), which for a write is a 0. After receiving and decoding the slave address byte the DS1371 outputs an acknowledge on SDA. After the DS1371 acknowledges the slave address + write bit, the master transmits a word address to the DS1371. This sets the register pointer on the DS1371, with the DS1371 acknowledging the transfer. The master may then transmit zero or more bytes of data, with the DS1371 acknowledging each byte received. The register pointer increments after each byte is transferred. The master generates a STOP condition to terminate the data write.

Slave transmitter mode (DS1371 read mode). The first byte is received and handled as in the slave receiver mode. However, in this mode, the direction bit indicates that the transfer direction is reversed. Serial data is transmitted on SDA by the DS1371 while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit. The slave address byte is the first byte received after the START condition is generated by the master. The slave address byte contains the 7-bit DS1371 address, which is 1101000, followed by the direction bit (R/$\overline{W}$), which for a read is a 1. After receiving and decoding the slave address byte, the DS1371 outputs an acknowledge on SDA. The DS1371 then begins to transmit data starting with the register address pointed to by the register pointer. If the register pointer is not written to before the initiation of a read mode the first address that is read is the last one stored in the register pointer. The DS1371 must receive a "not acknowledge" to end a read.

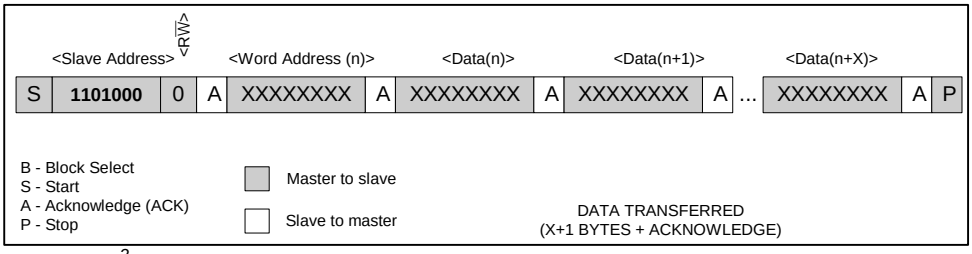


Figure 5. I²C Write Protocol

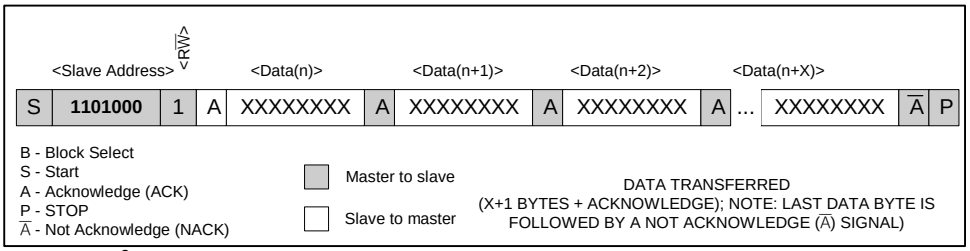


Figure 6. I²C Read Protocol

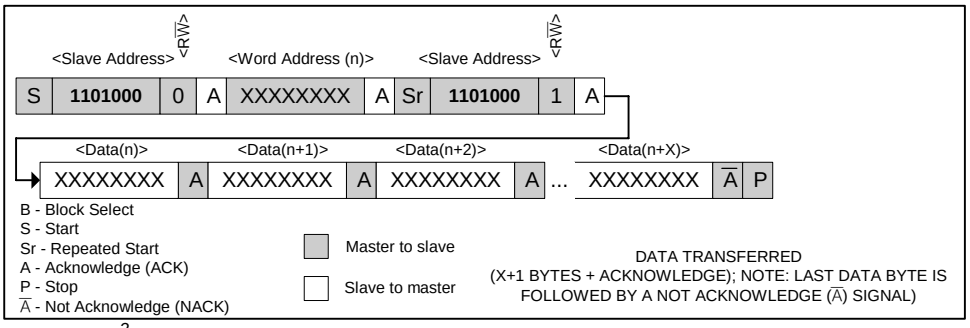


Figure 7. I²C Data Read (Write Pointer, Then Read) Protocol

Chip Information

TRANSISTOR COUNT: 11,036
PROCESS: CMOS
SUBSTRATE CONNECTED TO GROUND

Thermal Information

Theta-JA: 221°C/W
Theta-JC: 39°C/W

Package Information

For the latest package outline information, go to www.maxim-ic.com/DallasPackInfo.

PACKAGE	DOCUMENT NUMBER
8-pin µSOP	**21-0036**

Revision History

REV DATE	DESCRIPTION
110502	Initial data sheet release.
051203	(Page 14) In Figures 6 and 7, corrected the slave address and removed the second "START."
061406	Changed all 2-wire references to I^2C. (Page 1) Added lead-free packages to the *Ordering Information* table. (Page 2) Removed "A" from J-STD-020 (Soldering Temperature) reference. Removed Figure 3 (oscillator circuit) and incorporated into new Figure 2 (page 5). (Page 6) In *Pin Description* table, added sentence saying no external resistors or capacitors are required for pins 1 and 2 (X1 and X2). (Page 7) Removed guard ring from Figure 3 (formerly Figure 4). (Page 9) Updated the *Watchdog/Alarm Counter* section. (Page 10) In Table 3, added the control bits affecting SQW/$\overline{INT}$ output operation. (Page 11) In the *I^2C Serial Interface* section (formerly 2-Wire Serial Interface), added text about the part working in fast and standard I^2C modes. (Page 14) Added package drawing information table.
022207	(Page 1) Corrected top mark information in the *Ordering Information* table. (Page 2) Changed I_{DDR} max from 50nA to 100nA. (Page 7) In Table 1, changed ESR max from 45kΩ to 50kΩ. (Page 8) In Table 2, changed $\overline{WD}$/$\overline{ALM}$ to WD/$\overline{ALM}$ for address 07h (Control Register).
070607	(Page 2) Added "noncondensing" to Operating Temperature Range requirement in the *Absolute Maximum Ratings* section. (Page 14) Corrected/added I^2C read and write protocol figures. (Page 14) Changed package information document number to 21-0036.

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