DS1315
Phantom Time Chip

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FEATURES

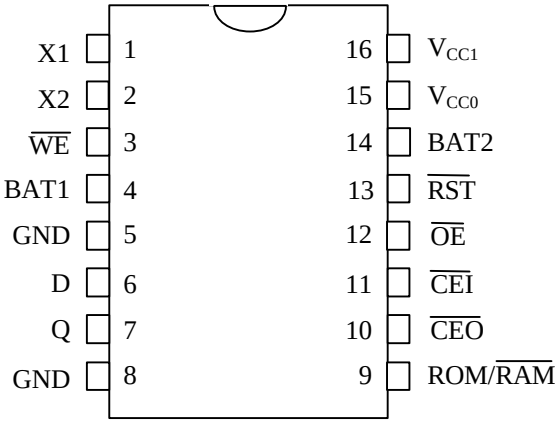
- Real time clock keeps track of hundredths of seconds, seconds, minutes, hours, days, date of the month, months, and years
- Adjusts for months with fewer than 31 days
- Automatic leap year correction valid up to 2100
- No address space required to communicate with RTC
- Provides nonvolatile controller functions for battery backup of SRAM
- Supports redundant battery attachment for high–reliability applications
- Full ±10% V_{CC} operating range
- +3.3 volt or +5 volt operation
- Industrial (–45°C to +85°C) operating temperature ranges available
- Drop in replacement for DS1215

ORDERING INFORMATION

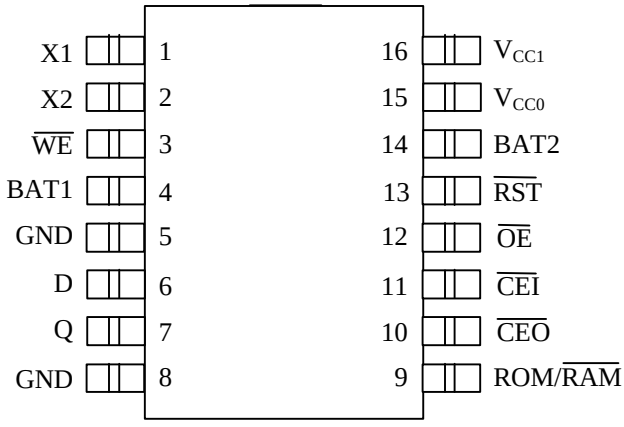
DS1315XX-XX

- 33-3.3 volt operation
  5-5 volt operation
- blank-commercial temp range
  N-industrial temp range
- blank-16-pin DIP
  S-16-pin SOIC
  E-20-pin TSSOP

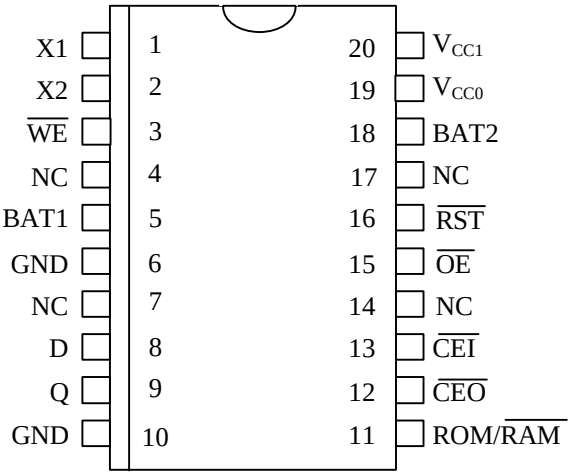
PIN ASSIGNMENT



16-Pin DIP (300-mil)



16-Pin SOIC (300-mil)



20-Pin TSSOP

PIN DESCRIPTION

X1, X2 - 32.768 kHz Crystal Connection
$\overline{WE}$ - Write Enable
BAT1 - Battery 1 Input
GND - Ground
D - Data Input
Q - Data Output
ROM/$\overline{RAM}$ - ROM/RAM Mode Select
$\overline{CEO}$ - Chip Enable Output
$\overline{CEI}$ - Chip Enable Input
$\overline{OE}$ - Output Enable
$\overline{RST}$ - Reset
BAT2 - Battery 2 Input
V_{CC0} - Switched Supply Output
V_{CC1} - Power Supply Input

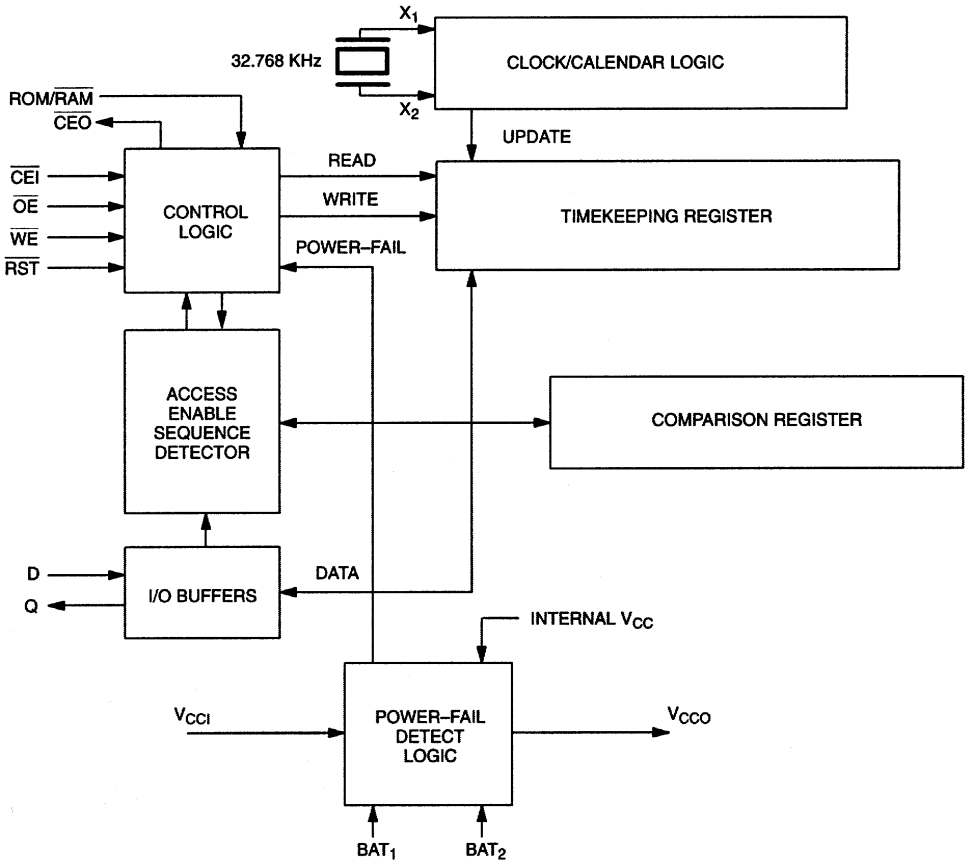
DESCRIPTION

The DS1315 Phantom Time Chip is a combination of a CMOS timekeeper and a nonvolatile memory controller. In the absence of power, an external battery maintains the timekeeping operation and provides power for a CMOS static RAM. The watch keeps track of hundredths of seconds, seconds, minutes, hours, day, date, month, and year information. The last day of the month is automatically adjusted for months with less than 31 days, including leap year correction. The watch operates in one of two formats: a 12-hour mode with an AM/PM indicator or a 24-hour mode. The nonvolatile controller supplies all the necessary support circuitry to convert a CMOS RAM to a nonvolatile memory. The DS1315 can be interfaced with either RAM or ROM without leaving gaps in memory.

OPERATION

The block diagram of Figure 1 illustrates the main elements of the Time Chip. The following paragraphs describe the signals and functions.

TIMING BLOCK DIAGRAM Figure 1



Communication with the Time Chip is established by pattern recognition of a serial bit stream of 64 bits which must be matched by executing 64 consecutive write cycles containing the proper data on data in (D). All accesses which occur prior to recognition of the 64-bit pattern are directed to memory via the chip enable output pin ($\overline{CEO}$).

After recognition is established, the next 64 read or write cycles either extract or update data in the Time Chip and $\overline{CEO}$ remains high during this time, disabling the connected memory.

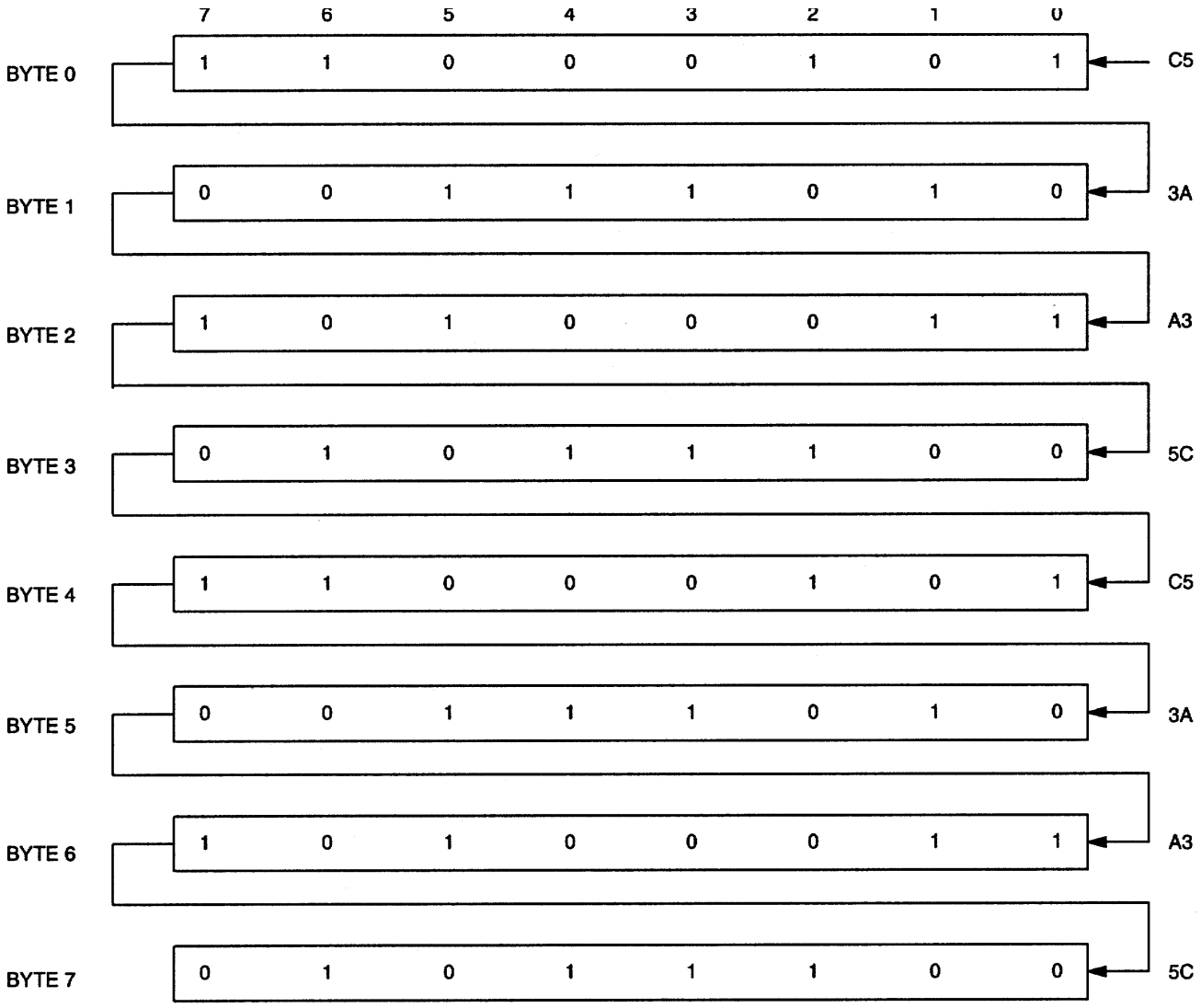
Data transfer to and from the timekeeping function is accomplished with a serial bit stream under control of chip enable input ($\overline{CEI}$), output enable ($\overline{OE}$), and write enable ($\overline{WE}$). Initially, a read cycle using the $\overline{CEI}$ and $\overline{OE}$ control of the Time Chip starts the pattern recognition sequence by moving pointer to the first bit of the 64-bit comparison register. Next, 64 consecutive write cycles are executed using the $\overline{CEI}$ and $\overline{WE}$ control of the Time Chip. These 64 write cycles are used only to gain access to the Time Chip.

When the first write cycle is executed, it is compared to bit 1 of the 64-bit comparison register. If a match is found, the pointer increments to the next location of the comparison register and awaits the next write cycle. If a match is not found, the pointer does not advance and all subsequent write cycles are ignored. If a read cycle occurs at any time during pattern recognition, the present sequence is aborted and the comparison register pointer is reset. Pattern recognition continues for a total of 64 write cycles as described above until all the bits in the comparison register have been matched. (This bit pattern is shown in Figure 2). With a correct match for 64 bits, the Time Chip is enabled and data transfer to or from the timekeeping registers may proceed. The next 64 cycles will cause the Time Chip to either receive data on D, or transmit data on Q, depending on the level of $\overline{OE}$ pin or the $\overline{WE}$ pin. Cycles to other locations

outside the memory block can be interleaved with $\overline{CEI}$ cycles without interrupting the pattern recognition sequence or data transfer sequence to the Time Chip.

A standard 32.768 kHz quartz crystal can be directly connected to the DS1315 via pins 1 and 2 (X1, X2). The crystal selected for use should have a specified load capacitance (C_L) of 6 pF. For more information on crystal selection and crystal layout considerations, please consult Application Note 58, "Crystal Considerations with Dallas Real Time Clocks."

TIME CHIP COMPARISON REGISTER DEFINITION Figure 2



NOTE:

The pattern recognition in Hex is C5, 3A, A3, 5C, C5, 3A, A3, 5C. The odds of this pattern being accidentally duplicated and causing inadvertent entry to the Phantom Time Chip are less than 1 in 10^{19}.

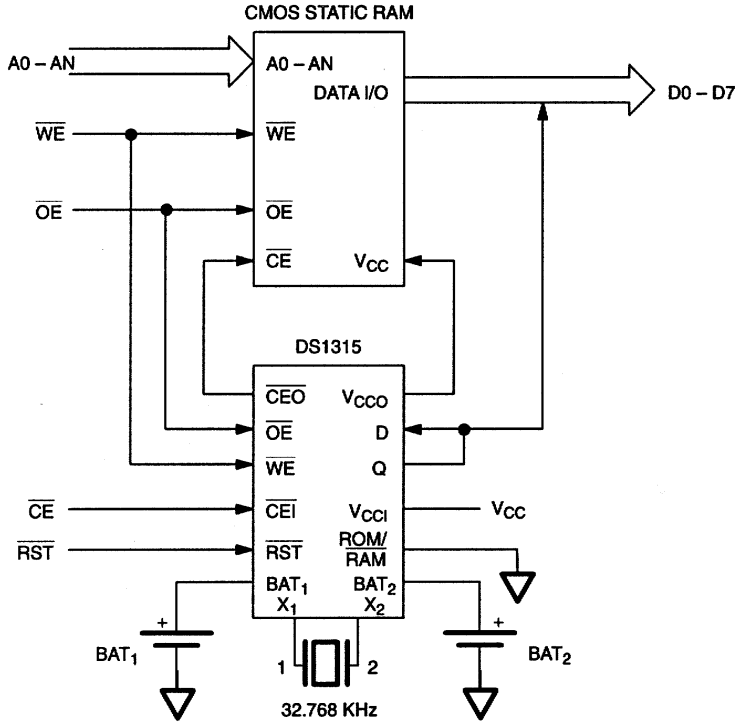
NONVOLATILE CONTROLLER OPERATION

The operation of the nonvolatile controller circuits within the Time Chip is determined by the level of the ROM/$\overline{\text{RAM}}$ select pin. When ROM/$\overline{\text{RAM}}$ is connected to ground, the controller is set in the RAM mode and performs the circuit functions required to make CMOS RAM and the timekeeping function nonvolatile. A switch is provided to direct power from the battery inputs or V_{CCI} to V_{CCO} with a maximum voltage drop of 0.3 volts. The V_{CCO} output pin is used to supply uninterrupted power to CMOS SRAM. The DS1315 also performs redundant battery control for high reliability. On power-fail, the battery with the highest voltage is automatically switched to V_{CCO}. If only one battery is used in the system, the unused battery input should be connected to ground.

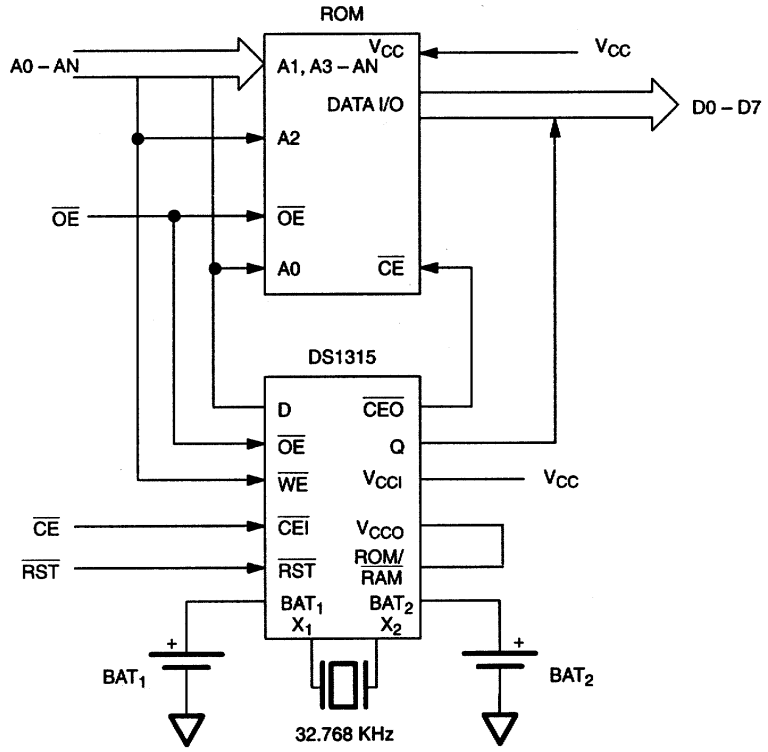
The DS1315 safeguards the Time Chip and RAM data by power-fail detection and write protection. Power-fail detection occurs when V_{CCI} falls below V_{PF} which is set by an internal bandgap reference. The DS1315 constantly monitors the V_{CCI} supply pin. When V_{CCI} is less than V_{PF}, power-fail circuitry forces the chip enable output ($\overline{\text{CEO}}$) to V_{CCI} or V_{BAT}-0.2 volts for external RAM write protection. During nominal supply conditions, $\overline{\text{CEO}}$ will track $\overline{\text{CEI}}$ with a propagation delay. Internally, the DS1315 aborts any data transfer in progress without changing any of the Time Chip registers and prevents future access until V_{CCI} exceeds V_{PF}. A typical RAM/Time Chip interface is illustrated in Figure 3.

When the ROM/$\overline{\text{RAM}}$ pin is connected to V_{CCO}, the controller is set in the ROM mode. Since ROM is a read-only device that retains data in the absence of power, battery backup and write protection is not required. As a result, the chip enable logic will force $\overline{\text{CEO}}$ low when power fails. However, the Time Chip does retain the same internal nonvolatility and write protection as described in the RAM mode. A typical ROM/Time Chip interface is illustrated in Figure 4.

DS1315 TO RAM/TIME CHIP INTERFACE Figure 3



ROM/TIME CHIP INTERFACE Figure 4



TIME CHIP REGISTER INFORMATION

Time Chip information is contained in eight registers of 8 bits, each of which is sequentially accessed 1 bit at a time after the 64-bit pattern recognition sequence has been completed. When updating the Time Chip registers, each must be handled in groups of 8 bits. Writing and reading individual bits within a register could produce erroneous results. These read/write registers are defined in Figure 5.

Data contained in the Time Chip registers is in binary coded decimal format (BCD). Reading and writing the registers is always accomplished by stepping though all eight registers, starting with bit 0 of register 0 and ending with bit 7 of register 7.

AM–PM/12/24 MODE

Bit 7 of the hours register is defined as the 12- or 24-hour mode select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the AM/PM bit with logic high being PM. In the 24-hour mode, bit 5 is the second 10-hour bit (20-23 hours).

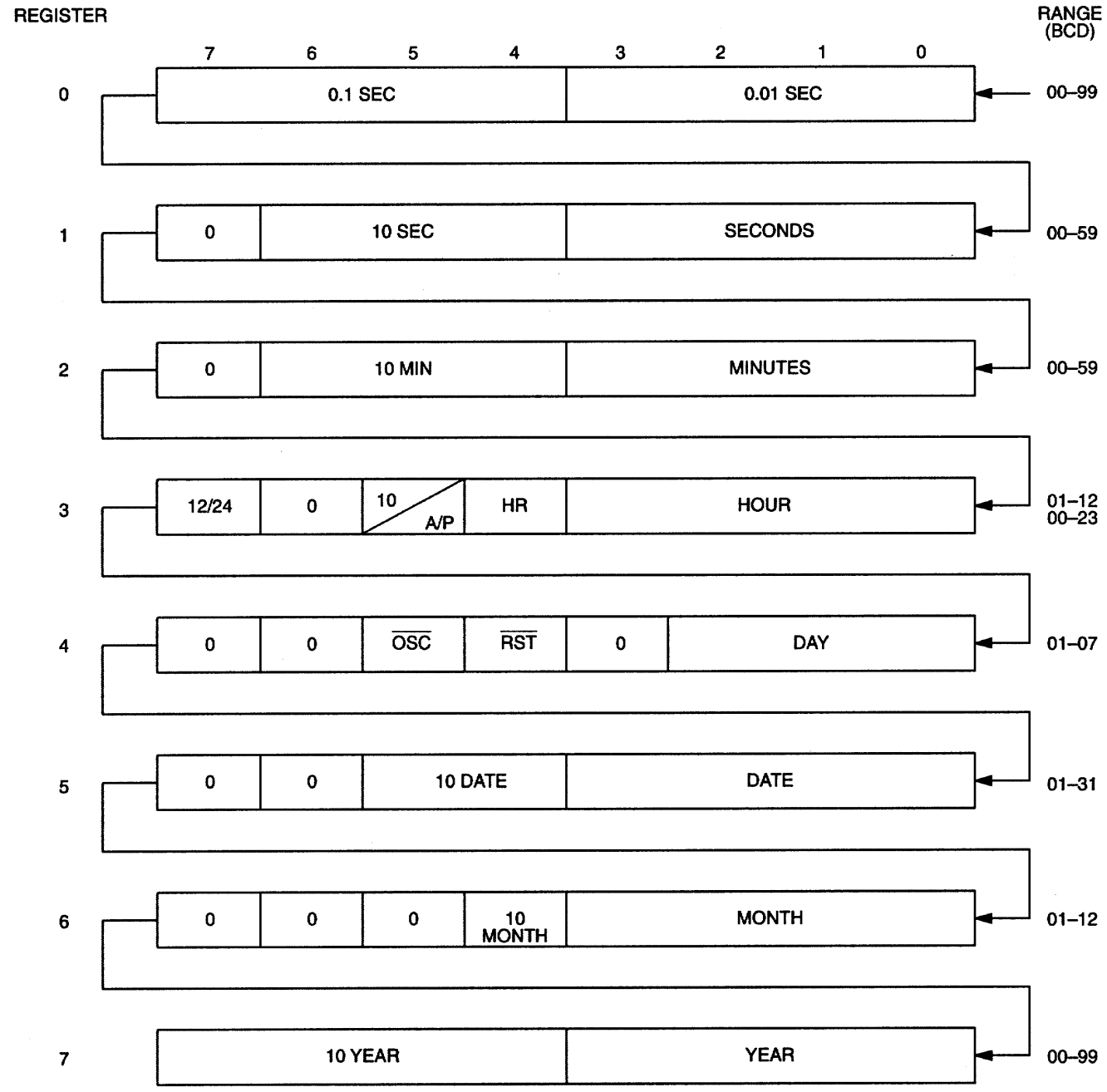
OSCILLATOR AND RESET BITS

Bits 4 and 5 of the day register are used to control the reset and oscillator functions. Bit 4 controls the reset pin input. When the reset bit is set to logic 1, the reset input pin is ignored. When the reset bit is set to logic 0, a low input on the reset pin will cause the Time Chip to abort data transfer without changing data in the timekeeping registers. Reset operates independently of all other in-puts. Bit 5 controls the oscillator. When set to logic 0, the oscillator turns on and the real time clock/calendar begins to increment.

ZERO BITS

Registers 1, 2, 3, 4, 5, and 6 contain 1 or more bits that will always read logic 0. When writing these locations, either a logic 1 or 0 is acceptable.

TIME CHIP REGISTER DEFINITION Figure 5



ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature, commercial range	0°C to 70°C
Operating Temperature, industrial range	-45°C to +85°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage 5 Volt Operation	V_{CC}	4.5	5.0	5.5	V	1
Power Supply Voltage 3.3 Volt Operation	V_{CC}	3.0	3.3	3.6	V	1
Input Logic 1	V_{IH}	2.2		V_{CC}+0.3	V	1
Input Logic 0	V_{IL}	-0.3		+0.6	V	1
Battery Voltage V_{BAT1} or V_{BAT2}	V_{BAT1}, V_{BAT2}	2.5		3.7	V	

DC OPERATING ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 5.0 ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Average V_{CC} Power Supply Current	I_{CC1}			5	mA	6
V_{CC} Power Supply Current, (V_{CC0} = V_{CCI}-0.3)	I_{CC01}			150	mA	7
TTL Standby Current ($\overline{CEI}$ = V_{IH})	I_{CC2}			3	mA	6
CMOS Standby Current ($\overline{CEI}$ = V_{CCI}-0.2)	I_{CC3}			1	mA	6
Input Leakage Current (any input)	I_{IL}	-1		+1	µA	10
Output Leakage Current (any input)	I_{OL}	-1		+1	µA	
Output Logic 1 Voltage (I_{OUT} = -1.0 mA)	V_{OH}	2.4			V	2
Output Logic 0 Voltage (I_{OUT} = 4.0 mA)	V_{OL}			0.4	V	2
Power-Fail Trip Point	V_{PF}	4.25		4.5	V	
Battery Switch Voltage	V_{SW}		V_{BAT1}, V_{BAT2}			13

DC POWER DOWN ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} < 4.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CEO}$ Output Voltage	V_{CEO}	V_{CCI}-0.2 or $V_{BAT1,2}$ -0.2			V	8
V_{BAT1} or V_{BAT2} Battery Current	I_{BAT}			0.5	µA	6
Battery Backup Current @ $V_{CCO} = V_{BAT}$-0.2V	I_{CCO2}			10	µA	9

AC ELECTRICAL OPERATING CHARACTERISTICS

ROM/$\overline{RAM}$ = GND (0°C to 70°C; V_{CC} = 5.0 ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	65			ns	
$\overline{CEI}$ Access Time	t_{CO}			55	ns	
$\overline{OE}$ Access Time	t_{OE}			55	ns	
$\overline{CEI}$ to Output Low Z	t_{COE}	5			ns	
$\overline{OE}$ to Output Low Z	t_{OEE}	5			ns	
$\overline{CEI}$ to Output High Z	t_{OD}			25	ns	
$\overline{OE}$ to Output High Z	t_{ODO}			25	ns	
Read Recovery	t_{RR}	10			ns	
Write Cycle	t_{WC}	65			ns	
Write Pulse Width	t_{WP}	55			ns	
Write Recovery	t_{WR}	10			ns	4
Data Setup	t_{DS}	30			ns	5
Data Hold Time	t_{DH}	0			ns	5
$\overline{CEI}$ Pulse Width	t_{CW}	55			ns	
$\overline{OE}$ Pulse Width	t_{OW}	55			ns	
$\overline{RST}$ Pulse Width	t_{RST}	65			ns	

AC ELECTRICAL OPERATING CHARACTERISTICS

ROM/$\overline{\text{RAM}}$ = V_{CCO} (0°C to 70°C; V_{CC} = 5.0 ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	65			ns	
$\overline{\text{CEI}}$ Access Time	t_{CO}			55	ns	
$\overline{\text{OE}}$ Access Time	t_{OE}			55	ns	
$\overline{\text{CEI}}$ to Output Low Z	t_{COE}	5			ns	
$\overline{\text{OE}}$ to Output Low Z	t_{OEE}	5			ns	
$\overline{\text{CEI}}$ to Output High Z	t_{OD}			25	ns	
$\overline{\text{OE}}$ to Output High Z	t_{ODO}			25	ns	
Address Setup Time	t_{AS}	5			ns	
Address Hold Time	t_{AH}	5			ns	
Read Recovery	t_{RR}	10			ns	
Write Cycle	t_{WC}	65			ns	
$\overline{\text{CEI}}$ Pulse Width	t_{CW}	55			ns	
$\overline{\text{OE}}$ Pulse Width	t_{OW}	55			ns	
Write Recovery	t_{WR}	10			ns	4
Data Setup	t_{DS}	30			ns	5
Data Hold Time	t_{DH}	0			ns	5
$\overline{\text{RST}}$ Pulse Width	t_{RST}	65			ns	

DC OPERATING ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 3.3 ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Average V_{CC} Power Supply Current	I_{CC1}			3	mA	6
Average V_{CC} Power Supply Current, (V_{CCO} = V_{CCI}-0.3)	I_{CC01}			100	mA	7
TTL Standby Current ($\overline{\text{CEI}}$ = V_{IH})	I_{CC2}			2	mA	6
CMOS Standby Current ($\overline{\text{CEI}}$ = V_{CCI}-0.2)	I_{CC3}			1	mA	6
Input Leakage Current (any input)	I_{IL}	-1		+1	µA	
Output Leakage Current (any input)	I_{LO}	-1		+1	µA	
Output Logic 1 Voltage (I_{OUT} = 0.4 mA)	V_{OH}	2.4			V	2
Output Logic 0 Voltage (I_{OUT} = 1.6 mA)	V_{OL}			0.4	V	2
Power-Fail Trip Point	V_{PF}	2.8		2.97	V	
Battery Switch Voltage	V_{SW}		V_{BAT1}, V_{BAT2}, or V_{PF}			14

DC POWER DOWN ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} < 2.97V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CEO}$ Output Voltage	V_{CEO}	V_{CCI} or $V_{BAT1,2}$ -0.2			V	8
V_{BAT1} OR V_{BAT2} Battery Current	I_{BAT}			0.3	µA	6
Battery Backup Current @ $V_{CCO} = V_{BAT}$-0.2	I_{CCO2}			10	µA	9

AC ELECTRICAL OPERATING CHARACTERISTICS

ROM/$\overline{RAM}$ = GND (0°C to 70°C; V_{CC} = 3.3 ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	120			ns	
$\overline{CEI}$ Access Time	t_{CO}			100	ns	
$\overline{OE}$ Access Time	t_{OE}			100	ns	
$\overline{CEI}$ to Output Low Z	t_{COE}	5			ns	
$\overline{OE}$ to Output Low Z	t_{OEE}	5			ns	
$\overline{CEI}$ to Output High Z	t_{OD}			40	ns	
$\overline{OE}$ to Output High Z	t_{ODO}			40	ns	
Read Recovery	t_{RR}	20			ns	
Write Cycle	t_{WC}	120			ns	
Write Pulse Width	t_{WP}	100			ns	
Write Recovery	t_{WR}	20			ns	4
Data Setup	t_{DS}	45			ns	5
Data Hold Time	t_{DH}	0			ns	5
$\overline{CEI}$ Pulse Width	t_{CW}	100			ns	
$\overline{OE}$ Pulse Width	t_{OW}	100			ns	
$\overline{RST}$ Pulse Width	t_{RST}	120			ns	

AC ELECTRICAL OPERATING CHARACTERISTICS

ROM/$\overline{\text{RAM}}$ = V_{CCO} (0°C to 70°C; V_{CC} = 3.3 ± 10%)

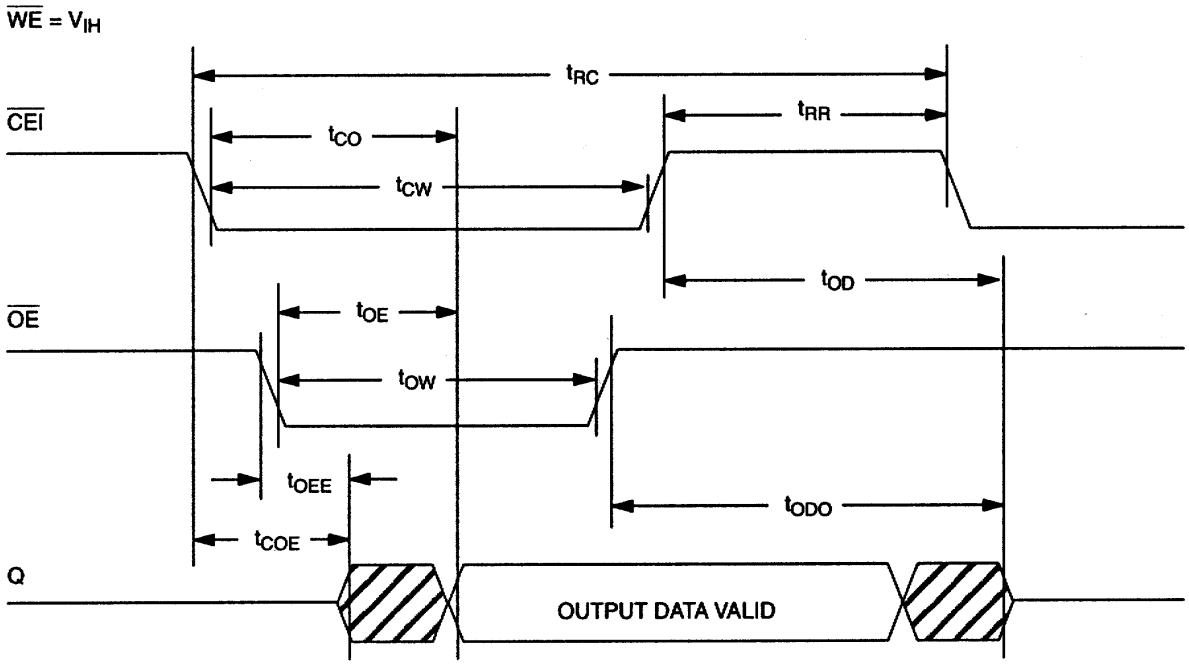
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	120			ns	
$\overline{\text{CEI}}$ Access Time	t_{CO}			100	ns	
$\overline{\text{OE}}$ Access Time	t_{OE}			100	ns	
$\overline{\text{CEI}}$ to Output Low Z	t_{COE}	5			ns	
$\overline{\text{OE}}$ to Output Low Z	t_{OEE}	5			ns	
$\overline{\text{CEI}}$ to Output High Z	t_{OD}			40	ns	
$\overline{\text{OE}}$ to Output High Z	t_{ODO}			40	ns	
Address Setup Time	t_{AS}	10			ns	
Address Hold Time	t_{AH}	10			ns	
Read Recovery	t_{RR}	20			ns	
Write Cycle	t_{WC}	120			ns	
$\overline{\text{CEI}}$ Pulse Width	t_{CW}	100			ns	
$\overline{\text{OE}}$ Pulse Width	t_{OW}	100			ns	
Write Recovery	t_{WR}	20			ns	4
Data Setup	t_{DS}	45			ns	5
Data Hold Time	t_{DH}	0			ns	5
$\overline{\text{RST}}$ Pulse Width	t_{RST}	120			ns	

CAPACITANCE

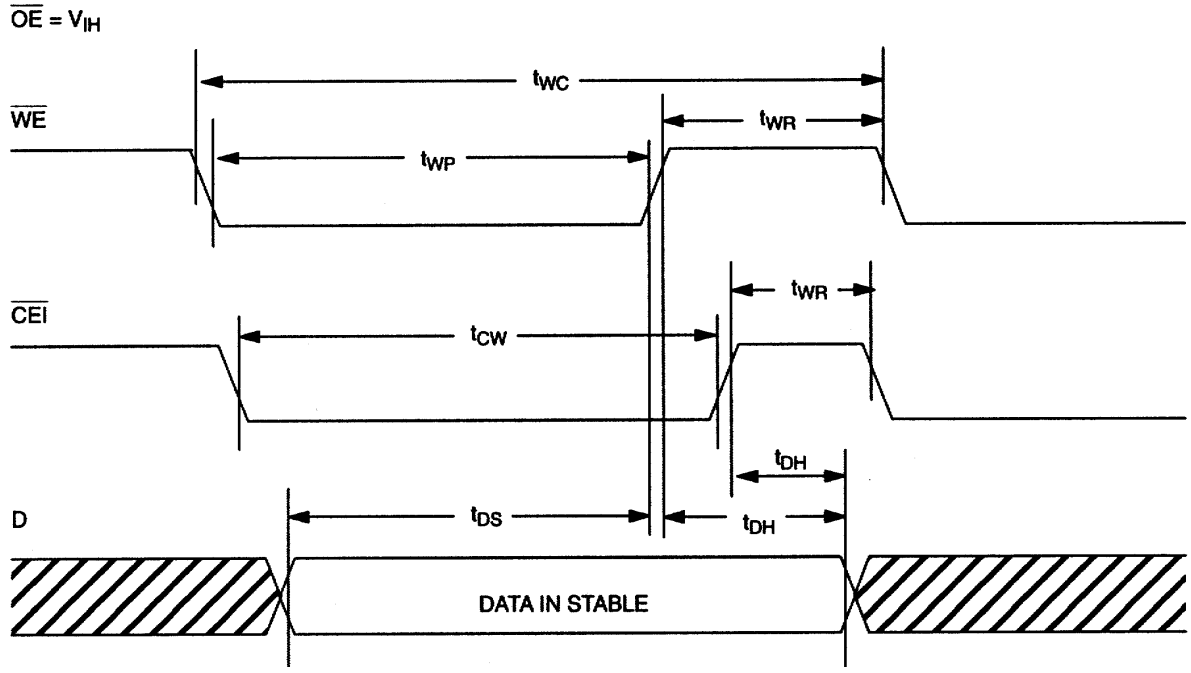
(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			10	pF	
Output Capacitance	C_{OUT}			10	pF	

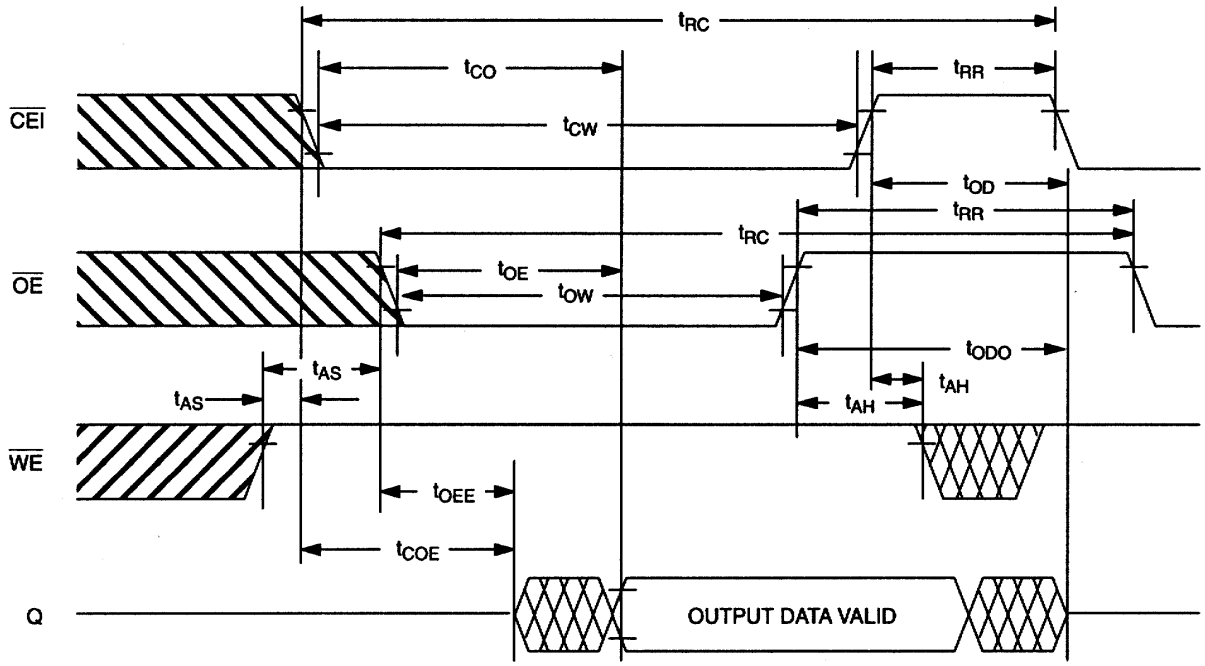
TIMING DIAGRAM: READ CYCLE TO TIME CHIP ROM/$\overline{\text{RAM}}$ = GND Figure 6



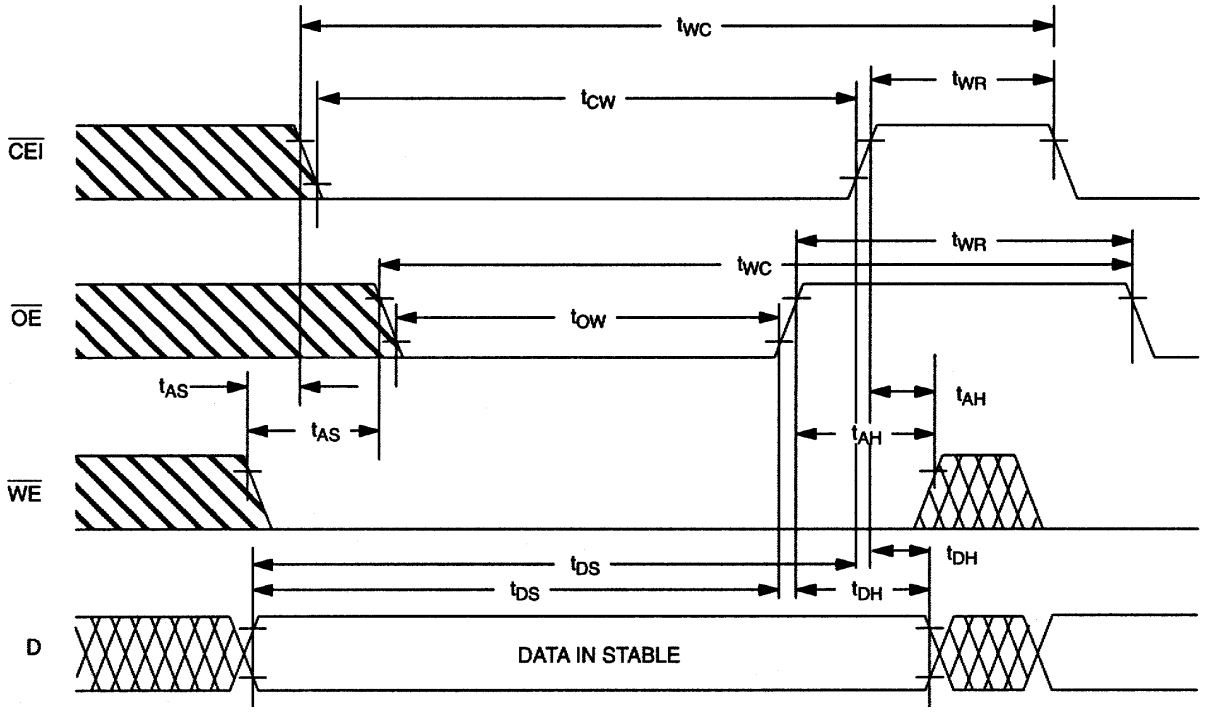
TIMING DIAGRAM: WRITE CYCLE TO TIME CHIP ROM/$\overline{\text{RAM}}$ = GND Figure 7



TIMING DIAGRAM: READ CYCLE TO TIME CHIP ROM/$\overline{RAM}$ = V_{CCO} Figure 8



TIMING DIAGRAM: WRITE CYCLE TO TIME CHIP ROM/$\overline{RAM}$ = V_{CCO} Figure 9

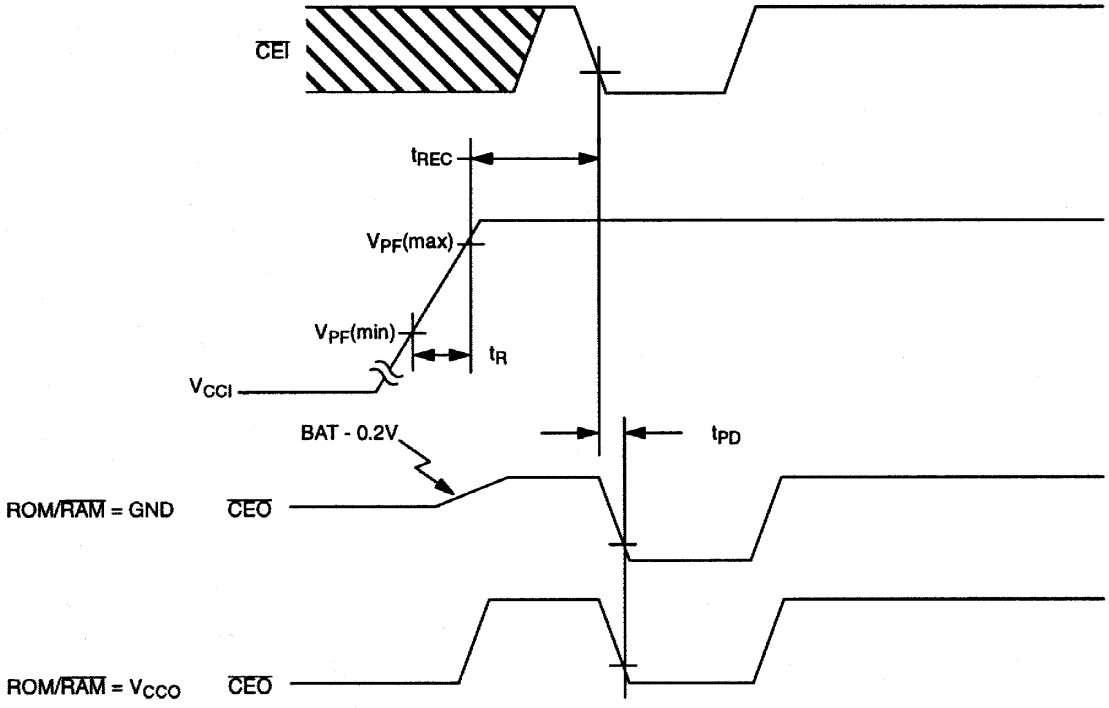


TIMING DIAGRAM: RESET PULSE Figure 10

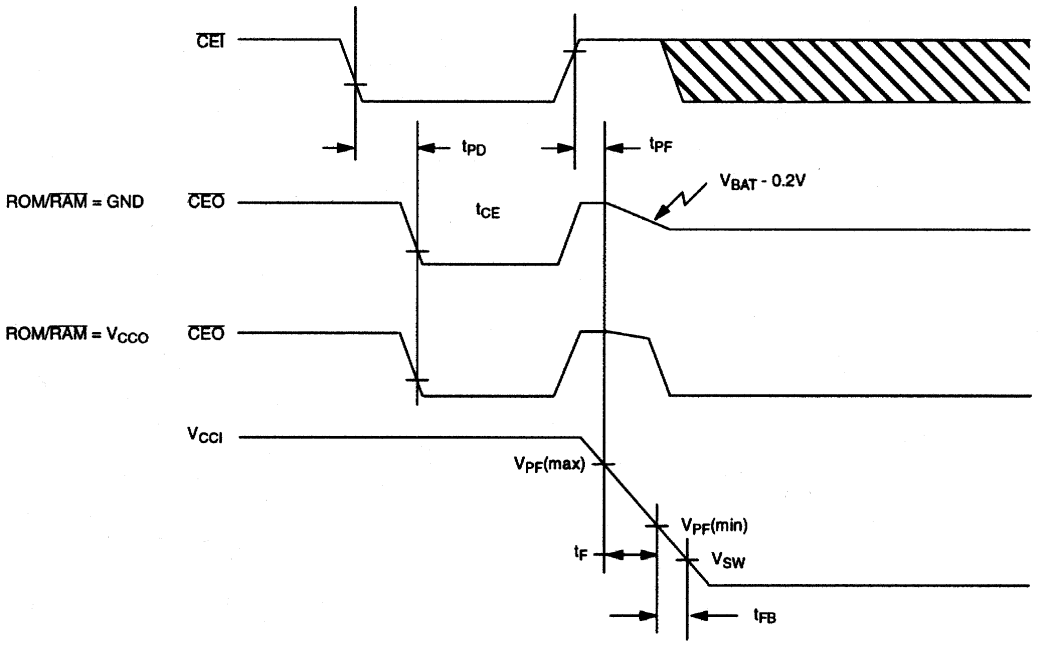
5V DEVICE POWER-UP POWER-DOWN CHARACTERISTICS, ROM/$\overline{\text{RAM}}$ = V_{CCO} OR GND (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Recovery Time at Power-Up	t_{REC}	1.5		2.5	mS	11
V_{CC} Slew Rate Power-Down V_{PF}(max) to V_{PF}(min)	t_F	300			µs	11
V_{CC} Slew Rate Power-Down V_{PF}(min) to V_{SW}	t_{FB}	10			µs	11
V_{CC} Slew Rate Power-Up V_{PF}(min) to V_{PF}(max)	t_R	0			µs	11
$\overline{\text{CEI}}$ High to Power-Fail	t_{PF}			0	µs	11
$\overline{\text{CEI}}$ Propagation Delay	t_{PD}			5	ns	2, 3, 11

5V DEVICE POWER-UP CONDITION Figure 11



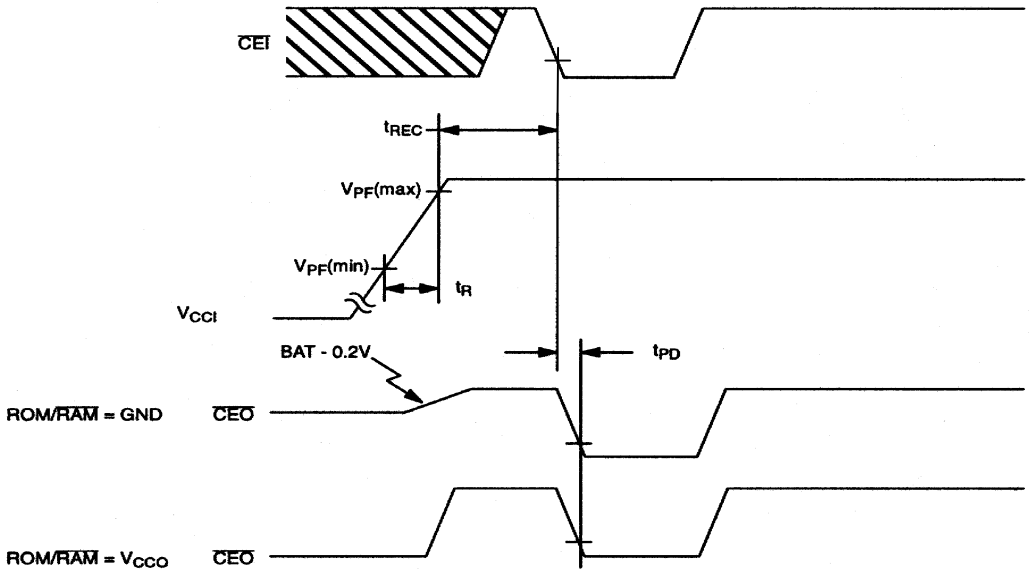
5V DEVICE POWER-DOWN CONDITION Figure 12



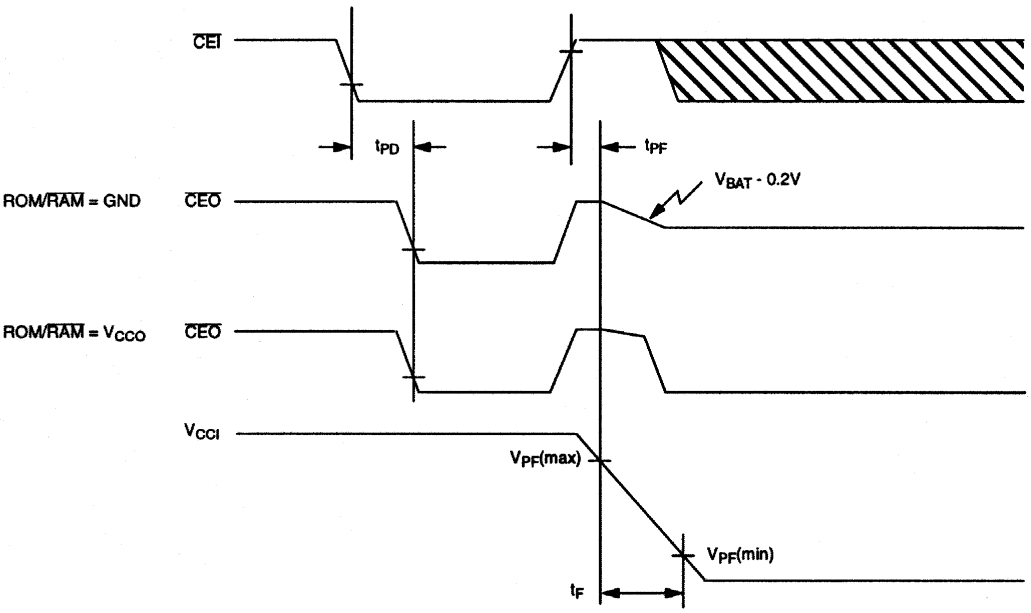
3.3V DEVICE POWER-UP POWER-DOWN CHARACTERISTICS, ROM/$\overline{\text{RAM}}$ = V_{CCO} OR GND (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Recovery Time at Power-Up	t_{REC}	1.5		2.5	ms	12
V_{CC} Slew Rate Power-Down V_{PF}(max) to V_{PF}(min)	t_F	300			µs	12
V_{CC} Slew Rate Power-Up V_{PF}(min) to V_{PF}(max)	t_R	0			µs	12
$\overline{\text{CEI}}$ High to Power-Fail	t_{PF}	0			µs	12
$\overline{\text{CEI}}$ Propagation Delay	t_{PD}			10	ns	2, 3, 11

3.3V DEVICE POWER-UP CONDITION Figure 13



3.3V DEVICE POWER-DOWN CONDITION Figure 14



NOTES:

1. All voltages are referenced to ground.

2. Measured with load shown in Figure 15.

3. Input pulse rise and fall times equal 10 ns.

4. t_{WR} is a function of the latter occurring edge of $\overline{WE}$ or $\overline{CE}$ in RAM mode, or $\overline{OE}$ or $\overline{CE}$ in ROM mode.

5. t_{DH} and t_{DS} are functions of the first occurring edge of $\overline{WE}$ or $\overline{CE}$ in RAM mode, or $\overline{OE}$ or $\overline{CE}$ in ROM mode.

6. Measured without RAM connected.

7. I_{CCO1} is the maximum average load current the DS1315 can supply to external memory.

8. Applies to $\overline{CEO}$ with the ROM/$\overline{RAM}$ pin grounded. When the ROM/$\overline{RAM}$ pin is connected to V_{CCO}, $\overline{CEO}$ will go to a low level as V_{CCI} falls below V_{BAT}.

9. I_{CCO2} is the maximum average load current that the DS1315 can supply to memory in the battery backup mode.

10. Applies to all input pins except $\overline{RST}$. $\overline{RST}$ is pulled internally to V_{CCI}.

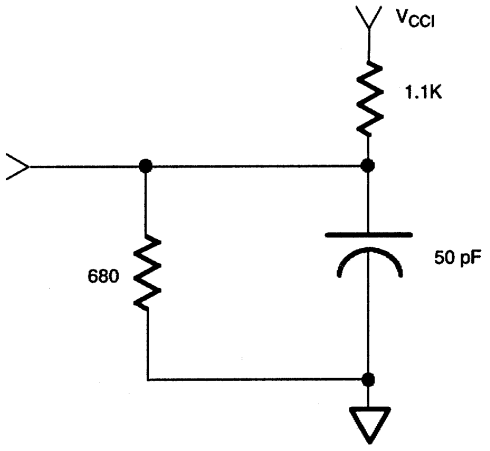
11. See Figures 11 and 12.

12. See Figures 13 and 14.

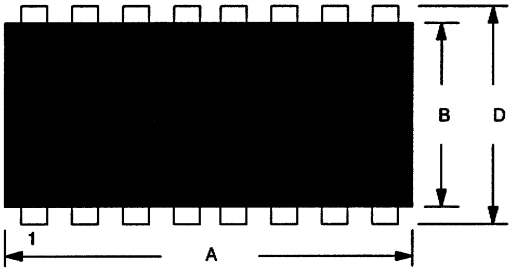
13. V_{SW} is determined by the larger of V_{BAT1} and V_{BAT2}.

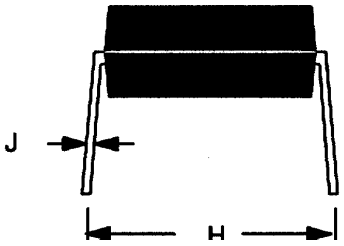
14. V_{SW} is determined by the smaller of V_{BAT1}, V_{BAT2}, and V_{PF}.

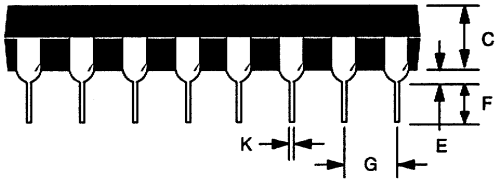
OUTPUT LOAD Figure 15



DS1315 TIME CHIP 16-PIN DIP

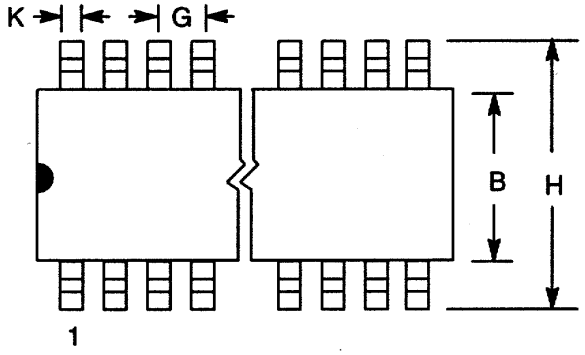


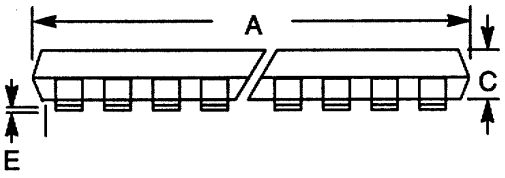


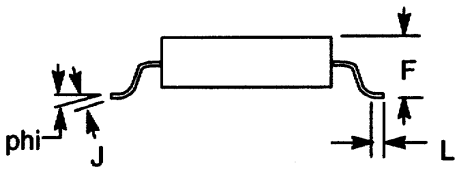


PKG	16-PIN	
DIM.	MIN	MAX
A IN. MM	0.740	0.780
B IN. MM	0.240	0.260
C IN. MM	0.120	0.140
D IN. MM	0.300	0.325
E IN. MM	0.015	0.040
F IN. MM	0.110	0.140
G IN. MM	0.090	0.110
H IN. MM	0.300	0.370
J IN. MM	0.008	0.012
K IN. MM	0.015	0.021

DS1315 TIME CHIP 16-PIN SOIC

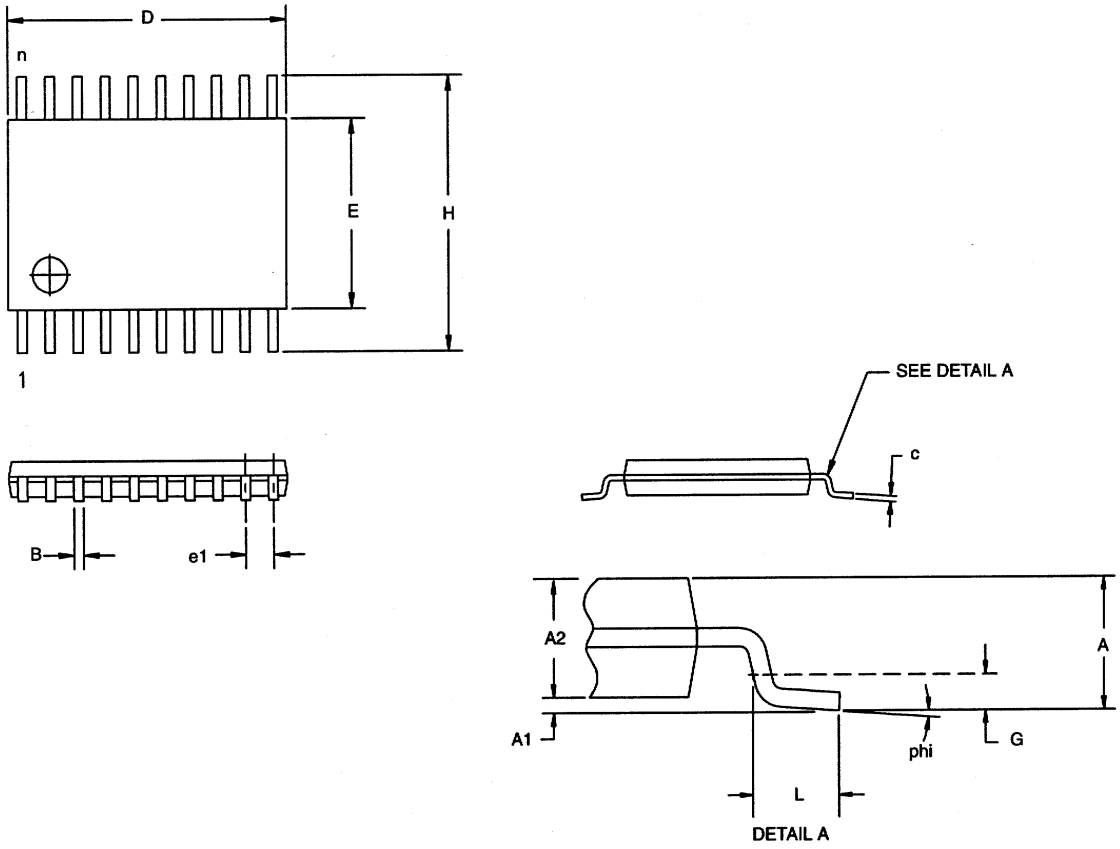






PKG	16-PIN	
DIM	MIN	MAX
A IN.	0.402	0.412
MM	10.21	10.46
B IN.	0.290	0.300
MM	7.37	7.65
C IN.	0.089	0.095
MM	2.26	2.41
E IN.	0.004	0.012
MM	0.102	0.30
F IN.	0.094	0.105
MM	2.38	2.68
G IN.	0.050 BSC	
MM	1.27 BSC	
H IN.	0.398	0.416
MM	10.11	10.57
J IN.	0.009	0.013
MM	0.229	0.33
K IN.	0.013	0.019
MM	0.33	0.48
L IN.	0.016	0.040
MM	0.40	1.02
PHI	0°	8°

DS1315 TIME CHIP 16-PIN TSSOP



DIM	MIN	MAX
A MM	-	1.10
A1 MM	0.05	-
A2 MM	0.75	1.05
C MM	0.09	0.18
L MM	0.50	0.70
e1 MM	0.65 BSC	
B MM	0.18	0.30
D MM	6.40	6.90
E MM	4.40 NOM	
G MM	0.25 REF	
H MM	6.25	6.55
phi	0°	8°