DS100DF410 Low Power 10GbE Quad Channel Retimer

1 Features

- Each Channel Independently Locks to 10.3125 Gbps
- Lock Operation (typically under 15 ms)
- Low Latency (~300 ps)
- Adaptive Equalization up to 34 dB Boost at 5 GHz
- Adjustable Transmit V_{OD}: 600 to 1300 mVp-p
- Adjustable Transmit De-emphasis to –12 dB
- Typical Power Dissipation (EQ+DFE+CDR+DE): 180 mW/channel
- Programmable Output Polarity Inversion
- Input Signal Detection, CDR Lock Detection/Indicator
- On-chip Eye Monitor (EOM), PRBS Generator
- Single 2.5 V ±5% Power Supply
- SMBus/EEPROM Configuration Modes
- Operating Temperature Range of –40°C to 85°C
- WQFN 48-Pin, 7 mm x 7 mm Package
- Easy Pin Compatible Upgrade Between Repeater and Retimers
  - DS100RT410 (EQ+CDR+DE): 10.3125 Gbps
  - DS100DF410 (EQ+DFE+CDR+DE): 10.3125 Gbps
  - DS110RT410 (EQ+CDR+DE): 8.5–11.3 Gbps
  - DS110DF410 (EQ+DFE+CDR+DE): 8.5–11.3 Gbps
  - DS125RT410 (EQ+CDR+DE): 9.8–12.5 Gbps
  - DS125DF410 (EQ+DFE+CDR+DE): 9.8–12.5 Gbps
  - DS100BR410 (EQ+DE): Up to 10.3125 Gbps

2 Applications

- Front Port SFF 8431 (SFP+) Optical and Direct Attach Copper
- Backplane Reach Extension, Data Retimer
- Ethernet: 10GbE, 1GbE

For other data rates and data transmission protocols, other pin-compatible devices in the retimer family can be used.

3 Description

The DS100DF410 is four channel retimers with integrated signal conditioning. Each channel can independently lock to 10.3125 Gbps data rate to support 10GbE. The device includes a fully adaptive Continuous-Time Linear Equalizer (CTLE), Clock and Data Recovery (CDR) and transmit De-Emphasis (DE) driver. The DS100DF410 also includes a self calibrating 5-tap Decision Feedback Equalizer (DFE) to enable data transmission over long, lossy and crosstalk-impaired highspeed serial links to achieve BER < 1×10^{-15}.

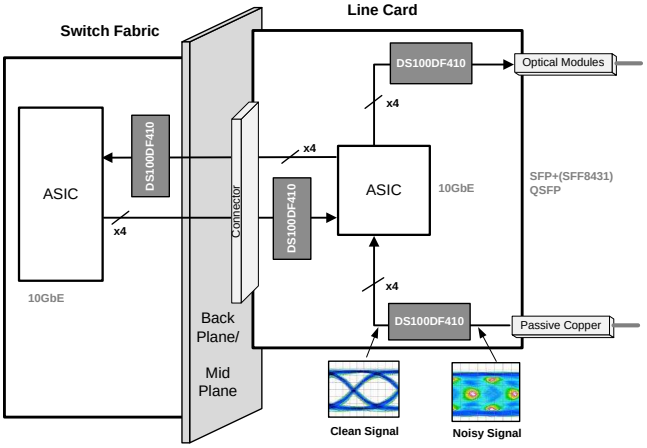
The programmable settings can be applied easily using the SMBus (I2C) interface, or they can be loaded via an external EEPROM. An on-chip eye monitor and a PRBS generator allow real-time measurement of high-speed serial data for system bring-up or field tuning. Flow-through pinout and single power supply make the DS100DF410 easy to use.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DS100DF410SQ	WQFN (48)	7.00 mm × 7.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Diagram



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4 Revision History

Changes from Revision A (February 2013) to Revision B **Page**

- Changed *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

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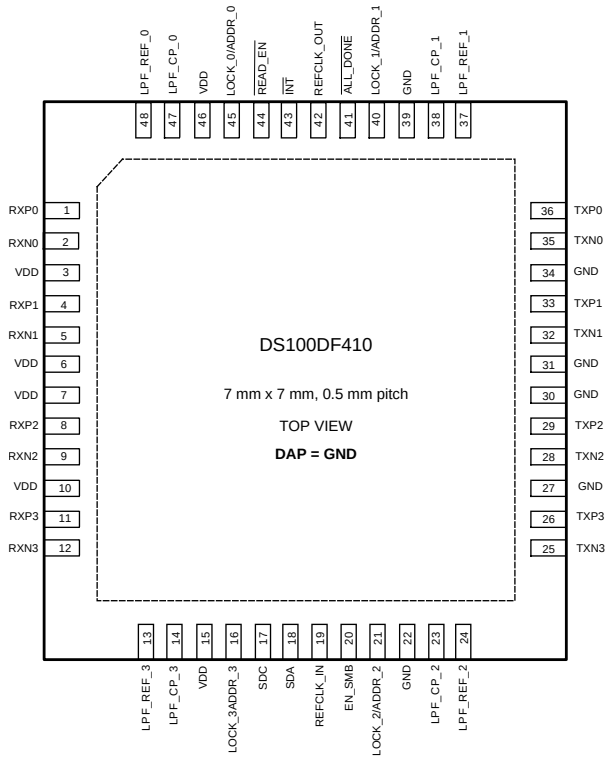
5 Pin Configuration and Functions

RHS Package
48 Pins
Top View



Pin Functions

PIN		TYPE (1)	DESCRIPTION
NAME	NUMBER		
HIGH-SPEED DIFFERENTIAL I/O			
RXP0 RXN0	1 2	I, CML	Inverting and non-inverting CML-compatible differential inputs to the equalizer. Nominal differential input impedance = 100Ω. Must be AC coupled.
RXP1 RXN1	4 5	I, CML	Inverting and non-inverting CML-compatible differential inputs to the equalizer. Nominal differential input impedance = 100Ω. Must be AC coupled.
RXP2 RXN2	8 9	I, CML	Inverting and non-inverting CML-compatible differential inputs to the equalizer. Nominal differential input impedance = 100Ω. Must be AC coupled.
RXP3 RXN3	11 12	I, CML	Inverting and non-inverting CML-compatible differential inputs to the equalizer. Nominal differential input impedance = 100Ω. Must be AC coupled.
TXP0 TXN0	36 35	O, CML	Inverting and non-inverting CML-compatible differential outputs from the driver. Nominal differential output impedance = 100Ω. Must be AC coupled.
TXP1 TXN1	33 32	O, CML	Inverting and non-inverting CML-compatible differential outputs from the driver. Nominal differential output impedance = 100Ω. Must be AC coupled.
TXP2 TXN2	29 28	O, CML	Inverting and non-inverting CML-compatible differential outputs from the driver. Nominal differential output impedance = 100Ω. Must be AC coupled.
TXP3 TXN3	26 25	O, CML	Inverting and non-inverting CML-compatible differential outputs from the driver. Nominal differential output impedance = 100Ω. Must be AC coupled.

(1) **Notes:** I = Input, O = Output and 2.5V LVCMOS pins are 2.5 V levels only.
Only SMBus pins SDA and SDC and $\overline{\text{INT}}$ pin are 3.3 V tolerant. These three pins are open-drain and require external pull-up resistors.

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Pin Functions (continued)

PIN		TYPE[1]	DESCRIPTION
NAME	NUMBER		
LOOP FILTER CONNECTION PINS			
LPF_CP_0 LPF_REF_0	47 48	I/O, analog	Loop filter connection Place a 22 nF ± 10% Capacitor between LPF_CP_0 and LPF_REF_0
LPF_CP_1 LPF_REF_1	38 37	I/O, analog	Loop filter connection Place a 22 nF ± 10% Capacitor between LPF_CP_1 and LPF_REF_1
LPF_CP_2 LPF_REF_2	23 24	I/O, analog	Loop filter connection Place a 22 nF ± 10% Capacitor between LPF_CP_2 and LPF_REF_2
LPF_CP_3 LPF_REF_3	14 13	I/O, analog	Loop filter connection Place a 22 nF ± 10% Capacitor between LPF_CP_3 and LPF_REF_3
REFERENCE CLOCK I/O			
REFCLK_IN	19	I, 2.5V analog	Input is 2.5 V, 25 MHz ± 100 ppm reference clock from external oscillator No stringent phase noise requirement
REFCLK_OUT	42	O, 2.5V analog	Output is 2.5 V, buffered replica of reference clock input for connecting multiple DS100DF410s on a board
LOCK INDICATOR PINS			
LOCK_0 LOCK_1 LOCK_2 LOCK_3	45 40 21 16	O, 2.5V LVCMOS	Output is 2.5 V, the pin is high when CDR lock is attained on the corresponding channel Note that these pins are shared with SMBus address strap input functions read at startup.
SMBus MASTER MODE PINS			
$\overline{\text{ALL_DONE}}$	41	O, 2.5V LVCMOS	Output is 2.5 V, the pin goes low to indicate that the SMBus master EEPROM read has been completed.
$\overline{\text{READ_EN}}$	44	I, 2.5V LVCMOS	Input is 2.5 V, a transition from high to low starts the load from the external EEPROM. The $\overline{\text{READ_EN}}$ pin must be tied low when in SMBus slave mode
INTERRUPT OUTPUT			
$\overline{\text{INT}}$	43	O, 3.3V LVCMOS, Open Drain	Used to signal horizontal or vertical eye opening out of tolerance, loss of signal detect, or CDR unlock External 2KΩ to 5KΩ pull-up resistor is required. Pin is 3.3 V LVCMOS tolerant.
SERIAL MANAGEMENT BUS (SMBus) INTERFACE			
EN_SMB	20	I, 2.5V analog	Input is 2.5 V, selects SMBus master mode or SMBus slave mode EN_SMB = High for slave mode EN_SMB = Float for master mode Tie $\overline{\text{READ_EN}}$ pin low for SMBus slave mode. See Table 1
SDA	18	I/O, 3.3V LVCMOS, Open Drain	Data Input / Open Drain Output External 2KΩ to 5KΩ pull-up resistor is required. Pin is 3.3 V LVCMOS tolerant.
SDC	17	I/O, 3.3V LVCMOS, Open Drain	Clock Input / Open Drain Clock Output External 2KΩ to 5KΩ pull-up resistor is required. Pin is 3.3 V LVCMOS tolerant.
ADDR_0 ADDR_1 ADDR_2 ADDR_3	45 40 21 16	I, 2.5V LVCMOS	Input is 2.5 V, the ADDR_[3:0] pins set the SMBus address for the retimer. These pins are strap inputs. Their state is read on power-up to set the SMBus address in SMBus control mode. High = 1KΩ to VDD, Low = 1KΩ to GND Note that these pins are shared with the lock indicator functions. See Table 2
POWER			
V_{DD}	3, 6, 7, 10, 15, 46	Power	V_{DD} = 2.5 V ± 5%
GND	22, 27, 30, 31, 34, 39	Power	Ground reference.
DAP	PAD	Power	Ground reference. The exposed pad at the center of the package must be connected to ground plane of the board with at least 4 vias to lower the ground impedance and improve the thermal performance of the package.

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6 Specifications

6.1 Absolute Maximum Ratings (1)

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Supply Voltage (V_{DD})	–0.5	2.75	V
2.5 I/O Voltage (LVCMOS and Analog)	–0.5	2.75	V
3.3 LVCMOS I/O Voltage (SDA, SDC, $\overline{INT}$)	–0.5	4.0	V
Signal Input Voltage (RXPn, RXNn)	–0.5	2.75	V
Signal Output Voltage (TXPn, TXNn)	–0.5	2.75	V
Junction Temperature		150	°C
Storage Temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	ESD Rating	Human Body Model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	±6000	V
		Machine Model (MM), STD - JESD22-A115-A (2)	±250	
		Charged Device Model (CDM), per JEDEC specification JESD22-C101, all pins (3)	±1250	

(1) JEDEC document JEP155 states that 6000-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V MM allows safe manufacturing with a standard ESD control process.
(3) JEDEC document JEP157 states that 1250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply Voltage (V_{DD} to GND)	2.375	2.5	2.625	V
Ambient Temperature	-40	25	+85	°C

6.4 Thermal Information (1)

THERMAL METRIC (2)		DS100DF410 WQFN 48 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	26.1	°C/W

(1) No airflow, 4-layer JEDEC, 9 thermal vias
(2) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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6.5 Electrical Characteristics

Over recommended operating supply and temperature ranges with default register settings unless otherwise specified. (1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER						
PD	Power supply consumption	Average Power Consumption (2)		720		mW
		Max Transient Power Supply Current (3)		500	610	mA
NT_{PS}	Supply noise tolerance (4)	50 Hz to 100 Hz		100		mV_{P-P}
		100 Hz to 10 MHz		40		mV_{P-P}
		10 MHz to 5.0 GHz		10		mV_{P-P}
2.5V LVCMOS DC SPECIFICATIONS						
V_{IH}	High level input voltage		1.75		V_{DD}	V
	High level (ADDR[3:0] pins)		2.28		VDD	V
V_{IL}	Low level input voltage		GND		0.7	V
	Low level input voltage (ADDR[3:0] pins)		GND		0.335	V
V_{OH}	High level output voltage	I_{OH} = -3mA	2.0			V
V_{OL}	Low level output voltage	I_{OL} = 3mA			0.4	V
I_{IN}	Input leakage current	$V_{IN} = V_{DD}$			10	µA
		V_{IN} = GND	–10			µA
I_{IH}	Input high current (EN_SMB pin)	$V_{IN} = V_{DD}$		55		µA
I_{IL}	Input low current (EN_SMB pin)	V_{IN} = GND		–110		µA
3.3 V LVCMOS DC SPECIFICATIONS (SDA, SDC, $\overline{INT}$)						
V_{IH}	High level input voltage	V_{DD} = 2.5 V	1.75		3.6	V
V_{IL}	Low level input voltage	V_{DD} = 2.5 V	GND		0.7	V
V_{OL}	Low level output voltage	I_{PULLUP} = 3mA			0.4	V
I_{IH}	Input high current	V_{IN} = 3.6 V, V_{DD} = 2.5 V	20		40	µA
I_{IL}	Input low current	V_{IN} = GND, V_{DD} = 2.5 V	–10		10	µA
f_{SDC}	SMBus clock rate	Slave Mode	10		400	kHz
		Master Mode (5)		400		kHz
DATA BIT RATES						
R_B	Bit rate range	10.3125 Gbps Ethernet	10.1		10.6	Gbps
		1.25 Gbps Ethernet	1.2		1.3	Gbps
SIGNAL DETECT						
SDH	Signal detect ON threshold level	Default differential input signal level to assert signal detect, 10.3125 Gbps, PRBS-31		70		mV_{p-p}
SDL	Signal detect OFF threshold level	Default differential input signal level to de-assert signal detect, 10.3125 Gbps, PRBS-31		10		mV_{p-p}

(1) Typical values represent most likely parametric norms at V_{DD} = 2.5V, T_A = 25°C, and at the Recommended Operation Conditions at the time of product characterization.
(2) V_{DD}= 2.5V, T_A = 25°C. All four channels active and locked. DFE powered-up and enabled.
(3) Maximum power supply current during lock acquisition. All four channels active, all four channels unlocked, all registers at default settings.
(4) Allowed supply noise (mV_{P-P} sine wave) under typical conditions.
(5) EEPROM device used for Master mode programming must support fSDC greater than 400kHz.

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Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges with default register settings unless otherwise specified. (1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RECEIVER INPUTS (RXPn, RXNn)						
$V_{TX2, min}$	Minimum source transmit launch signal level (IN, diff)	See (5)		600		mV_{P-P}
$V_{TX2, max}$				1000		mV_{P-P}
$V_{TX1, max}$		See (6)		1200		mV_{P-P}
$V_{TX0, max}$		See (7)		1600		mV_{P-P}
L_{RI}	Maximum differential input return loss - |SDD11|	100 MHz – 6 GHz (8)		-15		dB
Z_D	Differential input impedance	100 MHz – 6 GHz		100		Ω
Z_S	Single-ended input impedance	100 MHz – 6 GHz		50		Ω
DRIVER OUTPUTS (TXPn, TXNn)						
V_{OD0}	Differential output voltage	Differential measurement with OUT+ and OUT- terminated by 50Ω to GND, AC-Coupled, SMBus register VOD control (Register 0x2d bits 2:0) set to 0, minimum VOD De-emphasis control set to minimum (0 dB)	400		675	mV_{P-P}
V_{OD7}	Differential output voltage	Differential measurement with OUT+ and OUT- terminated by 50Ω to GND, AC-Coupled SMBus register VOD control (Register 0x2d bits 2:0) set to 7, maximum VOD De-emphasis control set to minimum (0 dB)	1000			mV_{P-P}
V_{OD_DE}	De-emphasis level (9)	Differential measurement with OUT+ and OUT- terminated by 50Ω to GND, AC-Coupled Set by SMBus register control to maximum de-emphasis setting Relative to the nominal 0 dB de-emphasis level set at the minimum de-emphasis setting		-12		dB
t_R, t_F	Transition time (rise and fall times) (9) (10)	Transition time control = Full Slew Rate		39		ps
		Transition time control = Limited Slew Rate		50		ps
L_{RO}	Maximum differential output return loss - |SDD22|	100 MHz – 6 GHz (8)		–15		dB
t_{DP}	Propagation delay	Retimed data (11)		300		ps
T_{DE}	De-emphasis pulse duration (12)	Measured at V_{OD} = 1000 mV_{P-P}, de-emphasis setting = -12 dB		75		ps

(6) Differential signal amplitude at the transmitter output providing < $1x10^{-12}$ bit error rate. Measured at 10.3125 Gbps with a PRBS-31 data pattern. Input transmission channel is 40-inch long FR-4 stripline, 4-mil trace width.
(7) Differential signal amplitude at the transmitter output providing < $1x10^{-12}$ bit error rate. Measured at 10.3125 Gbps with a PRBS-31 data pattern. No input transmission channel.
(8) Measured with 10 MHz clock pattern output.
(9) Measured with clock-like {11111 00000} pattern.
(10) Slew rate is controlled by SMBus register settings.
(11) Typical at 10.3125 Gbps bit rate.
(12) De-emphasis pulse width varies with V_{OD} and de-emphasis settings.

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Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges with default register settings unless otherwise specified. (1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TJ	Output total jitter	Measured at BER = 10^{-12} (13)		10		ps
T_{SKEW}	Intra pair skew	Difference in 50% crossing between TXPn and TXNn for any output		3		ps
	Channel-to-channel skew			7		ps
CLOCK AND DATA RECOVERY						
BW_{PLL}	PLL Bandwidth, -3 dB	Measured at 10.3125 Gbps		5		MHz
J_{TOL}	Input sinusoidal jitter tolerance 10 kHz to 250 MHz sinusoidal jitter frequency	Measured at BER = 10^{-15}		0.6		UI
J_{TRANS}	Jitter transfer sinusoidal jitter at 10 MHz jitter frequency	Measured at BER = 10^{-15}		-6		dB
T_{LOCK}	CDR Lock Time	Measured at 10.3125 Gbps		15		ms
RECOMMENDED REFERENCE CLOCK SPECS						
REF_f	Input reference clock frequency		24.9975	25	25.0025	MHz
$REFCLK_IN_{PW}$	Minimum REFCLK_IN Pulse Width	At REFCLK_IN pin		4		ns
$REFCLK_OUT_{DCD}$	REFCLK_OUT duty cycle distortion	C_L = 5 pF		0.55		ns
REF_{VIH}	Reference clock input min high threshold			1.75		V
REF_{VIL}	Reference clock input max low threshold			0.7		V

(13) Typical with no output de-emphasis, minimum output transmission channel.

6.6 Typical Characteristics

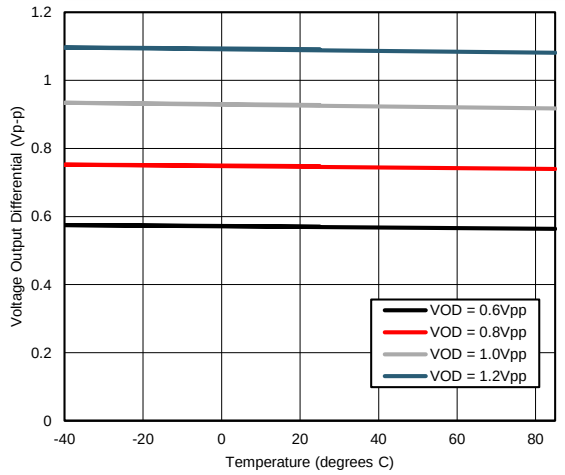

Figure 1. Typical VOD vs VDD

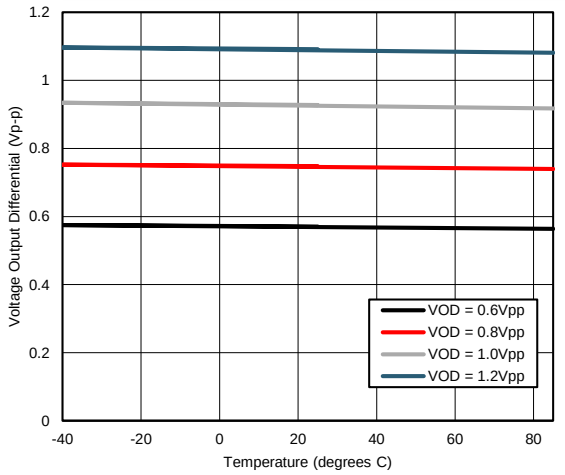

Figure 2. Typical VOD vs Temperature

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7 Detailed Description

7.1 Overview

The DS100DF410 is a low-power 10GbE 4-channel retimer. Each channel in the DS100DF410 operates independently. All channels include a Continuous Time Linear Equalizer (CTLE), Decision Feedback Equalizer (DFE), Clock and Data Recovery circuit (CDR) and a differential driver with programmable output voltage and de-emphasis. Each channel also has its own Eye Opening Monitor (EOM) and configurable Pseudo-Random Bit Sequence (PRBS) pattern generator that can be used for debug purposes.

The DS100DF410 is configurable through a single SMBus port. The DS100DF410 can also act as an SMBus master to configure itself from an EEPROM.

The sections below describe the functionality of the various circuits and features within the DS100DF410.

7.2 Functional Block Diagram

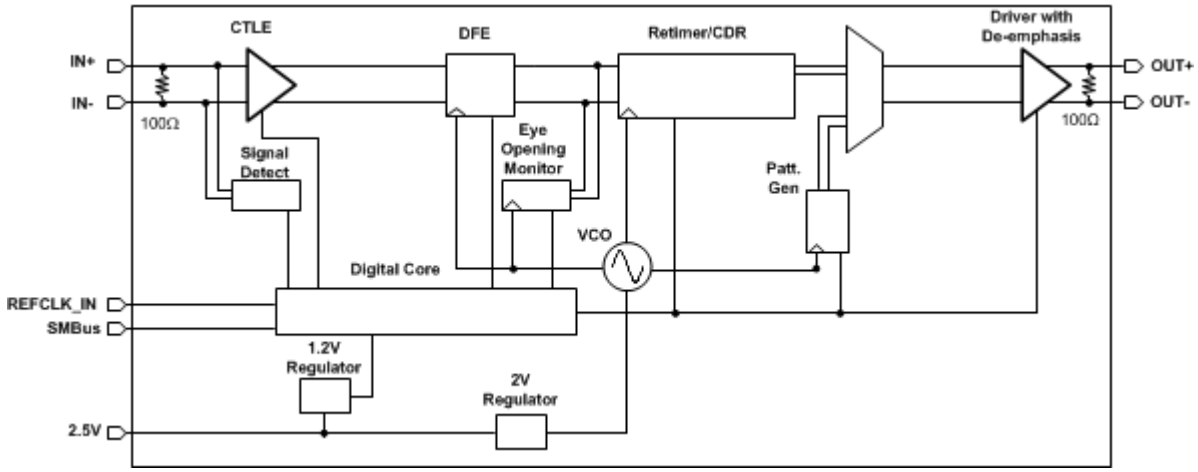

Figure 3. DS100DF410 Data Path Block Diagram: One of Four Channels

7.3 Feature Description

7.3.1 Device Data Path Operation

The data path operation of the DS100DF410 comprises the functional sections as shown in the data path block diagram of Figure 3. The functional sections are as follows.

- Signal Detect
- CTLE
- DFE
- CDR
- Differential Output Driver

7.3.2 Signal Detect

The signal detect circuit monitors the energy level on the receiver inputs and powers on or off the rest of the high speed data path if a signal is detected or not. By default, each channel allows the signal detect circuit to automatically power on or off the rest of the high speed data path depending on if a signal is present. The signal detect block can be manually controlled in the SMBus channel registers. This can be useful if it is desired manually force channels to be disabled.

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Feature Description (continued)

7.3.3 CTLE

The CTLE in the DS125DF410 is a fully adaptive equalizer with optional limiting stage. The CTLE adapts according to a Figure of Merit (FOM) calculation during the lock acquisition process. Once the CDR has locked and the CTLE has been adapted, the CTLE boost level will be frozen until a manual re-adapt command is issued or until the CDR re-enters the lock acquisition state. The CTLE is typically readapted by resetting the CDR. The CTLE consists of 4 stages, with each stage having 2-bit boost control. This allows for 256 different stage-boost combinations. The CTLE adaption algorithm allows the CTLE to adapt through 32 of these stage-boost combinations. These 32 stage-boost combinations comprise the EQ Table in the channel registers; see channel registers 0x40 through 0x5F. This EQ Table can be reprogrammed to support up to 32 of the 256 stage-boost settings.

CTLE boost levels are determined by summing the boosts levels of the 4 stages. Different stage-boost combinations that sum to the same number will have approximately the same boost level, but will result in a different shape for the EQ transfer function (boost curve).

The fourth stage in the CTLE can be programmed through the SMBus interface to become a limiting stage rather than a linear stage. This is useful in some applications, but it should not be typically used in combination with the DFE.

7.3.4 DFE

A 5-tap DFE can be enabled within the data path of each channel to assist with reducing the effects of cross talk, reflections, or post cursor inter-symbol interference (ISI). The DFE must be manually enabled, regardless of the selected adapt mode. The DFE can be manually configured to specified tap polarities and tap weights.

The DFE taps are all feedback taps with 1UI spacing. Each tap has a specified boost weight range and polarity bit.

7.3.5 Clock and Data Recovery

The DS100DF410 performs its clock and data recovery function by detecting the bit transitions in the incoming data stream and locking its internal VCO to the clock represented by the mean arrival times of these bit transitions. This process produces a recovered clock with jitter which is greatly reduced for jitter frequencies outside the bandwidth of the CDR Phase-Locked Loop (PLL). This is the primary benefit of using the DS100DF410 in a system. It significantly reduces the jitter present in the data stream, in effect resetting the jitter budget for the system.

7.3.6 Output Driver

The output driver is capable of driving variable output voltages with variable amounts of analog de-emphasis. The output voltage and de-emphasis level can be configured by writing registers over the SMBus. The DS100DF410 cannot determine independently the appropriate output voltage or de-emphasis setting, so the user is responsible for configuring these parameters. They can be set for each channel independently.

An idealized transmit waveform with analog de-emphasis applied is shown in Figure 4.

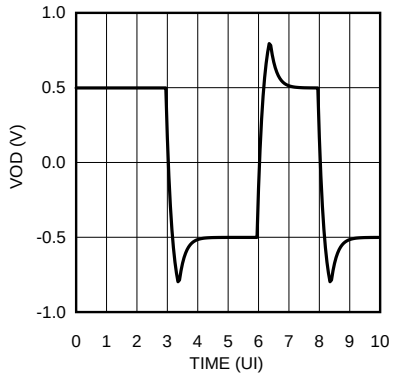

Figure 4. Idealized De-Emphasis Waveform

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Feature Description (continued)

7.3.7 CTLE Boost Setting

The CTLE is a four-stage amplifier with an adjustable, quasi-high-pass transfer function on each stage. The overall frequency response of the CTLE is set by adjusting the boost of each stage independently. Each stage of the CTLE can be set to one of four boost settings. The amount of high-frequency boost supplied by each stage generally increases with increasing boost settings.

The CTLE can also be configured to adapt automatically to provide the optimum boost level for its input signal. Automatic adaptation of the CTLE only is the default mode of operation for the DS100DF410.

7.3.8 DFE Tap Weight and Polarity Setting

The DS100DF410 includes a five-tap decision-feedback equalizer (DFE) which operates on the signal at the output of the CTLE.

When the tap weights and polarities are properly set, the DFE approximates a matched filter for the input transmission channel frequency response as modified by the CTLE frequency response. The CTLE and the DFE work together to compensate for the input transmission channel response.

The DFE discriminates against input noise and random jitter as well as against crosstalk at the input to the DS100DF410. When the DFE tap weights and polarities are properly set the DS100DF410 CDR operates at an acceptable BER with more severe channel impairments than can be compensated with the CTLE alone.

It is possible to automatically or manually set the tap weights and polarities in the DS100DF410. Determining the correct tap weights manually is difficult and time-consuming. The DS100DF410 automatically adapts the DFE tap weights and polarities in normal operation. This automatic adaptation provides superior BER performance for noisy channels and channels subject to crosstalk aggressors.

The DFE is powered down by default. In order for the DFE tap weights and polarities to be applied to the input signal, bit 3 of register 0x1e, the dfe_PD bit, should be set to 0 to power up the DFE. Also the adapt mode setting in register 0x31, bits[6:5] should be set to 2b'10 or 2b'11 so the device can automatically adapt the CTLE and DFE.

7.3.9 Driver Output Voltage

The differential output voltage of the DS100DF410 can be configured from a nominal setting of 600 mV peak-to-peak differential to a nominal setting of 1.3 V peak-to-peak differential, depending upon the application. The driver output voltage as set is the typical peak-to-peak differential output voltage with no de-emphasis enabled.

7.3.10 Driver Output De-Emphasis

The output de-emphasis level of the DS100DF410 can be configured from a nominal setting of 0 dB to a nominal setting of -12 dB depending upon the application. Larger absolute values of the de-emphasis setting provide more pre-distortion of the output driver waveform, accentuating the high-frequency components of the output driver waveform relative to the low-frequency components. Greater values of de-emphasis can compensate for greater dispersion in the transmission media at the output of the DS100DF410. The output de-emphasis level as set is the typical value to which the output signal will settle following the de-emphasis pulse interval in dB relative to the output VOD.

7.3.11 Driver Output Rise/Fall Time

In some applications, a longer rise/fall time for the output signal is desired. This can reduce electromagnetic interference (EMI) generated by fast switching waveforms. This is necessary in some applications for regulatory compliance. In others, it can reduce the crosstalk in the system.

The DS100DF410 can be configured to operate with a nominal rise/fall time corresponding to the maximum slew rate of the output drivers into the load capacitance. Alternatively, the DS100DF410 can be configured to operate with a slightly greater rise/fall time if desired. For the typical specifications on rise/fall time, see *Electrical Characteristics*.

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Feature Description (continued)

7.3.12 Ref_mode 0 Mode (Reference Clock Not Required)

The DS100DF410 can be used without using a reference clock and the input REFCLK_IN pin can be open. When register 0x36, bits [5:4] are set to 2'b00, the device operates without using a reference clock at 10.3125 Gbps mode.

For 1GbE applications, it is required to bypass the CDR by setting the override bit 5 of register 0x09 to 1, and set the data mux bits [7:5] to 3'b000 of register 0x1E.

7.3.13 Ref_mode 3 Mode (Reference Clock Required)

When using ref_mode 3, the device uses an external 25 MHz clock. This mode of operation is set in register 0x36 bits [5:4] = 2'b11 and is the default setting. In ref_mode 3, the external reference clock is used to aid initial phase lock, and to determine when its VCO is properly phase-locked. An external oscillator should be used to generate a 2.5V, 25 MHz reference signal which is connected to the DS100DF410 on the reference clock input pin (pin 19). The DS100DF410 does not include a crystal oscillator circuit, so a stand-alone external oscillator is required.

The reference clock speeds up the initial phase lock acquisition. The DS100DF410 is set to phase lock to a known data rate, or a constrained set of known data rates, and the digital circuitry in the DS100DF410 pre-configures the VCO frequency. This enables the DS100DF410 phase-lock to the incoming signal very quickly.

The reference clock is used to calibrate the VCO coarse tuning. However, the reference clock is not synchronous to the data stream, and the quality of the reference clock does not affect the jitter on the output retimed data. The retimed data clock for each channel is synchronous to the VCO internal to that channel of the DS100DF410.

The phase noise of the reference clock is not critical. Any commercially-available 25 MHz oscillator can provide an acceptable reference clock. The reference clock can be daisy-chained from one retimer to another so that only one reference oscillator is required in a system.

7.3.14 False Lock Detector Setting

The register 0x2F, bit 1 is set to 1 by default, which disables the false lock detector. This bit must be set to 0 to enable the false lock detector function.

7.3.15 Reference Clock In

REFCLK_IN pin 19 is for reference clock input. A 25 MHz oscillator should be connected to pin 19. See *Electrical Characteristics* for the requirements on the 25 MHz clock. The frequency of the reference clock should always be 25 MHz no matter what data rate or mode of operation is used.

7.3.16 Reference Clock Out

REFCLK_OUT pin 42 is the reference clock output pin. The DS100DF410 drives a buffered replica of the 25 MHz reference clock input on this output pin. If there are multiple DS100DF410 in the system, the REFCLK_OUT pin can be directly connected to the REFCLK_IN pin of another DS100DF410 in a daisy chain connection. The other option is to connect the external 25 MHz oscillator to a clock fanout buffer to distribute the 25 MHz clock to each DS100DF410, which ensures there is a reference clock for the DS100DF410.

7.3.17 Daisy Chain of REFCLK_OUT to REFCLK_IN

When daisy chaining the device REFCLK_OUT to the REFCLK_IN of another device, the trace connection should be less than 1.5 inches (about 5pF trace capacitance) and it is possible to cascade up to 9 devices. While in other systems with longer interconnecting trace or more capacitive loading, the daisy chain of multiple devices should be reduced. In a system which requires longer daisy chain, it is recommended to place an inverted gate after the 6th devices. The pre-distorted duty cycle from the inverter allows longer daisy chain. A better approach is to break the long daisy chain into shorter chains, each driven by a buffer version of the clock distribution and with each chain kept to a maximum of 6 cascade devices. As an example, if there are 12 devices in the system, the daisy chain connections can be divided into two groups of 6 devices and PCB trace length for the reference clock output to input connection. Should be 1.5 inch or less.

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Feature Description (continued)

7.3.18 $\overline{\text{INT}}$

The $\overline{\text{INT}}$ line is an open-drain, 3.3V tolerant, LVCMOS active-low output. The $\overline{\text{INT}}$ lines from multiple DS100DF410s can be wired together and connected to an external controller.

The DS100DF410 generates an interrupt when it detects a loss of signal after previously detecting the presence of a signal, or when it detects loss of lock after previously detecting phase lock. These interrupts are always enabled. In addition, the Horizontal Eye Opening/Vertical Eye Opening (HEO/VEO) interrupt can be enabled using SMBus control for each channel independently. This interrupt is disabled by default. The thresholds for horizontal and vertical eye opening that will trigger the interrupt can be set using the SMBus control for each channel.

If any interrupt occurs, registers in the DS100DF410 latch in information about the event that caused the interrupt. This can then be read out by the controller over the SMBus.

7.3.19 LOCK_3, LOCK_2, LOCK_1, and LOCK_0

Each channel of the DS100DF410 has an independent lock indication pin. These lock indication pins, LOCK_3, LOCK_2, LOCK_1, and LOCK_0, are pin 16, pin 21, pin 40, and pin 45 respectively. These pins are shared with the SMBus address strap lines. After the address values have been latched in on power-up, these lines revert to their lock indication function.

When the corresponding channel of the DS100DF410 is locked to the incoming data stream, the lock indication pin goes high. This pin can be used to drive an LED on the board, giving a visual indication of the lock status, or it can be connected to other circuitry which can interpret the lock status of the channel.

7.4 Device Functional Modes

The DS100DF410 can be configured using two different methods.

- SMBus Master Configuration Mode
- SMBus Slave Configuration Mode

The configuration mode is selected by the state of the EN_SMB pin (pin 20) when the DS100DF410 is powered-up. This pin should be either left floating or tied to the device V_{DD} through an optional 1kΩ resistor. The effect of each of these settings is shown in Table 1.

Table 1. SMBus Enable Settings

EN_SMB PIN SETTING	CONFIGURATION MODE	DESCRIPTION	$\overline{\text{READ_EN}}$ PIN
Float	SMBus Master Mode	Device reads its configuration from an external EEPROM on power-up	Pull low to initiate reading configuration data from external EEPROM
High (1)	SMBus Slave Mode	Device is configured over the SMBus by an external controller	Tie low to enable proper address strapping on power-up

7.4.1 SMBus Master Mode and SMBus Slave Mode

In SMBus master mode the DS100DF410 reads its initial configuration from an external EEPROM upon power-up. A description of the operation of this mode appears in a separate application note.

Some of the pins of the DS100DF410 perform the same functions in SMBus master and SMBus slave mode. Once the DS100DF410 has finished reading its initial configuration from the external EEPROM in SMBus master mode it reverts to SMBus slave mode and can be further configured by an external controller over the SMBus. Two device pins initiate reading the configuration from the external EEPROM and indicate when the configuration read is complete.

- $\overline{\text{ALL_DONE}}$
- $\overline{\text{READ_EN}}$

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These pins are meant to work together. When the DS100DF410 is powered up in SMBus master mode, it reads its configuration from the external EEPROM. This is triggered when the READ_EN pin goes low. When the DS100DF410 is finished reading its configuration from the external EEPROM, it drives its ALL_DONE pin low. In this mode, as the name suggests, the DS100DF410 acts as an SMBus master during the time it is reading its configuration from the external EEPROM. After the DS100DF410 has finished reading its configuration from the EEPROM, it releases control of the SMBus and becomes a SMBus slave. In applications where there is more than one DS100DF410 on the same SMBus, bus contention can result if more than one DS100DF410 tries to take command of the SMBus as the SMBus master at the same time. The READ_EN and ALL_DONE pins prevent this bus contention.

In a system where the DS100DF410s are meant to operate in SMBus master mode, the READ_EN pin of one retimer should be wired to the ALL_DONE pin of the next. The system should be designed so that the READ_EN pin of one (and only one) of the DS100DF410s in the system is driven low on power-up. This DS100DF410 will take command of the SMBus on power-up and will read its initial configuration from the external EEPROM. When it is finished reading its configuration, it will set its ALL_DONE pin low. This pin should be connected to the READ_EN pin of another DS100DF410. When this DS100DF410 senses its READ_EN pin driven low, it will take command of the SMBus and read its initial configuration from the external EEPROM, after which it will set its ALL_DONE pin low. By connecting the ALL_DONE pin of each DS100DF410 to the READ_EN pin of the next DS100DF410, each DS100DF410 can read its initial configuration from the EEPROM without causing bus contention.

For SMBus slave mode, the READ_EN pin **must be tied low**. Do not leave it floating or tie it high.

A connection diagram showing several DS100DF410s along with an external EEPROM and an external SMBus master is shown in Figure 5. The SMBus master must be prevented from trying to take control of the SMBus until the DS100DF410s have finished reading their initial configurations from the EEPROM.

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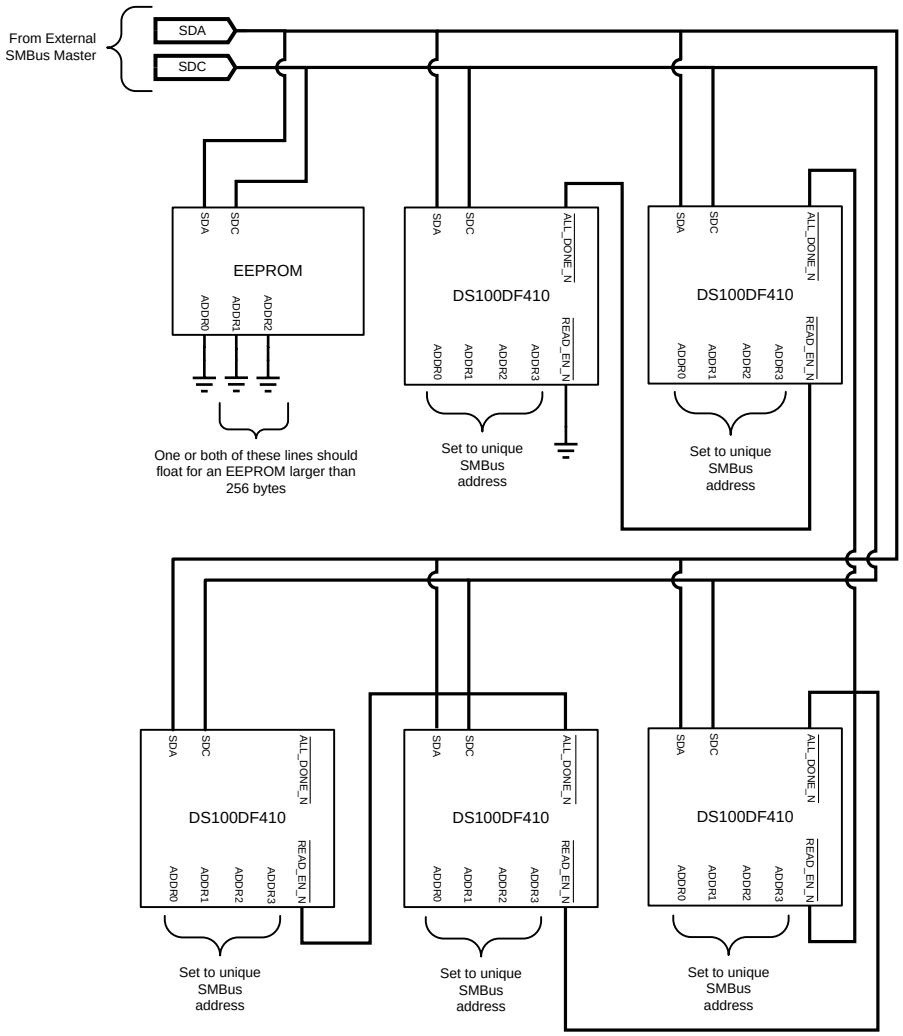

Figure 5. Connection Diagram for Multiple DS100DF410s in SMBus Master Mode

In SMBus master mode after the DS100DF410 has finished reading its initial configuration from the external EEPROM it reverts to SMBus slave mode. In either mode the SMBus data and clock lines, SDA and SDC, are used. Also, in either mode, the SMBus address is latched in on the address strap lines on power-up. In SMBus slave mode, if the $\overline{\text{READ_EN}}$ pin is not tied low, the DS100DF410 will not latch in the address on its address strap lines. It will instead latch in an SMBus write address of 0x30 regardless of the state of the address strap lines. This is a test feature. Obviously a system with multiple retimers cannot operate properly if all the retimers are responding to the same SMBus address. Tie the $\overline{\text{READ_EN}}$ pin low when operating in SMBus slave mode to avoid this condition.

The DS100DF410 reads its SMBus address upon power-up from the SMBus address lines.

7.4.2 Address Lines <ADDR_[3:0]>

In either SMBus master or SMBus slave mode the DS100DF410 must be assigned an SMBus address. A unique address must be assigned to each device on the SMBus.

The SMBus address is latched into the DS100DF410 on power-up. The address is read in from the state of the <ADDR_[3:0]> lines (pins 16, 21, 40, and 45 respectively) upon power-up. In either SMBus mode these address lines are input pins on power-up.

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The DS100DF410 can be configured with any of 16 SMBus addresses. The SMBus addressing scheme uses the least-significant bit of the SMBus address as the Read/Write_N address bit. When an SMBus device is addressed for writing, this bit is set to 0; for reading, to 1. Table 2 shows the write address setting for the DS100DF410 versus the values latched in on the address lines at power-up.

The address byte sent by the SMBus master over the SMBus is always 8 bits long. The least-significant bit indicates whether the address is for a write operation, in which the master will output data to the SMBus to be read by the slave, or a read operation, in which the slave will output data to the SMBus to be read by the master. if the least-significant bit is a 0, the address is for a write operation. If it is a 1, the address is for a read operation. Accordingly, SMBus addresses are sometimes referred to as seven-bit addresses. To produce the write address for the SMBus, the seven-bit address is left-shifted by one bit. To produce the read address, it is left shifted by one bit and the least-significant bit is set to 1. Table 2 shows the seven-bit addresses corresponding to each set of address line values.

When the DS100DF410 is used in SMBus slave mode, the $\overline{\text{READ_EN}}$ pin must be tied low. If it is tied high or floating, the DS100DF410 will not latch in its address from the address lines on power-up. When the $\overline{\text{READ_EN}}$ pin is tied high in SMBus slave mode *i.e.* when the EN_SMB pin (pin 20) is tied high, the DS100DF410 will revert to an SMBus write address of 0x30. This is a test feature. If there are multiple DS100DF410s on the same SMBus, they will all revert to an SMBus write address of 0x30, which can cause SMBus collisions and failure to access the DS100DF410s over the SMBus.

Table 2. DS100DF410 SMBus Write Address Assignment

ADDR_3	ADDR_2	ADDR_1	ADDR_0	SMBus WRITE ADDRESS	SEVEN-BIT SMBus ADDRESS
0	0	0	0	0x30	0x18
0	0	0	1	0x32	0x19
0	0	1	0	0x34	0x1a
0	0	1	1	0x36	0x1b
0	1	0	0	0x38	0x1c
0	1	0	1	0x3a	0x1d
0	1	1	0	0x3c	0x1e
0	1	1	1	0x3e	0x1f
1	0	0	0	0x40	0x20
1	0	0	1	0x42	0x21
1	0	1	0	0x44	0x22
1	0	1	1	0x46	0x23
1	1	0	0	0x48	0x24
1	1	0	1	0x4a	0x25
1	1	1	0	0x4c	0x26
1	1	1	1	0x4e	0x27

Once the DS100DF410 has latched in its SMBus address, its registers can be read and written using the two pins of the SMBus interface, Serial Data (SDA) and Serial Data Clock (SDC).

7.4.3 SDA and SDC

In both SMBus master and SMBus slave mode, the DS100DF410 is configured using the SMBus. The SMBus consists of two lines, the SDA or Serial Data line (pin 18) and the SDC or Serial Data Clock line (pin 17). In the DS100DF410 these pins are 3.3V tolerant. The SDA and SDC lines are both open-drain. They require a pull-up resistor to a supply voltage, which may be either 2.5V or 3.3V. A pull-up resistor in the 2KΩ to 5KΩ range will provide reliable SMBus operation.

The SMBus is a standard communications bus for configuring simple systems. For a specification of the SMBus an description of its operation, see http://smbus.org/specs/.

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7.5 Programming

7.5.1 SMBus Strap Observation

Register 0x00, bits 7:4 and register 0x06, bits 3:0

In order to communicate with the DS100DF410 over the SMBus, it is necessary for the SMBus controller to know the address of the DS100DF410 . The address strap observation bits in control/shared register 0x00 are primarily useful as a test of SMBus operation. There is no way to get the DS100DF410 to tell you what its SMBus address is unless you already know what it is.

In order to use the address strap observation bits of control/shared register 0x00, it is necessary first to set the diagnostic test control bits of control/shared register 0x06. This four-bit field should be written with a value of 0xa. When this value is written to bits 3:0 of control/shared register 0x06, then the value of the SMBus address straps can be read in register 0x00, bits 7:4. The value read will be the same as the value present on the ADDR3:ADDR0 lines when the DS100DF410 was powered up. For example, if a value of 0x1 is read from control/shared register 0x00, bits 7:4, then at power-up the ADDR0 line was set to 1 and the other address lines, ADDR3:ADDR1, were all set to 0. The DS100DF410 is set to an SMBus Write address of 0x32.

7.5.2 Device Revision and Device ID

Register 0x01

Control/shared register 0x01 contains the device revision and device ID. The device revision shown in Table 12 is the current revision for the DS100DF410. The device ID will be different for the different devices in the retimer family. The value shown in "For the DS100DF410, Register 0x01, bits 4:0 = 0x10" is the correct value for the DS100DF410. This register is useful because it can be interrogated by software to determine the device variant and revision installed in a particular system. The software might then configure the device with appropriate settings depending upon the device variant and revision.

7.5.3 Control/Shared Register Reset

Register 0x04, bit 6

Register 0x04, bit 6, clears all the control/shared registers back to their factory defaults. This bit is self-clearing, so it is cleared after it is written and the control/shared registers are reset to their factory default values.

7.5.4 Interrupt Channel Flag Bits

Register 0x05, bits 3:0

The operation of these bits is described in the section on interrupt handling later in this data sheet.

7.5.5 SMBus Master Mode Control Bits

Register 0x04, bits 5 and 4 and register 0x05, bits 7 and 4

Register 0x04, bit 5, can be used to reset the SMBus master mode. This bit should not be set if the DS100DF410 is in SMBus slave mode. This is an undefined condition.

When this bit is set, if the EN_SMB pin is floating (meaning that the DS100DF410 is in SMBus master mode), then the DS100DF410 will read the contents of the external EEPROM when the READ_EN pin is pulled low. This bit is not self-clearing, so it should be cleared after it is set.

When the DS100DF410 EN_SMB pin is floating (meaning that the DS100DF410 is in SMBus master mode), it will read from its external EEPROM when its READ_EN pin goes low. After the EEPROM read operation is complete, register 0x05, bit 4 will be set. Alternatively, the DS100DF410 will read from its external EEPROM when triggered by register 0x04, bit 4, as described below.

When register 0x04, bit 4, is set, the DS100DF410 reads its configuration from an external EEPROM over the SMBus immediately. When this bit is set, the DS100DF410 does not wait until the READ_EN pin is pulled low to read from the EEPROM. This EEPROM read occurs whether the DS100DF410 is in SMBus master mode or not. If the read from the EEPROM is not successful, for example because there is no EEPROM present, then the DS100DF410 may hang up and a power-up reset may be necessary to return it to proper operation. You should only set this bit if you know that the EEPROM is present and properly configured.

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If the EEPROM read has already completed, then setting register 0x04, bit 4, will not have any effect. To cause the DS100DF410 to read from the EEPROM again it is necessary to set bit 5 of register 0x04, resetting the SMBus master mode. If the DS100DF410 is not in SMBus master mode, do not set this bit. After setting this bit, it should be cleared before further SMBus operations.

After SMBus master mode has been reset, the EEPROM read may be initiated either by pulling the $\overline{\text{READ_EN}}$ pin low or by then setting register 0x04, bit 4.

Register 0x05, bit 7, disables SMBus master mode. This prevents the DS100DF410 from trying to take command of the SMBus to read from the external EEPROM. Obviously this bit will have no effect if the EEPROM read has already taken place. It also has no effect if an EEPROM read is currently in progress. The only situations in which disabling EEPROM master mode read is valid are (1) when the DS100DF410 is in SMBus master mode, but the $\overline{\text{READ_EN}}$ pin has not yet gone low, and (2) when register 0x04, bit 5, has been used to reset SMBus master mode but the EEPROM read operation has not yet occurred.

Do not set this bit and bit 4 of register 0x04 simultaneously. This is an undefined condition and can cause the DS100DF410 to hang up.

7.5.6 Resetting Individual Channels of the Retimer

Register 0x00, bit 2, and register 0x0a, bits 3:2

Bit 2 of channel register 0x00 are used to reset all the registers for the corresponding channel to their factory default settings. This bit is self-clearing. Writing this bit will clear any register changes you have made in the DS100DF410 since it was powered-up.

To reset just the CDR state machine without resetting the register values, which will re-initiate the lock and adaptation sequence for a particular channel, use channel register 0x0a. Set bit 3 of this register to enable the reset override, then set bit 2 to force the CDR state machine into reset. These bits can be set in the same operation. When bit 2 is subsequently cleared, the CDR state machine will resume normal operation. If a signal is present at the input to the selected channel, the DS100DF410 will attempt to lock to it and will adapt its CTLE and its DFE according to the currently configured adapt mode for the selected channel. The adapt mode is configured by channel register 0x31, bits 6:5.

7.5.7 Interrupt Status

Control/Shared Register 0x05, bits 3:0, Register 0x01, bits 4 and 0, Register 0x30, bit 4, Register 0x32, and Register 0x36, bit 6

Each channel of the DS100DF410 will generate an interrupt under several different conditions. The DS100DF410 will always generate an interrupt when it loses CDR lock or when a signal is no longer detected at its input. If the HEO/VEO interrupt is enabled by setting bit 6 of register 0x36, then the retimer will generate an interrupt when the horizontal or vertical eye opening falls below the preset values even if the retimer remains locked. When one of these interrupt conditions occurs, the retimer alerts the system controller via hardware and provides additional details via register reads over the SMBus.

First, the open-drain interrupt line $\overline{\text{INT}}$ is pulled low. This indicates that one or more of the channels of the retimer has generated an interrupt. The interrupt lines from multiple retimers can be wire-ANDed together so that if any retimer generates an interrupt the system controller can be notified using a single interrupt input.

if the interrupt has occurred because the horizontal or vertical eye opening has dropped below the pre-set threshold, which is set in channel register 0x32, then bit 4 of register 0x30 will go high. This indicates that the source of the interrupt was the HEO or VEO.

If the interrupt has occurred because the CDR has fallen out of lock, or because the signal is no longer detected at the input, then bit 4 and/or bit 0 of register 0x01 will go high, indicating the cause of the interrupt.

In either case, the control/shared register set will indicate which channel caused the interrupt. This is read from bits 3:0 of control/shared register 0x05.

When an interrupt is detected by the controller on the interrupt input, the controller should take the following steps to determine the cause of the interrupt and clear it.

1. The controller detects the interrupt by detecting that the $\overline{\text{INT}}$ line has been pulled low by one of the retimers to which it is connected.

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2. The controller reads control/shared register 0x05 from all the DS100DF410s connected to the $\overline{\text{INT}}$ line. For at least one of these devices, at least one of the bits 3:0 will be set in this register.
3. For each device with a bit set in bits 3:0 of control/shared register 0x05, the controller determines which channel or channels produced an interrupt. Refer to Table 12 for a mapping of the bits in this bit field to the channel producing the interrupt.
4. When the controller detects that one of the retimers has a 1 in one of the four LSBs of this register, the controller selects the channel register set for that channel of that retimer by writing to the channel select register, 0xff, as previously described.
5. For each channel that generated an interrupt, the controller reads channel register 0x01. If bit 4 of this register is set, then the interrupt was caused by a loss of CDR lock. If bit 0 is set, then the interrupt was caused by a loss of signal. it is possible that both bits 0 and 4 could be set. Reading this register will clear these bits.
6. Optionally, for each channel that generated an interrupt, the controller reads channel register 0x30. If bit 4 of this register is set, then the interrupt was caused by HEO and/or VEO falling out of the configured range. This interrupt will only occur if bit 6 of channel register 0x36 is set, enabling the HEO/VEO interrupt. Reading register 0x30 will clear this interrupt bit.
7. Once the controller has determined what condition caused the interrupt, the controller can then take the appropriate action. For example, the controller might reset the CDR to cause the retimer to re-adapt to the incoming signal. If there is no longer an incoming signal (indicated by a loss of signal interrupt, bit 0 of channel register 0x01), then the controller might alert an operator or change the channel configuration. This is system dependent.
8. Reading the interrupt status registers will clear the interrupt. if this does not cause the interrupt input to go high, then another device on the same input has generated an interrupt. The controller can address the next device using the procedure above.
9. Once all the interrupt registers for all channels for all DS100DF410s that generated interrupts have been read, clearing all the interrupt indications, the $\overline{\text{INT}}$ line should go high again. This indicates that all the existing interrupt conditions have been serviced.

The channel registers referred to above, registers 0x01, 0x30, 0x32, and 0x36, are described in the channel registers table, Table 14.

7.5.8 Overriding the CTLE Boost Setting

Register 0x03, Register 0x13, bit 2, and Register 0x3a

To override the CTLE boost settings, register 0x03 is used. This register contains the currently-applied CTLE boost settings. The boost values can be overridden by using the two-bit fields in this register as shown in the table.

The final stage of the CTLE has an additional control bit which sets it to a limiting mode. For some channels, this additional setting improves the bit error rate performance. This bit is bit 2 of register 0x13.

If the DS100DF410 loses lock because of a change in the CTLE settings, the DS100DF410 will initiate its lock and adaptation sequence again. Thus, if you write new CTLE boost values to register 0x03 and 0x13 which cause the DS100DF410 to drop out of lock, the DS100DF410 may, in the process of reacquiring the CDR lock, reset the CTLE settings to different values than those you set in register 0x03 and 0x13. If this behavior is not understood, it can appear that the DS100DF410 did not accept the values you wrote to the CTLE boost registers. What's really happening, however, is that the lock and adaptation sequence is overriding the CTLE values you wrote to the CTLE boost registers. This will not happen unless the DS100DF410 drops out of lock.

If the adapt mode is set to 0 (bits 6:5 of channel register 0x31), then the CTLE boost values will not be overridden, but the DS100DF410 may still lose lock. If this happens, the DS100DF410 will attempt to reacquire lock. if the reference mode is set correctly, and if the rate/subrate code is set to permit it, the DS100DF410 will begin searching for CDR lock at the highest allowable VCO divider ratio – that is, at the lowest configured bit rate. At this lowest bit rate, the CTLE boost settings used will come not from the values in register 0x03, and

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0x13, but rather from register 0x3a, the fixed CTLE boost setting for lower data rates. This setting will be written into boost setting register 0x03 during the lock search process. This value may be different from the value you set in register 0x03, so, again, it may appear that the DS100DF410 has not accepted the CTLE boost settings you set in registers 0x03 and 0x13. The interactions of the lock and adaptation sequences with the manually-set CTLE boost settings can be difficult to understand.

To manually override the CTLE boost under all conditions, perform the following steps.

1. Set the DS100DF410 channel adapt mode to 0 by writing 0x0 to bits 6:5 of channel register 0x31.
2. Set the desired CTLE boost setting in register 0x3a. If the DS100DF410 loses lock and attempts to lock to a lower data rate, it will use this CTLE boost setting.
3. Set the desired CTLE boost setting in register 0x03. This may cause the DS100DF410 to lose lock.
4. If desired, set the CTLE stage 3 limiting bit, bit 2 of register 0x13.

If the DS100DF410 loses lock when the CTLE boost settings are set according to the sequence above, the DS100DF410 will try to reacquire lock, but it will not change the CTLE boost settings in order to do so.

7.5.9 Overriding the VCO CAP DAC Values

Register 0x08, bits 4:0, Register 0x09, bit 7, Register 0x0b, bits 4:0, Register 0x36, bits 5:4, and Register 0x2f, bits 7:6 and 5:4

Registers 0x08 and 0x0b contain CAP DAC override values. Normally, when bits 5:4 of register 0x36 are set to 2'b11, then the DS100DF410 performs an initial search to determine the correct CAP DAC setting (coarse VCO tuning) for the selected rate and subrate. The rate and subrate settings (bits 7:6 and 5:4 of register 0x2f) determine the frequency range to be searched, with the 25 MHz reference clock used as the frequency reference for the frequency search.

The CAP DAC value can be overridden by writing new values to bits 4:0 of register 0x08 (for CAP DAC setting 1) and bits 4:0 of 0x0b (for CAP DAC setting 2). The override bit, bit 7 of register 0x09 must be set for the override CAP DAC values to take effect. Since the valid rate and subrate setting for 10 GbE and 1 GbE applies to multiple data rates, there are two CAP DAC values for this rate. The first is in register 0x08, bits 4:0, and the second is in register 0x0b, bits 4:0. The DS100DF410 will use the CAP DAC value in register 0x08 for the larger divide ratio (8) associated with the selected rate and subrate to try and acquire lock. If it fails to acquire lock, it will use the CAP DAC value in register 0x0b with the smaller divide ratio (higher VCO frequency) associated with the selected rate and subrate (1). It will continue to try to acquire lock in this way until it either succeeds or the override bit (bit 7 of register 0x09) is cleared.

7.5.10 Overriding the Output Multiplexer

Register 0x09, bit 5, Register 0x14, bits 7:6, and Register 0x1e, bits 7:5

By default, the DS100DF410 output for each channel will be as shown in Table 3.

Table 3. Default Output Status Description

INPUT SIGNAL STATUS	CHANNEL STATUS	OUTPUT STATUS
Not Present	No Signal Detected	Muted
Present	Not Locked	Muted
Present	Locked	Retimed Data

This default behavior can be modified by register writes.

Register 0x1e, bits 7:5, contain the output multiplexer override value. The values of this three-bit field and the corresponding meanings of each are shown in Table 4.

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Table 4. Output Multiplexer Override Settings

BIT FIELD VALUE	OUTPUT MULTIPLEXER SETTING	COMMENTS
0x7	Mute	Default when no signal is present or when the retimer is unlocked
0x6	N/A	Invalid Setting
0x5	10 MHz Clock	Internal 10 MHz clock Clock frequency may not be precise
0x4	PRBS Generator	PRBS Generator must be enabled to output PRBS sequence
0x3	VCO Q-Clock	Register 0x09, bit 4, and register 0x1e, bit 0, must be set to enable the VCO Q-Clock
0x2	VCO I-Clock	
0x1	Retimed Data	Default when the retimer is locked
0x0	Raw Data	

If the output multiplexer is not overridden, that is, if bit 5 of register 0x09 is not set, then the value in register 0x1e, bits 7:5, controls the output produced when the retimer has a signal at its input, but is not locked to it. The default value for this bit field, 0x7, causes the retimer output to mute when the retimer is not locked to an input signal. Writing a value of 0x0 to this bit field, for example, will cause the retimer to output raw data when it is not locked to its input signal.

Setting the override bit, bit 5 of register 0x09, will cause the retimer to output the value selected by the bit field in register 0x1e, bits 7:5, even when the retimer is locked.

When no signal is present at the input to the selected channel of the DS100DF410 the signal detect circuitry will power down the channel. This includes the output driver which is therefore muted when no signal is present at the input. If you want to get an output when no signal is present at the input, for example to enable a free-running PRBS sequence, the first step is to override the signal detect. In order to force the signal detect on, set bit 7 and clear bit 6 of channel register 0x14. Even if there is no signal at the input to the channel, the channel will be enabled. If the channel was disabled before, the current drain from the supply will increase by 100–150 mA depending upon the other channel settings in the device. This increased current drain indicates that the channel is now enabled.

The second step is to override the output multiplexer setting. This is accomplished by setting bit 5 of register 0x09, the output multiplexer override. Once this bit is set, the value of register 0x1e, bits 7:5 will control the output of the channel. Note that if either retimed or raw data is selected, the output will just be noise. The device output may saturate to a static 1 or 0.

If there is no signal, the VCO clock will be free-running. Its frequency will depend upon the divider and CAP DAC settings and it will vary from part to part and over temperature.

If the PRBS generator is enabled, the PRBS generator output can be selected. This can either be at a data rate determined by the free-running VCO or at a data rate determined by the input signal, if one is present. If a signal is present at the input and the DS100DF410 can lock to it, the output of the PRBS generator will be synchronous with the input signal, but the bit stream output will be determined by the PRBS generator selection.

The 10 MHz clock is always available at the output when the output multiplexer is overridden. The 10 MHz clock is a free-running oscillator in the DS100DF410 and is not synchronous to the input or to anything else in the system. The clock frequency will be approximately 10 MHz, but this will vary from part to part.

If there is a signal present at the input, it is not necessary to override the signal detect. Clearing bits 7 and 6 of register 0x14 will return control of the signal detect to the DS100DF410. Normally, when the retimer is locked to a signal at its input, it will output retimed data. However, if desired, the output multiplexer can be overridden in this condition to output raw data. It can also be set to output any of the other signals shown in Table 4. If there is an input signal, and if the DS100DF410 is locked to it, the VCO I-Clock, the VCO Q-Clock, and the output of the PRBS generator, if it is enabled, will be synchronous to the input signal.

When a signal is present at the input, it might be desired to output the raw data in order to see the effects of the CTLE and the DFE without the CDR. It might also be desired to enable the PRBS generator and output this signal, replacing the data content of the input signal with the internally-generated PRBS sequence.

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7.5.11 Overriding the VCO Divider Selection

Register 0x09, bit 2, and Register 0x18, bits 6:4

In normal operation, the DS100DF410 sets its VCO divider to the correct divide ratio, either 1, 2, 4, 8, or 16, depending upon the bit rate of the signal at the channel input. It is possible to override the divider selection. This might be desired if the VCO is set to free-run, for example, to output a signal at a sub-harmonic of the actual VCO frequency.

In order to override the VCO divider settings, first set bit 2 of register 0x09. This is the VCO divider override enable. Once this bit is set, the VCO divider setting is controlled by the value in register 0x18, bits 6:4. The valid values for this three-bit field are 0x0 to 0x4. The mapping of the bit field values to the divider ratio is shown in Table 5.

Table 5. Divider Ratio Mapping to Register 0x18, Bits 6:4

BIT FIELD VALUE	DIVIDER RATIO
0	1
1	2
2	4
3	8
4	16

In normal operation, the DS100DF410 will determine the required VCO divider ratio automatically. The most common application for overriding the divider ratio is when the VCO is set to free-run. Normally the divider ratio should not be overridden except in this case.

7.5.12 Using the PRBS Generator

Register 0x0d, bit 5, Register 0x1e, bit 4, and Register 0x30, bit 3 and bits 1:0

The DS100DF410 includes an internal PRBS generator which can generate standard PRBS-9 and PRBS-31 bit sequences. The PRBS generator can produce a PRBS sequence that is synchronous to the incoming data signal, or it can generate a PRBS sequence using the internal free-running VCO as a clock. Both modes of operation are described in the paragraphs that follow.

To produce a PRBS sequence that is synchronized to the incoming data signal, the DS100DF410 must be locked to the incoming signal. When this is true, the signal detect is set and the channel is active. In addition, the VCO is locked to the incoming signal The VCO will remain locked to the incoming signal regardless of the state of the output multiplexer.

To activate the PRBS generator, first set bit 4 of register 0x1e. This bit enables the PRBS generator digital circuitry. Then reset the PRBS clock by clearing bit 3 of register 0x30. Select either PRBS-9 or PRBS-31 by setting bits 1:0 of register 0x30. Set this bit field to 0x0 for PRBS-9 and to 0x2 for PRBS-31. Then load the PRBS clock by setting bit 3 of register 0x30. Finally, enable the PRBS clock by setting bit 5 of register 0x0d. This sequence of register writes will enable the internal PRBS generator.

As described above, to select the PRBS generator as the output for the selected channel, set bit 5 of register 0x09, the output multiplexer override. Then write 0x4 to bits 7:5 of register 0x1e. This selects the PRBS generator for output.

For the case described above, the output PRBS sequence will be synchronous to the incoming data. There are two other cases of interest. The first is when there is an input signal but the PRBS sequence should not be synchronous to it. In other words, in this case it is desired that the VCO should free-run. The second case is when there is no input signal, but the PRBS sequence should still be output. Again, in this case, the VCO is free-running.

The register settings for these two cases are almost the same. The only difference is that, if there is no input signal, then the channel will be disabled and powered-down by default. In order to force enable the channel, write a 1 to bit 7 and a 0 to bit 6 of register 0x14. This forces the signal detect to be active and enables the selected channel.

The remainder of the register write sequence is designed to disable the phase-locked loop so that the VCO can free run.

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First write a 1 to bit 3 of register 0x09, then 0x0 to bits 1:0 of register 0x1b. This disables the charge pump for the phase-locked loop.

Next write a 1 to bit 2 of register 0x09. This enables the VCO divider override. Then set the VCO divider ratio by writing to register 0x18 as shown in Table 5. For an output frequency of approximately 10.3125 GHz, set the divider ratio to 1 by writing 0x0 to bits 6:4 of register 0x18. Do not clear bit 3 when you write a 1 to bit 2 of register 0x09.

Now write a 1 to bit 7 of register 0x09. This enables the VCO CAP DAC override. Write the desired VCO cap count to register 0x08, bits 4:0. The mapping of VCO frequencies to cap count will vary somewhat from part to part. The VCO cap count should be set to 0x0c to yield an output VCO frequency of approximately 10.3125 GHz. Do not clear bits 3 and 2 when you write a 1 to bit 7 of register 0x09.

Now write a 1 to bit 6 of register 0x09. This enables the VCO LPF DAC which can generate a VCO control voltage internally to the DS100DF410. Once the LPF DAC is enabled, write the desired value of the LPF DAC output in register 0x1f, bits 4:0. For an output VCO frequency of approximately 10.3125 GHz, set the LPF DAC setting to 0x12. Do not clear the remaining bits of register 0x09 when you write a 1 to bit 6.

Now, as above, enable the PRBS generator and set it to the desired bit sequence, then select the output to be the PRBS generator by setting the output multiplexer. Notice that when this entire sequence has been completed, bits 7:2 of register 0x09 will all be set. The default value of register 0x09 is 0x00, so you can clear all the overrides when you are ready to return to normal operation by writing 0x00 to register 0x09.

The VCO frequency in free-run will vary somewhat from part to part. In order to determine exact values of the CAP DAC and LPF DAC settings, it will be necessary to directly measure the VCO frequency using some sort of frequency-measurement device such as a frequency counter or a spectrum analyzer. When the VCO is set to free-run mode as above, you can select the VCO I-clock (in-phase clock) to be the output as shown in Table 4. You can measure the frequency of the VCO I-clock while adjusting the CAP DAC and LPF DAC values until the VCO I-clock frequency is acceptable for your application. Then you can once again select the PRBS generator as the output using the output multiplexer selection field.

7.5.13 Using the Internal Eye Opening Monitor

Register 0x11, bits 7:6 and bit 5, Register 0x22, bit 7, Register 0x24, bit 7 and bit 0, Register 0x25, Register 0x26, Register 0x27, Register 0x28, and Register 0x2a

The DS100DF410 includes an internal eye opening monitor. The eye opening monitor is used by the retimer to compute a figure of merit for automatic adaptation of the CTLE and the DFE. It can also be controlled and queried through the SMBus by a system controller.

The eye opening monitor produces error hit counts for settable phase and voltage offsets of the comparator in the retimer. This is similar to the way many Bit Error Rate Test Sets measure eye opening. At each phase and amplitude offset setting, the eye opening monitor determines the nominal bit value (“0” or “1”) using its primary comparator. This is the bit value that is resynchronized to the recovered clock and presented at the output of the DS100DF410. The eye opening monitor also determines the bit value detected by the offset comparator. This information yields an eye contour. Here's how this works.

If the offset comparator is offset in voltage by an amount larger than the vertical eye opening, for example, then the offset comparator will always decide that the current bit has a bit value of “0”. When the bit is really a “1”, as determined by the primary comparator, this is considered a bit error. The number of bit errors is counted for a settable interval at each setting of the offset phase and voltage of the offset comparator. These error counts can be read from registers 0x25 and 0x26 for sequential phase and voltage offsets. These error counts for each phase and voltage offsets form a 64 X 64 point array. A surface or contour plot of the error hit count versus phase and voltage offset produces an eye diagram, which can be plotted by external software.

The eye opening monitor works in two modes. In the first, only the horizontal and vertical eye openings are measured. The eye opening monitor first sweeps its variable-phase clock through one unit interval with the comparison voltage set to the mid point of the signal. This determines the midpoint of the horizontal eye opening. The eye opening monitor then sets its variable phase clock to the midpoint of the horizontal eye opening and sweeps its comparison voltage. These two measurements determine the horizontal and vertical eye openings. The horizontal eye opening value is read from register 0x27 and the vertical eye opening from register 0x28. Both values are single byte values.

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The measurement of horizontal and vertical eye opening is very fast. The speed of this measurement makes it useful for determining the adaptation figure of merit. In normal operation, the HEO and VEO are automatically measured periodically to determine whether the DS100DF410 is still in lock. Reading registers 0x27 and 0x28 will yield the most-recently measured HEO and VEO values.

In normal operation, the eye monitor circuitry is powered down most of the time to save power. When the eye is to be measured under external control, it must first be enabled by writing a 0 to bit 5 of register 0x11. The default value of this bit is 1, which powers down the eye monitor except when it is powered-up periodically by the CDR state machine and used to test CDR lock. The eye monitor must be powered up to measure the eye under external SMBus control.

Bits 7:6 of register 0x11 are also used during eye monitor operation to set the EOM voltage range. This is described below. A single write to register 0x11 can set both bit 5 and bits 7:6 in one operation.

Register 0x3e, bit 7, enables horizontal and vertical eye opening measurements as part of the lock validation sequence. When this bit is set, the CDR state machine periodically uses the eye monitor circuitry to measure the horizontal and vertical eye opening. If the eye openings are too small, according to the pre-determined thresholds in register 0x6a, then the CDR state machine declares lock loss and begins the lock acquisition process again. For SMBus acquisition of the internal eye, this lock monitoring function must be disabled. Prior to overriding the EOM by writing a 1 to bit 0 of register 0x24, disable the lock monitoring function by writing a 0 to bit 7 of register 0x3e. Once the eye has been acquired, you can reinstate HEO and VEO lock monitoring by once again writing a 1 to bit 7 of register 0x3e.

Under external SMBus control, the eye opening monitor can be programmed to sweep through all its 64 states of phase and voltage offset autonomously. This mode is initiated by setting register 0x24, bit 7, the fast_eom mode bit. Register 0x22, bit 7, the eom_ov bit, should be cleared in this mode.

When the fast_eom bit is set, the eye opening monitor operation is initiated by setting bit 0 of register 0x24, which is self-clearing. As soon as this bit is set, the eye opening monitor begins to acquire eye data. The results of the eye opening monitor error counter are stored in register 0x25 and 0x26. In this mode the eye opening monitor results can be obtained by repeated multi-byte reads from register 0x25. It is not necessary to read from register 0x26 for a multi-byte read. As soon as the eight most significant bits are read from register 0x25, the eight least significant bits for the current setting are loaded into register 0x25 and they can be read immediately. As soon as the read of the eight most significant bits has been initiated, the DS100DF410 sets its phase and voltage offsets to the next setting and starts its error counter again. The result of this is that the data from the eye opening monitor is available as quickly as it can be read over the SMBus with no further register writes required. The external controller just reads the data from the DS100DF410 over the SMBus as fast as it can. When all the data has been read, the DS100DF410 clears the eom_start bit.

If multi-byte reads are not used, meaning that the device is addressed each time a byte is read from it, then it is necessary to read register 0x25 to get the MSB (the eight most significant bits) and register 0x26 to get the LSB (the eight least significant bits) of the current eye monitor measurement. Again, as soon as the read of the MSB has been initiated, the DS100DF410 sets its phase and voltage offsets to the next setting and starts its error counter again. In this mode both registers 0x25 and 0x26 must be read in order to get the eye monitor data. The eye monitor data for the next set of phase and voltage offsets will not be loaded into registers 0x25 and 0x26 until both registers have been read for the current set of phase and voltage offsets.

In all eye opening monitor modes, the amount of time during which the eye opening monitor accumulates eye opening data can be set by the value of register 0x2a. In general, the greater this value the longer the accumulation time. When this value is set to its maximum possible value of 0xff, the maximum number of samples acquired at each phase and amplitude offset is approximately 2^{18}. Even with this setting, the eye opening monitor values can be read from the SMBus with no delay. The eye opening monitor operation is sufficiently fast that the SMBus read operation cannot outrun it.

The eye opening is measured at the input to the data comparator. At this point in the data path, a significant amount of gain has been applied to the signal by the CTLE. In many cases, the vertical eye opening as measured by the EOM will be on the order of 400 to 500 mV peak-to-peak. The secondary comparator, which is used to measure the eye opening, has an adjustable voltage range from ±100 mV to ±400 mV. The EOM voltage range is normally set by the CDR state machine during lock and adaptation, but the range can be overridden by setting bit 6 to 0 of register 0x2C, so the voltage range can scale with the values in register 0x11, bits [7:6]. The values of this code and the corresponding EOM voltage ranges are shown in Table 6.

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Table 6. EOM Voltage Range vs. Bits 7:6 of Register 0x11

VALUE in Bits 7:6 of REGISTER 0x11	EOM VOLTAGE RANGE (± mV)
0x0	±100
0x1	±200
0x2	±300
0x3	±400

Note that the voltage ranges shown in Table 6 are the voltage ranges of the signal at the input to the data path comparator. These values are not directly equivalent to any observable voltage measurements at the input to the DS100DF410 . Note also that if the EOM voltage range is set too small the voltage sweep of the secondary comparator may not be sufficient to capture the vertical eye opening. When this happens the eye boundaries will be outside the vertical voltage range of the eye measurement.

7.5.14 Overriding the DFE Tap Weights and Polarities

Register 0x11, bits 3:0, Register 0x12, bit 7 and bits 4:0, Register 0x15, bit 7, Register 0x1e, bit 3, Register 0x20, Register 0x21, Register 0x23, bit 6, Register 0x24, bit 2, Register 0x2f, bit 0, and Registers 0x71–0x75

For the DS100DF410 the DFE tap weights and polarities are normally set automatically by the adaptation procedure. These values can be overridden by the user if desired.

Prior to overriding the DFE tap weights and polarities, the dfe_ov bit, bit 6 of register 0x23, should be set. This bit is set by default. In order for the DFE tap weights and polarities to be applied to the input signal, bit 3 of register 0x1e, the dfe_PD bit, must be set to 0. It is necessary to change the default settings of these registers, because the DFE is powered down by default.

It is also necessary to set bit 7 of register 0x15 in order to manually set the DFE tap weights. This bit is cleared by default.

Bits 4:0 of register 0x12 set the five-bit weight for DFE tap 1. The first DFE tap has a five-bit setting, while the other taps are set using four bits. Often the first DFE tap has the largest effect in improving the bit error rate of the system, which is why this tap has a five-bit weight setting.

The polarity of the tap weight for tap 1 is set using bit 7 of the same register, register 0x12. The polarity is set to 0 by default, which corresponds to a negative algebraic sign for the tap.

The other four taps are set using four-bit fields in registers 0x20 and 0x21. The polarities of these taps are set by bits 3:0 in register 0x11. These tap polarities are all set to 0 by default.

As is the case for the CTLE settings, if changing the DFE tap weights or polarities causes the DS100DF410 to lose lock, it may readapt its CTLE in order to reacquire lock. If this occurs, the CTLE settings may appear to change spontaneously when the DFE tap weights are changed. The mechanism is the same as that described above for the CTLE boost settings.

When the DS100DF410 is set to adapt mode 2 or 3 using bits 6:5 of register 0x31, it will automatically adapt its DFE whenever its CDR state machine is reset. This occurs when the user manually resets the CDR state machine using bits 3:2 of register 0x0a, or when a signal is first presented at the input to the channel when the channel is in an unlocked state.

Regardless of the adapt mode, DFE adaptation can be initiated under SMBus control. Because the DFE tap weight registers are used by the DFE state machine during adaptation, they may be reset prior to adaptation, which can cause the adaptation to fail. The DFE tap observation registers can be used to prevent this.

Prior to initiating DFE adaptation under SMBus control, write the starting values of the DFE tap settings into the DFE tap weight registers, registers 0x11, 0x12, 0x20, and 0x21. The values can be read from the observation registers, registers 0x71 through 0x75. For each DFE tap, read the current value in the observation register. Both the polarities and the tap weights are contained in the observation registers as shown in Table 12. For each DFE tap, write the current tap polarity and tap weight into the DFE tap register. Once all these values have been written, DFE adaptation can be initiated and it will proceed normally. If the DS100DF410 fails to find a set of DFE tap weights producing a better adaptation figure of merit than the starting tap weights, the starting tap weights will be retained and used.

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CTLE adaptation can also be initiated manually. Setting and then clearing bit 0 of register 0x2f will initiate adaptation of the CTLE. As with the DFE, if the DS100DF410 fails to find a set of CTLE settings that produce a better adaptation figure of merit than the starting CTLE values, the starting CTLE values will be retained and used.

7.5.15 Enabling Slow Rise/Fall Time on the Output Driver

Register 0x18, bit 2

Normally the rise and fall times of the output driver of the DS100DF410 are set by the slew rate of the output transistors. By default, the output transistors are biased to provide the maximum possible slew rate, and hence the minimum possible rise and fall times. In some applications, slower rise and fall times may be desired. For example, slower rise and fall times may reduce the amplitude of electromagnetic interference (EMI) produced by a system.

Setting bit 2 of register 0x18 will adjust the output driver circuitry to increase the rise and fall times of the signal. Setting this bit will approximately double the nominal rise and fall times of the DS100DF410 output driver. This bit is cleared by default.

7.5.16 Inverting the Output Polarity

Register 0x1f, bit 7

In some systems, the polarity of the data does not matter. In systems where it does matter, it is sometimes necessary, for the purposes of trace routing, for example, to invert the normal polarities of the data signals.

The DS100DF410 can invert the polarity of the data signals by means of a register write. Writing a 1 to bit 7 of register 0x1f inverts the polarity of the output signal for the selected channel. This can provide additional flexibility in system design and board layout.

7.5.17 Overriding the Figure of Merit for Adaptation

Register 0x2c, bits 5:4, Register 0x31, bits 6:5, Register 0x6b, Register 0x6c, Register 0x6d, and Register 0x6e, bits 7 and 6

The default figure of merit for both the CTLE and DFE adaptation is simple. The horizontal and vertical eye openings are measured for each CTLE boost setting or set of DFE tap weights and polarities. The vertical eye opening is scaled to a constant reference vertical eye opening and the smaller of the horizontal or vertical eye opening is taken as the figure of merit for that set of equalizer settings. The objective is to adapt the equalizer to a point where the horizontal and vertical eye openings are both as large as possible. This usually provides optimum bit error rate performance for most transmission channels.

In some systems the adaptation can reach a better setting if only the horizontal or vertical eye opening is used to compute the figure of merit rather than using both. This will be system-dependent and the user must determine through experiment whether this provides better adaptation in the user's system. For the DS100DF410, the DFE figure of merit type can be set using register 0x2c, bits 5:4. The value of this two-bit field versus the configured figure of merit type is shown in Table 7.

Table 7. Figure of Merit Type Setting

REGISTER 0x2c, BITS 5:4	FIGURE of MERIT TYPE
0x0	Both HEO and VEO are used
0x1	Only HEO is used
0x2	Only VEO is used
0x3	Both HEO and VEO are used (default)

The CTLE figure of merit type is selected using the two-bit field in register 0x31, bits 6:5, with the same effect as in Table 7.

For some transmission media the adaptation can reach a better setting if a different figure of merit is used. The DS100DF410 includes the capability of adapting based on a configurable figure of merit. The configurable figure of merit is structured as shown in Equation 1.

$$FOM = (HEO - b) \times a + (VEO - c) \times (1 - a) \quad (1)$$

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In this equation, HEO is horizontal eye opening, VEO is vertical eye opening, FOM is the figure of merit, and the factors a, b, and c are set using registers 0x6b, 0x6c, and 0x6d respectively.

In order to use the configurable figure of merit, the enable bits must be set. To use the configurable figure of merit for the CTLE adaptation, set bit 7 of register 0x6e, the en_new_fom_ctle bit. To use the configurable figure of merit for the DFE adaptation set bit 6 of register 0x6e, the en_new_fom_dfe bit. The same scaling factors are used for both CTLE and DFE adaptation when the configurable figure of merit is enabled.

7.5.18 Setting the Rate and Subrate for Lock Acquisition

Register 0x2f, bits 7:6 and 5:4

The rate and subrate settings, which configure the set of VCO frequencies to which the VCO coarse tuning is to be calibrated are set using channel register 0x2f. Bits 7:6 are RATE<1:0>, and bits 5:4 are SUBRATE<1:0>.

7.5.19 Setting the Adaptation/Lock Mode

Register 0x31, bits 6:5, and Register 0x33, bits 7:4 and 3:0, Register 0x34, bits 3:0, Register 0x35, bits 4:0, Register 0x3e, bit 7, and Register 0x6a

There are four adaptation modes available in the DS100DF410.

- Mode 0: The user is responsible for setting the CTLE and DFE values. this mode is used if the transmission channel response is fixed.
- Mode 1: Only the CTLE is adapted to equalize the transmission channel. The DFE is enabled but the tap weights are all set to 0. This mode is primarily used for smoothly-varying high-loss transmission channels such as cables and simple PCB traces.
- Mode 2: In this mode, both the CTLE and the DFE are adapted to compensate for additional loss, reflections, and crosstalk in the input transmission channel.
  - The maximum DFE tap weights can be constrained using register 0x34, bits 3:0, and register 0x35, bits 4:0 as shown in Table 14.
- Mode 3: In this mode, both the CTLE and DFE are adapted as in mode 2. However, in mode 3, more emphasis is placed on the DFE setting. This mode may give better results for high crosstalk transmission channels.

Bits 6:5 of register 0x31 determine the adaptation mode to be used. The mapping of these register bits to the adaptation algorithm is shown in Table 14.

Table 8. DS100DF410 Adaptation Algorithm Settings

REGISTER 0X31, BIT 6 ADAPT_MODE[1]	REGISTER 0x31, BIT 5 ADAPT_MODE[0]	ADAPT MODE SETTING <1:0>	ADAPTATION ALGORITHM
0	0	00	No Adaptation
0	1	01	Adapt CTLE Until Optimum (Default)
1	0	10	Adapt CTLE Until Optimum then DFE, then CTLE Again
1	1	11	Adapt CTLE Until Lock, then DFE, the CTLE Again

By default the DS100DF410 requires that the equalized internal eye exhibit horizontal and vertical eye openings greater than a pre-set minimum in order to declare a successful lock. The minimum values are set in register 0x6a.

The DS100DF410 continuously monitors the horizontal and vertical eye openings while it is in lock. If the eye opening falls below the threshold set in register 0x6a, the DS100DF410 will declare a loss of lock.

The continuous monitoring of the horizontal and vertical eye openings may be disabled by clearing bit 7 of register 0x3e.

7.5.20 Initiating Adaptation

Register 0x24, bit 2, and Register 0x2f, bit 0

When the DS100DF410 becomes unlocked, it will automatically try to acquire lock. If an adaptation mode is selected using bits 6:5 in register 0x31, the DS100DF410 will also try to adapt its CTLE and its DFE.

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Adaptation can also be initiated by the user. CTLE adaptation can be initiated by setting and then clearing register 0x2f, bit 0. DFE adaptation can be initiated by setting and then clearing bit 2 of register 0x24.

7.5.21 Setting the Reference Enable Mode

Register 0x36, bits 5:4

Register 0x36, bits 5:4, are the ref_mode<1:0> bits. These bits should be set to a value of 2'b11. Note that this is not the default. The reference mode must be set prior to using the DS100DF410.

A 25 MHz reference clock signal must be provided on the reference in pin (pin 19). The use of the reference clock in the DS100DF410 is explained below.

First, the reference clock allows the DS100DF410 to calibrate its VCO frequency at power-up and upon reset. This enables the DS100DF410 to determine the optimum coarse VCO tuning setting *a-priori*, which makes phase lock much faster. The DS100DF410 is not required to tune through the available coarse VCO tuning settings as it tries to acquire lock to an input signal. It can select the correct setting immediately.

Second, if the DS100DF410 loses lock for some reason and the VCO drifts from its phase-locked frequency, the DS1010DF410 can detect this very quickly using the reference clock. Detecting an out-of-lock condition quickly allows the DS100DF410 to raise an interrupt indicating that it has lost lock quickly, which the system controller can then service to correct the problem quickly.

Finally, some data signals with large jitter spurs in their frequency spectra can cause the DS1100DF410 to false lock. This occurs when the data pattern exhibits strong discrete frequency components in its frequency spectrum, or when the data pattern has a lot of periodic jitter imposed on it. If you look at such a signal in the frequency domain using a spectrum analyzer, it will clearly show “spurs” close in to the fundamental data rate frequency. These spurs can cause the DS100DF410 to false lock.

Using the 25 MHz reference clock, the DS100DF410 can detect when it is locked to a jitter spur. When this happens, the DS100DF410 will re-initiate the adaptation and lock sequence until it locks to the correct data rate. This provides immunity to false lock conditions.

The reference clock mode is set by a two-bit field, register 0x36, bits 5:4. This field should always be set to a value of 3 or 2'b11.

7.5.22 Overriding the CTLE Settings Used for CTLE Adaptation

Register 0x2c, bits 3:0, Register 0x2f, bit 3, Register 0x39, bits 4:0, and Registers 0x50-0x5f

The CTLE adaptation algorithm operates by setting the CTLE boost stage controls to a set of pre-determined boost settings, each of which provides progressively more high-frequency boost. At each stage in the adaptation process, the DS100DF410 attempts to phase lock to the equalized signal. If the phase lock succeeds, the DS100DF410 measures the horizontal and vertical eye openings using the internal eye monitor circuit. The DS100DF410 computes a figure of merit for the eye opening and compares it to the previous best value of the figure of merit. While the figure of merit continues to improve, the DS100DF410 continues to try additional values of the CTLE boost setting until the figure of merit ceases to improve and begins to degrade. When the figure of merit starts to degrade, the DS100DF410 still continues to try additional CTLE settings for a pre-determined trial count called the “look-beyond” count, and if no improvement in the figure of merit results, it resets the CTLE boost values to those that produced the best figure of merit. The resulting CTLE boost values are then stored in register 0x03. The “look-beyond” count is configured by the value in register 0x2c, bits 3:0. The value is 0x2 by default.

The set of boost values used as candidate values during CTLE adaptation are stored as bit fields in registers 0x40-0x5f. The default values for these settings are shown in Table 9. These values may be overridden by setting the corresponding register values over the SMBus. If these values are overridden, then the next time the CTLE adaptation is performed the set of CTLE boost values stored in these registers will be used for the adaptation. Resetting the channel registers by setting bit 2 of channel register 0x00 will reset the CTLE boost settings to their defaults. So will power-cycling the DS100DF410.

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Table 9. CTLE Settings for Adaptation

REGISTER (HEX)	BITS 7:6 (CTLE STAGE 0)	BITS 5:4 (CTLE STAGE 1)	BITS 3:2 (CTLE STAGE 2)	BITS 1:0 (CTLE STAGE 3)	CTLE BOOST STRING	CTLE ADAPTATION INDEX
40	0	0	0	0	0000	0
41	0	0	0	1	0001	1
42	0	0	1	0	0010	2
43	0	1	0	0	0100	3
44	1	0	0	0	1000	4
45	0	0	2	0	0020	5
46	0	0	0	2	0002	6
47	2	0	0	0	2000	7
48	0	0	0	3	0003	8
49	0	0	3	0	0030	9
4A	0	3	0	0	0300	10
4B	1	0	0	1	1001	11
4C	1	1	0	0	1100	12
4D	3	0	0	0	3000	13
4E	1	2	0	0	1200	14
4F	2	1	0	0	2100	15
50	2	0	2	0	2020	16
51	2	0	0	2	2002	17
52	2	2	0	0	2200	18
53	1	0	1	2	1012	19
54	1	1	0	2	1102	20
55	2	0	3	0	2030	21
56	2	3	0	0	2300	22
57	3	0	2	0	3020	23
58	1	1	1	3	1113	24
59	1	1	3	1	1131	25
5A	1	2	2	1	1221	26
5B	1	3	1	1	1311	27
5C	3	1	1	1	3111	28
5D	2	1	2	1	2121	29
5E	2	1	1	2	2112	30
5F	2	2	1	1	2211	31

As an alternative to, or in conjunction with, writing the CTLE boost setting registers 0x40 through 0x5f, it is possible to set the starting CTLE boost setting index. To override the default setting, which is 0, set bit 3 of register 0x2f. When this bit is set, the starting index for adaptation comes from register 0x39, bits 4:0. This is the index into the CTLE settings table in registers 0x40 through 0x5f. When this starting index is 0, which is the default, CTLE adaptation starts at the first setting in the table, the one in register 0x40, and continues until the optimum FOM is reached.

7.5.23 Setting the Output Differential Voltage

Register 0x2d, bits 2:0

There are eight levels of output differential voltage available in the DS100DF410, from 0.6 V to 1.3 V in 0.1 V increments. The values drv_sel_vod[2:0] in bits 2:0 of register 0x2d set the output VOD. The available VOD settings and the corresponding values of this bit field are shown in Table 10.

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Table 10. VOD Settings

BIT 2, DRV_SEL_VOD[2]	BIT 1, DRV_SEL_VOD[1]	BIT 0, DRV_SEL_VOD[0]	SELECTED VOD (V, PEAK-TO-PEAK, DIFFERENTIAL)
0	0	0	0.6
0	0	1	0.7
0	1	0	0.8
0	1	1	0.9
1	0	0	1.0
1	0	1	1.1
1	1	0	1.2
1	1	1	1.3

7.5.24 Setting the Output De-emphasis Setting

Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS100DF410, ranging from 0 dB to -12 dB. The de-emphasis values come from register 0x15, bits 2:0, which make up the bit field dvr_dem<2:0>, and register 0x15, bit 6, which is the de-emphasis range bit.

The available driver de-emphasis settings and the mapping to these bits are shown in Table 11.

Table 11. Driver De-Emphasis Settings

REGISTER 0X15, BIT 2, DVR_DEM[2]	REGISTER 0X15, BIT 1, DRV_DEM[1]	REGISTER 15, BIT 0, DRV_DEM[0]	REGISTER 0x15, BIT 6, DRV_DEM_RANGE	DE-EMPHASIS SETTING (dB)
0	0	0	X	0.0
0	0	1	1	-0.9
0	0	1	0	-1.5
0	1	0	1	-2.0
0	1	1	1	-2.8
1	0	0	1	-3.3
0	1	0	0	-3.5
1	0	1	1	-3.9
1	1	0	1	-4.5
0	1	1	0	-5.0
1	1	1	1	-5.6
1	0	0	0	-6.0
1	0	1	0	-7.5
1	1	0	0	-9.0
1	1	1	0	-12.0

7.6 Register Maps

7.6.1 Register Information

There are two types of device registers in the DS100DF410. These are the control/shared registers and the channel registers. The control/shared registers control or allow observation of settings which affect the operation of all channels of the DS100DF410. They are also used to select which channel of the device is to be the target channel for reads from and writes to the channel registers.

The channel registers are used to set all the configuration settings of the DS100DF410. They provide independent control for each channel of the DS100DF410 for all the settable device characteristics.

Any registers not described in the tables that follow should be treated as reserved. The user should not try to write new values to these registers. The user-accessible registers described in the tables that follow provide a complete capability for customizing the operation of the DS100DF410 on a channel-by-channel basis.

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Register Maps (continued)

7.6.2 Bit Fields in the Register Set

Many of the registers in the DS100DF410 are divided into bit fields. This allows a single register to serve multiple purposes, which may be unrelated.

Often configuring the DS100DF410 requires writing a bit field that makes up only part of a register value while leaving the remainder of the register value unchanged. The procedure for accomplishing this is to read in the current value of the register to be written, modify only the desired bits in this value, and write the modified value back to the register. Of course, if the entire register is to be changed, rather than just a bit field within the register, it is not necessary to read in the current value of the register first.

In all the register configuration procedures described in the following sections, this procedure should be kept in mind. In some cases, the entire register is to be modified. When only a part of the register is to be changed, however, the procedure described above should be used.

7.6.3 Writing to and Reading from the Control/Shared Registers

Any write operation targeting register 0xff writes to the control/shared register 0xff. This is the only register in the DS100DF410 with an address of 0xff.

Bit 2 of register 0xff is used to select either the control/shared register set or a channel register set. If bit 2 of register 0xff is cleared (written with a 0), then all subsequent read and write operations over the SMBus are directed to the control/shared register set. This situation persists until bit 2 of register 0xff is set (written with a 1).

There is a register with address 0x00 in the control/shared register set, and there is also a register with address 0x00 in each channel register set. If you read the value in register 0x00 when bit 2 of register 0xff is cleared to 0, then the value returned by the DS100DF410 is the value in register 0x00 of the control/shared register set. If you read the value in register 0x00 when bit 2 of register 0xff is set to 1, then the value returned by the DS100DF410 is the value in register 0x00 of the selected channel register set. The channel register set is selected by bits 1:0 of register 0xff.

If bit 3 of register 0xff is set to 1 and bit 2 of register 0xff is also set to 1, then any write operation to any register address will write all the channel register sets in the DS100DF410 simultaneously. This situation will persist until either bit 3 of register 0xff or bit 2 of register 0xff is cleared. Note that when you write to register 0xff, independent of the current settings in register 0xff, the write operation **ALWAYS** targets the control/shared register 0xff. This channel select register, register 0xff, is unique in this regard.

Table 12 shows the control/shared register set. Any register addresses or register bits in the control/shared register set not shown in this table should be considered reserved. In this table, the mode is either R for Read-Only, R/W for Read-Write, or R/W/SC for Read-Write-Self-Clearing. If you try to write to a Read-Only register, the DS100DF410 will ignore it.

Table 12. Control/Shared Registers

ADDRESS (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
0	7	0	R	N	SMBus_Addr3	SMBus Address Strapped 7-bit addres is 0x18 + SMBus_Addr[3:0]
	6	0	R	N	SMBus_Addr2	
	5	0	R	N	SMBus_Addr1	
	4	0	R	N	SMBus_Addr0	
	3:0	0			RESERVED	
1	7	0	R	N	Version2	Device version
	6	1	R	N	Version1	
	5	1	R	N	Version0	
	4	1	R	N	Device_ID4	Device ID code
	3	0	R	N	Device_ID3	
	2	0	R	N	Device_ID2	
	1	0	R	N	Device_ID1	
	0	0	R	N	Device_ID0	

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Register Maps (continued)

Table 12. Control/Shared Registers (continued)

ADDRESS (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
2	7:0	0	RW	N	RESERVED	
3	7:0	0		N	RESERVED	
4	7	0	RW	N	RESERVED	
	6	0	RWSC	N	RST_SMB_REGS	1: Resets share registers. Self-clearing.
	5	0	RWSC	N	RST_SMB_MAS	1: Reset for SMBus Master Mode
	4	0	RW	N	rc_eeprm_rd	1: Force EEPROM Configuration
	3	0	RW	N	RESERVED	
	2	0	RW	N	RESERVED	
	1	0	RW	N	RESERVED	
	0	1	RW	N	RESERVED	
5	7	0	RW	N	disab_eeprm_cfg	Disable Master Mode EEPROM Configuration
	6:5	0	RW	N	RESERVED	
	4	1	R	N	EEPROM_READ_DONE	This bit is set to 1 when read from EEPROM is done
	3	0	R	N	int_ch0	Set on Channel 0 Interrupt
	2	0	R	N	int_ch1	Set on Channel 1 Interrupt
	1	0	R	N	int_ch2	Set on Channel 2 Interrupt
	0	0	R	N	int_ch3	Set on Channel 3 Interrupt
6	7:0	0	RW	N	RESERVED	
7	7:0	0x05	RW	N	RESERVED	
FF	7:4	0	RW	N	RESERVED	
	3	0	RW	N	WRITE_ALL_CH	Selects All Channels for Register Write. See Table 3.
	2	0	RW	N	EN_CH_SMB	Enable Register Write to One or all Channels and Register Read from One Channel. See Table 3.
	1:0	0	RW	N	SEL_CH_SMB	Selects Target Channel for Register Reads and Writes. See Table 3.

7.6.4 Channel Select Register

Register 0xff, bits 3:0

Register 0xff, as described above, selects the channel or channels for channel register reads and writes. It is worth describing the operation of this register again for clarity. If bit 3 of register 0xff is set, then any channel register write applies to all channels. Channel register read operations always target only the channel specified in bits 1:0 of register 0xff regardless of the state of bit 3 of register 0xff. Read and write operations target the channel register sets only when bit 2 of register 0xff is set.

Bit 2 of register 0xff is the universal channel register enable. This bit must be set in order for any channel register reads and writes to occur. If this bit is set, then read operations from or write operations to register 0x00, for example, target channel register 0x00 for the selected channel rather than the control/shared register 0x00. In order to access the control/shared registers again, bit 2 of register 0xff should be cleared. Then the control/shared registers can again be accessed using the SMBus. Write operations to register 0xff always target the register with address 0xff in the control/shared register set. There is no other register, and specifically, no channel register, with address 0xff.

The contents of the channel select register, register 0xff, cannot be read back over the SMBus. Read operations on this register will always yield an invalid result. All eight bits of this register should always be set to the desired values whenever this register is written. Always write 0x0 to the four MSBs of register 0xff. The register set target selected by each valid value written to the channel select register is shown in Table 13.

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Table 13. Channel Select Register Values Mapped to Register Set Target

REGISTER 0XFF VALUE (HEX)	SHARED/CHANNEL REGISTER SELECTION	BROADCAST CHANNEL REGISTER SELECTION	TARGETED CHANNEL SELECTION	COMMENTS
0x00	Shared	N/A	N/A	All reads and writes target shared register set
0x04	Channel	No	0	All reads and writes target channel 0 register set
0x05	Channel	No	1	All reads and writes target channel 1 register set
0x06	Channel	No	2	All reads and writes target channel 2 register set
0x07	Channel	No	3	All reads and writes target channel 3 register set
0x0c	Channel	Yes	0	All writes target all channel register sets, all reads target channel 0 register set
0x0d	Channel	Yes	1	All writes target all channel register sets, all reads target channel 1 register set
0x0e	Channel	Yes	2	All writes target all channel register sets, all reads target channel 2 register set
0x0f	Channel	Yes	3	All writes target all channel register sets, all reads target channel 3 register set

7.6.5 Reading to and Writing from the Channel Registers

Each of the four channels has a complete set of channel registers associated with it. The channel registers or the control/shared registers are selected by channel select register 0xff. The settings in this register control the target for subsequent register reads and writes until the contents of register 0xff are explicitly changed by a register write to register 0xff. As noted, there is only one register with an address of 0xff, the channel select register.

Table 14. Channel Registers

Address (Hex)	Bits	Default Value (Hex)	Mode	EEPROM	Field Name	Description
0	7:4	0	RW	N	RESERVED	
	3	0	RW	N	RST_CORE	1: Reset core state machine 0: Normal Operation
	2	0	RW	N	RST_REGS	1: Resets channel registers, restores default values 0: Normal Operation
	1	0	RW	N	RST_REFCLK	1: Reset reference clock domain 0: Normal Operation
	0	0	RW	N	RST_VCO	1: Reset VCO DIV clock domain 0: Normal Operation
1	7:5	0	RW	N	RESERVED	
	4	0	R	N	CDR_LOCK_LOSS_INT	1: indicates loss of CDR lock after having acquired it. Bit clears on read.
	3:1	0	R	N	RESERVED	
	0	0	R	N	SIG_DET_LOSS_INT	Loss of signal indicator. Bit is set once signal is acquired and then lost.
2	7:0	0x0	R	N	cdr_status	CDR Status [7:0] Bit[7] = PPM Count met Bit[6] = Auto Adapt Complete Bit[5] = Fail Lock Check Bit[4] = Lock Bit[3] = CDR Lock Bit[2] = Single Bit Limit Reached Bit[1] = Comp LPF High Bit[0] = Comp LPF Low

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Table 14. Channel Registers (continued)

Address (Hex)	Bits	Default Value (Hex)	Mode	EEPROM	Field Name	Description
3	7	0	RW	Y	EQ_BST0[1]	This register can be used to force an EQ boost setting if used in conjunction with channel register 0x2D[3].
	6	0	RW	Y	EQ_BST0[0]	
	5	0	RW	Y	EQ_BST1[1]	
	4	0	RW	Y	EQ_BST1[0]	
	3	0	RW	Y	EQ_BST2[1]	
	2	0	RW	Y	EQ_BST2[0]	
	1	0	RW	Y	EQ_BST3[1]	
	0	0	RW	Y	EQ_BST3[0]	
4	7:0	0	RW	N	RESERVED	
5	7:0	0	RW	N	RESERVED	
6	7:0	0	RW	N	RESERVED	
7	7:0	0	RW	N	RESERVED	
8	7:5	0	RW	Y	RESERVED	
	4	0	RW	Y	CDR_CAP_DAC_START4	Starting VCO Cap Dac Setting 0
	3	0	RW	Y	CDR_CAP_DAC_START3	Starting VCO Cap Dac Setting 0
	2	0	RW	Y	CDR_CAP_DAC_START2	Starting VCO Cap Dac Setting 0
	1	0	RW	Y	CDR_CAP_DAC_START1	Starting VCO Cap Dac Setting 0
	0	0	RW	Y	CDR_CAP_DAC_START0	Starting VCO Cap Dac Setting 0
9	7	0	RW	Y	DIVSEL_VCO_CAP_OV	Enable bit to override cap_cnt with value in register 0x0B[4:0]
	6	0	RW	Y	SET_CP_LVL_LPF_OV	Enable bit to override lpf_dac_val with value in register 0x1F[4:0]
	5	0	RW	Y	BYPASS_PFD_OV	Enable bit to override sel_retimed_loopthru and sel_raw_loopthru with values in reg 0x1E[7:5]
	4	0	RW	Y	EN_FD_PD_VCO_PDIQ_OV	Enable bit to override en_fd, pd_pd, pd_vco, pd_pdiq with reg 0x1E[0], reg 0x1E[2], reg 0x1C[0], reg 0x1C[1]
	3	0	RW	Y	EN_PD_CP_OV	Enable bit to override pd_fd_cp and pd_pd_cp with value in reg 0x1B[1:0]
	2	0	RW	Y	DIVSEL_OV	Enable bit to override divsel with value in reg 0x18[6:4] 1: Override enable 0: Normal operation
	1	0	RW	Y	EN_FLD_OV	Enable to override pd_fld with value in reg 0x1E[1]
	0	0	RW	Y	PFD_LOCK_MODE_SM	Enable FD in lock state
A	7	0	RW	Y	SBT_EN	Enable bit to override sbt_en with value in reg 0x1D[7]
	6	0	RW	Y	EN_IDAC_PD_CP_OV EN_IDAC_FD_CP_OV	Enable bit to overridephase detector charge pump settings with reg 0x1C[7:5] Enable bit to override frequency detector charge pump settings with reg 0x1C[4:2]
	5	0	RW	Y	DAC_LPF_HIGH_PHASE_OV DAC_LPF_LOW_PHASE_OV	Enable bit to override loop filter comparator trip voltage with reg 0x16[7:0]
	4	1	RW	Y	EN150_LPF_OV	Enable bit to override en150_lpf with value in reg 0x1F[6]
	3	0	RW	N	CDR_RESET_OV	Enable bit to override CDR reset with reg 0x0A[2]
	2	0	RW	N	CDR_RESET_SM	1: CDR is put into reset 0: normal CDR operation
	1	0	RW	N	CDR_LOCK_OV	Enable CDR lock signal override with reg 0x0A[0]
	0	0	RW	N	CDR_LOCK	CDR lock signal override bit

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Table 14. Channel Registers (continued)

Address (Hex)	Bits	Default Value (Hex)	Mode	EEPROM	Field Name	Description
B	7	0	RW	Y	RESERVED	
	6	0	RW	Y	RESERVED	
	5	0	RW	Y	RESERVED	
	4	0	RW	Y	CAP_DAC_START1[4]	Starting VCO cap dac setting 1
	3	1	RW	Y	CAP_DAC_START1[3]	Starting VCO cap dac setting 1
	2	1	RW	Y	CAP_DAC_START1[2]	Starting VCO cap dac setting 1
	1	1	RW	Y	CAP_DAC_START1[1]	Starting VCO cap dac setting 1
	0	1	RW	Y	CAP_DAC_START1[0]	Starting VCO cap dac setting 1
C	7:4	0	RW	N	RESERVED	
	3	1	RW	Y	SINGLE_BIT_LIMIT_CHECK_ON	1: Normal operation, device checks for single bit transitions as a gate to achieving CDR lock
	2	0	RW	Y	RESERVED	
	1	0	RW	Y	RESERVED	
	0	0	RW	Y	RESERVED	
D	7:6	0	RW	Y	RESERVED	
	5	0	RW	Y	PRBS_PATT_SHIFT_EN	PRBS Generator Clock Enable
	4:0	0	RW	Y	RESERVED	
E	7:0	0x93	RW	N	RESERVED	
F	7:0	0x69	RW	N	RESERVED	
10	7:0	0x3A	RW	Y	RESERVED	
11	7	0	RW	Y	EOM_SEL_VRANGE[1]	Manually set the EOM vertical range, used with channel register 0x2C[6]: 00: ±100 mV 01: ±200 mV 10: ±300 mV 11: ±400 mV
	6	0	RW	Y	EOM_SEL_VRANGE[0]	
	5	1	RW	Y	EOM_PD	1: Normal operation
	4	0	RW	N	RESERVED	
	3	0	RW	Y	DFE_TAP2_POL	Bit forces DFE tap 2 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	2	0	RW	Y	DFE_TAP3_POL	Bit forces DFE tap 3 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	1	0	RW	Y	DFE_TAP4_POL	Bit forces DFE tap 4 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	0	0	RW	Y	DFE_TAP5_POL	Bit forces DFE tap 5 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
12	7	1	RW	Y	DFE_TAP1_POL	Bit forces DFE tap 1 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	6	1	RW	N	RESERVED	
	5	1	RW	Y	DFE_SEL_NEG_GM	
	4	0	RW	Y	DFE_WT1[4]	Bits force DFE tap 1 weight, manual DFE operation required to take effect
	3	0	RW	Y	DFE_WT1[3]	
	2	0	RW	Y	DFE_WT1[2]	
	1	0	RW	Y	DFE_WT1[1]	
	0	0	RW	Y	DFE_WT1[0]	

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Table 14. Channel Registers (continued)

Address (Hex)	Bits	Default Value (Hex)	Mode	EEPROM	Field Name	Description
13	7	0	RW	N	RESERVED	
	6	0	RW	Y	RESERVED	
	5	1	RW	Y	RESERVED	
	4	1	RW	Y	EQ_EN_DC_OFF	1: Normal operation
	3	0	RW	Y	RESERVED	
	2	0	RW	Y	EQ_LIMIT_EN	1: Configures the final stage of the equalizer to be a limiting stage. 0: Normal operation, final stage of the equalizer is configured to be a linear stage.
	1	0	RW	Y	RESERVED	
	0	0	RW	Y	RESERVED	
14	7	0	RW	Y	EQ_SD_PRESET	1: Forces signal detect HIGH, and force enables the channel. Should not be set if bit 6 is set. 0: Normal Operation.
	6	0	RW	Y	EQ_SD_RESET	1: Forces signal detect LOW and force disables the channel. Should not be set if bit 7 is set. 0: Normal Operation.
	5	0	RW	Y	EQ_REFA_SEL1	Controls the signal detect assert levels.
	4	0	RW	Y	EQ_REFA_SEL0	
	3	0	RW	Y	EQ_REFD_SEL1	Controls the signal detect de-assert levels.
	2	0	RW	Y	EQ_REFD_SEL0	
	1:0	0	RW	N	RESERVED	
15	7	0	RW	Y	DFE_FORCE_EN	Enables manual DFE tap settings
	6	0	RW	Y	drv_dem_range	Driver De-emphasis Range
	5	0	RW	Y	RESERVED	
	4	1	RW	Y	RESERVED	
	3	0	RW	N	DRV_PD	1: Powers down the high speed driver 0: Normal operation
	2	0	RW	Y	DRV_DEM2	Driver De-emphasis Setting[2:0]
	1	0	RW	Y	DRV_DEM1	
	0	0	RW	Y	DRV_DEM0	
16	7:0	0x7A	RW	Y	RESERVED	
17	7:0	0x36	RW	Y	RESERVED	
18	7	0	RW	N	RESERVED	
	6	1	RW	Y	PDIQ_SEL_DIV2	These bits will force the divider setting if 0x09[2] is set. 000: Divide by 1 001: Divide by 2 010: Divide by 4 011: Divide by 8 100: Divide by 16 All other values are reserved.
	5	0	RW	Y	PDIQ_SEL_DIV1	
	4	0	RW	Y	PDIQ_SEL_DIV0	
	3	0	RW	N	RESERVED	
	2	0	RW	N	DRV_SEL_SLOW	
	1:0	0	RW	N	RESERVED	
19	7:6	0x23	RW	N	RESERVED	
	5:0		RW	Y	RESERVED	
1A	7:4	0x0	RW	Y	RESERVED	
	3:0	0x0	RW	N	RESERVED	
1B	7:2	0	RW	N	RESERVED	
	1	1	RW	Y	CP_EN_CP_PD	1: Normal operation
	0	1	RW	Y	CP_EN_CP_FD	1: Normal operation

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Table 14. Channel Registers (continued)

Address (Hex)	Bits	Default Value (Hex)	Mode	EEPROM	Field Name	Description
1C	7	0	RW	Y	EN_IDAC_PD_CP2	Phase detector charge pump setting. MSB located in channel register 0x0C[0]. Override bit required for these bits to take effect
	6	0	RW	Y	EN_IDAC_PD_CP1	
	5	1	RW	Y	EN_IDAC_PD_CP0	
	4	0	RW	Y	EN_IDAC_FD_CP2	Frequency detector charge pump setting. MSB located in channel register 0x0C[1]. Override bit required for these bits to take effect
	3	0	RW	Y	EN_IDAC_FD_CP1	
	2	1	RW	Y	EN_IDAC_FD_CP0	
	1:0	0	RW	Y	RESERVED	
1D	7	0	RW	Y	SBT_EN	SBT enable override 0: Normal operation
	6:0	0	RW	N	RESERVED	
1E	7	1	RW	Y	PFD_SEL_DATA_MUX2	For these values to take effect, register 0x09[5] must be set to 1. 000: Raw Data* 001: Retimed Data 100: Pattern Generator 111: Mute All other values are reserved.
	6	1	RW	Y	PFD_SEL_DATA_MUX1	
	5	1	RW	Y	PFD_SEL_DATA_MUX0	
	4	0	RW	N	PRBS_EN	1: Enable PRBS Generator
	3	1	RW	Y	DFE_PD	This bit must be cleared for the DFE to be functional in any adapt mode. 0: DFE enabled 1: DFE disabled
	2	0	RW	Y	PFD_PD_PD	PFD phase detector power down override
	1	0	RW	Y	PFD_EN_FLD	PFD enable FLD override
	0	1	RW	Y	PFD_EN_FD	PFD enable frequency detector override
1F	7	0	RW	Y	Drv_sel_inv	Select Output Polarity Inverted
20	7	0	RW	Y	DFE_WT5[3]	Bits force DFE tap 5 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT5[2]	
	5	0	RW	Y	DFE_WT5[1]	
	4	0	RW	Y	DFE_WT5[0]	
	3	0	RW	Y	DFE_WT4[3]	Bits force DFE tap 4 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT4[2]	
	1	0	RW	Y	DFE_WT4[1]	
	0	0	RW	Y	DFE_WT4[0]	
21	7	0	RW	Y	DFE_WT3[3]	Bits force DFE tap 3 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT3[2]	
	5	0	RW	Y	DFE_WT3[1]	
	4	0	RW	Y	DFE_WT3[0]	
	3	0	RW	Y	DFE_WT2[3]	Bits force DFE tap 2 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT2[2]	
	1	0	RW	Y	DFE_WT2[1]	
	0	0	RW	Y	DFE_WT2[0]	
22	7	0	RW	N	EOM_OV	1: Override enable for EOM manual control 0: Normal operation
	6	0	RW	N	EOM_SEL_RATE_OV	1: Override enable for EOMrate selection 0: Normal operation
	5:0	0	RW	N	RESERVED	
23	7	0	RW	N	EOM_GET_HEO_VEO_OV	1: Override enable for manual control of the HEO/VEO trigger 0: Normal operation
	6	1	RW	Y	DFE_OV	1: Normal operation, DFE must be enabled in channel register 0x1E[3]
	5:0	0	RW	N	RESERVED	

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Table 14. Channel Registers (continued)

Address (Hex)	Bits	Default Value (Hex)	Mode	EEPROM	Field Name	Description
24	7	0	RW	N	FAST_EOM	1: Enables fast EOM mode for fully eye capture. In this mode the phase DAC and voltage DAC of the EOM are automatically incremented through a 64 x 64 matrix. Values for each point are stored in channel registers 25 and 26.
	6	0	RW	N	DFE_EQ_ERROR_NO_LOCK	DFE/CTLE SM quit due to loss of lock
	5	0	RW	N	GET_HEO_VEO_ERROR_NO_HITS	GET_HEO_VEO sees no hits at zero crossing
	4	0	RW	N	GET_HEO_VEO_ERROR_NO_OPENING	GET_HEO_VEO cannot see a vertical eye opening
	3	0	RW	N	RESERVED	
	2	0	RW	N	DFE_ADAPT	1: Manually start DFE adaption, self-clearing. 0: Normal operation
	1	0	RW	N	EOM_GET_HEO_VEO	1: Manually triggers a HEO/VEO measurement. Must be enabled with channel register 0x23[7].
	0	0	RW	N	EOM_START	1: Starts EOM counter, self clearing
25	7	0	R	N	EOM_COUNT15	MSBs of EOM counter
	6	0	R	N	EOM_COUNT14	
	5	0	R	N	EOM_COUNT13	
	4	0	R	N	EOM_COUNT12	
	3	0	R	N	EOM_COUNT11	
	2	0	R	N	EOM_COUNT10	
	1	0	R	N	EOM_COUNT9	
	0	0	R	N	EOM_COUNT8	
26	7	0	R	N	EOM_COUNT7	LSBs of EOM counter
	6	0	R	N	EOM_COUNT6	
	5	0	R	N	EOM_COUNT5	
	4	0	R	N	EOM_COUNT4	
	3	0	R	N	EOM_COUNT3	
	2	0	R	N	EOM_COUNT2	
	1	0	R	N	EOM_COUNT1	
	0	0	R	N	EOM_COUNT0	
27	7	0	R	N	HEO7	HEO value, requires CDR to be locked for valid measurement
	6	0	R	N	HEO6	
	5	0	R	N	HEO5	
	4	0	R	N	HEO4	
	3	0	R	N	HEO3	
	2	0	R	N	HEO2	
	1	0	R	N	HEO1	
	0	0	R	N	HEO0	
28	7	0	R	N	VEO7	VEO value, requires CDR to be locked for valid measurement
	6	0	R	N	VEO6	
	5	0	R	N	VEO5	
	4	0	R	N	VEO4	
	3	0	R	N	VEO3	
	2	0	R	N	VEO2	
	1	0	R	N	VEO1	
	0	0	R	N	VEO0	

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Table 14. Channel Registers (continued)

Address (Hex)	Bits	Default Value (Hex)	Mode	EEPROM	Field Name	Description
29	7	0	RW	N	RESERVED	
	6	0	R	N	EOM_VRANGE_SETTING1	Use these bits to read back the EOM voltage range setting: 00: ±100 mV 01: ±200 mV 10: ±300 mV 11: ±400 mV
	5	0	R	N	EOM_VRANGE_SETTING0	
	4:0	0	RW	N	RESERVED	
2A	7	0	RW	Y	EOM_TIMER_THR7	Controls the amount of time the EOM samples each point in the eye for. The total counter bit width is 16-bits. This register is the upper 8-bits. The counter counts in 32-bit words. Therefore, the total number of bits is 32 times this value
	6	0	RW	Y	EOM_TIMER_THR6	
	5	1	RW	Y	EOM_TIMER_THR5	
	4	1	RW	Y	EOM_TIMER_THR4	
	3	0	RW	Y	EOM_TIMER_THR3	
	2	0	RW	Y	EOM_TIMER_THR2	
	1	0	RW	Y	EOM_TIMER_THR1	
	0	0	RW	Y	EOM_TIMER_THR0	
2B	7:6	0	RW	N	RESERVED	
	5:4	0	RW	Y	RESERVED	
	3	0	RW	Y	EOM_MIN_REQ_HITS3	These bits set the number of hits for a particular phase and voltage location in the EOM before the EOM will indicate a hit has occurred. This filtering only affects the HEO measurement. Filter threshold ranges from 0 to 15 hits.
	2	0	RW	Y	EOM_MIN_REQ_HITS2	
	1	0	RW	Y	EOM_MIN_REQ_HITS1	
	0	0	RW	Y	EOM_MIN_REQ_HITS0	
2C	7	0	RW	N	RESERVED	
	6	1	RW	Y	VEO_SCALE	Scale VEO based on EOM vrange
	5	1	RW	Y	DFE_SM_FOM1	00: not valid 01: SM uses only HEO 10: SM uses only VEO 11: SM uses both HEO and VEO
	4	1	RW	Y	DFE_SM_FOM0	
	3	0	RW	Y	DFE_ADAPT_COUNTER3	DFE look-beyond count.
	2	0	RW	Y	DFE_ADAPT_COUNTER2	
	1	1	RW	Y	DFE_ADAPT_COUNTER1	
	0	0	RW	Y	DFE_ADAPT_COUNTER0	
2D	7	1	RW	Y	RESERVED	
	6	0	RW	Y	RESERVED	
	5	0	RW	Y	RESERVED	
	4	0	RW	Y	RESERVED	
	3	0	RW	Y	EQ_BST_OV	Allow override control of the EQ setting by writing to channel register 0x03. Not recommended for normal operation.
	2	0	RW	Y	DRV_SEL_VOD2	Controls the VOD levels of the high speed drivers
	1	0	RW	Y	DRV_SEL_VOD1	
	0	0	RW	Y	DRV_SEL_VOD0	
2E	7:0	0	RW	N	RESERVED	

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Table 14. Channel Registers (continued)

Address (Hex)	Bits	Default Value (Hex)	Mode	EEPROM	Field Name	Description
2F	7	0	RW	Y	RATE1	
	6	0	RW	Y	RATE0	
	5	0	RW	Y	SUBRATE1	
	4	0	RW	Y	SUBRATE0	
	3	0	RW	Y	INDEX_OV	If this bit is set to 1, reg 0x13 is to be used as a 5 bit index to the [31:0] array of EQ settings.
	2	1	RW	Y	EN_PPM_CHECK	1: PPM check to be used as a qualifier when performing lock detect
	1	1	RW	Y	EN_FLD_CHECK	For default ref_mode 3 0: FLD is enabled 1: FLD is disabled
	0	0	RWSC	N	CTLE_ADAPT	Starts CTLE adaption, self-clearing
30	7	0	RW	N	RESERVED	
	6	0	RW	N	RESERVED	
	5	0	R	N	EOM_VRANGE_LIMIT_ERROR	
	4	0	R	N	HEO_VEO_INTERRUPT	
	3	0	RW	Y	PRBS_EN_DIG_CLK	
	2	0	RW	N	RESERVED	
	1	0	RW	Y	PRBS_PATTERN_SEL1	
	0	0	RW	Y	PRBS_PATTERN_SEL0	
31	7	0	RW	Y	RSERVED	
	6	0	RW	Y	ADAPT_MODE1	00: no adaption 01: adapt CTLE only 10: adapt CTLE until optimal, then DFE, then CTLE again 11: adapt CTLE until lock, then DFE, then EQ until optimal
	5	0	RW	Y	ADAPT_MODE0	
	4	0	RW	Y	EQ_SM_FOM1	00: not valid 01: SM uses HEO only 10: SM uses VEO only 11: SM uses both HEO and VEO
	3	0	RW	Y	EQ_SM_FOM0	
	2	0	RW	N	RESERVED	
	1	0	RW	N	RESERVED	
	0	0	RW	N	RESERVED	
32	7	0	RW	Y	HEO_INT_THRESH3	These bits set the threshold for the HEO and VEo interrupt. Each threshold bit represents 8 counts of HEO or VEO.
	6	0	RW	Y	HEO_INT_THRESH2	
	5	0	RW	Y	HEO_INT_THRESH1	
	4	1	RW	Y	HEO_INT_THRESH0	
	3	0	RW	Y	VEO_INT_THRESH3	
	2	0	RW	Y	VEO_INT_THRESH2	
	1	0	RW	Y	VEO_INT_THRESH1	
	0	1	RW	Y	VEO_INT_THRESH0	
33	7	1	RW	Y	HEO_THRESH3	In adapt mode 3, the register sets the minimum HEO and VEO required for CTLE adaption, before starting DFE adaption. This can be a max of 15.
	6	0	RW	Y	HEO_THRESH2	
	5	0	RW	Y	HEO_THRESH1	
	4	0	RW	Y	HEO_THRESH0	
	3	1	RW	Y	VEO_THRESH3	
	2	0	RW	Y	VEO_THRESH2	
	1	0	RW	Y	VEO_THRESH1	
	0	0	RW	Y	VEO_THRESH0	

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Table 14. Channel Registers (continued)

Address (Hex)	Bits	Default Value (Hex)	Mode	EEPROM	Field Name	Description
34	7	0	RW	N	PPM_ERR_RDY	1: Indicates that a PPM error count is read to be read from channel register 0x3B and 0x3C
	6	0	RW	Y	LOW_POWER_MODE_DISABLE	By default, all blocks (except signal detect) power down after 100ms after signal detect goes low.
	5	1	RW	Y	LOCK_COUNTER1	After achieving lock, the CDR continues to monitor the lock criteria. If the lock criteria fail, the lock is checked for a total of N number of times before declaring an out of lock condition, where N is set by this the value in these registers, with a max value of +3, for a total of 4. If during the N lock checks, lock is regained, then the lock condition is left HI, and the counter is reset back to zero.
	4	1	RW	Y	LOCK_COUNTER0	
	3	1	RW	Y	DFE_MAX_TAP2_5[3]	These four bits are used to set the maximum value by which DFE taps 2-5 are able to adapt with each subsequent adaptation. Same used for both polarities.
	2	1	RW	Y	DFE_MAX_TAP2_5[2]	
	1	1	RW	Y	DFE_MAX_TAP2_5[1]	
	0	1	RW	Y	DFE_MAX_TAP2_5[0]	
35	7	0	RW	Y	DATA_LOCK_PPM1	Modifies the value of the ppm delta tolerance from channel register 0x64: 00 - ppm_delta[7:0] =1 x ppm_delta[7:0] 01 - ppm_delta[7:0] =1 x ppm_delta[7:0] + ppm_delta[3:1] 10 - ppm_delta[7:0] =2 x ppm_delta[7:0] 11 - ppm_delta[7:0] =2 x ppm_delta[7:0] + ppm_delta[3:1]
	6	0	RW	Y	DATA_LOCK_PPM0	
	5	0	RW	N	GET_PPM_ERROR	Get ppm error from ppm_count - clears when done. Normally updates continuously, but can be manually triggered with read value from channel register 0x3B and 0x3C
	4	1	RW	Y	DFE_MAX_TAP1[4]	Determines max tap limit for DFE tap 1
	3	1	RW	Y	DFE_MAX_TAP1[3]	
	2	1	RW	Y	DFE_MAX_TAP1[2]	
	1	1	RW	Y	DFE_MAX_TAP1[1]	
	0	1	RW	Y	DFE_MAX_TAP1[0]	
36	7	0	RW	Y	RESERVED	
	6	0	RW	Y	HEO_VEO_INT_EN	1: Enable HEO/VEO interrupt capability
	5	1	RW	Y	REF_MODE1	11: Fast_lock all cap dac ref clock enabled (**recommended**) 10: constrained cap dac, ref clock enabled 01: referenceless constained cap dac 00: referenceless all cap dac
	4	1	RW	Y	REF_MODE0	
	3	0	RW	Y	RESERVED	
	2	0	RW	Y	CDR_CAP_DAC_RNG_OV	Over-ride enable for Cap DAC range
	1	0	RW	Y	cdr_cap_dac_rng[1]	Sets the stop value based on start value - (rng+1): 11:stop = start - 4 10: stop = start - 3 01: stop = start - 2 00: stop = start - 1
	0	1	RW	Y	cdr_cap_dac_rng[0]	
37	7	0	R	N	CTLE_STATUS7	Feature is reserved for future use
	6	0	R	N	CTLE_STATUS6	
	5	0	R	N	CTLE_STATUS5	
	4	0	R	N	CTLE_STATUS4	
	3	0	R	N	CTLE_STATUS3	
	2	0	R	N	CTLE_STATUS2	
	1	0	R	N	CTLE_STATUS1	
	0	0	R	N	CTLE_STATUS0	

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Table 14. Channel Registers (continued)

Address (Hex)	Bits	Default Value (Hex)	Mode	EEPROM	Field Name	Description
38	7	0	R	N	DFE_STATUS7	Feature is reserved for future use
	6	0	R	N	DFE_STATUS6	
	5	0	R	N	DFE_STATUS5	
	4	0	R	N	DFE_STATUS4	
	3	0	R	N	DFE_STATUS3	
	2	0	R	N	DFE_STATUS2	
	1	0	R	N	DFE_STATUS1	
	0	0	R	N	DFE_STATUS0	
39	7	0	RW	N	RESERVED	
	6	0	RW	Y	EOM_RATE1	With eom_ov=1, these bits control the Eye Monitor Rate: 11: Use for Full Rate, Fastest 10 : Use for 1/2 Rate 01: Use for 1/4 Rate 00: Use for 1/8 Rate, Slowest
	5	0	RW	Y	EOM_RATE0	
	4	0	RW	Y	START_INDEX4	Start index for EQ adaptation
	3	0	RW	Y	START_INDEX3	
	2	0	RW	Y	START_INDEX2	
	1	0	RW	Y	START_INDEX1	
	0	0	RW	Y	START_INDEX0	
3A	7	1	RW	Y	FIXED_EQ_BST0[1]	During adaptation, if the divider setting is >2, then a fixed EQ setting from this register will be used. However, if channel register 0x6F[7] is enabled, then an EQ adaptation will be performed instead
	6	0	RW	Y	FIXED_EQ_BST0[0]	
	5	1	RW	Y	FIXED_EQ_BST1[1]	
	4	0	RW	Y	FIXED_EQ_BST1[0]	
	3	0	RW	Y	FIXED_EQ_BST2[1]	
	2	1	RW	Y	FIXED_EQ_BST2[0]	
	1	0	RW	Y	FIXED_EQ_BST3[1]	
	0	1	RW		FIXED_EQ_BST3[0]	
3B	7	0	R	N	RESERVED	
	6	0	R	N	RESERVED	
	5	0	R	N	RESERVED	
	4	0	R	N	RESERVED	
	3	0	R	N	RESERVED	
	2	0	R	N	RESERVED	
	1	0	R	N	RESERVED	
	0	0	R	N	RESERVED	
3C	7	0	R	N	RESERVED	
	6	0	R	N	RESERVED	
	5	0	R	N	RESERVED	
	4	0	R	N	RESERVED	
	3	0	R	N	RESERVED	
	2	0	R	N	RESERVED	
	1	0	R	N	RESERVED	
	0	0	R	N	RESERVED	

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Table 14. Channel Registers (continued)

Address (Hex)	Bits	Default Value (Hex)	Mode	EEPROM	Field Name	Description
3D	7	0	RW	Y	RESERVED	
	6	0	RW	Y	RESERVED	
	5	0	RW	Y	RESERVED	
	4	0	RW	Y	RESERVED	
	3	0	RW	Y	RESERVED	
	2	0	RW	Y	RESERVED	
	1	0	RW	Y	RESERVED	
	0	0	RW	Y	RESERVED	
3E	7	1	RW	Y	HEO_VEO_LOCKMON_EN	Enable HEO/VEO lock monitoring.
	6	0	RW	Y	RESERVED	
	5	0	RW	Y	RESERVED	
	4	0	RW	Y	RESERVED	
	3	0	RW	Y	RESERVED	
	2	0	RW	Y	RESERVED	
	1	0	RW	Y	RESERVED	
	0	0	RW	Y	RESERVED	
3F	7	0	RW	Y	RESERVED	
	6	0	RW	Y	RESERVED	
	5	0	RW	Y	RESERVED	
	4	0	RW	Y	RESERVED	
	3	0	RW	Y	RESERVED	
	2	0	RW	Y	RESERVED	
	1	0	RW	Y	RESERVED	
	0	0	RW	Y	RESERVED	
40-5F	CTLE Settings for adaption – see Table 11					
60	7	0	RW	Y	GRP0_OV_CNT7	Group 0 count LSB
	6	0	RW	Y	GRP0_OV_CNT6	
	5	0	RW	Y	GRP0_OV_CNT5	
	4	0	RW	Y	GRP0_OV_CNT4	
	3	0	RW	Y	GRP0_OV_CNT3	
	2	0	RW	Y	GRP0_OV_CNT2	
	1	0	RW	Y	GRP0_OV_CNT1	
	0	0	RW	Y	GRP0_OV_CNT0	
61	7	0	RW	Y	CNT_DLTA_OV_0	Override enable for group 0 manual data rate selection
	6	0	RW	Y	GRP0_OV_CNT14	Group 0 count MSB
	5	0	RW	Y	GRP0_OV_CNT13	
	4	0	RW	Y	GRP0_OV_CNT12	
	3	0	RW	Y	GRP0_OV_CNT11	
	2	0	RW	Y	GRP0_OV_CNT10	
	1	0	RW	Y	GRP0_OV_CNT9	
	0	0	RW	Y	GRP0_OV_CNT8	
62	7	0	RW	Y	GRP1_OV_CNT7	Group 1 count LSB
	6	0	RW	Y	GRP1_OV_CNT6	
	5	0	RW	Y	GRP1_OV_CNT5	
	4	0	RW	Y	GRP1_OV_CNT4	
	3	0	RW	Y	GRP1_OV_CNT3	
	2	0	RW	Y	GRP1_OV_CNT2	
	1	0	RW	Y	GRP1_OV_CNT1	
	0	0	RW	Y	GRP1_OV_CNT0	

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Table 14. Channel Registers (continued)

Address (Hex)	Bits	Default Value (Hex)	Mode	EEPROM	Field Name	Description
63	7	0	RW	Y	CNT_DLTA_OV_1	Override enable for group 1 manual data rate selection
	6	0	RW	Y	GRP1_OV_CNT14	Group 1 count MSB
	5	0	RW	Y	GRP1_OV_CNT13	
	4	0	RW	Y	GRP1_OV_CNT12	
	3	0	RW	Y	GRP1_OV_CNT11	
	2	0	RW	Y	GRP1_OV_CNT10	
	1	0	RW	Y	GRP1_OV_CNT9	
	0	0	RW	Y	GRP1_OV_CNT8	
64	7	0	RW	Y	GRP0_OV_DLTA3	Sets the PPM delta tolerance for the PPM counter lock check for group 0. Must also program channel register 0x67[7].
	6	0	RW	Y	GRP0_OV_DLTA2	
	5	0	RW	Y	GRP0_OV_DLTA1	
	4	0	RW	Y	GRP0_OV_DLTA0	
	3	0	RW	Y	GRP1_OV_DLTA3	Sets the PPM delta tolerance for the PPM counter lock check for group 1. Must also program channel register 0x67[6].
	2	0	RW	Y	GRP1_OV_DLTA2	
	1	0	RW	Y	GRP1_OV_DLTA1	
	0	0	RW	Y	GRP1_OV_DLTA0	
65	7:0	0	RW	N	RESERVED	
66	7:0	0	RW	N	RESERVED	
67	7:0	0x20	RW	Y	RESERVED	
68	7:0	0	RW	N	RESERVED	
69	7:5	0	RW	N	RESERVED	
	4	0	RW	N	CTLE_ADPT_FRC_EN	This feature is reserved for future use.
	3	1	RW	Y	HV_LCKMON_CNT_MS3	
	2	0	RW	Y	HV_LCKMON_CNT_MS2	
	1	1	RW	Y	HV_LCKMON_CNT_MS1	
	0	0	RW	Y	HV_LCKMON_CNT_MS0	
6A	7	0	RW	Y	VEO_LCK_THRSH3	VEO threshold to meet before lock is established. The LSB step size is 4 counts of VEO.
	6	0	RW	Y	VEO_LCK_THRSH2	
	5	1	RW	Y	VEO_LCK_THRSH1	
	4	0	RW	Y	VEO_LCK_THRSH0	
	3	0	RW	Y	HEO_LCK_THRSH3	HEO threshold to meet before lock is established. The LSB step size is 4 counts of VEO.
	2	0	RW	Y	HEO_LCK_THRSH2	
	1	1	RW	Y	HEO_LCK_THRSH1	
	0	0	RW	Y	HEO_LCK_THRSH0	
6B	7	0	RW	Y	FOM_A7	Alternate Figure of Merit variable A. Max value for this register is 128, do not use the MSB
	6	1	RW	Y	FOM_A6	
	5	0	RW	Y	FOM_A5	
	4	0	RW	Y	FOM_A4	
	3	0	RW	Y	FOM_A3	
	2	0	RW	Y	FOM_A2	
	1	0	RW	Y	FOM_A1	
	0	0	RW	Y	FOM_A0	
6C	7	0	RW	Y	FOM_B7	HEO adjustment for Alternate FoM, variable B
	6	1	RW	Y	FOM_B6	
	5	0	RW	Y	FOM_B5	
	4	0	RW	Y	FOM_B4	
	3	0	RW	Y	FOM_B3	
	2	0	RW	Y	FOM_B2	
	1	0	RW	Y	FOM_B1	
	0	0	RW	Y	FOM_B0	

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Table 14. Channel Registers (continued)

Address (Hex)	Bits	Default Value (Hex)	Mode	EEPROM	Field Name	Description
6D	7	0	RW	Y	FOM_C7	VEO adjustment for Alternate FoM, variable C
	6	1	RW	Y	FOM_C6	
	5	0	RW	Y	FOM_C5	
	4	0	RW	Y	FOM_C4	
	3	0	RW	Y	FOM_C3	
	2	0	RW	Y	FOM_C2	
	1	0	RW	Y	FOM_C1	
	0	0	RW	Y	FOM_C0	
6E	7	0	RW	Y	EN_NEW_FOM_CTLE	1: CTLE adaption state machine will use the alternate FoM HEO_ALT = (HEO-B)*A*2 VEO_ALT = (VEO-C)*(1-A)*2 The values of A,B,C are set in channel register 0x6B, 0x6C, and 0x6D. The value of A is equal to the register value divided by 128. The Alternate FoM = (HEOB)* A*2 + (VEO-C)*(1-A)*2
	6	0	RW	Y	EN_NEW_FOM_DFE	1: DFE adaption state machine will use the alternate FoM HEO_ALT = (HEO-B)*A*2 VEO_ALT = (VEO-C)*(1-A)*2 The values of A,B,C are set in channel register 0x6B, 0x6C, and 0x6D. The value of A is equal to the register value divided by 128 The Alternate FoM = (HEOB)*A*2 + (VEO-C)*(1-A)*2
	5:1	0	RW	N	RESERVED	
	0	0	RW	N	GET_HV_ST_FRC_EN	This feature is reserved for future use.
6F	705	0	RW	Y	RESERVED	
	4:0	0	RW	N	RESERVED	
70	7:4	0	RW	N	RESERVED	
	3	0	RW	N	RESERVED	
	2	0	RW	Y	EQ_LB_CNT2	CTLE look beyond count for adaption
	1	1	RW	Y	EQ_LB_CNT1	
	0	1	RW	Y	EQ_LB_CNT0	
71	7:6	0	RW	N	RESERVED	
	5	0	R	N	DFE_POL_1_OBS	Primary observation point for DFE tap 1 polarity
	4	0	R	N	DFE_WT1_OBS4	Primary observation point for DFE tap 1 weight
	3	0	R	N	DFE_WT1_OBS3	
	2	0	R	N	DFE_WT1_OBS2	
	1	0	R	N	DFE_WT1_OBS1	
	0	0	R	N	DFE_WT1_OBS0	
72	7:5	0	RW	N	RESERVED	
	4	0	R	N	DFE_POL_2_OBS	Primary observation point for DFE tap 2 polarity
	3	0	R	N	DFE_WT2_OBS3	Primary observation point for DFE tap 2 weight
	2	0	R	N	DFE_WT2_OBS2	
	1	0	R	N	DFE_WT2_OBS1	
	0	0	R	N	DFE_WT2_OBS0	
73	7:5	0	RW	N	RESERVED	
	4	0	R	N	DFE_POL_3_OBS	Primary observation point for DFE tap 3 polarity
	3	0	R	N	DFE_WT3_OBS3	Primary observation point for DFE tap 3 weight
	2	0	R	N	DFE_WT3_OBS2	
	1	0	R	N	DFE_WT3_OBS1	
	0	0	R	N	DFE_WT3_OBS0	

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Table 14. Channel Registers (continued)

Address (Hex)	Bits	Default Value (Hex)	Mode	EEPROM	Field Name	Description
74	7:5	0	RW	N	RESERVED	
	4	0	R	N	DFE_POL_4_OBS	Primary observation point for DFE tap 4 polarity
	3	0	R	N	DFE_WT4_OBS3	Primary observation point for DFE tap 4 weight
	2	0	R	N	DFE_WT4_OBS2	
	1	0	R	N	DFE_WT4_OBS1	
	0	0	R	N	DFE_WT4_OBS0	
75	7:5	0	RW	N	RESERVED	
	4	0	R	N	DFE_POL_5_OBS	Primary observation point for DFE tap 5 polarity
	3	0	R	N	DFE_WT5_OBS3	Primary observation point for DFE tap 5 weight
	2	0	R	N	DFE_WT5_OBS2	
	1	0	R	N	DFE_WT5_OBS1	
	0	0	R	N	DFE_WT5_OBS0	

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DS100DF410 can be configured by the user to optimize its operation. The four channels can be optimized independently in SMBus master or SMBus slave mode. The operational settings available for user configuration include the following.

- CTLE boost setting
- DFE tap weight and polarity setting
- Driver output voltage
- Driver output de-emphasis
- Driver output rise/fall time

Configuration of the DS100DF410 is accomplished by writing the appropriate values into various device registers over the SMBus. This can either be done while the device is operating or upon initial power-up. When the DS100DF410 is operating it behaves like an SMBus slave device, and its register contents can be read or written over the SMBus. Optionally, when the DS100DF410 first powers up, it can behave like an SMBus master and read its register contents autonomously from an external EEPROM.

8.2 Typical Application

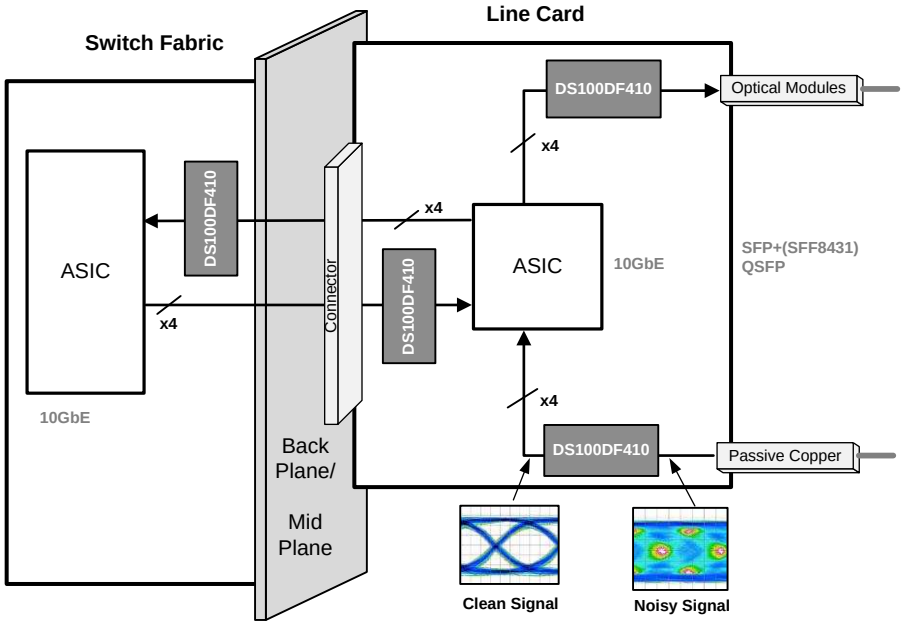

Figure 6. Typical Application Diagram

Typical Application (continued)

8.2.1 Design Requirements

This section lists some critical areas for high speed printed circuit board design consideration and study.

- Utilize 100-Ω differential impedance traces.
- Back-drill connector vias and signal vias to minimize stub length.
- Use reference plane vias to ensure a low inductance path for the return current.
- Place AC-Coupling capacitors for the transmitter links near the receiver for that channel.
- The maximum body size for AC-coupling capacitors is 0402.

8.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Maximum power draw for PCB regulator selection. For this calculation use the maximum transient power supply current specified in the datasheet. The lock time for each channel is typically very short, so this power calculation should not be used for the thermal simulations of the PCB.
- Maximum operational power for thermal calculations. For this calculation use the Average Power Consumption number in the datasheet.
- Select a reference clock frequency and routing scheme.
- Plan out channel connectivity. Be sure to note any desired polarity inversion routing in the board schematics.
- Ensure that each device has a unique SMBus address if the control bus is shared with other devices or components.
- Use the IBIS-AMI model for simple channel simulations before PCB layout is complete.

8.2.3 Application Curves

Figure 7 shows a typical output eye diagram for the DS100DF410 operating at 10.3125 Gbps with default VOD of 600mVp-p and de-emphasis setting of -2dB.

Figure 8 shows an example of Tx de-emphasis for a DS100DF410 operating at 10.3125 Gbps. In this example, the high speed output is configured for 600mVp-p VOD and de-emphasis is set to -4.5dB. An 8T pattern is used to evaluate the driver, which consists of 0xFF00.

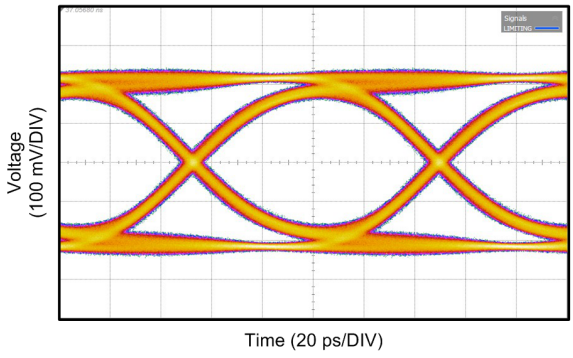

Figure 7. Typical Application Transmit Eye Diagram, 10.3125 Gbps

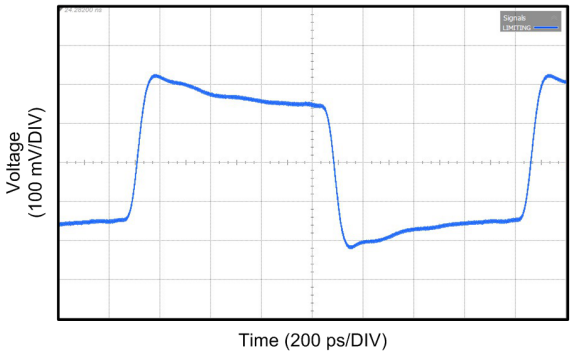

Figure 8. Transmit Equalization Example, 10.3125Gbps

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9 Power Supply Recommendations

Figure 9 depicts an example power connections diagram for the DS100DF410. The supply (VDD) and ground (GND) Pins should be connected to power planes routed on adjacent layers of the printed circuit board. The layer thickness of the dielectric should be minimized so that the VDD and GND planes create a low inductance supply with distributed capacitance. Second, careful attention to supply bypassing through the proper use of bypass capacitors is required. A 0.1-µF bypass capacitor should be connected to each VDD Pin such that the capacitor is placed as close as possible to the DS100DF410. Smaller body size capacitors can help facilitate proper component placement. Additionally, capacitor with capacitance in the range of 1 µF to 10 µF should be incorporated in the power supply bypassing design as well. These capacitors can be either tantalum or an ultra-low ESR ceramic.

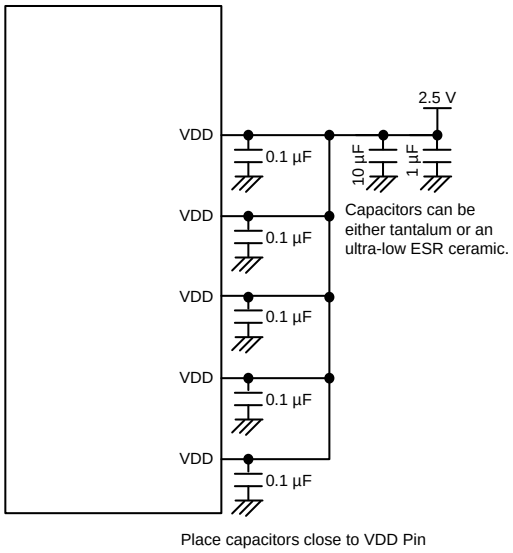

Figure 9. Example Power Connection

10 Layout

10.1 Layout Guidelines

The CML inputs and outputs have been optimized to work with interconnects using a controlled differential impedance of 100 Ω. It is preferable to route differential lines exclusively on one layer of the board, particularly for the input traces. The use of vias should be avoided if possible. If vias must be used, they should be used sparingly and must be placed symmetrically for each side of a given differential pair. Whenever differential vias are used the layout must also provide for a low inductance path for the return currents as well. Route the differential signals away from other signals and noise sources on the printed circuit board. See AN-1187 *Leadless Leadframe Package (LLP) Application Report* (SNOA401) for additional information on QFN (WQFN) packages.

10.2 Layout Example

To minimize the effects of crosstalk, a 5:1 ratio or greater should be maintained between inter-pair spacing.

Figure 10 depicts different transmission line topologies which can be used in various combinations to achieve the optimal system performance. Impedance discontinuities at the differential via can be minimized or eliminated by increasing the swell around each hole and providing for a low inductance return current path. When the via structure is associated with thick backplane PCB, further optimization such as back drilling is often used to reduce the detrimental high frequency effects of stubs on the signal path.

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Layout Example (continued)

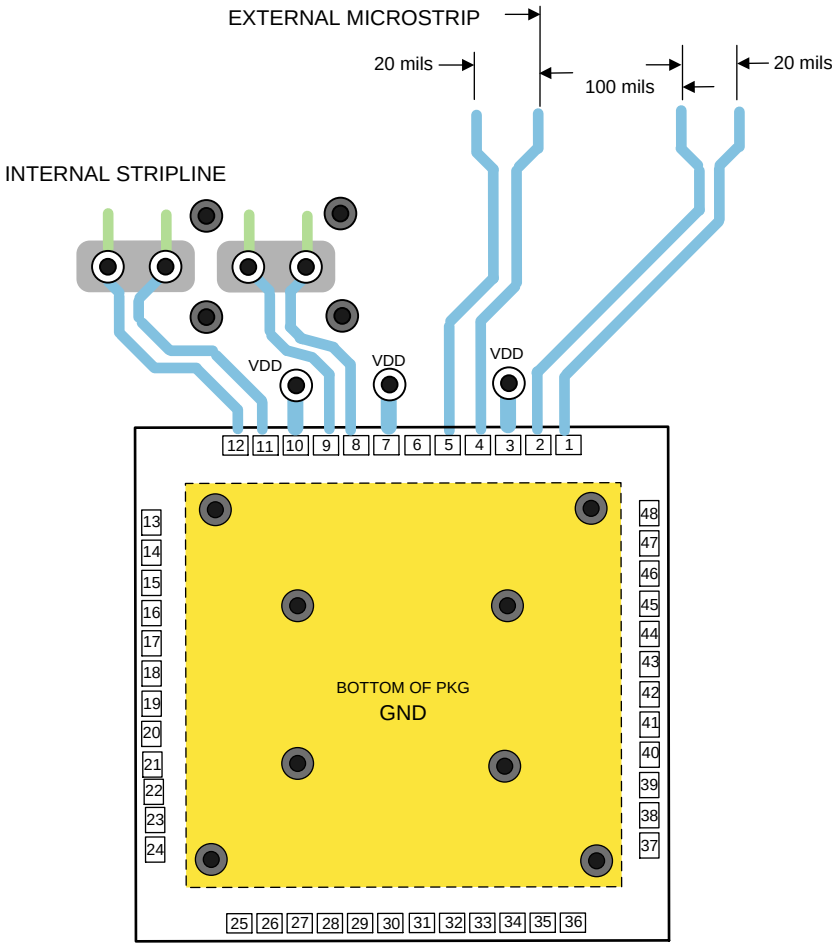

Figure 10. Different Transmission Line Topologies

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11 Device and Documentation Support

11.1 Trademarks

All trademarks are the property of their respective owners.

11.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS100DF410SQ/NOPB	ACTIVE	WQFN	RHS	48	1000	Green (RoHS & no Sb/Br)	SN	Level-3-260C-168 HR	-40 to 85	100DF410	Samples
DS100DF410SQE/NOPB	ACTIVE	WQFN	RHS	48	250	Green (RoHS & no Sb/Br)	SN	Level-3-260C-168 HR	-40 to 85	100DF410	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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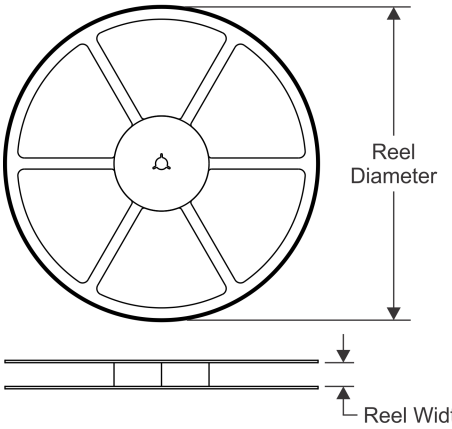
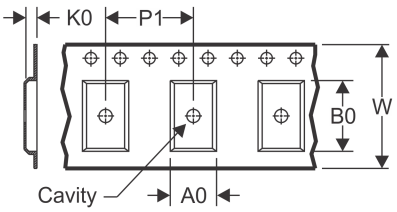
TAPE AND REEL INFORMATION

REEL DIMENSIONS

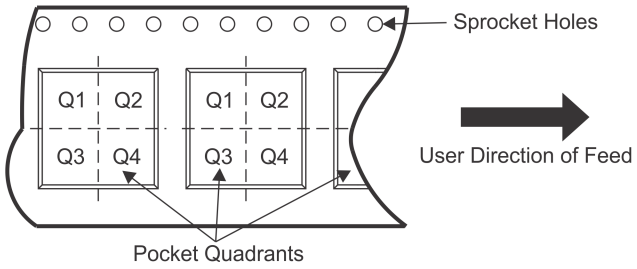


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

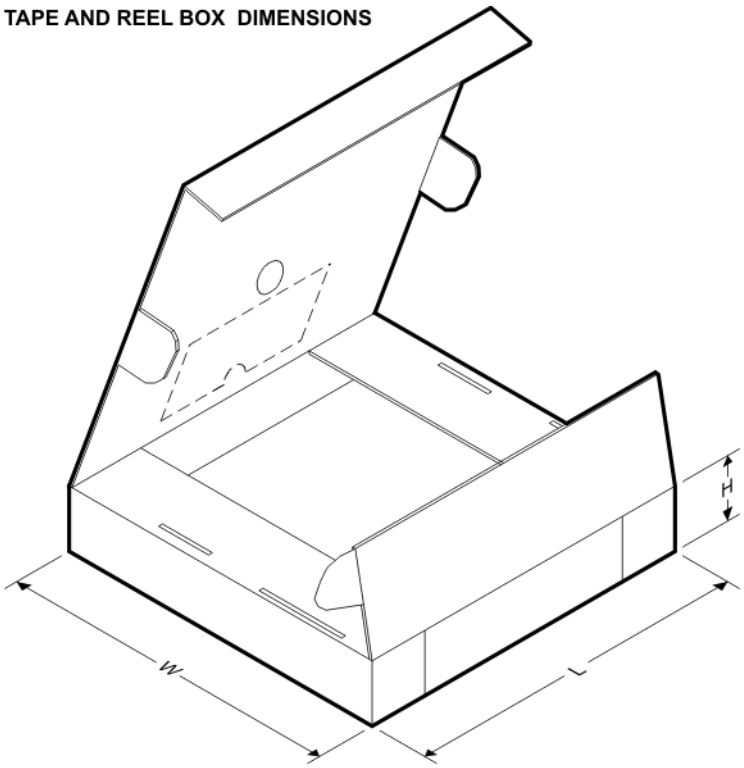
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS100DF410SQ/NOPB	WQFN	RHS	48	1000	330.0	16.4	7.3	7.3	1.3	12.0	16.0	Q1
DS100DF410SQE/NOPB	WQFN	RHS	48	250	178.0	16.4	7.3	7.3	1.3	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

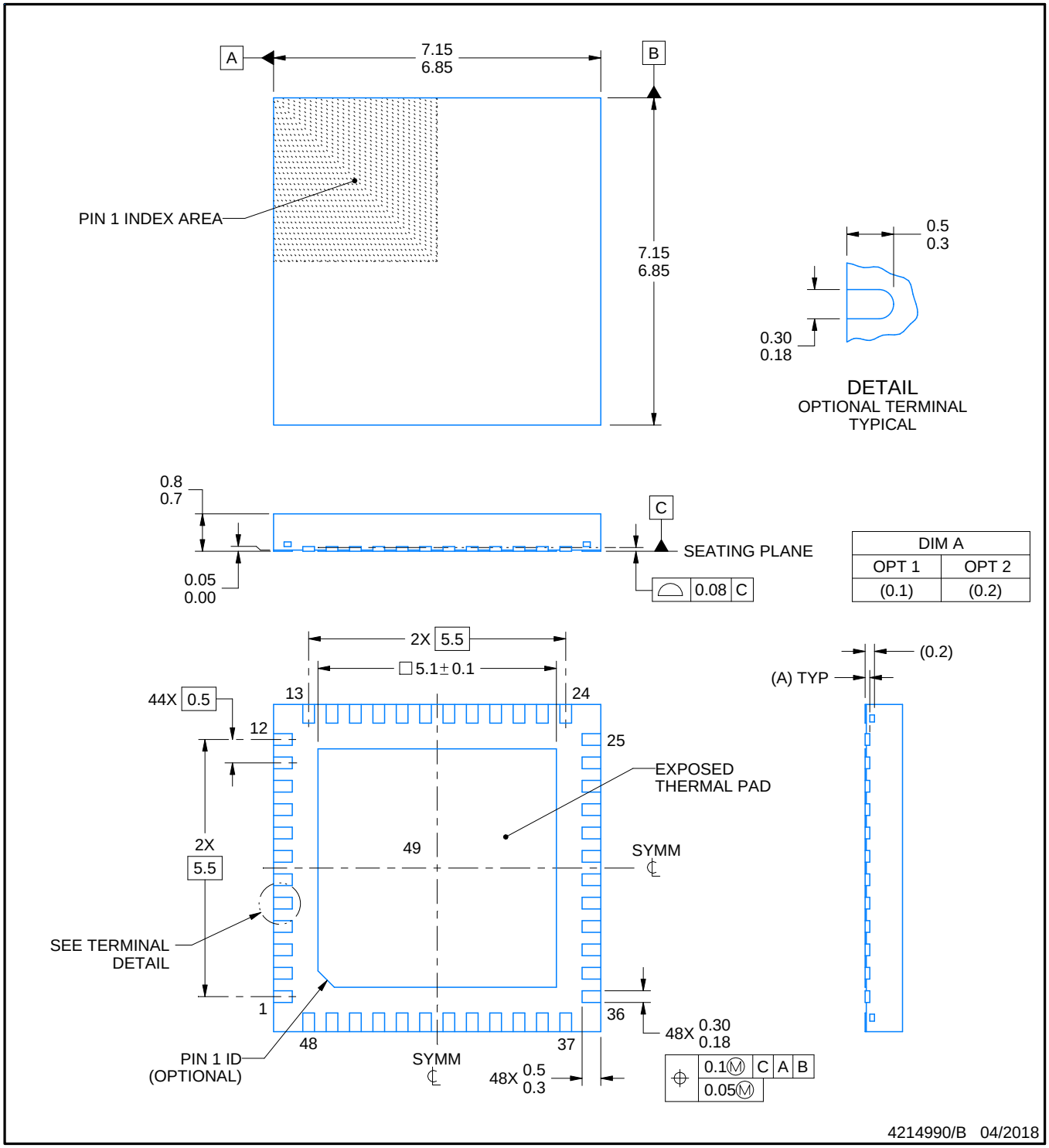
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS100DF410SQ/NOPB	WQFN	RHS	48	1000	367.0	367.0	38.0
DS100DF410SQE/NOPB	WQFN	RHS	48	250	210.0	185.0	35.0

PACKAGE OUTLINE

RHS0048A

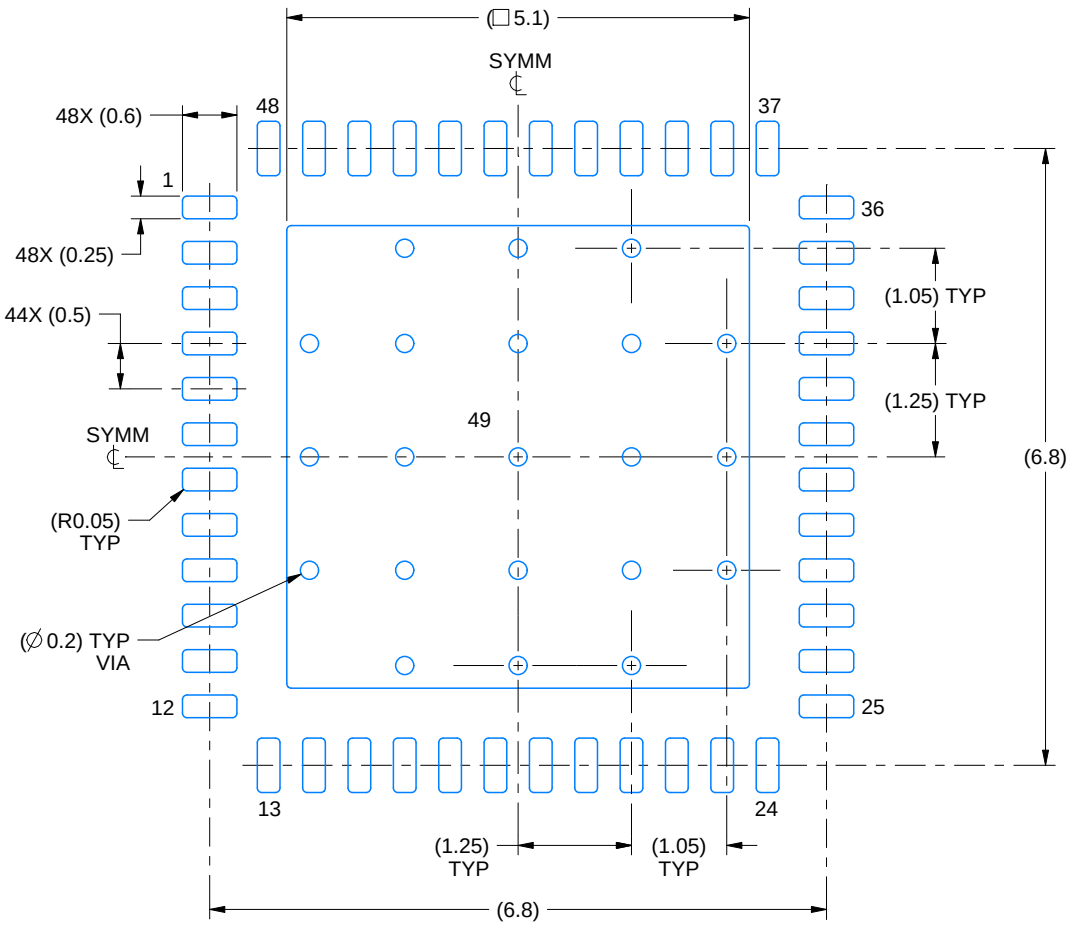
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

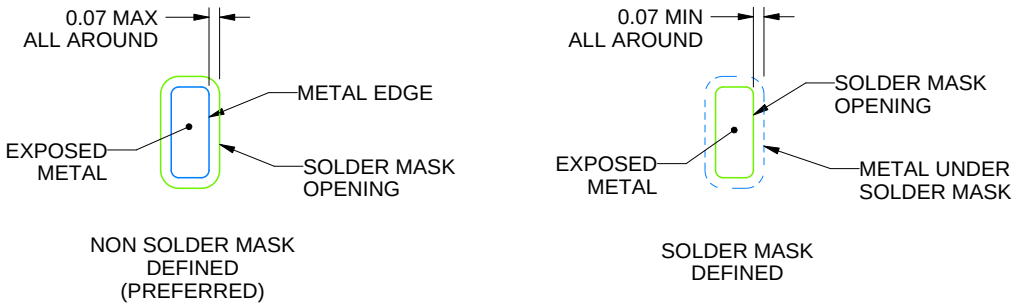


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:12X



SOLDER MASK DETAILS

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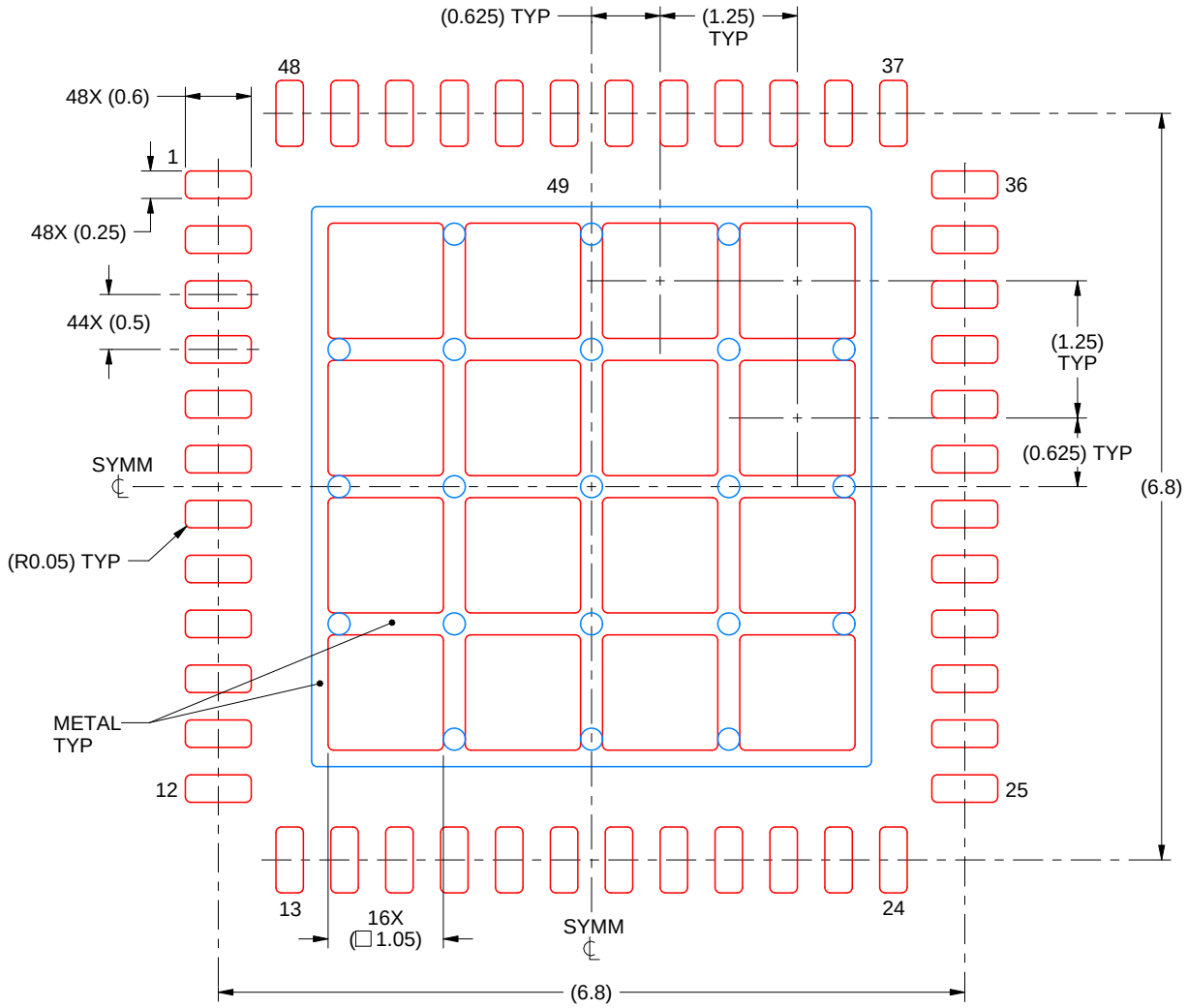
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 49
68% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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