DRV8821 Dual Stepper Motor Controller and Driver

1 Features

- Dual PWM Microstepping Motor Driver
  - Built-In Microstepping Indexers
  - Up to 1.5-A Current Per Winding
  - Three-Bit Winding Current Control Allows up to Eight Current Levels
  - Low MOSFET On-Resistance
  - Selectable Slow or Mixed Decay Modes
- 8-V to 32-V Operating Supply Voltage Range
- Internal Charge Pump for Gate Drive
- Built-in 3.3-V Reference
- Simple Step/Direction Interface
- Fully Protected Against Undervoltage, Overtemperature, and Overcurrent
- Thermally-Enhanced Surface Mount Package

2 Applications

- Printers
- Scanners
- Office Automation Machines
- Gaming Machines
- Factory Automation
- Robotics

3 Description

The DRV8821 provides a dual microstepping-capable stepper motor controller/driver solution for printers, scanners, and other office automation equipment applications.

Two independent stepper motor driver circuits include four H-bridge drivers and microstepping-capable indexer logic. Each of the motor driver blocks employ N-channel power MOSFETs configured as an H-bridge to drive the motor windings.

A simple step/direction interface allows easy interfacing to controller circuits. Pins allow configuration of the motor in full-step, half-step, quarter-step, or eighth step modes, and the selection of slow or mixed decay modes.

Internal shutdown functions are provided for over current protection, short-circuit protection, undervoltage lockout, and overtemperature.

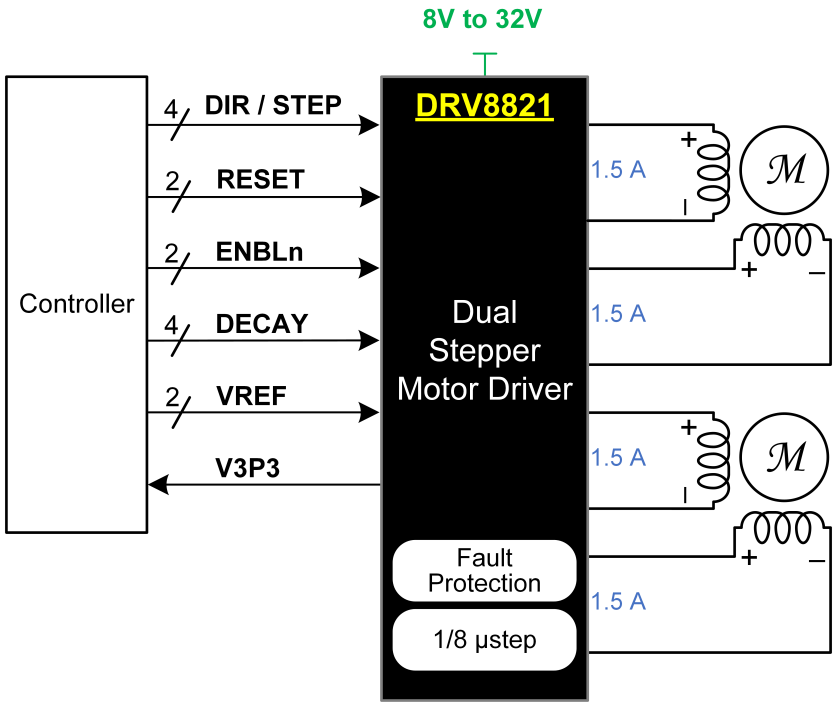
The DRV8821 is packaged in a 48-pin HTSSOP package (Eco-friendly : RoHS & no Sb/Br).

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DRV8821	HTSSOP (48)	6.10 mm x 12.50 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

1 Features ... 1
2 Applications ... 1
3 Description ... 1
4 Revision History ... 2
5 Pin Configuration and Functions ... 3
6 Specifications ... 4
6.1 Absolute Maximum Ratings ... 4
6.2 ESD Ratings ... 4
6.3 Recommended Operating Conditions ... 5
6.4 Thermal Information ... 5
6.5 Electrical Characteristics ... 5
6.6 Timing Requirements ... 6
6.7 Dissipation Ratings ... 6
6.8 Typical Characteristics ... 7
7 Detailed Description ... 9
7.1 Overview ... 9
7.2 Functional Block Diagram ... 10
7.3 Feature Description ... 10
7.4 Device Functional Modes ... 14
8 Application and Implementation ... 16
8.1 Application Information ... 16
8.2 Typical Application ... 16
9 Power Supply Recommendations ... 19
9.1 Bulk Capacitance ... 19
10 Layout ... 20
10.1 Layout Guidelines ... 20
10.2 Layout Example ... 21
10.3 Thermal Considerations ... 22
11 Device and Documentation Support ... 24
11.1 Documentation Support ... 24
11.2 Community Resources ... 24
11.3 Trademarks ... 24
11.4 Electrostatic Discharge Caution ... 24
11.5 Glossary ... 24
12 Mechanical, Packaging, and Orderable Information ... 24

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision I (January 2014) to Revision J **Page**

- Added *Pin Functions* table, *ESD Ratings* table, *Thermal Information* table, *Detailed Description* section, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

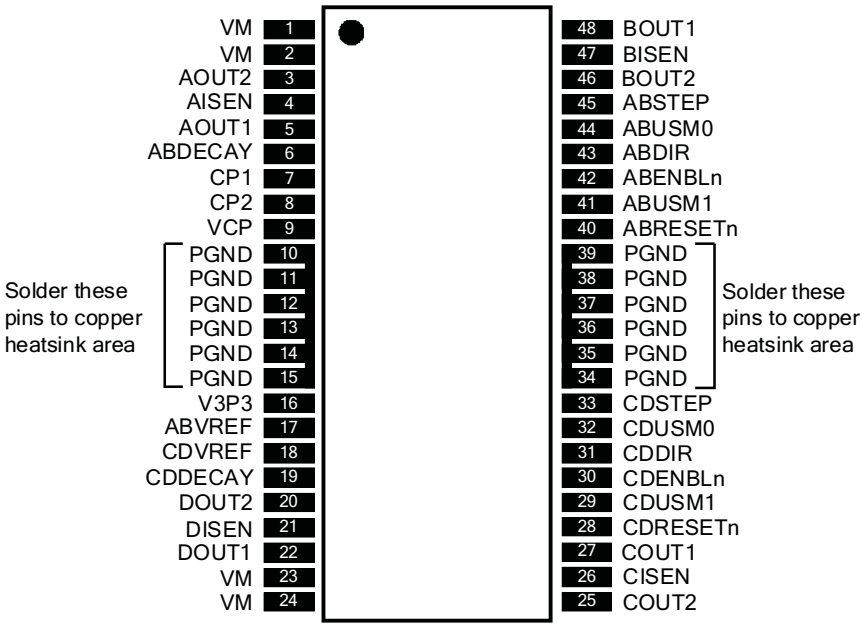
Changes from Revision H (August 2013) to Revision I **Page**

- Changed typo in *Overcurrent Protection* section ... 14

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5 Pin Configuration and Functions

DCA Package
48-Pin HTSSOP
Top View



Pin Functions

PIN		I/O(1)	DESCRIPTION	EXTERNAL COMPONENTS OR CONNECTIONS
NAME	NO.			
POWER AND GROUND				
VM (4 pins)	1,2, 23, 24	—	Motor supply voltage (multiple pins)	Connect all VM pins together to motor supply voltage. Bypass each VM to GND with a 0.1-µF, 35-V ceramic capacitor.
V3P3	16	—	3.3 V regulator output	Bypass to GND with 0.47-µF, 6.3-V ceramic capacitor.
GND	10-15, 34-39	—	Power ground (multiple pins)	Connect all PGND pins to GND and solder to copper heatsink areas.
CP1	7	IO	Charge pump flying capacitor	Connect a 0.01-µF capacitor between CP1 and CP2
CP2	8	IO		
VCP	9	IO	Charge pump storage capacitor	Connect a 0.1-µF, 16 V ceramic capacitor to V_M
MOTOR AB				
ABSTEP	45	I	Motor AB step input	Rising edge causes the indexer to move one step.
ABDIR	43	I	Motor AB direction input	Level sets the direction of stepping.
ABUSM0	44	I	Motor AB microstep mode 0	USM0 and USM1 set the step mode - full step, half step, quarter step, or eight microsteps/step.
ABUSM1	41	I	Motor AB microstep mode 1	
ABENBLn	42	I	Motor AB enable input	Logic high to disable motor AB outputs, logic low to enable.
ABRESETn	40	I	Motor AB reset input	Active-low reset input initializes the indexer logic and disables the H-bridge outputs for motor AB.
ABDECAY	6	I	Motor AB decay mode	Logic low for slow decay mode, high for mixed decay.
ABVREF	17	I	Motor AB current set reference voltage	Sets current trip threshold.
AOUT1	5	O	Bridge A output 1	Connect to first coil of bipolar stepper motor AB, or DC motor winding.
AOUT2	3	O	Bridge A output 2	
AISEN	4	—	Bridge A current sense	Connect to current sense resistor for bridge A.

(1) Directions: i = input, O = output, OZ = 3-state output, OD = open-drain ouput, IO = input/ouput

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Pin Functions (continued)

PIN		I/O[1]	DESCRIPTION	EXTERNAL COMPONENTS OR CONNECTIONS
NAME	NO.			
BOUT1	48	O	Bridge B output 1	Connect to second coil of bipolar stepper motor AB, or DC motor winding.
BOUT2	46	O	Bridge B output 2	
BISEN	47	—	Bridge B current sense	Connect to current sense resistor for bridge B.
MOTOR CD				
CDSTEP	33	I	Motor CD step input	Rising edge causes the indexer to move one step.
CDDIR	31	I	Motor CD direction input	Level sets the direction of stepping.
CDUSM0	32	I	Motor CD microstep mode 0	USM0 and USM1 set the step mode - full step, half step, quarter step, or eight microsteps/step.
CDUSM1	29	I	Motor CD microstep mode 1	
CDENBLn	30	I	Motor CD enable input	Logic high to disable motor CD outputs, logic low to enable.
CDRESETn	28	I	Motor CD reset input	Active-low reset input initializes the indexer logic and disables the H-bridge outputs for motor CD.
CDDECAY	19	I	Motor CD decay mode	Logic low for slow decay mode, high for mixed decay.
CDREF	18	I	Motor CD current set reference voltage	Sets current trip threshold.
COUT1	27	O	Bridge C output 1	Connect to first coil of bipolar stepper motor CD, or DC motor winding.
COUT2	25	O	Bridge C output 2	
CISEN	26	—	Bridge C current sense	Connect to current sense resistor for bridge C.
DOUT1	22	O	Bridge D output 1	Connect to second coil of bipolar stepper motor CD, or DC motor winding.
DOUT2	20	O	Bridge D output 2	
DISEN	21	—	Bridge D current sense	Connect to current sense resistor for bridge D.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1] [2]

		MIN	MAX	UNIT
V_M	Power supply voltage	–0.3	34	V
V_I	Logic input voltage [3]	–0.5	5.75	V
$I_{O(peak)}$	Peak motor drive output current, t < 1 µs	Internally limited		
I_O	Motor drive output current [4]		1.5	A
P_D	Continuous total power dissipation	See *Dissipation Ratings*		
T_J	Operating virtual junction temperature	–40	150	°C
T_A	Operating ambient temperature	–40	85	°C
T_{stg}	Storage temperature	–60	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) Input pins may be driven in this voltage range regardless of presence or absence of V_M.
(4) Power dissipation and thermal limits must be observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins [1]	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins [2]	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_M	Motor power supply voltage	8		32	V
I_{MOT}	Continuous motor drive output current(1)		1	1.5	A
V_{REF}	VREF input voltage	1		4	V

(1) Power dissipation and thermal limits must be observed.

6.4 Thermal Information

THERMAL METRIC(1)		DRV8821 DCA (HTSSOP) 48 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	31.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	16.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	15	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	14.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES						
I_{VM}	V_M operating supply current	V_M = 24 V, no loads		5	8	mA
I_{VMSD}	V_M shutdown supply current	V_M = 24 V, ABENBLn = CDENBLn = 1			2.5	µA
V_{UVLO}	V_M undervoltage lockout voltage	V_M rising		6.5	8	V
V_{CP}	Charge pump voltage	Relative to V_M		12		V
V_{V3P3}	V_{V3P3} output voltage		3.20	3.30	3.40	V
LOGIC-LEVEL INPUTS						
V_{IL}	Input low voltage				0.7	V
V_{IH}	Input high voltage		2			V
V_{HYS}	Input hysteresis		0.3	0.45	0.6	V
I_{IN}	Input current (internal pulldown current)	VIN = 3.3 V			100	µA
OVERTEMPERATURE PROTECTION						
t_{TSD}	Thermal shutdown temperature	Die temperature	150			°C
MOTOR DRIVER						
$R_{ds(on)}$	Motor AB FET on resistance (each individual FET)	V_M = 24 V, I_O = 0.8 A, T_J = 25°C		0.25		Ω
		V_M = 24 V, I_O = 0.8 A, T_J = 85°C		0.31	0.37	
$R_{ds(on)}$	Motor CD FET on resistance (each individual FET)	V_M = 24 V, I_O = 0.8 A, T_J = 25°C		0.30		Ω
		V_M = 24 V, I_O = 0.8 A, T_J = 85°C		0.38	0.45	
I_{OFF}	Off-state leakage current				±12	µA
f_{PWM}	Motor PWM frequency(1)		45	50	55	kHz
t_{BLANK}	ITRIP blanking time(2)			3.75		µs
t_F	Output fall time		50		300	ns
t_R	Output rise time		50		300	ns

(1) Factory option 100 kHz.
(2) Factory options for 2.5 µs, 5 µs or 6.25 µs.

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Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{OCP}	Overcurrent protect level		1.5	3	4.5	A
t_{OCP}	Overcurrent protect trip time		2.5			µs
t_{MD}	Mixed decay percentage	Measured from beginning of PWM cycle		75%		
VREF INPUT/CURRENT CONTROL ACCURACY						
I_{REF}	xVREF input current	xVREF = 3.3 V	–3		3	µA
ΔI_{CHOP}	Chopping current accuracy	xVREF = 2.5 V, derived from V3P3; 71% to 100% current	–5%		5%	
		xVREF = 2.5 V, derived from V3P3; 20% to 56% current	–10%		10%	

6.6 Timing Requirements

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
1	f_{STEP}	Step frequency		200	kHz
2	$t_{WH(STEP)}$	Pulse duration, xSTEP high	2.5		µs
3	$t_{WL(STEP)}$	Pulse duration, xSTEP low	2.5		µs
4	$t_{SU(STEP)}$	Setup time, command to xSTEP rising	200		ns
5	$t_{H(STEP)}$	Hold time, command to xSTEP rising	200		ns
6	t_{WAKE}	Wakeup time, SLEEPn inactive to xSTEP	1		ms

6.7 Dissipation Ratings

BOARD	PACKAGE	$R_{\theta JA}$	DERATING FACTOR ABOVE T_A = 25°C	T_A < 25°C	T_A = 70°C	T_A = 85°C
Low-K(1)	DCA	75.7°C/W	13.2 mW/°C	1.65 W	1.06 W	0.86 W
Low-K(2)		32°C/W	31.3 mW/°C	3.91 W	2.50 W	2.03 W
High-K(3)		30.3°C/W	33 mW/°C	4.13 W	2.48 W	2.15 W
High-K(4)		22.3°C/W	44.8 mW/°C	5.61 W	3.59 W	2.91 W

(1) The JEDEC Low-K board used to derive this data was a 76-mm x 114-mm, 2-layer, 1.6-mm thick PCB with no backside copper.
(2) The JEDEC Low-K board used to derive this data was a 76-mm x 114-mm, 2-layer, 1.6-mm thick PCB with 25-cm^2 2-oz copper on back side.
(3) The JEDEC High-K board used to derive this data was a 76-mm x 114-mm, 4-layer, 1.6-mm thick PCB with no backside copper and solid 1-oz internal ground plane.
(4) The JEDEC High-K board used to derive this data was a 76-mm x 114-mm, 4-layer, 1.6-mm thick PCB with 25-cm^2 1-oz copper on back side and solid 1-oz internal ground plane.

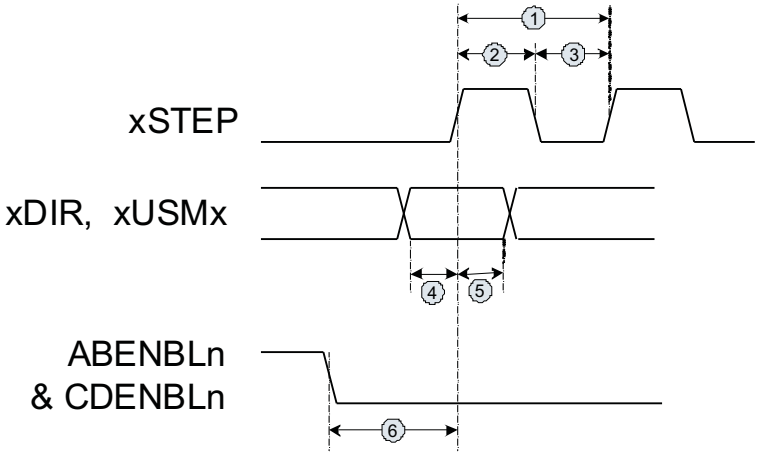


Figure 1. Timing Diagram

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6.8 Typical Characteristics

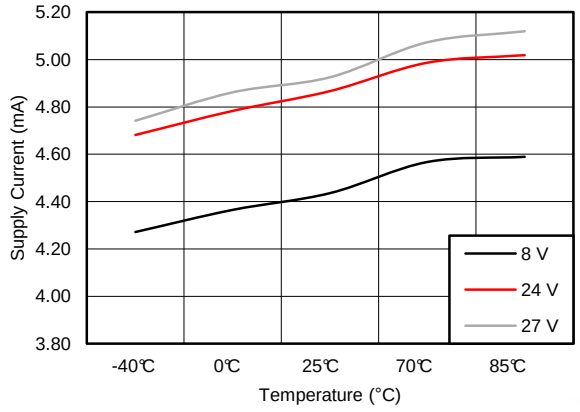


Figure 2. Supply Current over Temperature

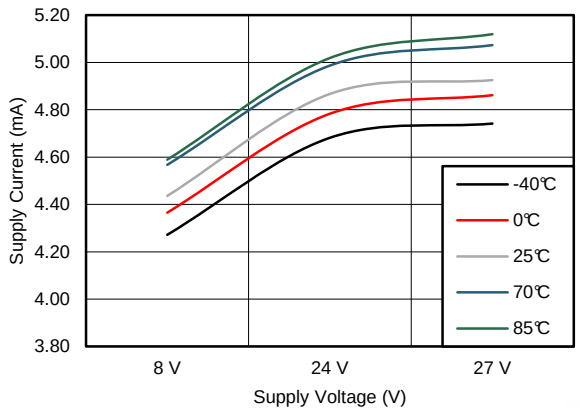


Figure 3. Supply Current over Supply Voltage

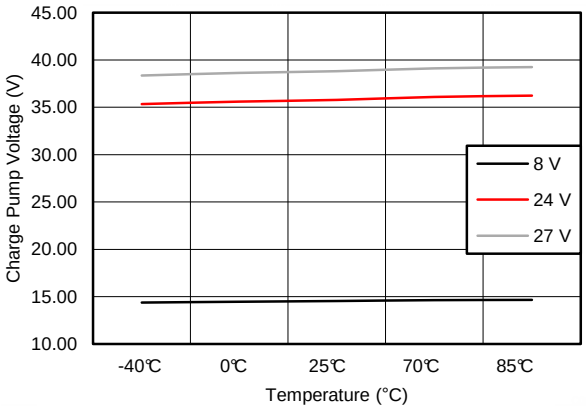


Figure 4. Charge Pump Voltage over Temperature

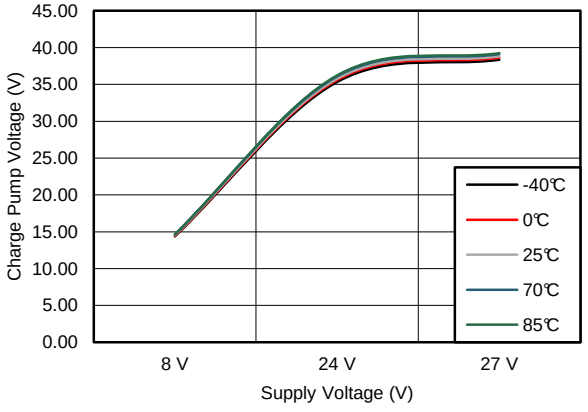


Figure 5. Charge Pump Voltage over Supply Voltage

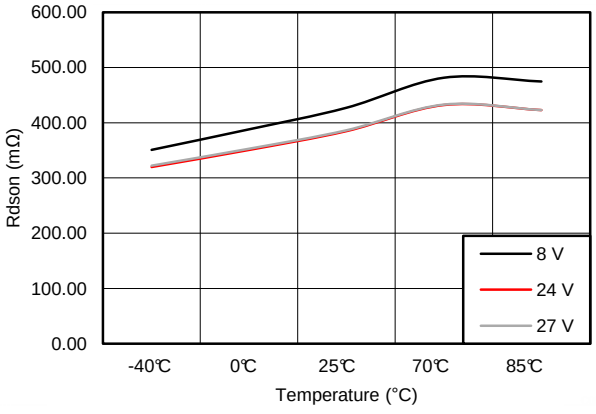


Figure 6. LS R_{DSON} A_{OUT2} over Temperature

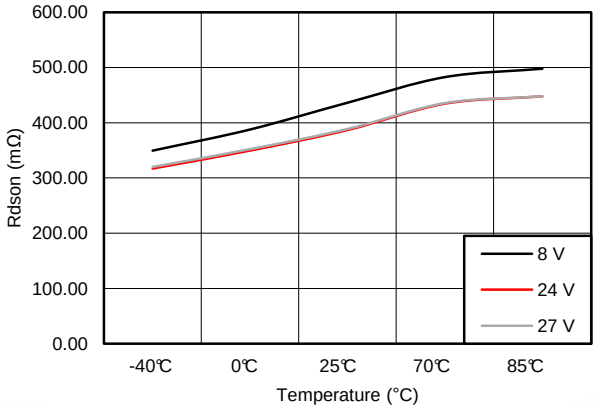


Figure 7. LS R_{DSON} A $_{OUT1}$over Temperature

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Typical Characteristics (continued)

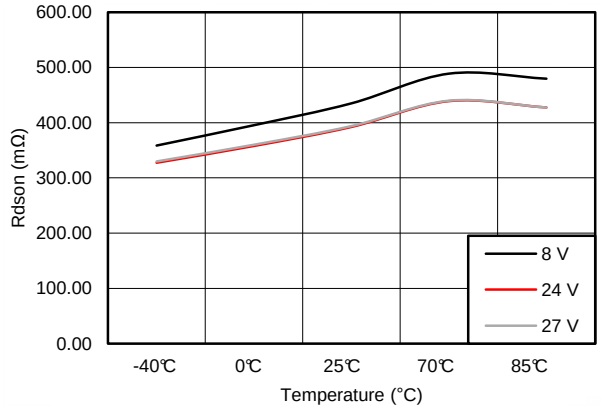


Figure 8. HS R_{DSON} A_{OUT2} over Temperature

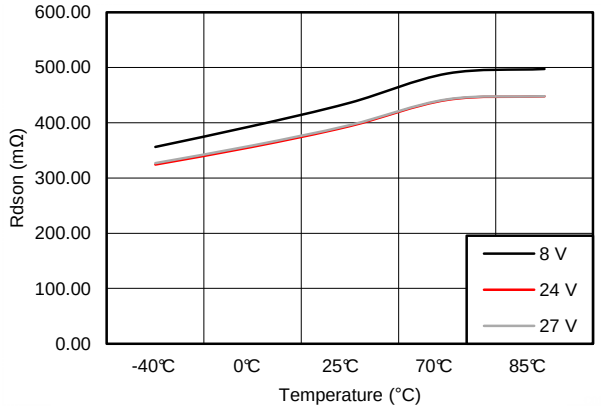


Figure 9. HS R_{DSON} A_{OUT1} over Temperature

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7 Detailed Description

7.1 Overview

The DRV8821 is a dual stepper motor driver solution for applications that require independent control of two different motors. The device integrates four NMOS H-bridges, a microstepping indexer, and various fault protection features. The DRV8821 can be powered with a supply voltage between 8 and 32 V, and is capable of providing an output current up to 1.5-A full scale. Actual full-scale current will depend on ambient temperature, supply voltage, and PCB ground size.

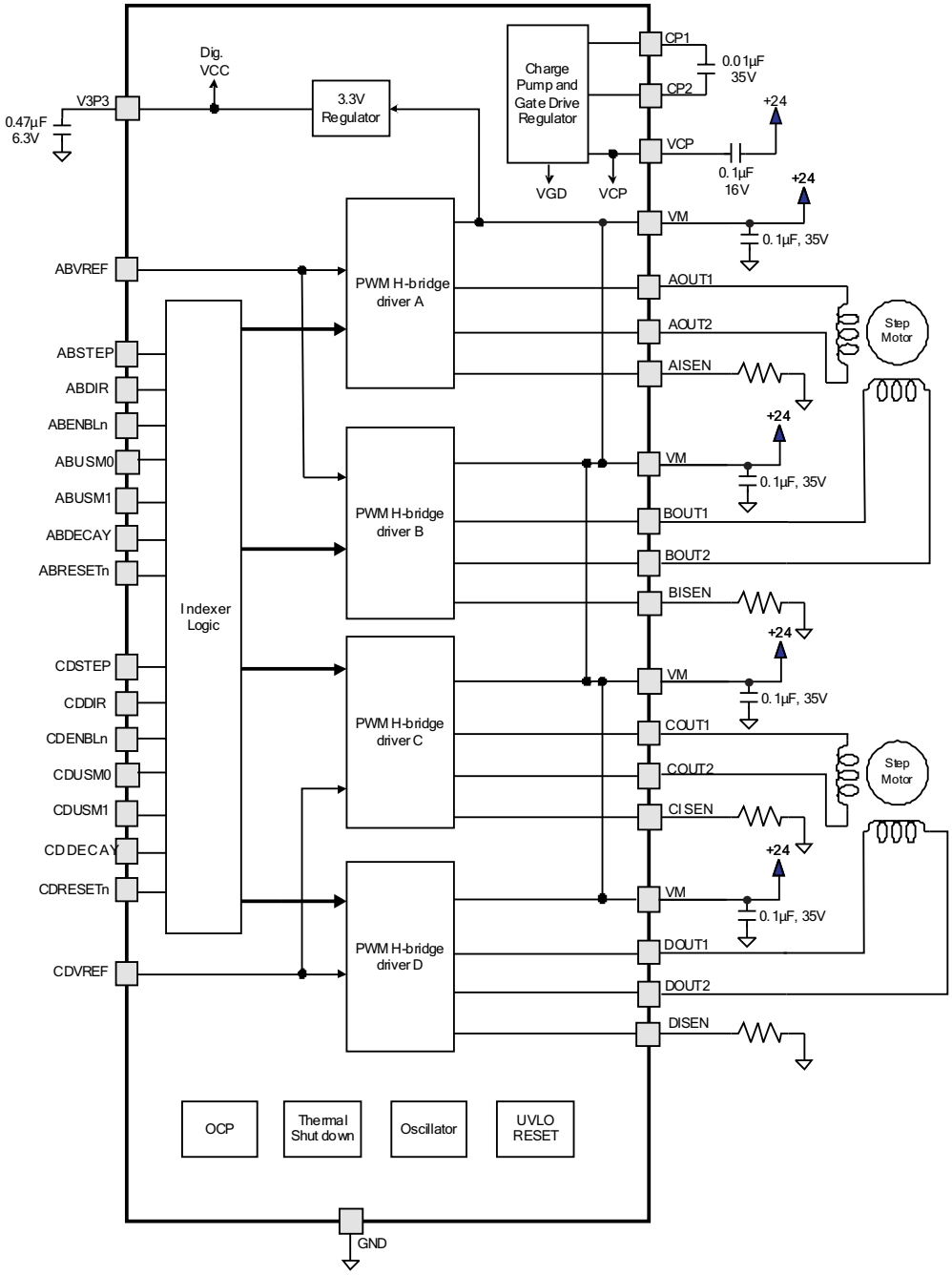
A simple STEP/DIR interface allows easy interfacing to the controller circuit. The internal indexer is able to execute high-accuracy microstepping without requiring the processor to control the current level. The indexer is cable of full step and half step as well as microstepping to 1/4 and 1/8.

The current regulation is configurable with two different decay modes; slow decay and mixed decay. The mixed decay mode uses slow decay on increasing current steps and mixed decay on decreasing current steps, while slow decay mode will always use slow decay regardless increasing or decreasing steps.

The gate drive to each FET in all four H-Bridges is controlled to prevent any cross-conduction (shoot through current) during transitions.

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7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 PWM Motor Drivers

The DRV8821 contains four H-bridge motor drivers with current-control PWM circuitry. A block diagram showing drivers A and B of the motor control circuitry (as typically used to drive a bipolar stepper motor) is shown below. Drivers C and D are the same as A and B (though the $R_{ds(on)}$ of the output FETs is different).

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Feature Description (continued)

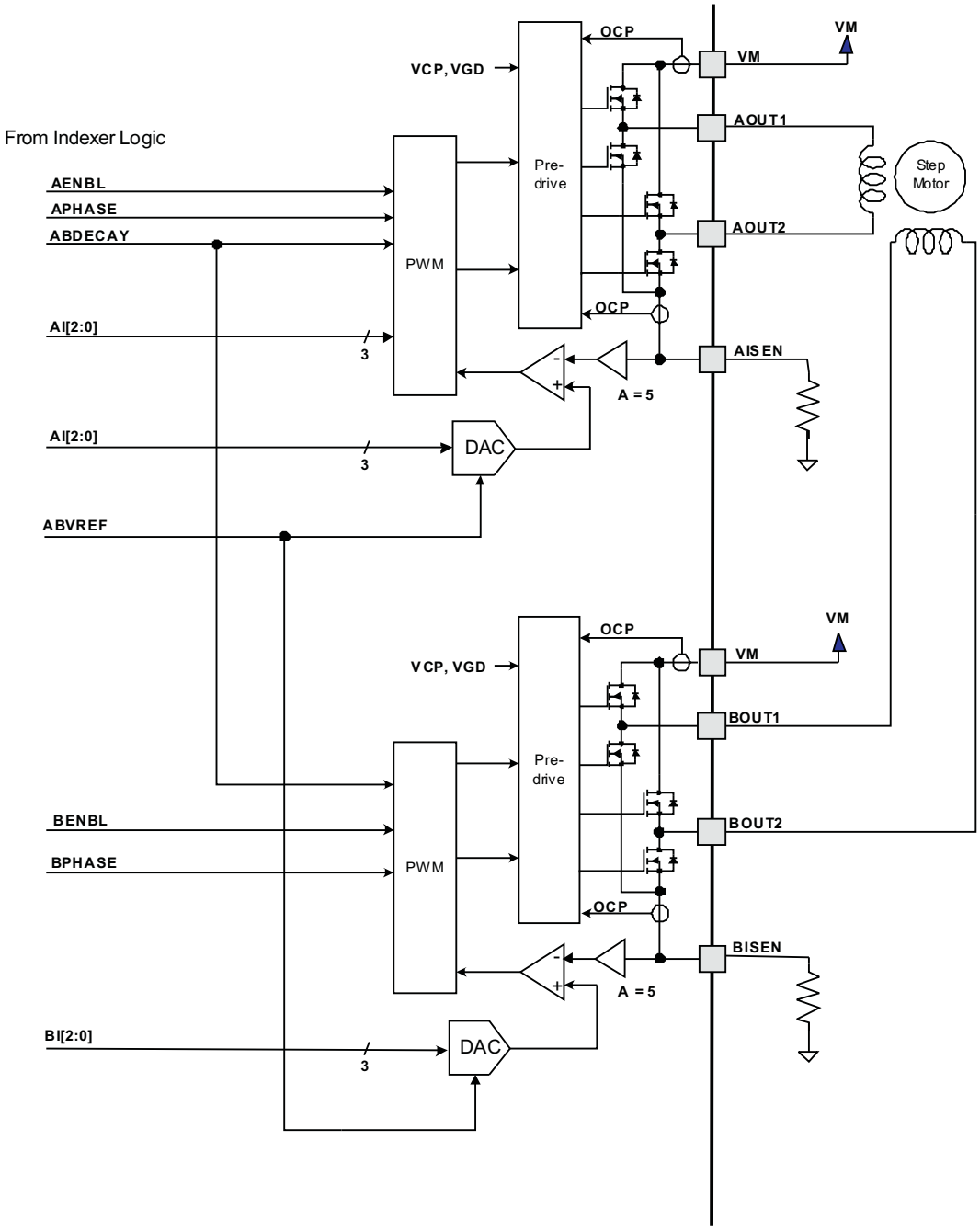


Figure 10. Block Diagram

Note that there are multiple VM motor power supply pins. All VM pins must be connected together to the motor supply voltage.

7.3.2 Current Regulation

The PWM chopping current is set by a comparator which compares the voltage across a current sense resistor connected to the xISEN pins, multiplied by a factor of 5, with a reference voltage. The reference voltage is input from the xVREF pin.

Feature Description (continued)

The full-scale (100%) chopping current is calculated as follows:

$$I_{CHOP} = \frac{V_{REFX}}{5 \bullet R_{ISENSE}} \quad (1)$$

Example:

If a 0.5-Ω sense resistor is used and the VREFx pin is 2.5 V, the full-scale (100%) chopping current is 2.5 V/(5 × 0.5 Ω) = 1 A.

The reference voltage is also scaled by an internal DAC that allows torque control for fractional stepping of a bipolar stepper motor, as described in *Microstepping Indexer*.

7.3.3 Blanking Time

After the current is enabled in an H-bridge, the voltage on the xISEN pin is ignored for a fixed period of time before enabling the current sense circuitry. This blanking time is fixed at 3.75 µs. Note that the blanking time also sets the minimum on time of the PWM.

7.3.4 Microstepping Indexer

Built-in indexer logic in the DRV8821 allows a number of different stepping configurations. The xUSM1 and xUSM0 pins are used to configure the stepping format as shown in the table below:

Table 1. Microstepping Selection Bits

xUSM1	xUSM0	STEP MODE
0	0	Full step (2-phase excitation)
0	1	½ step (1-2 phase excitation)
1	0	1/4 step (W1-2 phase excitation)
1	1	Eight microsteps/steps

The following table shows the relative current and step directions for different settings of xUSM1 and xUSM0. At each rising edge of the xSTEP input, the indexer travels to the next state in the table. The direction is shown with the DIR pin high; if the xDIR pin is low the sequence is reversed. Positive current is defined as xOUT1 = positive with respect to xOUT2.

Note that the home state is 45 degrees. This state is entered at power-up, during sleep mode, or application of xRESETn.

Motor AB and motor CD act independently, and their indexer logic functions identically.

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Table 2. Microstepping Indexer

FULL STEP xUSM = 00	½ STEP xUSM = 01	1/4 STEP xUSM = 10	1/8 STEP xUSM = 11	AOUTx CURRENT (% FULL-SCALE)	BOUTx CURRENT (% FULL-SCALE)	STEP ANGLE (DEGREES)
	1	1	1	100	0	0
			2	98	20	11.25
		2	3	92	38	22.5
			4	83	56	33.75
1	2	3	5	71	71	45 (home state)
			6	56	83	56.25
		4	7	38	92	67.5
			8	20	98	78.75
	3	5	9	0	100	90
			10	–20	98	101.25
		6	11	–38	92	112.5
			12	–56	83	123.75
2	4	7	13	–71	71	135
			14	–83	56	146.25
		8	15	–92	38	157.5
			16	–98	20	168.75
	5	9	17	–100	0	180
			18	–98	–20	191.25
		10	19	–92	–38	202.5
			20	–83	–56	213.75
3	6	11	21	–71	–71	225
			22	–56	–83	236.25
		12	23	–38	–92	247.5
			24	–20	–98	258.75
	7	13	25	0	–100	270
			26	20	–98	281.25
		14	27	38	–92	292.5
			28	56	–83	303.75
4	8	15	29	71	–71	315
			30	83	–56	326.25
		16	31	92	–38	337.5
			32	98	–20	348.75

7.3.5 xRESETn and xENBLn Operation

The xRESETn pin, when driven active low, resets the step table to the home position. It also disables the H-bridge drivers. The xSTEP input is ignored while xRESETn is active. Note that there is a separate xRESETn pin for each motor; each acts only on one of the two motor controllers.

The xENABLEn pin is used to control the output drivers. When xENBLn is low, the output H-bridges are enabled. When xENBLn is high, the H-bridges are disabled and the outputs are in a high-impedance state.. Note that there is a separate xENBLn pin for each motor; each acts only on one of the two motor drivers.

Note that when xENBLn is high, the input pins and control logic, including the indexer (xSTEP and xDIR pins) are still functional.

Driving both ABENBLn and CDENBLn high will put the device into a low power sleep state. In this state, the H-bridges are disabled, both indexers are reset to the home state, the gate drive charge pump is stopped, and all internal clocks are stopped. In this state all inputs are ignored until one or both of the xENBLn pits return active low.

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7.3.6 Protection Circuits

The DRV8821 is fully protected against undervoltage, overcurrent and overtemperature events.

7.3.6.1 Overcurrent Protection (OCP)

All of the drivers in DRV8821 are protected with an OCP (Over-Current Protection) circuit.

The OCP circuit includes an analog current limit circuit, which acts by removing the gate drive from each output FET if the current through it exceeds a preset level. This circuit will limit the current to a level that is safe to prevent damage to the FET.

A digital circuit monitors the analog current limit circuits. If any analog current limit condition exists for longer than a preset period, all drivers in the device will be disabled.

The device is re-enabled upon the removal and re-application of power at the VM pins.

7.3.6.2 Thermal Shutdown (TSD)

If the die temperature exceeds safe limits, all drivers in the device will be shut down.

The device will remain disabled until the die temperature has fallen to a safe level. After the temperature has fallen, the device may be re-enabled upon the removal and re-application of power at the VM pin.

7.3.6.3 Undervoltage Lockout (UVLO)

If at any time the voltage on the VM pins falls below the undervoltage lockout threshold voltage, all circuitry in the device will be disabled. Operation will resume when VM rises above the UVLO threshold. The indexer logic will be reset to its initial condition in the event of an undervoltage lockout.

7.3.6.4 Shoot-Through Current Prevention

The gate drive to each FET in the H-bridge is controlled to prevent any cross-conduction (shoot through current) during transitions.

7.4 Device Functional Modes

7.4.1 Decay Mode

The DRV8821 supports two different decay modes: slow decay or mixed decay. The mixed decay mode uses slow decay on increasing steps and mixed decay on decreasing steps. Mixed decay mode begins as fast decay but after a period of time (75% of the PWM cycle), switches to slow decay mode for the remainder of the fixed PWM period.

During PWM current chopping, the H-bridge is enabled to drive through the motor winding until the PWM current chopping threshold is reached. This is shown in Figure 11 as case 1. The current flow direction shown indicates positive current flow in Figure 11.

Once the chopping current threshold is reached, the H-bridge can operate in two different states, fast decay or slow decay.

In fast decay mode, once the PWM chopping current level has been reached, the H-bridge reverses state to allow winding current to flow in a reverse direction. As the winding current approaches zero, the bridge is disabled to prevent any reverse current flow. Fast-decay mode is shown in Figure 11 as case 2.

In slow-decay mode, winding current is re-circulated by enabling both of the low-side FETs in the bridge. This is shown in Figure 11 as case 3.

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Device Functional Modes (continued)

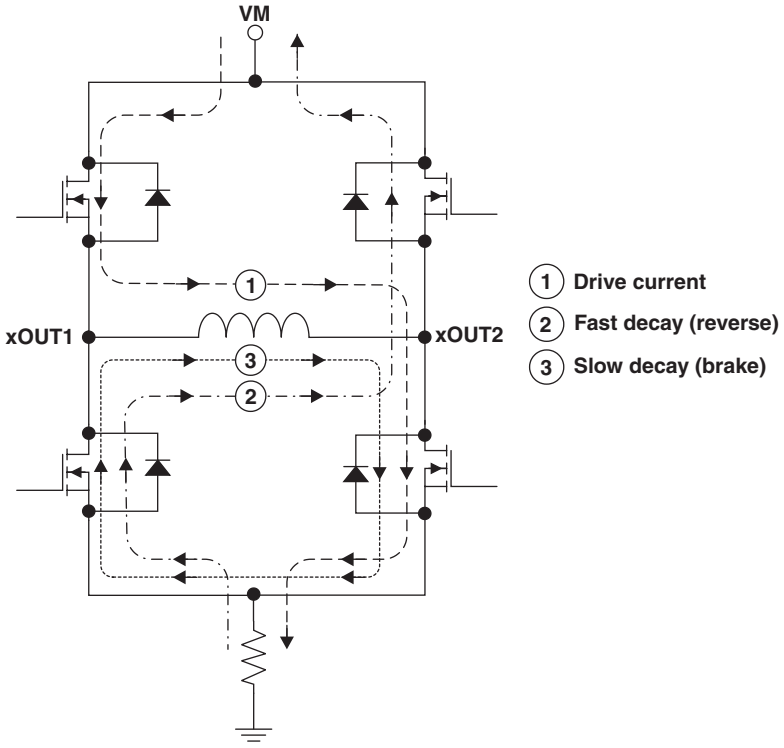


Figure 11. Decay Mode

The DRV8821 also supports a mixed decay mode. Mixed decay mode begins as fast decay, but after a period of time (75% of the PWM cycle) switches to slow decay mode for the remainder of the fixed PWM period.

Mixed decay mode is only active if the current through the winding is decreasing (per the indexer step table); if the current is increasing, then slow decay is always used.

Slow or mixed decay mode is selected by the state of the xDECAY pins - logic low selects slow decay, and logic high selects mixed decay operation.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DRV8821 can be used to drive two bipolar stepper motors.

8.2 Typical Application

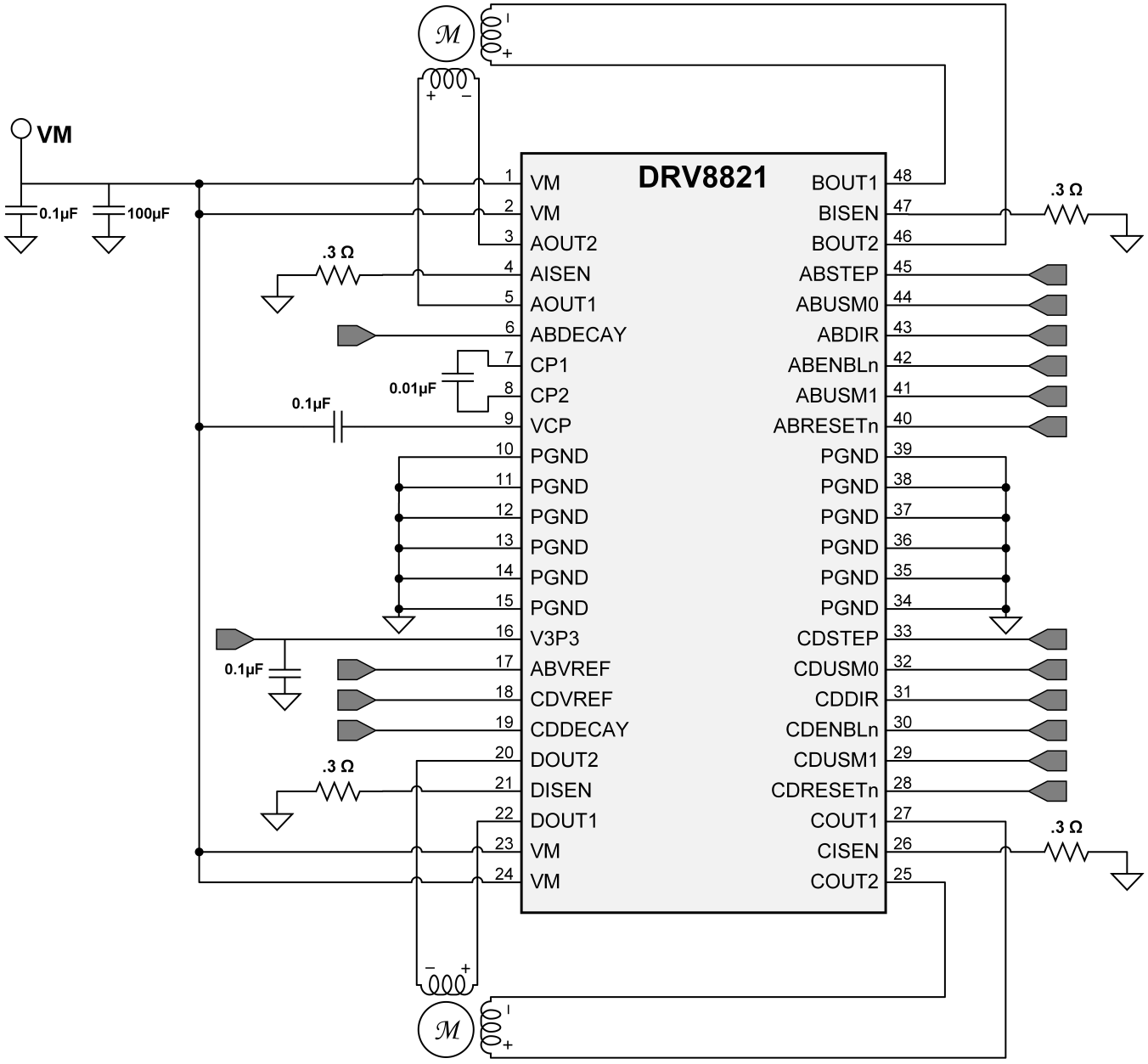


Figure 12. Typical Application Schematic

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Typical Application (continued)

8.2.1 Design Requirements

Table 3 shows the design parameters.

Table 3. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Supply voltage	V_M	24 V
Motor winding resistance	R_L	7.4 Ω/phase
Motor step full angle	θ_{step}	1.8°/step
Target microstepping angle	n_m	1/8 step
Target motor speed	V	120 rpm
Target full-scale current	I_{FS}	1 A

8.2.2 Detailed Design Procedure

8.2.2.1 Stepper Motor Speed

The first step in configuring the DRV8821 requires the desired motor speed and stepping level. The DRV8821 can support from full step to 1/8 step mode. If the target motor speed is too high, the motor will not spin. Make sure that the motor can support the target speed. For a desired motor speed (v), a microstepping level (n_m), and motor full step angle (θ_{step}).

$$f_{step}\ (\text{steps/s}) = \frac{\text{v (rpm)} \times 360\ (^\circ/\text{rot})}{\theta_{step}\ (^\circ/\text{step}) \times n_m\ (\text{steps/mirostep}) \times 60\ (\text{s/min})} \quad (2)$$

θ_{step} can be found in the stepper motor data sheet or often written on the motor itself.

For DRV8821, the microstepping levels are set by the xUSM0/xUSM1 pins and can be any of the settings in Table 1. Higher microstepping means a smoother motor motion and less audible noise, but increases the switching losses and requires a higher f_{step} to achieve the same motor speed.

8.2.2.2 Current Regulation

The chopping current (I_{CHOP}) is the maximum current driven through either winding. This quality will depend on the sense resistor value (R_{XISEN}).

$$I_{CHOP} = \frac{V_{REFX}}{5 \times R_{ISENSE}} \quad (3)$$

I_{CHOP} is set by a comparator which compares the voltage across R_{XISEN} to a reference voltage. Note that I_{CHOP} must follow Equation 4 to avoid saturating the motor.

$$I_{CHOP}\ (A) < \frac{VM\ (V)}{R_L\ (\Omega) + 2 \times R_{DS(ON)}\ (\Omega) + R_{SENSE}\ (\Omega)} \quad (4)$$

where

- VM is the motor supply voltage.
- R_L is the motor winding resistance.

8.2.3 Application Curves

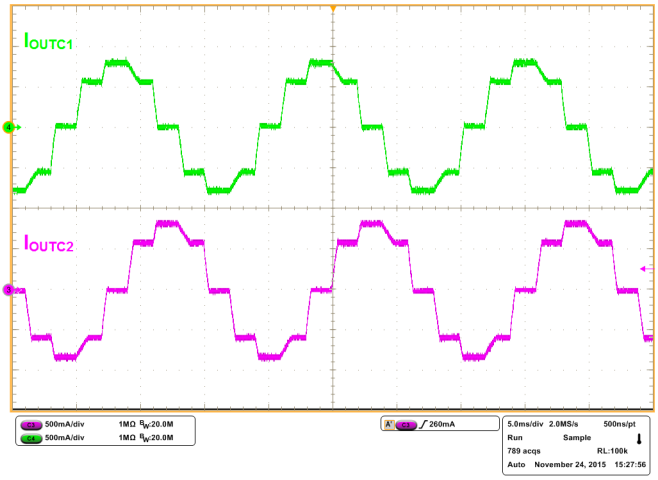


Figure 13. ½ Step Microstepping with Slow Decay

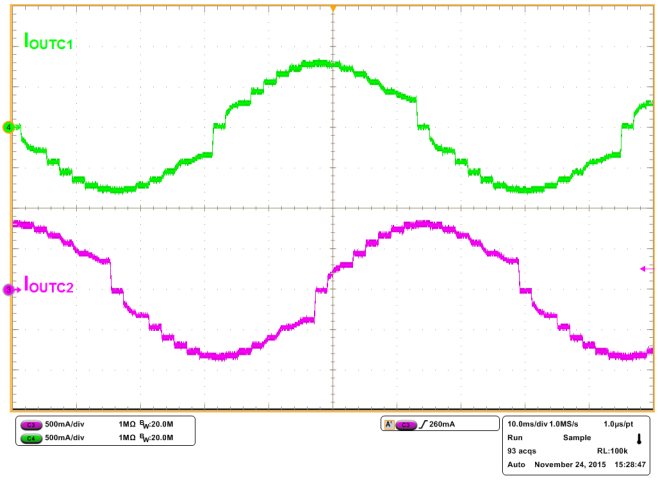


Figure 14. 1/8 Step Microstepping with Slow Decay

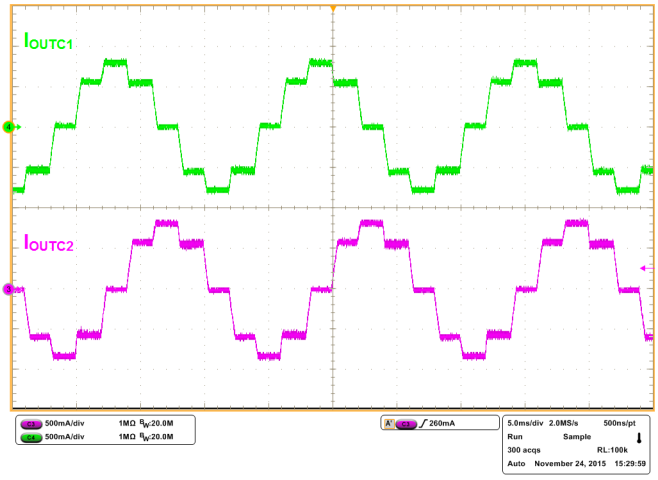


Figure 15. 1/2 Step Microstepping with Mixed Decay

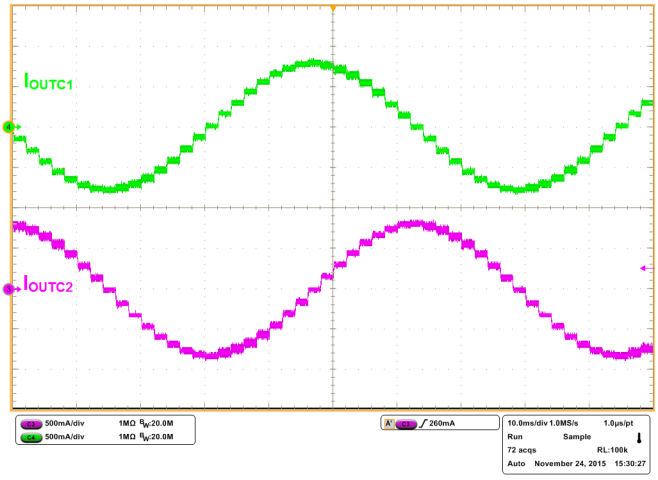


Figure 16. 1/8 Step Microstepping with Mixed Decay

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9 Power Supply Recommendations

9.1 Bulk Capacitance

Having appropriate local bulk capacitance is an important factor in motor drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system.
- The power supply's capacitance and ability to source current.
- The amount of parasitic inductance between the power supply and motor system.
- The acceptable voltage ripple.
- The type of motor used (Brushed DC, Brushless DC, Stepper).
- The motor breaking method.

The inductance between the power supply and motor drive system will limit the rate current can change from the power supply. If the local bulk capacitance is too small, the system will respond to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The datasheet generally provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor.

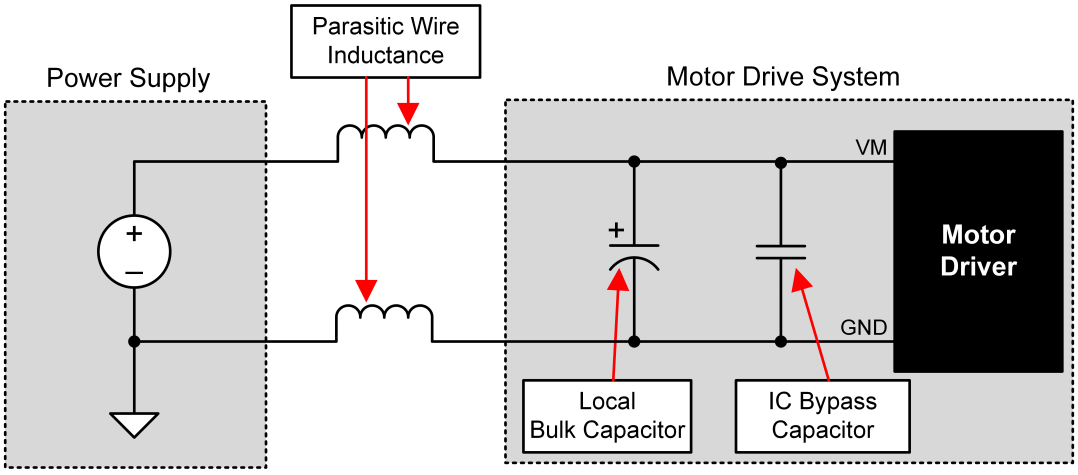


Figure 17. Example Setup of Motor Drive System with External Power Supply

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

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10 Layout

10.1 Layout Guidelines

The bulk capacitor should be placed to minimize the distance of the high-current path through the motor driver device. The connecting metal trace widths should be as wide as possible, and numerous vias should be used when connecting PCB layers. These practices minimize inductance and allow the bulk capacitor to deliver high current.

Small-value capacitors should be ceramic, and placed closely to device pins.

The high-current device outputs should use wide metal traces.

The device thermal pad should be soldered to the PCB top-layer ground plane. Multiple vias should be used to connect to a large bottom-layer ground plane. The use of large metal planes and multiple vias help dissipate the $I^2 \times R_{DS(on)}$ heat that is generated in the device.

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10.2 Layout Example

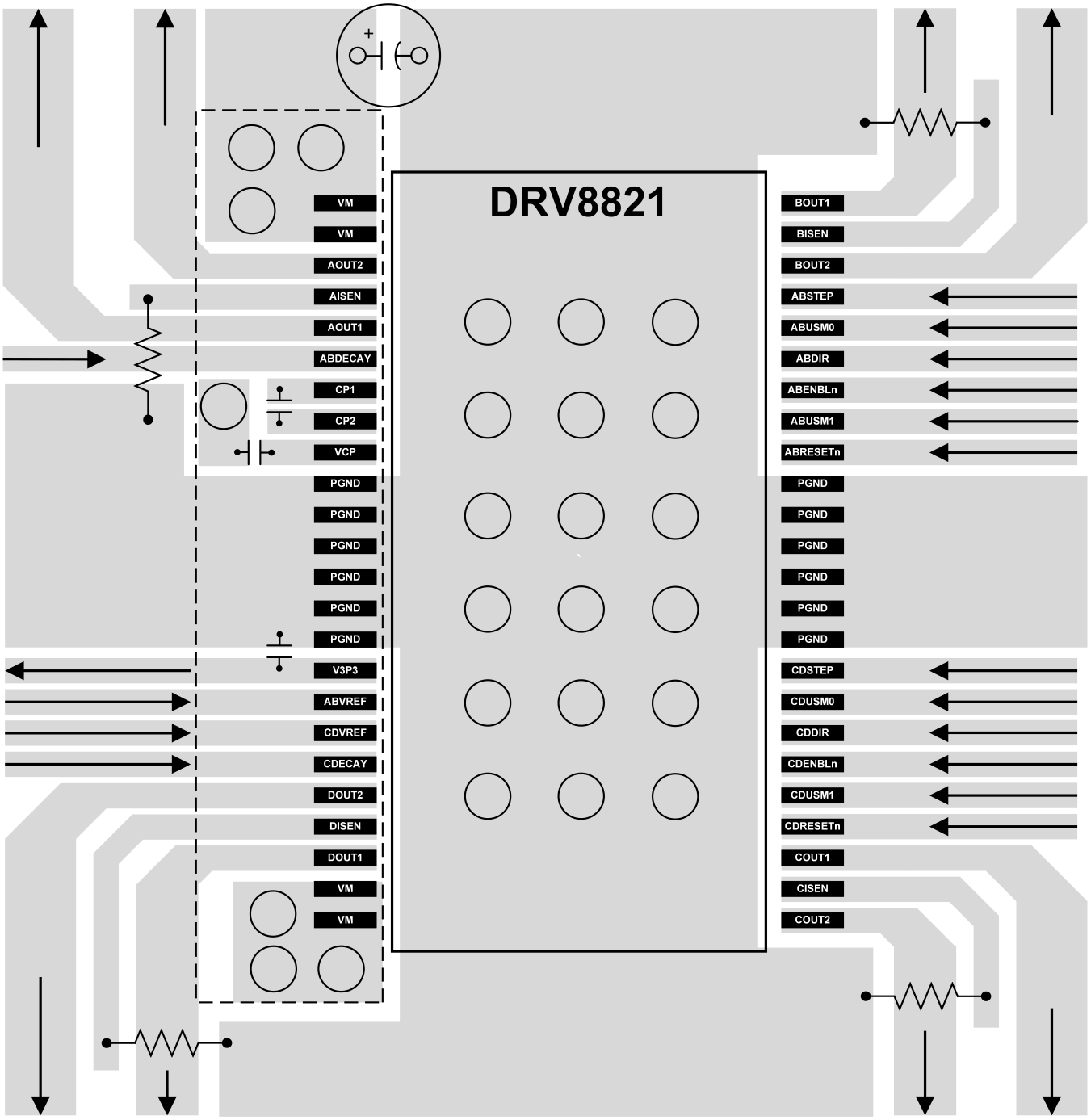


Figure 18. Typical Layout of DRV8821

10.3 Thermal Considerations

The DRV8821 has thermal shutdown (TSD) as described *Thermal Shutdown (TSD)*. If the die temperature exceeds approximately 150°C, the device will be disabled until the temperature drops to a safe level.

Any tendency of the device to enter thermal shutdown is an indication of either excessive power dissipation, insufficient heatsinking, or too high an ambient temperature.

10.3.1 Power Dissipation

Power dissipation in the DRV8821 is dominated by the power dissipated in the output FET resistance, or $R_{DS(ON)}$. Average power dissipation when running a stepper motor can be roughly estimated by Equation 5.

$$P_{TOT} = 4 \bullet R_{DS(ON)} \bullet (I_{OUT(RMS)})^2 \quad (5)$$

where P_{TOT} is the total power dissipation, $R_{DS(ON)}$ is the resistance of each FET, and $I_{OUT(RMS)}$ is the RMS output current being applied to each winding. $I_{OUT(RMS)}$ is equal to the approximately 0.7x the full-scale output current setting. The factor of 4 comes from the fact that there are two motor windings, and at any instant two FETs are conducting winding current for each winding (one high-side and one low-side). Remember that the DRV8821 has two stepper motor drivers, so the power dissipation of each must be added together to determine the total device power dissipation.

The maximum amount of power that can be dissipated in the DRV8821 is dependent on ambient temperature and heatsinking. The thermal dissipation ratings table in the datasheet can be used to estimate the temperature rise for typical PCB constructions.

Note that $R_{DS(ON)}$ increases with temperature, so as the device heats, the power dissipation increases. This must be taken into consideration when sizing the heatsink.

10.3.2 Heatsinking

The PowerPAD™ package uses an exposed pad to remove heat from the device. For proper operation, this pad must be thermally connected to copper on the PCB to dissipate heat. On a multi-layer PCB with a ground plane, this can be accomplished by adding a number of vias to connect the thermal pad to the ground plane. On PCBs without internal planes, copper area can be added on either side of the PCB to dissipate heat. If the copper area is on the opposite side of the PCB from the device, thermal vias are used to transfer the heat between top and bottom layers.

For details about how to design the PCB, refer to TI application report, *PowerPAD™ Thermally Enhanced Package* SLMA002 and TI application brief, *PowerPAD™ Made Easy,* SLMA004 available at www.ti.com.

In general, the more copper area that can be provided, the more power can be dissipated. Figure 19 shows thermal resistance vs. copper plane area for both a single-sided PCB with 2-oz copper heatsink area, and a 4-layer PCB with 1-oz copper and a solid ground plane. Both PCBs are 76 mm x 114 mm, and 1.6 mm thick. It can be seen that the heatsink effectiveness increases rapidly to about 20 cm^2, then levels off somewhat for larger areas.

Six pins on the center of each side of the package are also connected to the device ground. A copper area can be used on the PCB that connects to the PowerPAD™ as well as to all the ground pins on each side of the device. This is especially useful for single-layer PCB designs.

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Thermal Considerations (continued)

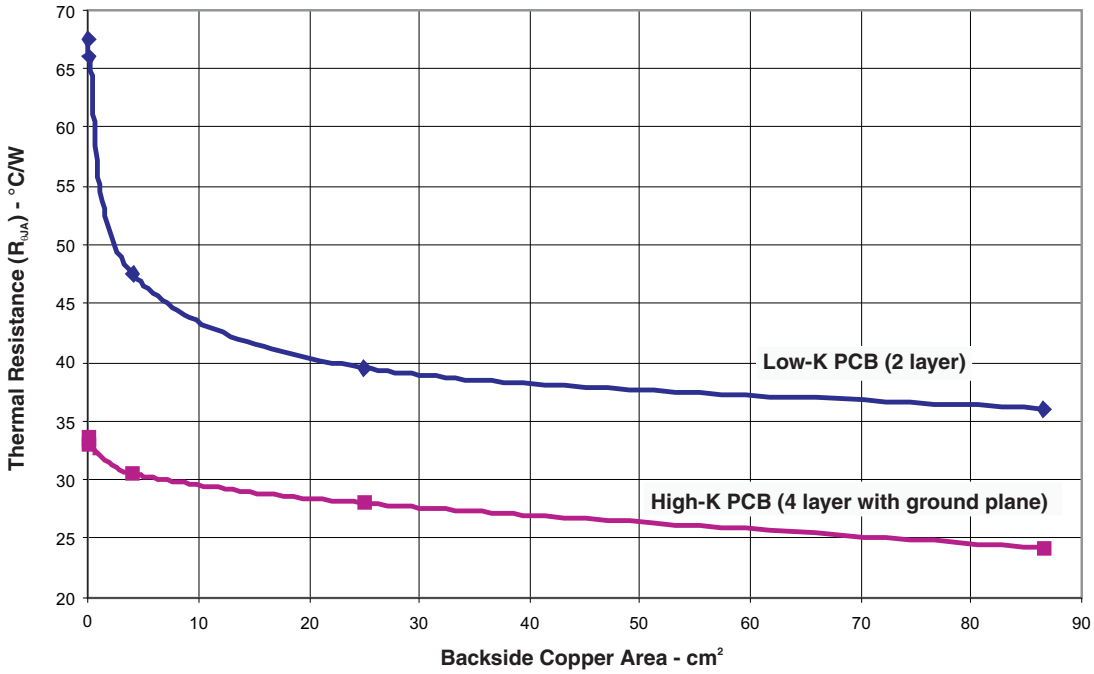


Figure 19. Thermal Resistance vs Copper Plane Area

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For details about how to design the PCB, refer to TI application report, *PowerPAD™ Thermally Enhanced Package* SLMA002 and TI application brief, *PowerPAD™ Made Easy,* SLMA004 available at www.ti.com.

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV8821DCA	ACTIVE	HTSSOP	DCA	48	40	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 85	DRV8821	Samples
DRV8821DCAR	ACTIVE	HTSSOP	DCA	48	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 85	DRV8821	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

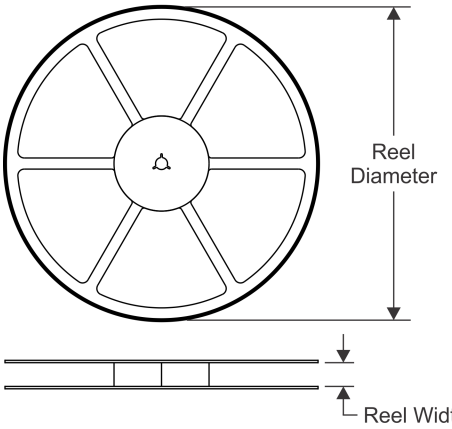
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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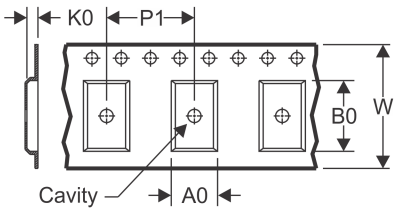
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

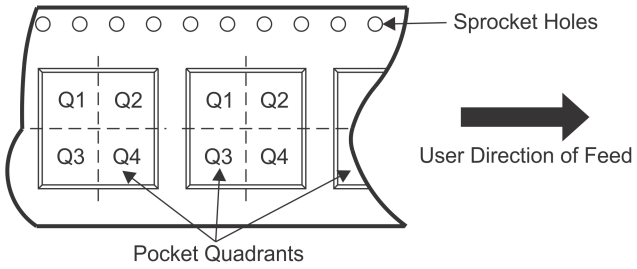


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

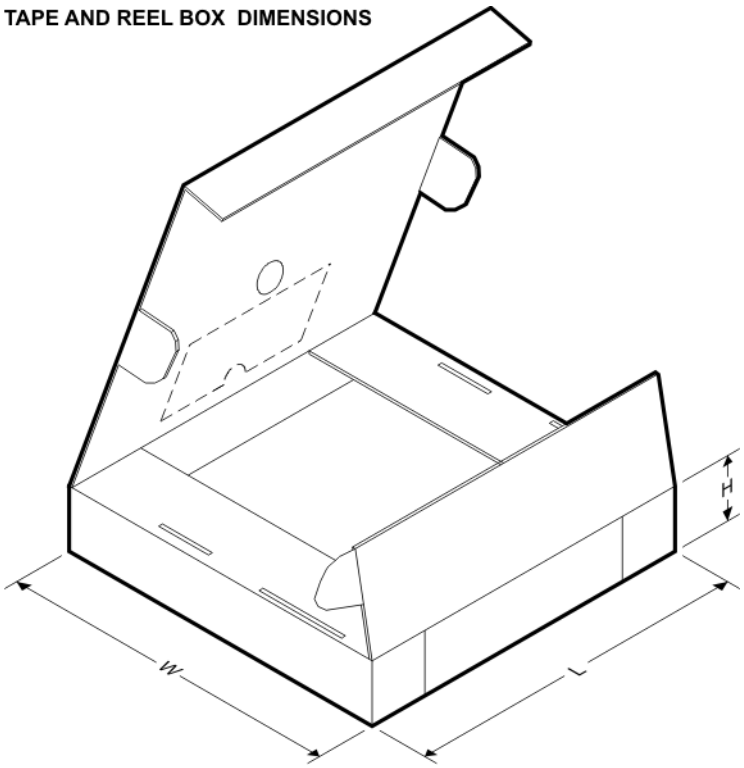
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8821DCAR	HTSSOP	DCA	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1

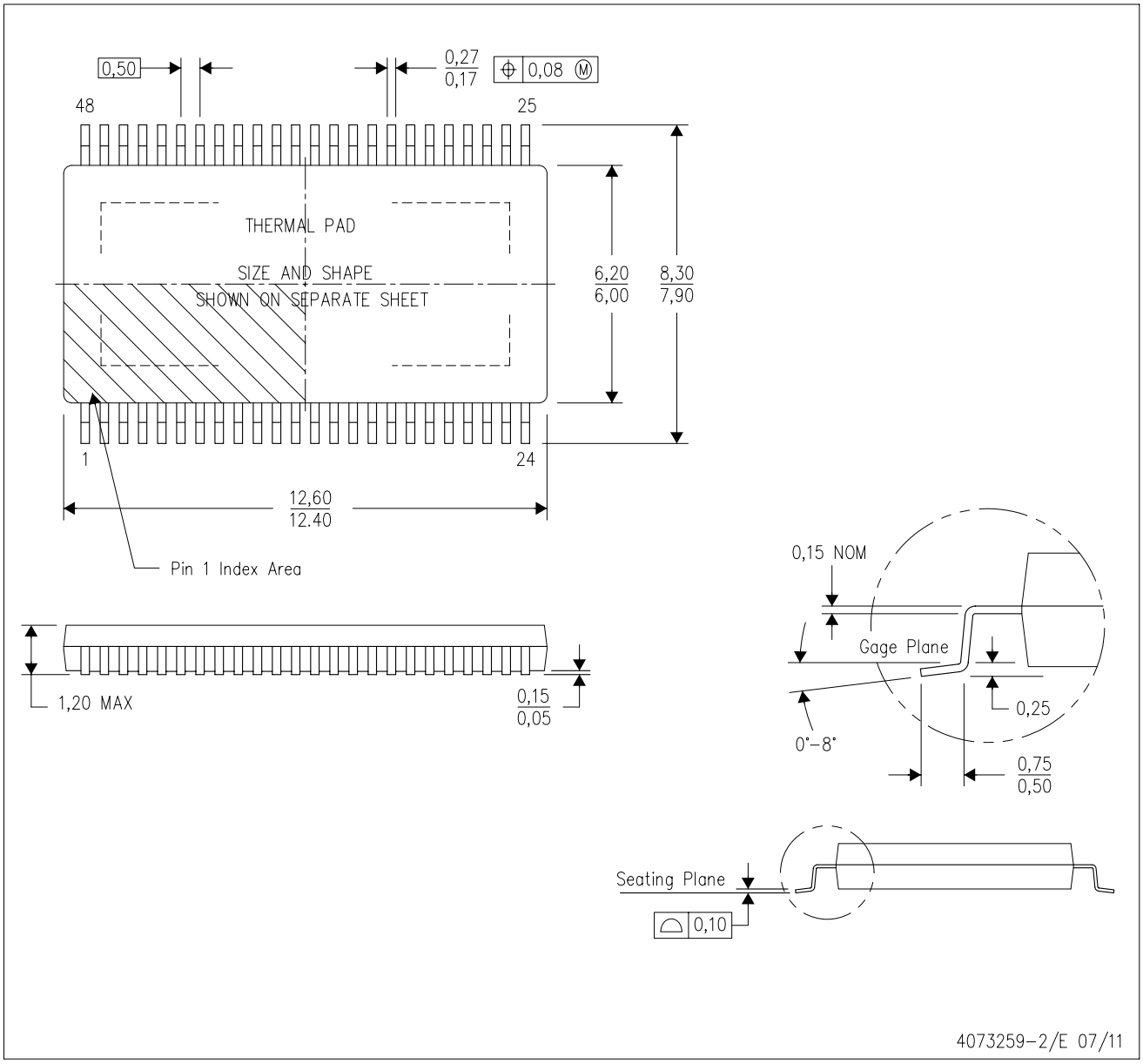
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8821DCAR	HTSSOP	DCA	48	2000	350.0	350.0	43.0

DCA (R–PDSO–G48) PowerPAD™ PLASTIC SMALL–OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

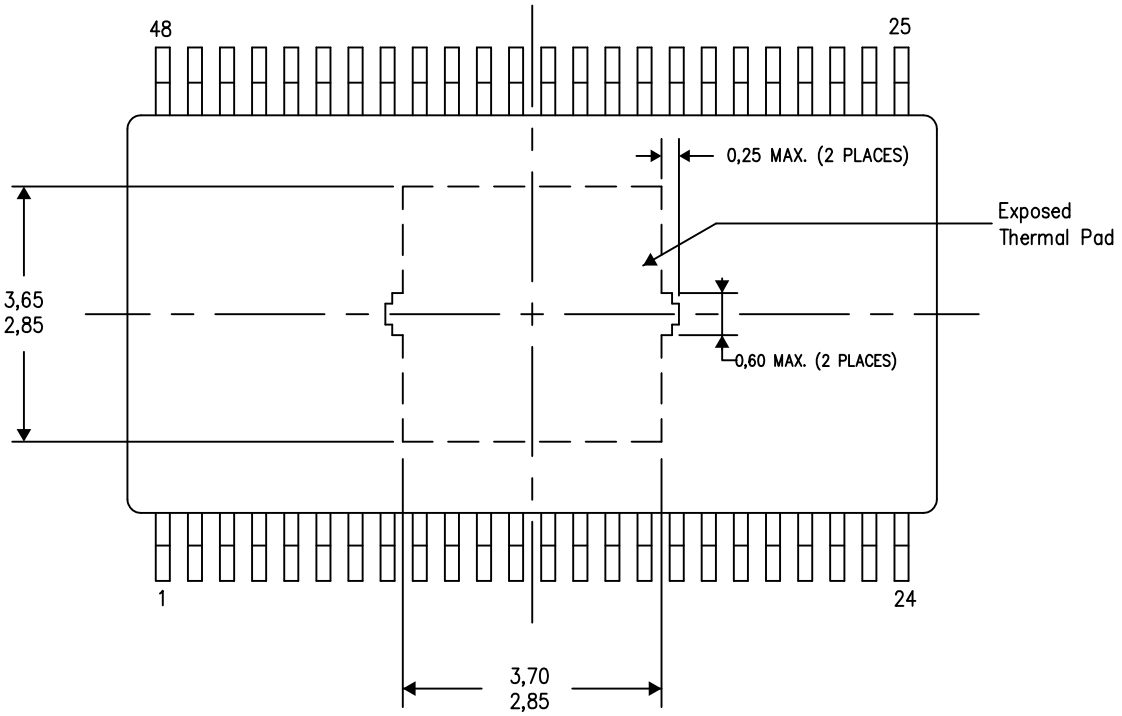
DCA (R–PDSO–G48) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

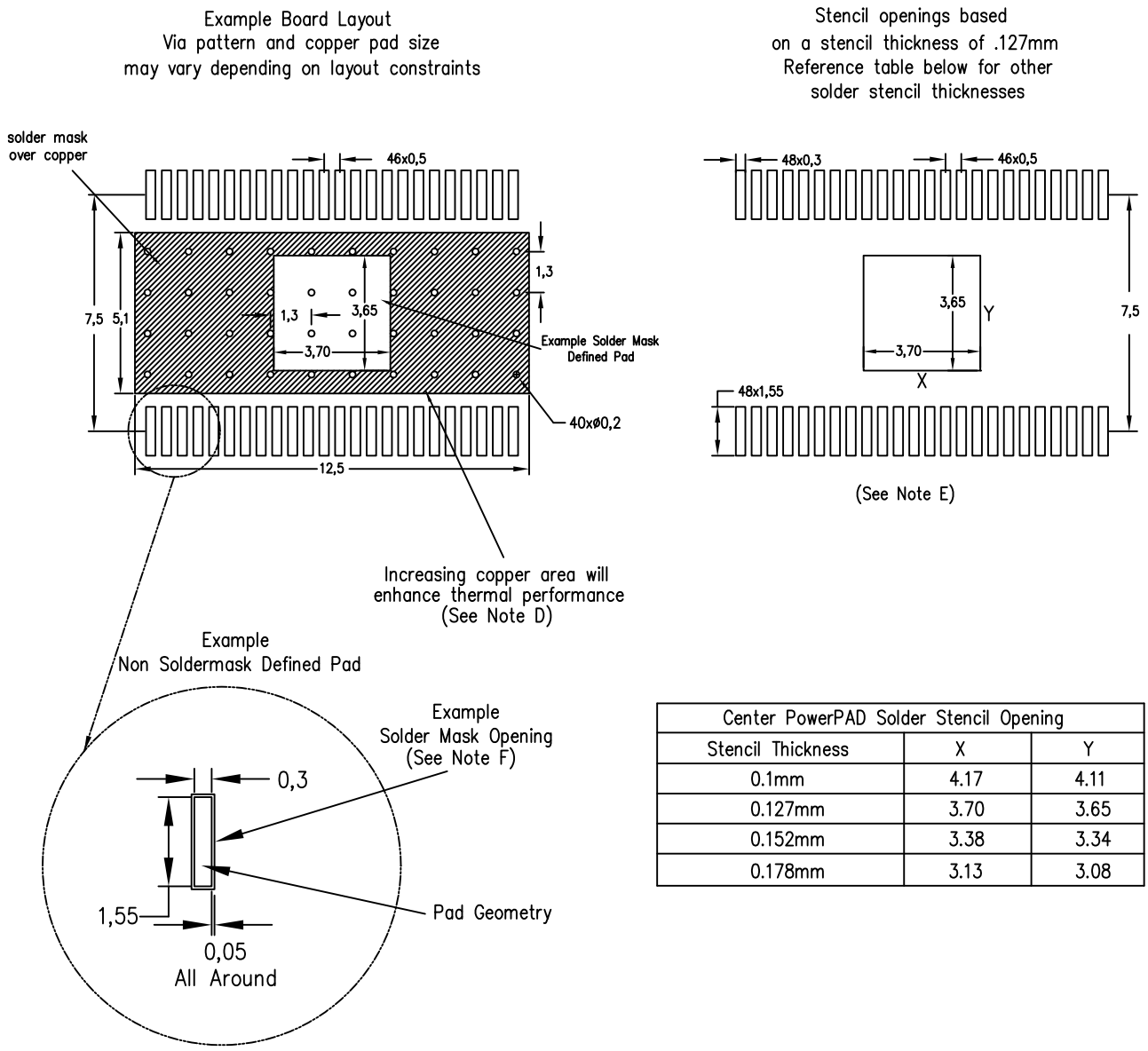
Exposed Thermal Pad Dimensions

4206320–6/S 11/14

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments.

DCA (R–PDSO–G48) PowerPAD™ PLASTIC SMALL OUTLINE PACKAGE



Center PowerPAD Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	4.17	4.11
0.127mm	3.70	3.65
0.152mm	3.38	3.34
0.178mm	3.13	3.08

4208546–5/H 11/14

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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