UNIPOLAR STEPPER MOTOR DRIVER IC

Check for Samples: DRV8805

FEATURES

- **4-Channel Protected Low-Side Driver**
  - **Four NMOS FETs With Overcurrent Protection**
  - **Integrated Inductive Catch Diodes**
- **Indexer/Translator for Unipolar Stepper Motors**
  - **Simple Step/Direction Interface**
  - **Three Step Modes (2-Phase Full-Step, 1-2-Phase Half-Step, 1-Phase Wave Drive)**
- **DW Package: 1.5-A (Single Channel On) / 800-mA (Four Channels On) Maximum Drive Current per Channel (at 25°C)**
- **PWP Package: 2-A (Single Channel On) / 1-A (Four Channels On) Maximum Drive Current per Channel (at 25°C, With Proper PCB Heatsinking)**
- **8.2-V to 60-V Operating Supply Voltage Range**
- **Thermally Enhanced Surface Mount Package**

APPLICATIONS

- **Gaming Machines**
- **General Unipolar Stepper Motor Drivers**

DESCRIPTION

The DRV8805 provides an integrated solution for driving unipolar stepper motors. It includes four low side drivers with overcurrent protection and provides built-in diodes to clamp turn-off transients generated by the motor windings.

Indexer logic to control a unipolar stepper motor using a simple step/direction interface is also integrated. Three stepping modes are supported: 2 phase (full-step), 1-2 phase (half-step), and 1-phase (wave drive).

In the SOIC (DW) package, the DRV8805 can supply up to 1.5-A (one channel on) or 800-mA (all channels on) continuous output current per channel, at 25°C. In the HTSSOP (PWP) package, it can supply up to 2-A (one channel on) or 1-A (four channels on) continuous output current per channel, at 25°C with proper PCB heatsinking.

Internal shutdown functions are provided for over current protection, short circuit protection, under voltage lockout and overtemperature and faults are indicated by a fault output pin.

The DRV8805 is available in a 20-pin thermally-enhanced SOIC package and a 16-pin HTSSOP package (Eco-friendly: RoHS & no Sb/Br).

ORDERING INFORMATION(1)

PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
(SOIC) - DW	Reel of 2000	DRV8805DWR	DRV8805
	Tube of 25	DRV8805DW	DRV8805
(HTSSOP) - PWP	Reel of 2000	DRV8805PWPR	DRV8805
	Tube of 90	DRV8805PWP	DRV8805

(1) For the most current packaging and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

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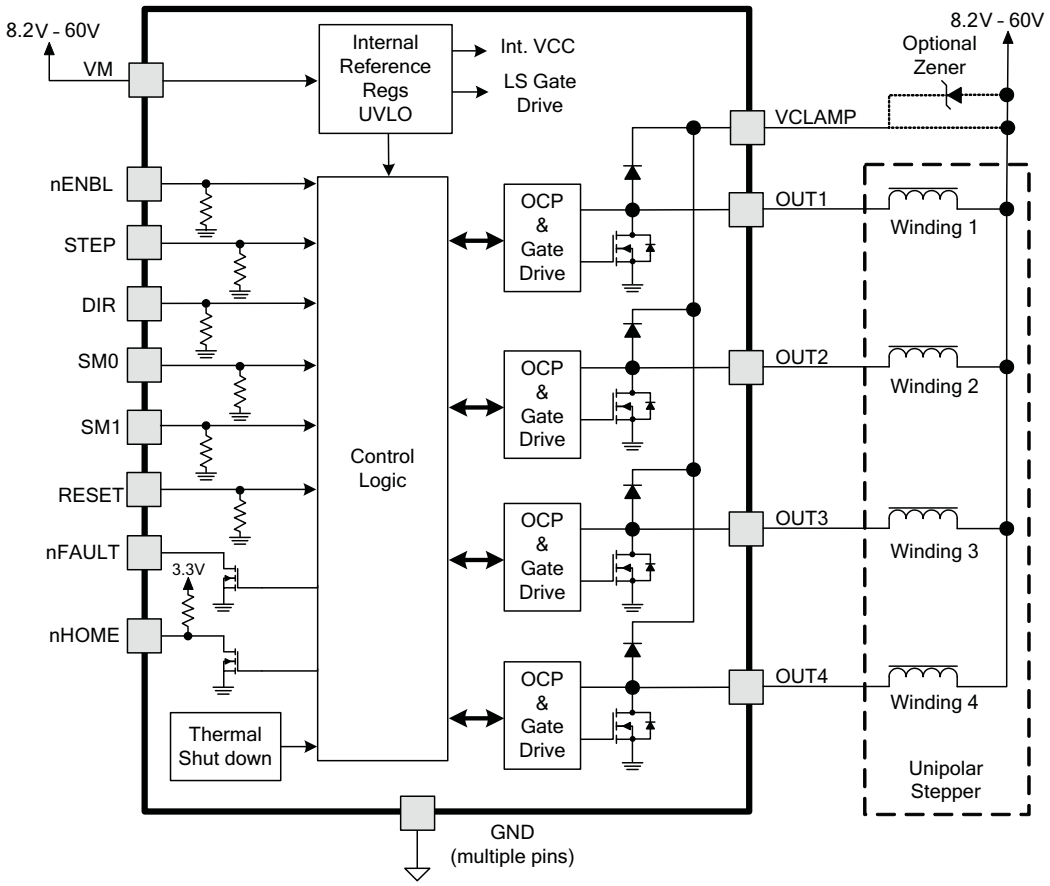
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DEVICE INFORMATION

Functional Block Diagram



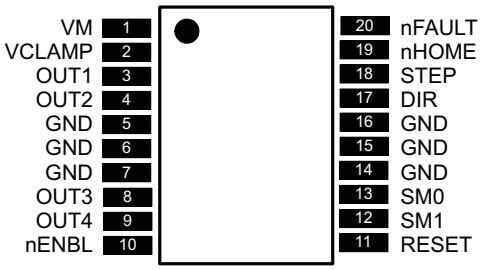
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Table 1. TERMINAL FUNCTIONS

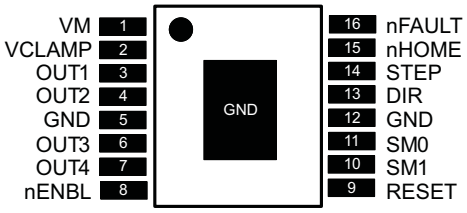
NAME	PIN (SOIC)	PIN (HTSSOP)	I/O(1)	DESCRIPTION	EXTERNAL COMPONENTS OR CONNECTIONS
POWER AND GROUND					
GND	5, 6, 7, 14, 15, 16	5, 12, PPAD	-	Device ground	All pins must be connected to GND.
VM	1	1	-	Device power supply	Connect to motor supply (8.2 V - 60 V).
CONTROL					
nENBL	10	8	I	Enable input	Active low enables outputs – internal pulldown
RESET	11	9	I	Reset input	Active-high reset input initializes internal logic – internal pulldown
STEP	18	14	I	Step input	Rising edge advances motor to next step – internal pulldown
DIR	17	13	I	Direction input	Level controls direction of rotation – internal pulldown
SM0	13	11	I	Step mode	Sets step mode – see step modes section for details – internal pulldowns
SM1	12	10			
STATUS					
nFAULT	20	16	OD	Fault	Logic low when in fault condition (overtemp, overcurrent)
nHOME	19	15	OD	Home	Logic low when indexer is at home position – weak internal pullup to 3.3 V
OUTPUT					
OUT1	3	3	O	Output 1	Connect to load 1
OUT2	4	4	O	Output 2	Connect to load 2
OUT3	8	6	O	Output 3	Connect to load 3
OUT4	9	7	O	Output 4	Connect to load 4
VCLAMP	2	2	-	Output clamp voltage	Connect to VM supply, or zener diode to VM supply

(1) Directions: I = input, O = output, OD = open-drain output

DW (WIDE SOIC) PACKAGE
(TOP VIEW)



PWP (HTSSOP) PACKAGE
(TOP SIDE)



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ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1) (2)

		VALUE	UNIT
VM	Power supply voltage range	–0.3 to 65	V
VOUTx	Output voltage range	–0.3 to 65	V
VCLAMP	Clamp voltage range	–0.3 to 65	V
nHOME, nFAULT	Output current	20	mA
	Peak clamp diode current	2	A
	DC or RMS clamp diode current	1	A
	Digital input pin voltage range	–0.5 to 7	V
nHOME, nFAULT	Digital output pin voltage range	–0.5 to 7	V
	Peak motor drive output current, t < 1 µS	Internally limited	A
	Continuous total power dissipation	See Dissipation Ratings table	
T_J	Operating virtual junction temperature range	–40 to 150	°C
T_{stg}	Storage temperature range	–60 to 150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

THERMAL INFORMATION

THERMAL METRIC		DRV8805 DW 20 PINS	DRV8805 PWP 16 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(1)	67.7	39.6	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(2)	32.9	24.6	
θ_{JB}	Junction-to-board thermal resistance(3)	35.4	20.3	
ψ_{JT}	Junction-to-top characterization parameter(4)	8.2	0.7	
ψ_{JB}	Junction-to-board characterization parameter(5)	34.9	20.1	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(6)	N/A	2.3	

(1) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(2) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(3) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(4) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(5) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

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RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_M	Power supply voltage range	8.2		60	V
V_{CLAMP}	Output clamp voltage range(1)	0		60	V
I_{OUT}	Continuous output current, single channel on, T_A = 25°C, SOIC package(2)			1.5	A
	Continuous output current, four channels on, T_A = 25°C, SOIC package(2)			0.8	
	Continuous output current, single channel on, T_A = 25°C, HTSSOP package(2)			1.5	
	Continuous output current, four channels on, T_A = 25°C, HTSSOP package(2)			0.8	

(1) V_{CLAMP} is used only to supply the clamp diodes. It is not a power supply input.
(2) Power dissipation and thermal limits must be observed.

ELECTRICAL CHARACTERISTICS

T_A = 25°C, over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES						
I_{VM}	VM operating supply current	V_M = 24 V		1.6	2.1	mA
V_{UVLO}	VM undervoltage lockout voltage	V_M rising			8.2	V
LOGIC-LEVEL INPUTS (SCHMITT TRIGGER INPUTS WITH HYSTERESIS)						
V_{IL}	Input low voltage			0.6	0.7	V
V_{IH}	Input high voltage		2			V
V_{HYS}	Input hysteresis			0.45		V
I_{IL}	Input low current	VIN = 0	–20		20	µA
I_{IH}	Input high current	VIN = 3.3 V			100	µA
R_{PD}	Pulldown resistance			100		kΩ
nFAULT OUTPUT (OPEN-DRAIN OUTPUT)						
V_{OL}	Output low voltage	I_O = 5 mA			0.5	V
I_{OH}	Output high leakage current	V_O = 3.3 V			1	µA
nHOME OUTPUT (OPEN-DRAIN OUTPUT WITH WEAK INTERNAL PULLUP)						
V_{OL}	Output low voltage	I_O = 5 mA			0.5	V
V_{OH}	Output high voltage	I_O = 100 µA, V_M = 24 V		3.3		V
I_{OH}	Output high leakage current	V_O = 3.3 V			1	µA
LOW-SIDE FETS						
$R_{DS(ON)}$	FET on resistance	V_M = 24 V, I_O = 700 mA, T_J = 25°C		0.5		Ω
		V_M = 24 V, I_O = 700 mA, T_J = 85°C		0.75	0.8	
I_{OFF}	Off-state leakage current		–50		50	µA
HIGH-SIDE DIODES						
V_F	Diode forward voltage	V_M = 24 V, I_O = 700 mA, T_J = 25°C		1.2		V
I_{OFF}	Off-state leakage current	V_M = 24 V, T_J = 25°C	–50		50	µA
OUTPUTS						
t_R	Rise time	V_M = 24 V, I_O = 700 mA, Resistive load	50		300	ns
t_F	Fall time	V_M = 24 V, I_O = 700 mA, Resistive load	50		300	ns
PROTECTION CIRCUITS						
I_{OCP}	Overcurrent protection trip level		2.3		3.8	A
t_{OCP}	Overcurrent protection deglitch time			3.5		µs
t_{RETRY}	Overcurrent protection retry time			1.2		ms
t_{TSD}	Thermal shutdown temperature	Die temperature(1)	150	160	180	°C

(1) Not production tested.

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TIMING REQUIREMENTS

over operating free-air temperature range (unless otherwise noted)(1)

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
1	f_{STEP}	Step frequency		250	kHz
2	$t_{WH(STEP)}$	Pulse duration, STEP high	1.9		µs
3	$t_{WL(STEP)}$	Pulse duration, STEP low	1.9		µs
4	$t_{SU(STEP)}$	Setup time, DIR, SMx to STEP rising	1		µs
5	$t_{H(STEP)}$	Hold time, DIR, SMx to STEP rising	1		µs
6	$t_{OE(ENABLE)}$	Enable time, nENBL to output low		50	ns
7	$t_{PD(L-H)}$	Propagation delay time, STEP to OUTx, low to high		500	ns
8	$t_{PD(H-L)}$	Propagation delay time, STEP to OUTx, high to low		500	ns
-	t_{RESET}	RESET pulse width	20		µs

(1) Not production tested.

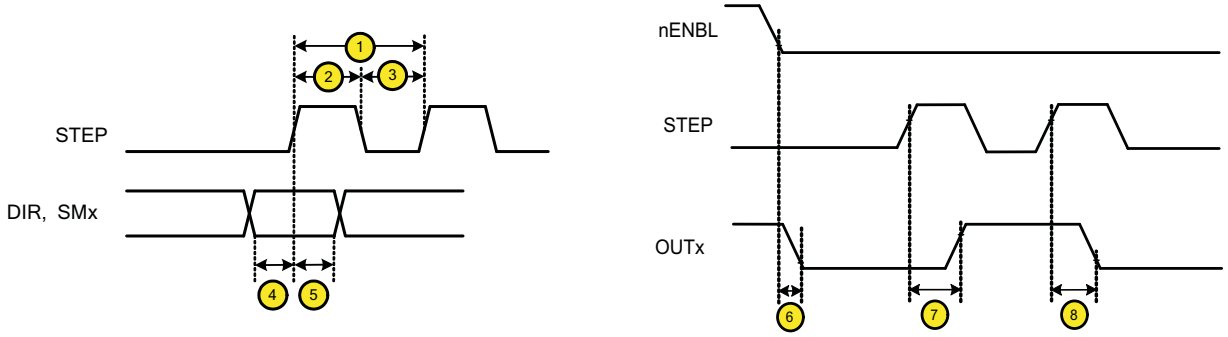


Figure 1. DRV8805 Timing Requirements

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FUNCTIONAL DESCRIPTION

Output Drivers

The DRV8805 contains four protected low-side drivers. Each output has an integrated clamp diode connected to a common pin, VCLAMP.

VCLAMP can be connected to the main power supply voltage, VM. It can also be connected to a zener or TVS diode to VM, allowing the switch voltage to exceed the main supply voltage VM. This connection can be beneficial when driving loads that require very fast current decay, such as unipolar stepper motors.

In all cases, the voltage on the outputs must not be allowed to exceed the maximum output voltage specification.

Indexer Operation

The DRV8805 integrates an indexer to allow motor control with a simple step and direction interface. Logically, the indexer is shown in Figure 2.

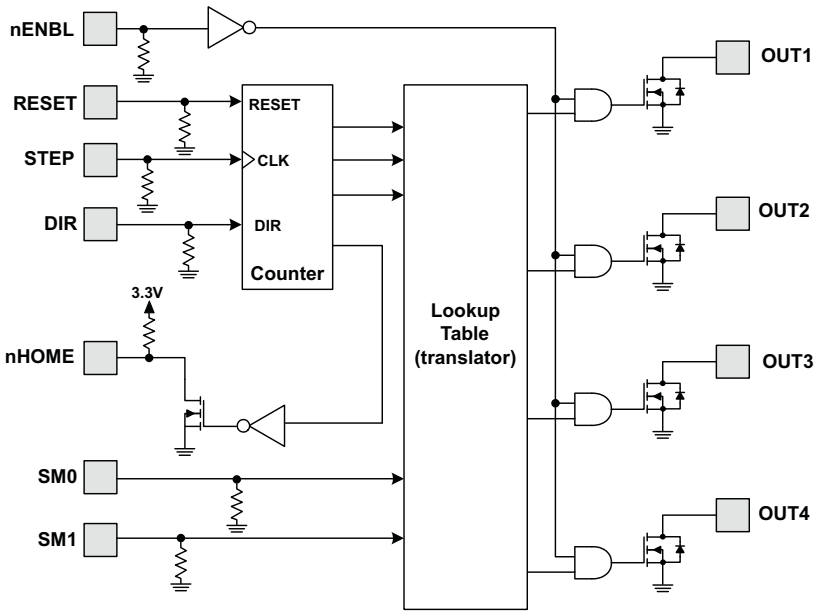


Figure 2. Indexer Operation

Step Modes

The SM0 and SM1 pins select the stepping mode of the translator as shown in Table 2.

Table 2. Step Modes

SM1	SM0	MODE
0	0	2-phase drive (full step)
0	1	1-2 phase drive (half step)
1	0	1-phase excitation (wave drive)
1	1	Reserved

In all modes, during a fault condition, the STEP input will be ignored. See the Protection Circuits section below.

The sequence of the outputs is shown in Table 3 through Table 5.

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Table 3. 2-Phase Excitation (Full-Step)

Function	Step	RESET	DIR	STEP	nHOME	OUT1	OUT2	OUT3	OUT4
Reset	1	1	X	X	0	ON	OFF	OFF	ON
CW	2	0	1	↑	1	ON	ON	OFF	OFF
CW	3	0	1	↑	1	OFF	ON	ON	OFF
CW	4	0	1	↑	1	OFF	OFF	ON	ON
CW to home	1	0	1	↑	0	ON	OFF	OFF	ON
CCW	4	0	0	↑	1	OFF	OFF	ON	ON
CCW	3	0	0	↑	1	OFF	ON	ON	OFF
CCW	2	0	0	↑	1	ON	ON	OFF	OFF
CCW to home	1	0	0	↑	0	ON	OFF	OFF	ON
Hold	X	0	X	$\overline{\uparrow}$	no chg	no chg	no chg	no chg	no chg

Table 4. 1-2-Phase Excitation (Half-Step)

Function	Step	RESET	DIR	STEP	nHOME	OUT1	OUT2	OUT3	OUT4
Reset	1	1	X	X	0	ON	OFF	OFF	OFF
CW	2	0	1	↑	1	ON	ON	OFF	OFF
CW	3	0	1	↑	1	OFF	ON	OFF	OFF
CW	4	0	1	↑	1	OFF	ON	ON	OFF
CW	5	0	1	↑	1	OFF	OFF	ON	OFF
CW	6	0	1	↑	1	OFF	OFF	ON	ON
CW	7	0	1	↑	1	OFF	OFF	OFF	ON
CW	8	0	1	↑	1	ON	OFF	OFF	ON
CW to home	1	0	1	↑	0	ON	OFF	OFF	OFF
CCW	8	0	0	↑	1	ON	OFF	OFF	ON
CCW	7	0	0	↑	1	OFF	OFF	OFF	ON
CCW	6	0	0	↑	1	OFF	OFF	ON	ON
CCW	5	0	0	↑	1	OFF	OFF	ON	OFF
CCW	4	0	0	↑	1	OFF	ON	ON	OFF
CCW	3	0	0	↑	1	OFF	ON	OFF	OFF
CCW	2	0	0	↑	1	ON	ON	OFF	OFF
CCW to home	1	0	0	↑	0	ON	OFF	OFF	OFF
Hold	X	0	X	$\overline{\uparrow}$	no chg	no chg	no chg	no chg	no chg

Table 5. 1-Phase Excitation (Wave Drive)

Function	Step	RESET	DIR	STEP	nHOME	OUT1	OUT2	OUT3	OUT4
Reset	1	1	X	X	0	ON	OFF	OFF	OFF
CW	2	0	1	↑	1	OFF	ON	OFF	OFF
CW	3	0	1	↑	1	OFF	OFF	ON	OFF
CW	4	0	1	↑	1	OFF	OFF	OFF	ON
CW to home	1	0	1	↑	0	ON	OFF	OFF	OFF
CCW	4	0	0	↑	1	OFF	OFF	OFF	ON
CCW	3	0	0	↑	1	OFF	OFF	ON	OFF
CCW	2	0	0	↑	1	OFF	ON	OFF	OFF
CCW to home	1	0	0	↑	0	ON	OFF	OFF	OFF
Hold	X	0	X	$\overline{\uparrow}$	no chg	no chg	no chg	no chg	no chg

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nENBL and RESET Operation

The nENBL pin enables or disables the output drivers. nENBL must be low to enable the outputs. nENBL does not affect the operation of the serial interface logic. Note that nENBL has an internal pulldown.

The RESET pin, when driven active high, resets the internal logic. The indexer is reset to the home state. All inputs are ignored while RESET is active. Note that RESET has an internal pulldown. An internal power-up reset is also provided, so it is not required to drive RESET at power-up.

Protection Circuits

The DRV8805 is fully protected against undervoltage, overcurrent and overtemperature events.

Overcurrent Protection (OCP)

An analog current limit circuit on each FET limits the current through the FET by removing the gate drive. If this analog current limit persists for longer than the t_{OCP} deglitch time (approximately 3.5 µs), the driver will be disabled and the nFAULT pin will be driven low. The driver will remain disabled for the t_{RETRY} retry time (approximately 1.2 ms), then the fault will be automatically cleared. The fault will be cleared immediately if either RESET pin is activated or VM is removed and re-applied.

Thermal Shutdown (TSD)

If the die temperature exceeds safe limits, all output FETs will be disabled and the nFAULT pin will be driven low. The STEP input will be ignored. Once the die temperature has fallen to a safe level, operation will automatically resume.

Undervoltage Lockout (UVLO)

If at any time the voltage on the VM pin falls below the undervoltage lockout threshold voltage, all circuitry in the device will be disabled, and internal logic will be reset. Operation will resume when VM rises above the UVLO threshold.

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THERMAL INFORMATION

Thermal Protection

The DRV8805 has thermal shutdown (TSD) as described above. If the die temperature exceeds approximately 150°C, the device will be disabled until the temperature drops to a safe level.

Any tendency of the device to enter TSD is an indication of either excessive power dissipation, insufficient heatsinking, or too high an ambient temperature.

Power Dissipation

Power dissipation in the DRV8805 is dominated by the power dissipated in the output FET resistance, or RDS(ON). Average power dissipation of each FET when running a static load can be roughly estimated by Equation 1:

$$P = R_{DS(ON)} \bullet (I_{OUT})^2 \quad (1)$$

where P is the power dissipation of one FET, $R_{DS(ON)}$ is the resistance of each FET, and I_{OUT} is equal to the average current drawn by the load. Note that at start-up and fault conditions this current is much higher than normal running current; these peak currents and their duration also need to be taken into consideration. When driving more than one load simultaneously, the power in all active output stages must be summed.

The maximum amount of power that can be dissipated in the device is dependent on ambient temperature and heatsinking.

Note that $R_{DS(ON)}$ increases with temperature, so as the device heats, the power dissipation increases. This must be taken into consideration when sizing the heatsink.

Heatsinking

The DRV8805DW package uses a standard SOIC outline, but has the center pins internally fused to the die pad in order to more efficiently remove heat from the device. The two center leads on each side of the package should be connected together to as large a copper area on the PCB as is possible to remove heat from the device. If the copper area is on the opposite side of the PCB from the device, thermal vias are used to transfer the heat between top and bottom layers.

In general, the more copper area that can be provided, the more power can be dissipated.

The DRV8805PWP package uses an HTSSOP package with an exposed PowerPAD™. The PowerPAD package uses an exposed pad to remove heat from the device. For proper operation, this pad must be thermally connected to copper on the PCB to dissipate heat. On a multi-layer PCB with a ground plane, this can be accomplished by adding a number of vias to connect the thermal pad to the ground plane. On PCBs without internal planes, copper area can be added on either side of the PCB to dissipate heat. If the copper area is on the opposite side of the PCB from the device, thermal vias are used to transfer the heat between top and bottom layers.

For details about how to design the PCB, refer to TI Application Report SLMA002, "PowerPAD Thermally Enhanced Package" and TI Application Brief SLMA004, "PowerPAD Made Easy", available at www.ti.com.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
DRV8805DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
DRV8805DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
DRV8805PWP	ACTIVE	HTSSOP	PWP	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
DRV8805PWPR	ACTIVE	HTSSOP	PWP	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

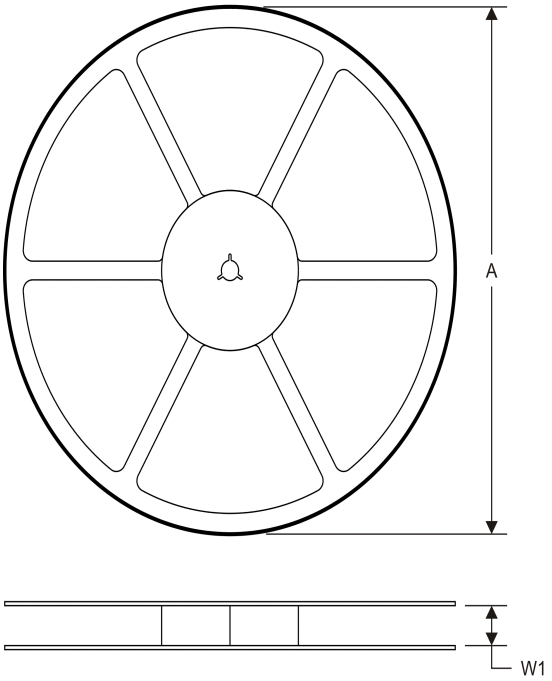
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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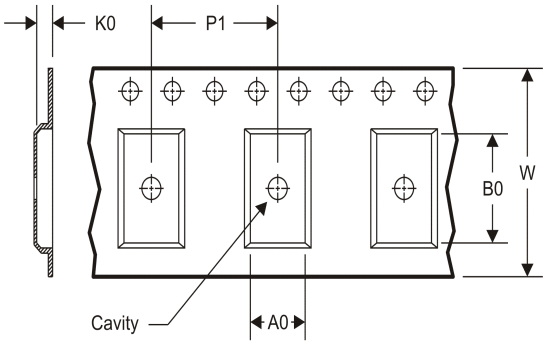
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TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



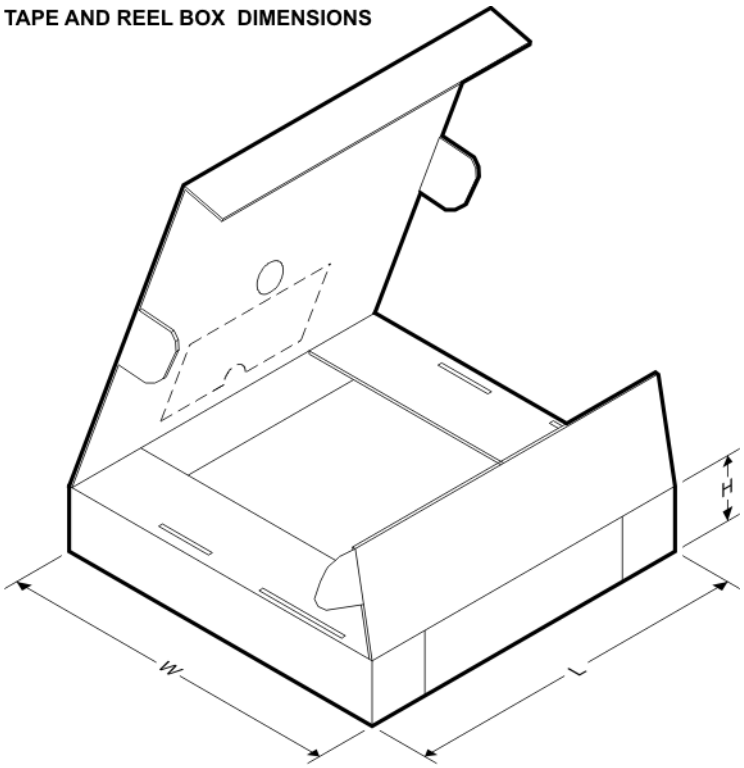
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8805DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
DRV8805PWPR	HTSSOP	PWP	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

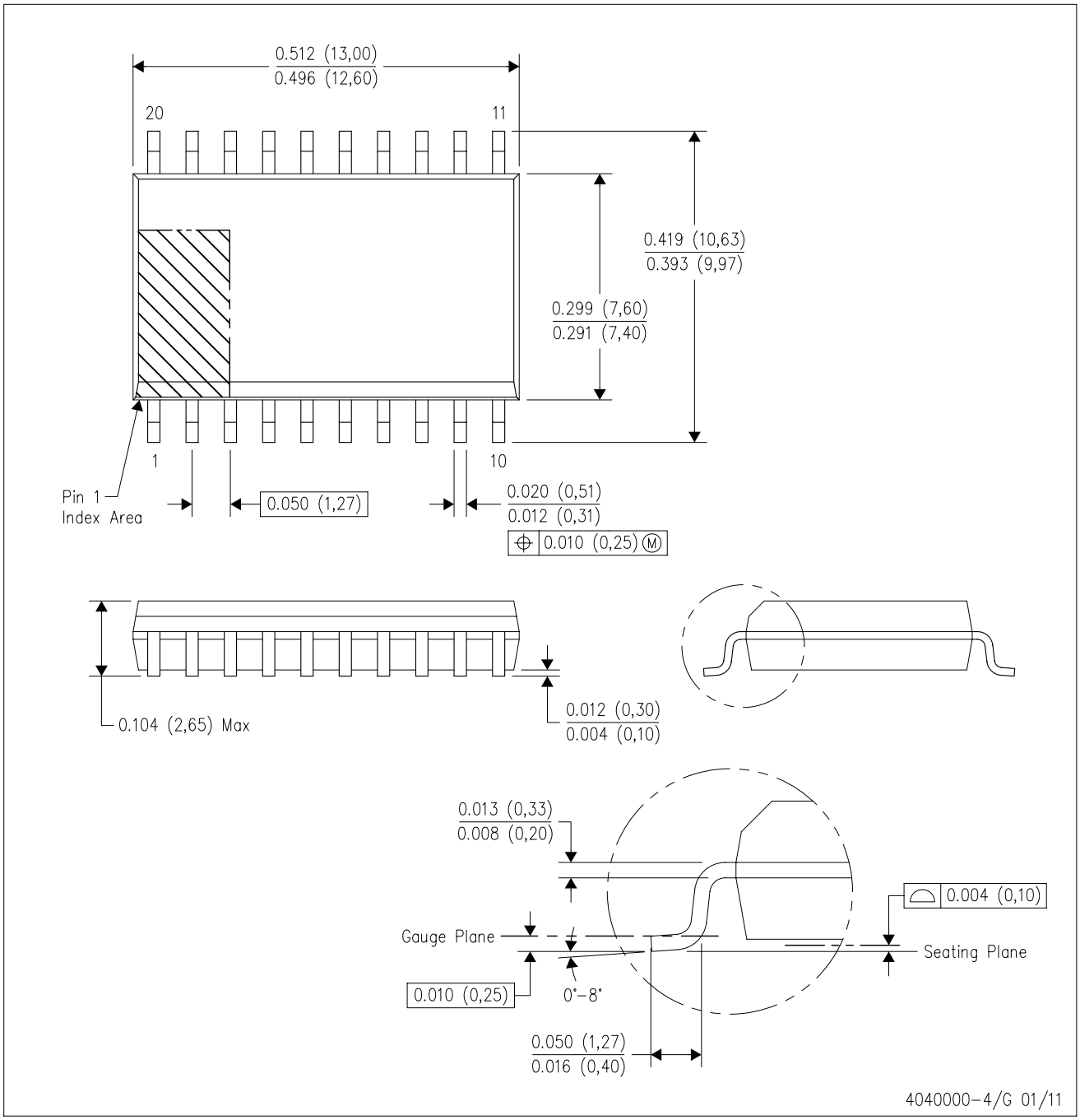
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

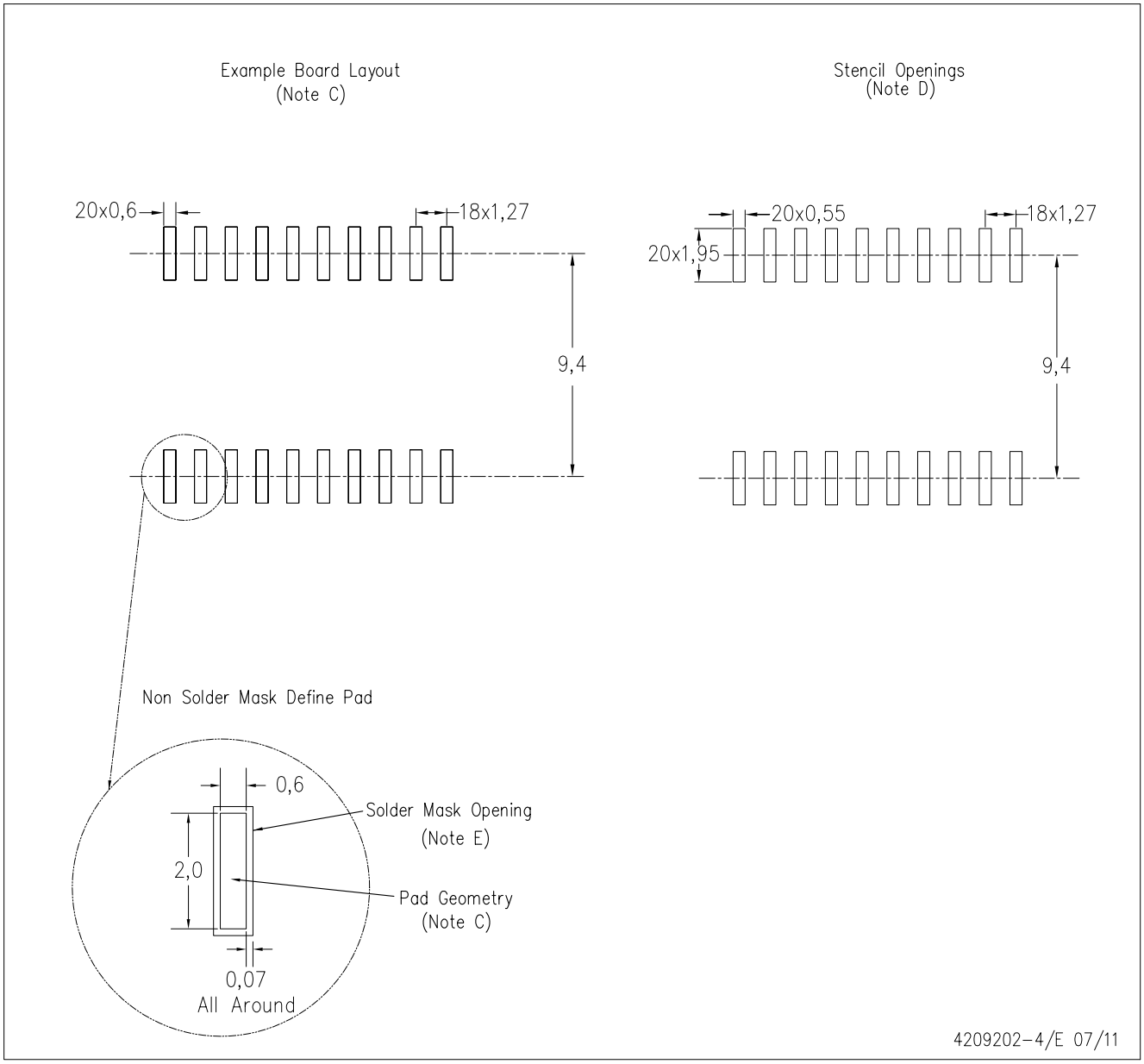
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8805DWR	SOIC	DW	20	2000	367.0	367.0	45.0
DRV8805PWPR	HTSSOP	PWP	16	2000	367.0	367.0	35.0

DW (R–PDSO–G20) PLASTIC SMALL OUTLINE



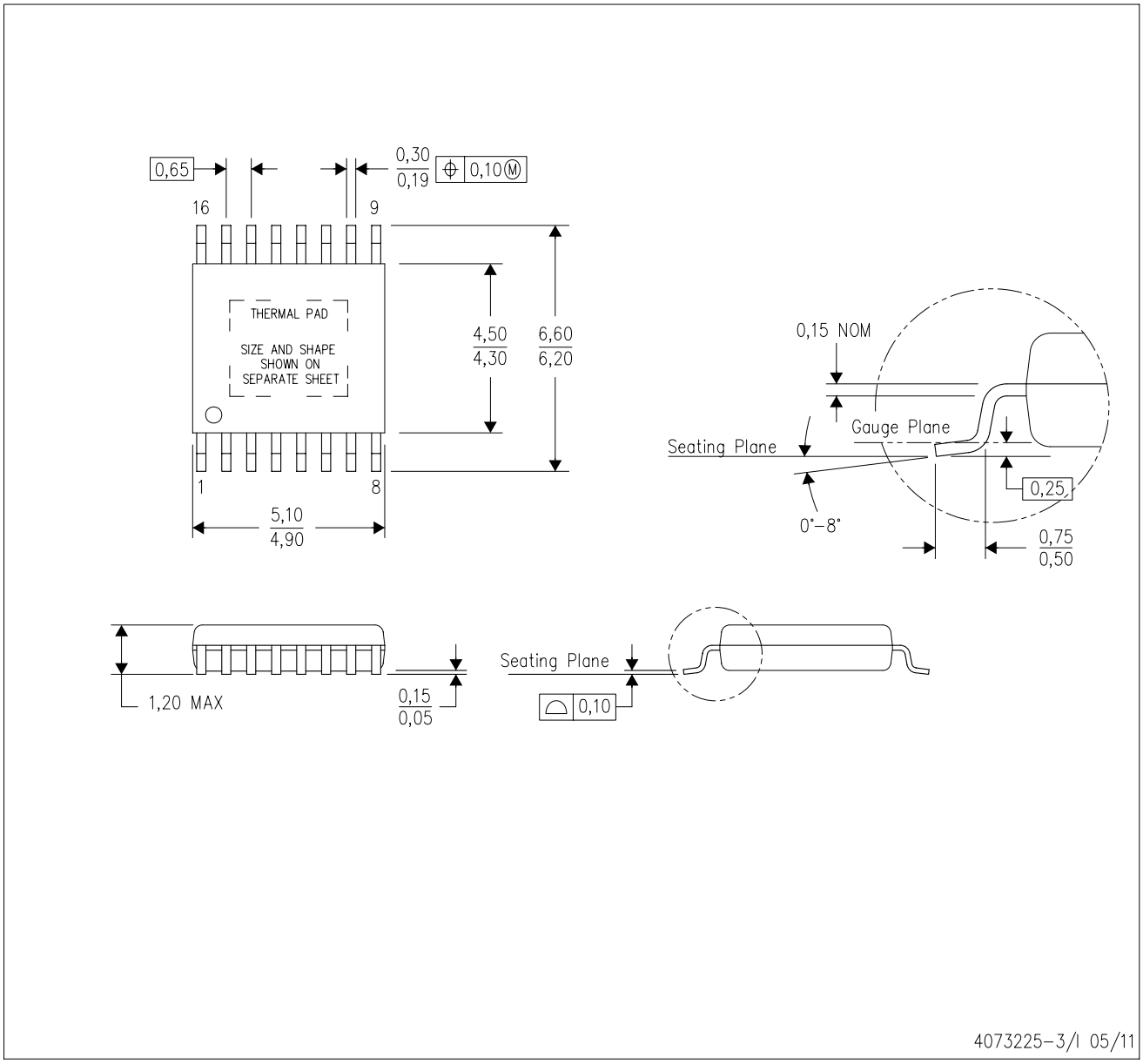
NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AC.

DW (R–PDSO–G20) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Refer to IPC7351 for alternate board design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PWP (R–PDSO–G16) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

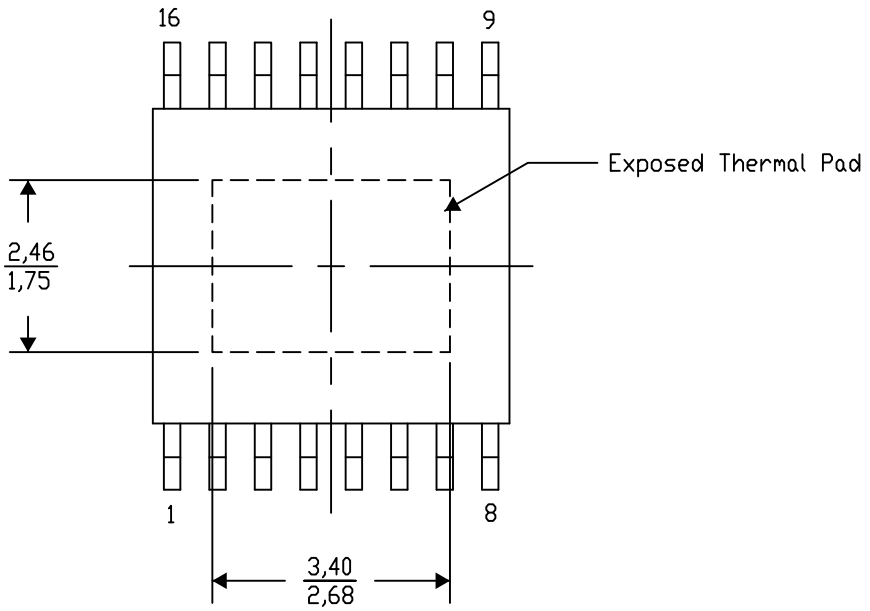
PWP (R–PDSO–G16) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

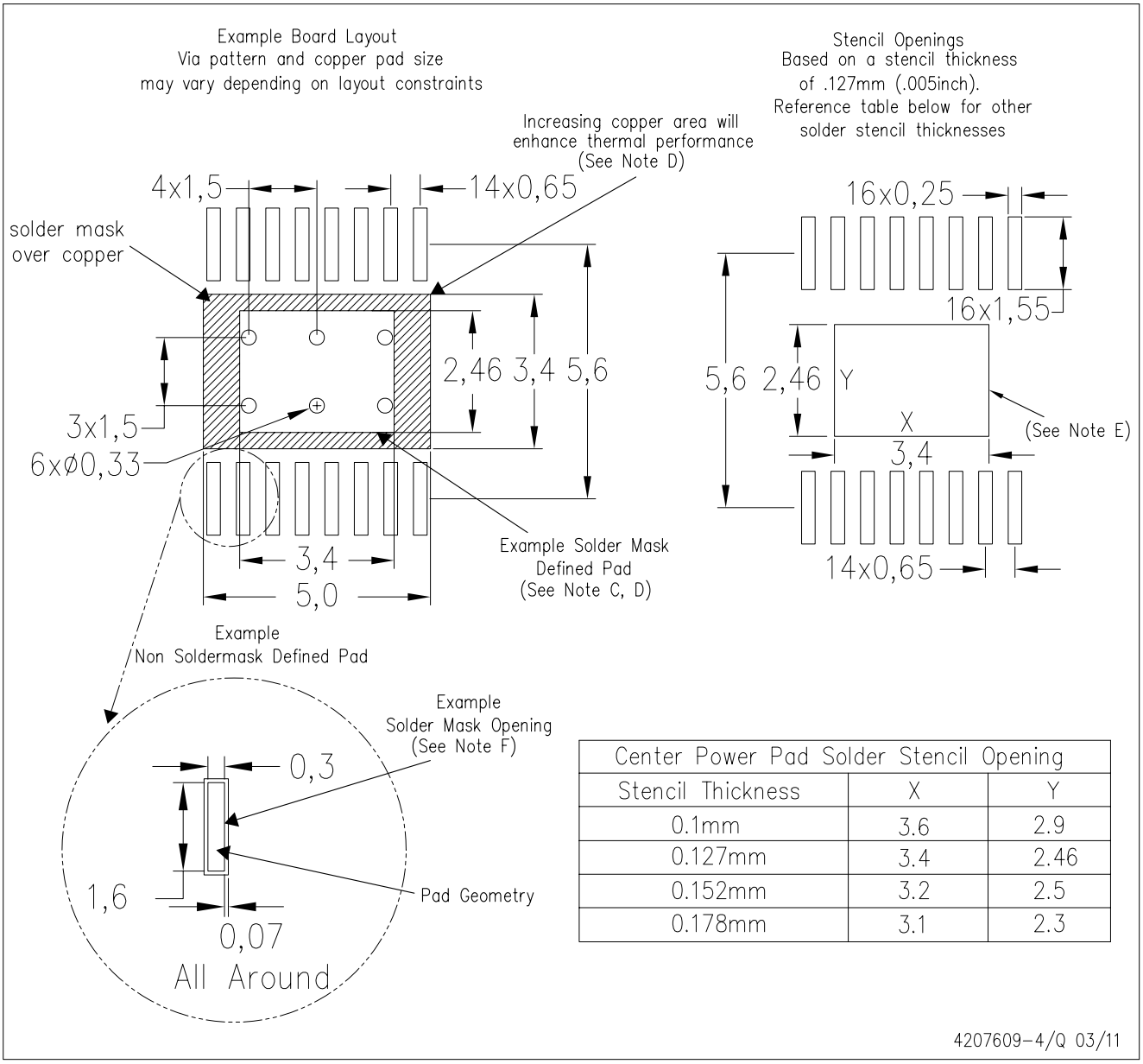
Exposed Thermal Pad Dimensions

4206332–7/AC 07/12

NOTE: A. All linear dimensions are in millimeters

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PWP (R–PDSO–G16) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.6	2.9
0.127mm	3.4	2.46
0.152mm	3.2	2.5
0.178mm	3.1	2.3

4207609–4/Q 03/11

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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