Dual Full Bridge PWM Motor Driver

Check for Samples: DRV8402

FEATURES

- **High-Efficiency Power Stage (up to 96%) with Low $R_{DS(on)}$ MOSFETs (80 mΩ at T_J = 25°C)**
- **Operating Supply Voltage up to 50 V (65 V Absolute Maximum)**
- **10 A Continuous Output Current and 24 A Peak Current per Device**
- **PWM Operating Frequency up to 500 kHz**
- **Integrated Self-Protection Circuits**
- **Programmable Cycle-by-Cycle Current Limit Protection**
- **Independent Supply and Ground Pins for Each Half Bridge**
- **Intelligent Gate Drive and Cross Conduction Prevention**
- **No External Snubber or Schottky Diode is Required**
- **Thermally Enhanced DKD (36-pin PSOP3) Package**

APPLICATIONS

- **Brushed DC, Brushless DC, and Stepper Motors**
- **Three Phase Permanent Magnet Synchronous Motors**
- **Robotic and Haptic Control System**
- **Actuators and Pumps**
- **Precision Instruments**
- **TEC Drivers**

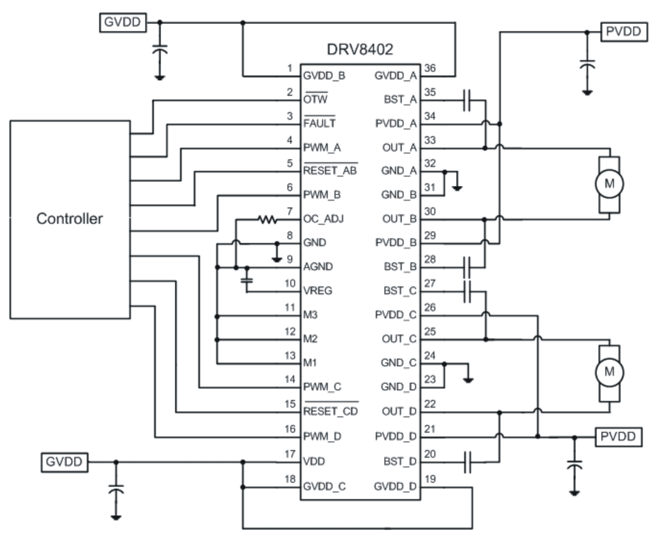
DESCRIPTION

The DRV8402 is a high performance, integrated dual full bridge motor driver with an advanced protection system. Because of the low $R_{DS(on)}$ and intelligent gate drive design, the efficiency of this motor driver can be up to 96%, which enables the use of smaller power supplies and heatsinks, and is a good candidate for energy efficient applications. This device requires two power supplies, one at 12V for GVDD and VDD, and one up to 50V for PVDD. The DRV8402 is capable of driving 5 A continuous RMS current and 12 A peak current per full bridge with low idle power dissipation. It can also be used for up to 10 A continuous current and 24 A peak current in parallel full bridge operation.

The DRV8402 can operate at up to 500 kHz switching frequency while still maintaining precise control and high efficiency. It also has an innovative protection system integrated on-chip, safeguarding the device against a wide range of fault conditions that could damage the system. These safeguards are short-circuit protection, overcurrent protection, undervoltage protection, and two-stage thermal protection. The DRV8402 has a current-limiting circuit that prevents device shutdown during load transients such as motor start-up. A programmable overcurrent detector allows adjustable current limit and protection level to meet different motor requirements.

The DRV8402 has unique independent supply and ground pins for each half bridge, which makes it possible to provide current measurement through external shunt resistor and support multiple motors with different power supply voltage requirements.

Simplified Application Diagram



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range unless otherwise noted (1)

PARAMETER	VALUE
VDD to AGND	–0.3 V to 13.2 V
GVDD_X to AGND	–0.3 V to 13.2 V
PVDD_X to GND_X (2)	–0.3 V to 65 V
OUT_X to GND_X (2)	–0.3 V to 65V
BST_X to GND_X (2)	–0.3 V to 75 V
Transient peak output current (per pin), pulse width limited by internal over-current protection circuit.	15 A
VREG to AGND	–0.3 V to 4.2 V
GND_X to GND	–0.3 V to 0.3 V
GND_X to AGND	–0.3 V to 0.3 V
GND to AGND	–0.3 V to 0.3 V
PWM_X, OC_ADJ, M1, M2, M3 to AGND	–0.3 V to 4.2 V
$\overline{\text{RESET\_X}}$, $\overline{\text{FAULT}}$, $\overline{\text{OTW}}$ to AGND	–0.3 V to 7 V
Maximum continuous sink current ($\overline{\text{FAULT}}$, $\overline{\text{OTW}}$)	9 mA
Maximum operating junction temperature range, T_J	–40°C to 150°C
Storage temperature, T_{stg}	–55°C to 150°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) These voltages represent the dc voltage + peak ac waveform measured at the terminal of the device in all conditions.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	DESCRIPTION	MIN	NOM	MAX	UNIT
PVDD_X	Half bridge X (A, B, C, or D) DC supply voltage	0	50	52.5	V
GVDD_X	Supply for logic regulators and gate-drive circuitry	11.4	12.3	13.2	V
VDD	Digital regulator input	11.4	12.3	13.2	V
I_{O_pulse}	Pulsed peak current per output pin			12	A
I_O	Continuous current per output pin			5	A
F_{SW}	PWM switching frequency			500	kHz
L_O	Minimum output inductance under short-circuit condition and parallel mode		4		μH
R_{OCP_CBC}	OC programming resistor range in cycle by cycle current limit modes, Resistor tolerance = 5%	27		39	kΩ
R_{OCP_OCL}	OC programming resistor range in OC latching shutdown modes, Resistor tolerance = 5%	22		39	kΩ
T_A	Operating ambient temperature	-40		85	°C

Package Heat Dissipation Ratings

PARAMETER	VALUE
$R_{\theta JC}$, junction-to-case (heat slug) thermal resistance (all bridges running)	1°C/W
$R_{\theta JA}$, junction-to-ambient thermal resistance	This device is not intended to be used without a heatsink. Therefore, $R_{\theta JA}$ is not specified. See the *Thermal Information* section.
Exposed heat slug area	80 mm^2

DEVICE INFORMATION

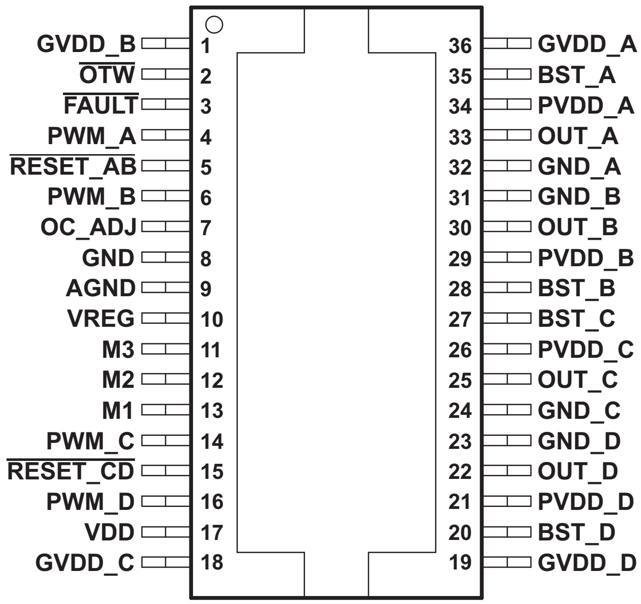
Pin Assignment

The DRV8402 is available in a thermally enhanced package:

- 36-pin PSOP3 package (DKD)

This package contains a heat slug that is located on the top side of the device for convenient thermal coupling to the heatsink.

DKD PACKAGE
(TOP VIEW)



MODE Selection Pins

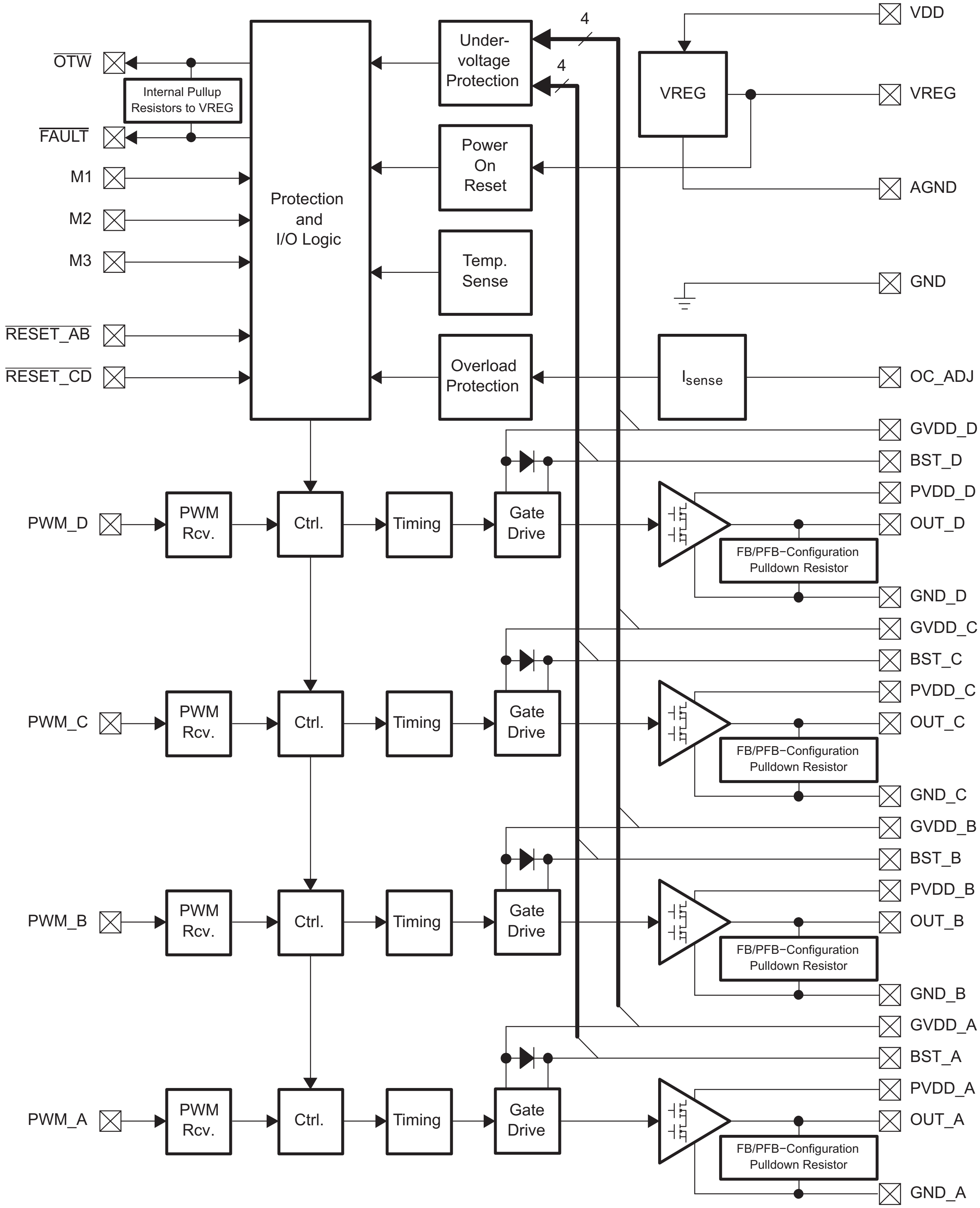
MODE PINS			OUTPUT CONFIGURATION	DESCRIPTION
M3	M2	M1		
0	0	0	2 FB	Dual full bridge with cycle-by-cycle current limit
0	0	1	2 FB	Dual full bridge with OC latching shutdown (no cycle-by-cycle current limit)
0	1	0	1 PFB	Parallel full bridge with cycle-by-cycle current limit
0	1	1	1 PFB	Parallel full bridge with OC latching shutdown
1	0	0	4 HB	Half bridge with cycle-by-cycle current limit. Protection works similarly to full bridge mode. Only difference in half bridge mode is that OUT_X is Hi-Z instead of a pulldown through internal pulldown resistor when RESET pin is low.
1	0	1	4 HB	Half bridge with OC latching shutdown. Protection works similarly to full bridge mode. Only difference in half bridge mode is that OUT_X is Hi-Z instead of a pulldown through internal pulldown resistor when RESET pin is low.
1	1	0	Reserved	
1	1	1		

Pin Functions

PIN		FUNCTION (1)	DESCRIPTION
NAME	DKD NO.		
AGND	9	P	Analog ground
BST_A	35	P	High side bootstrap supply (BST), external capacitor to OUT_A required
BST_B	28	P	High side bootstrap supply (BST), external capacitor to OUT_B required
BST_C	27	P	High side bootstrap supply (BST), external capacitor to OUT_C required
BST_D	20	P	High side bootstrap supply (BST), external capacitor to OUT_D required
GND	8	P	Ground
GND_A	32	P	Power ground for half-bridge A
GND_B	31	P	Power ground for half-bridge B
GND_C	24	P	Power ground for half-bridge C
GND_D	23	P	Power ground for half-bridge D
GVDD_A	36	P	Gate-drive voltage supply requires 0.1-μF capacitor to AGND
GVDD_B	1	P	Gate-drive voltage supply requires 0.1-μF capacitor to AGND
GVDD_C	18	P	Gate-drive voltage supply requires 0.1-μF capacitor to AGND
GVDD_D	19	P	Gate-drive voltage supply requires 0.1-μF capacitor to AGND
M1	13	I	Mode selection pin
M2	12	I	Mode selection pin
M3	11	I	Mode selection pin
OC_ADJ	7	O	Analog overcurrent programming pin requires resistor to ground
$\overline{\text{OTW}}$	2	O	Overtemperature warning signal, open-drain, active-low
OUT_A	33	O	Output, half-bridge A
OUT_B	30	O	Output, half-bridge B
OUT_C	25	O	Output, half-bridge C
OUT_D	22	O	Output, half-bridge D
PVDD_A	34	P	Power supply input for half-bridge A requires close decoupling of 0.01-μF capacitor in parallel with a 1.0-μF capacitor to GND_A.
PVDD_B	29	P	Power supply input for half-bridge B requires close decoupling of 0.01-μF capacitor in parallel with a 1.0-μF capacitor to GND_B.
PVDD_C	26	P	Power supply input for half-bridge C requires close decoupling of 0.01-μF capacitor in parallel with a 1.0-μF capacitor to GND_C.
PVDD_D	21	P	Power supply input for half-bridge D requires close decoupling of 0.01-μF capacitor in parallel with a 1.0-μF capacitor to GND_D.
PWM_A	4	I	Input signal for half-bridge A
PWM_B	6	I	Input signal for half-bridge B
PWM_C	14	I	Input signal for half-bridge C
PWM_D	16	I	Input signal for half-bridge D
$\overline{\text{RESET\_AB}}$	5	I	Reset signal for half-bridge A and half-bridge B, active-low
$\overline{\text{RESET\_CD}}$	15	I	Reset signal for half-bridge C and half-bridge D, active-low
$\overline{\text{FAULT}}$	3	O	Fault signal, open-drain, active-low
VDD	17	P	Power supply for digital voltage regulator requires a 47-μF capacitor in parallel with a 0.1-μF capacitor to GND for decoupling.
VREG	10	P	Digital regulator supply filter pin requires 0.1-μF capacitor to AGND.

(1) I = input, O = output, P = power

SYSTEM BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Ta = 25 °C, PVDD = 50 V, GVDD = VDD = 12 V, F_{Sw} = 400 kHz, unless otherwise noted. All performance is in accordance with recommended operating conditions unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Internal Voltage Regulator and Current Consumption						
V_{REG}	Voltage regulator, only used as a reference node	VDD = 12 V	2.95	3.3	3.65	V
I_{VDD}	VDD supply current	Idle, reset mode		9	12	mA
I_{GVDD_X}	Gate supply current per half-bridge	Reset mode		1.7	2	mA
I_{PVDD_X}	Half-bridge X (A, B, C, or D) idle current	Reset mode		0.5	1	mA
Output Stage						
$R_{DS(on)}$	MOSFET drain-to-source resistance, low side (LS)	T_J = 25°C, includes metallization resistance, GVDD = 12 V		90		mΩ
	MOSFET drain-to-source resistance, high side (HS)	T_J = 25°C, includes metallization resistance, GVDD = 12 V		90		mΩ
V_F	Diode forward voltage drop	T_J = 25°C - 125°C, I_O = 5 A		1		V
t_R	Output rise time	Resistive load, I_O = 5 A		9		nS
t_F	Output fall time	Resistive load, I_O = 5 A		9		nS
t_{PD_ON}	Propagation delay when FET is on	Resistive load, I_O = 5 A		42		nS
t_{PD_OFF}	Propagation delay when FET is off	Resistive load, I_O = 5 A		40		nS
t_{DT}	Dead time between HS and LS FETs	Resistive load, I_O = 5 A		5		nS
I/O Protection						
$V_{uvp,G}$	Gate supply voltage GVDD_X undervoltage protection			8.5		V
$V_{uvp,hyst}$ (1)	Hysteresis for gate supply undervoltage event			0.8		V
OTW(1)	Overtemperature warning		115	125	135	°C
OTW_{hyst} (1)	Hysteresis temperature to reset $\overline{OTW}$ event			25		°C
OTSD(1)	Overtemperature shut down			150		°C
OTE-$OTW_{differential}$ (1)	OTE-OTW overtemperature detect temperature difference			25		°C
$OTSD_{HYST}$ (1)	Hysteresis temperature for $\overline{FAULT}$ to be released following an OTSD event.			25		°C
I_{OC}	Overcurrent limit protection	Resistor—programmable, nominal, R_{OCP} = 27 kΩ		10.6		A
I_{OCT}	Overcurrent response time	Time from application of short condition to Hi-Z of affected FET(s)		250		ns
R_{PD}	Internal pulldown resistor at the output of each half-bridge	Connected when $\overline{RESET\_AB}$ or $\overline{RESET\_CD}$ is active to provide bootstrap capacitor charge. Not used in SE mode		1		kΩ
Static Digital Specifications						
V_{IH}	High-level input voltage	PWM_A, PWM_B, PWM_C, PWM_D, M1, M2, M3, $\overline{RESET\_AB}$, $\overline{RESET\_CD}$	2			V
V_{IL}	Low-level input voltage				0.8	V
I_{lkg}	Input leakage current		-100		100	μA
OTW / FAULT						
R_{INT_PU}	Internal pullup resistance, $\overline{OTW}$ to VREG, $\overline{FAULT}$ to VREG		20	26	35	kΩ
V_{OH}	High-level output voltage	Internal pullup resistor only	2.95	3.3	3.65	V
		External pullup of 4.7 kΩ to 5 V	4.5		5	
V_{OL}	Low-level output voltage	I_O = 4 mA		0.2	0.4	V

(1) Specified by design

TYPICAL CHARACTERISTICS

EFFICIENCY
vs
SWITCHING FREQUENCY

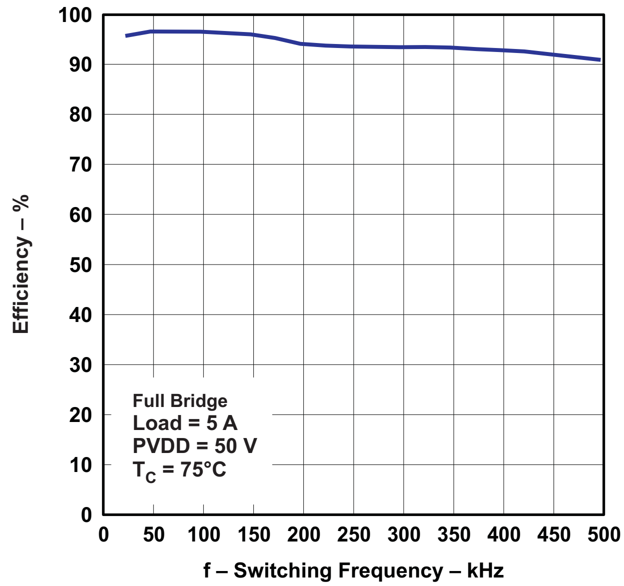


Figure 1.

NORMALIZED $R_{DS(on)}$
vs
GATE DRIVE, GVDD

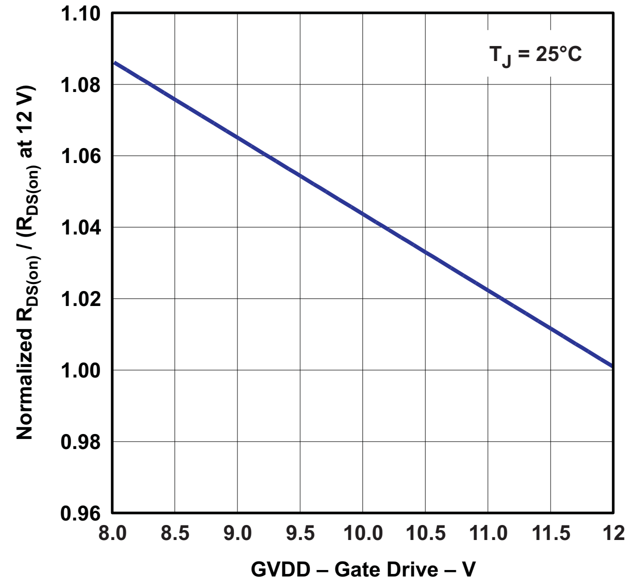


Figure 2.

NORMALIZED $R_{DS(on)}$
vs
JUNCTION TEMPERATURE

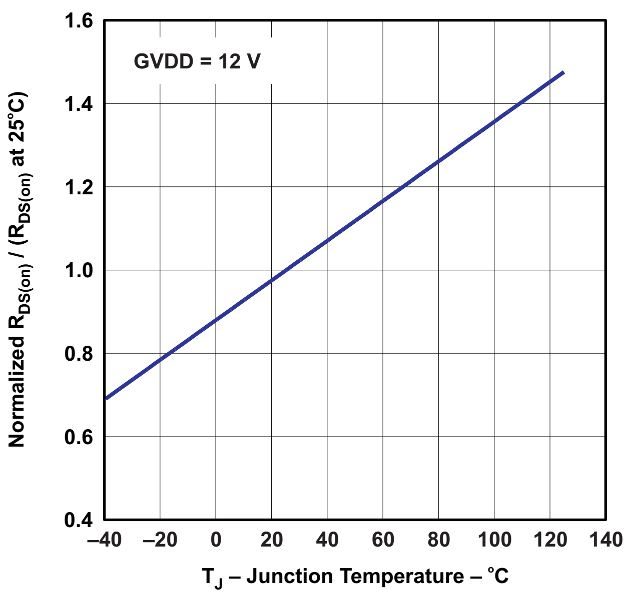


Figure 3.

DRAIN TO SOURCE DIODE FORWARD
ON CHARACTERISTICS

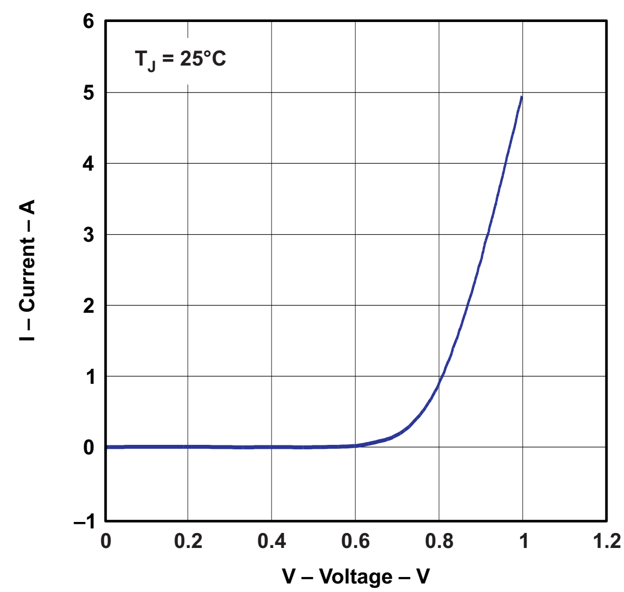


Figure 4.

TYPICAL CHARACTERISTICS (continued)

OUTPUT DUTY CYCLE
vs
INPUT DUTY CYCLE

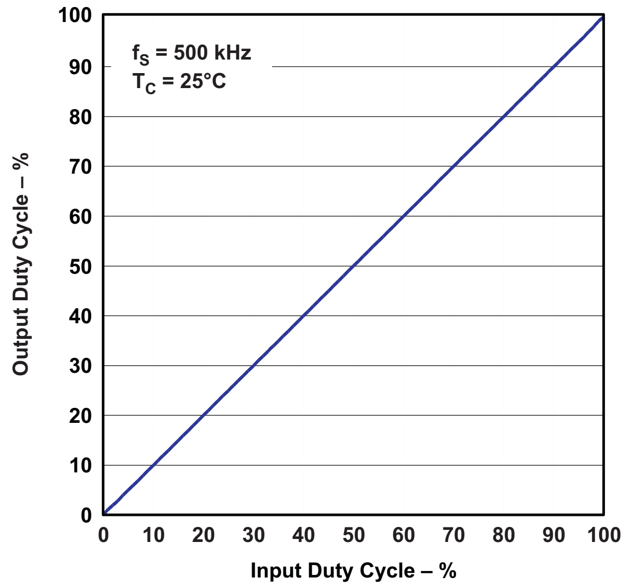


Figure 5.

THEORY OF OPERATION

POWER SUPPLIES

To help with system design, the DRV8402 needs only a 12 V supply in addition to power-stage supply. An internal voltage regulator provides suitable voltage levels for the digital and low-voltage analog circuitry. Additionally, all circuitry requiring a floating voltage supply, for example, the high-side gate drive, is accommodated by built-in bootstrap circuitry requiring only a few external capacitors.

To provide electrical characteristics, the PWM signal path including gate drive and output stage is designed as identical, independent half-bridges. For this reason, each half-bridge has separate gate drive supply (GVDD_X), bootstrap pins (BST_X), and power-stage supply pins (PVDD_X). Furthermore, an additional pin (VDD) is provided as supply for all common circuits. Although supplied from the same 12-V source, it is recommended that a 1 – 10 Ω resistor is used to separate the GVDD_X pins from VDD on the printed-circuit board (PCB). Special attention should be paid to placing all decoupling capacitors as close to their associated pins as possible. In general, inductance between the power supply pins and decoupling capacitors must be avoided.

For a properly functioning bootstrap circuit, a small ceramic capacitor must be connected from each bootstrap pin (BST_X) to the power-stage output pin (OUT_X). When the power-stage output is low, the bootstrap capacitor is charged through an internal diode connected between the gate-drive power-supply pin (GVDD_X) and the bootstrap pin. When the power-stage output is high, the bootstrap capacitor potential is shifted above the output potential and thus provides a suitable voltage supply for the high-side gate driver. In an application with PWM switching frequencies in the range from 25 kHz to 500 kHz, the use of 47 nF ceramic capacitors, size 0603 or 0805, is recommended for the bootstrap supply. These 47 nF capacitors ensure sufficient energy storage, even during minimal PWM duty cycles, to keep the high-side power stage FET fully turned on during the remaining part of the PWM cycle. In an application running at a switching frequency lower than 25 kHz, the bootstrap capacitor might need to be increased in value.

Special attention should be paid to the power-stage power supply; this includes component selection, PCB placement, and routing. As indicated, each half-bridge has independent power-stage supply pins (PVDD_X). For optimal electrical performance, EMI compliance, and system reliability, it is important that each PVDD_X pin is decoupled with a ceramic capacitor placed as close as possible to each supply pin. It is recommended to follow the PCB layout of the DRV8402 in EVM board.

The 12 V supply should be from a low-noise, low-output-impedance voltage regulator. Likewise, the 50 V power-stage supply is assumed to have low output impedance and low noise. The power-supply sequence is not critical as facilitated by the internal power-on-reset circuit. Moreover, the DRV8402 is fully protected against erroneous power-stage turn-on due to parasitic gate charging. Thus, voltage-supply ramp rates (dv/dt) are non-critical within the specified range (see the *Recommended Operating Conditions* section of this data sheet).

SYSTEM POWER-UP/POWER-DOWN SEQUENCE

Powering Up

The DRV8402 does not require a power-up sequence. The outputs of the H-bridges remain in a high-impedance state until the gate-drive supply voltage (GVDD_X) and VDD voltage are above the undervoltage protection (UVP) voltage threshold (see the *Electrical Characteristics* section of this data sheet). Although not specifically required, holding $\overline{\text{RESET\_AB}}$ and $\overline{\text{RESET\_CD}}$ in a low state while powering up the device is recommended. This allows an internal circuit to charge the external bootstrap capacitors by enabling a weak pulldown of the half-bridge output (except in half-bridge modes).

Powering Down

The DRV8402 does not require a power-down sequence. The device remains fully operational as long as the gate-drive supply (GVDD_X) voltage and VDD voltage are above the UVP voltage threshold (see the *Electrical Characteristics* section of this data sheet). Although not specifically required, it is a good practice to hold $\overline{\text{RESET\_AB}}$ and $\overline{\text{RESET\_CD}}$ low during power down to prevent any unknown state during this transition.

ERROR REPORTING

The FAULT and OTW pins are both active-low, open-drain outputs. Their function is for protection-mode signaling to a PWM controller or other system-control device.

Any fault resulting in device shutdown is signaled by the FAULT pin going low. Likewise, OTW goes low when the device junction temperature exceeds 125°C (see Table 1).

Table 1.

FAULT	OTW	DESCRIPTION
0	0	Overtemperature warning and (overtemperature shut down or overcurrent shut down or undervoltage protection) occurred
0	1	Overcurrent shut-down or undervoltage protection occurred
1	0	Overtemperature warning
1	1	Device under normal operation

Note that asserting either RESET_AB or RESET_CD low forces the FAULT signal high, independent of faults being present. For proper error reporting, set both RESET_AB and RESET_CD high during normal operation.

TI recommends monitoring the OTW signal using the system microcontroller and responding to an OTW signal by reducing the load current to prevent further heating of the device resulting in device overtemperature shutdown (OTSD).

To reduce external component count, an internal pullup resistor to 3.3 V is provided on both FAULT and OTW outputs. Level compliance for 5-V logic can be obtained by adding external pull-up resistors to 5 V (see the *Electrical Characteristics* section of this data sheet for further specifications).

DEVICE PROTECTION SYSTEM

The DRV8402 contains advanced protection circuitry carefully designed to facilitate system integration and ease of use, as well as to safeguard the device from permanent failure due to a wide range of fault conditions such as short circuits, overcurrent, overtemperature, and undervoltage. The DRV8402 responds to a fault by immediately setting the power stage in a high-impedance (Hi-Z) state and asserting the FAULT pin low. In situations other than overcurrent or overtemperature, the device automatically recovers when the fault condition has been removed or the gate supply voltage has increased. For highest possible reliability, recovering from an overcurrent shut down (OCSD) or OTSD fault requires external reset of the device (see the *Device Reset* section of this data sheet) no sooner than 1 second after the shutdown.

Bootstrap Capacitor Under Voltage Protection

When the device runs at a low switching frequency (e.g. less than 20 kHz with 47 nF bootstrap capacitor), the bootstrap capacitor voltage might not be able to maintain a proper voltage level for the high-side gate driver. A bootstrap capacitor undervoltage protection circuit (BST_UVP) will start under this circumstance to prevent the potential failure of the high-side MOSFET. When the voltage on the bootstrap capacitors is less than required for safe operation, the DRV8402 will initiate bootstrap capacitor recharge sequences (turn off high side FET for a short period) until the bootstrap capacitors are properly charged for safe operation. This function may also be activated when PWM duty cycle is too high (e.g. higher than 99.5%). Note that bootstrap capacitor might not be able to be charged up if no load is presented at output.

Because the extra pulse width to charge bootstrap capacitor is so short, that the output current disruption due to the extra charge is negligible most of the time when output inductor is present.

Overcurrent (OC) Protection

The device has independent, fast-reacting current detectors with programmable trip threshold (OC threshold) on all high-side and low-side power-stage FETs. There are two settings for OC protection through Mode selection pins: cycle-by-cycle (CBC) current limiting mode and OC latching (OCL) shut down mode.

In CBC current limiting mode, the detector outputs are monitored by two protection systems. The first protection system controls the power stage in order to prevent the output current from further increasing, i.e., it performs a CBC current-limiting function rather than prematurely shutting down the device. This feature could effectively limit the inrush current during motor start-up or transient without damaging the device. During short to power and short to ground condition, the current limit circuitry might not be able to control the current in a proper level, a second protection system triggers a latching shutdown, resulting in the power stage being set in the high-impedance (Hi-Z) state. Current limiting and overcurrent protection are independent for half-bridges A, B, C, and, D, respectively.

In OCL shut down mode, the cycle-by-cycle current limit and error recovery circuitry is disabled and an overcurrent condition will cause the device to shutdown immediately. After shutdown, RESET_AB and/or RESET_CD must be asserted to restore normal operation after the overcurrent condition is removed.

For added flexibility, the OC threshold is programmable within a limited range using a single external resistor connected between the OC_ADJ pin and AGND pin. See Table 2 for information on the correlation between programming-resistor value and the OC threshold. It should be noted that a properly functioning overcurrent detector assumes the presence of a proper inductor at the power-stage output (minimum 2 µH). Short-circuit protection is not provided directly at the output pins of the power stage, but only after the inductor. If a further smaller inductor is preferred for any reason, using OCL mode setting is recommended.

Table 2.

OC-Adjust Resistor Values (kΩ)	Max. Current Before OC Occurs (A)
22 (1)	12.2
24 (1)	11.5
27	10.6
30	9.9
33	9.3
36	8.7
39	8.2

(1) Recommended to use in OCL Mode Only

Overtemperature Protection

The DRV8402 has a two-level temperature-protection system that asserts an active-low warning signal (OTW) when the device junction temperature exceeds 125°C (nominal) and, if the device junction temperature exceeds 150°C (nominal), the device is put into thermal shutdown, resulting in all half-bridge outputs being set in the high-impedance (Hi-Z) state and FAULT being asserted low. OTSD is latched in this case and RESET_AB and RESET_CD must be asserted low.

Undervoltage Protection (UVP) and Power-On Reset (POR)

The UVP and POR circuits of the DRV8402 fully protect the device in any power-up/down and brownout situation. While powering up, the POR circuit resets the overcurrent circuit and ensures that all circuits are fully operational when the GVDD_X and VDD supply voltages reach 9.8 V (typical). Although GVDD_X and VDD are independently monitored, a supply voltage drop below the UVP threshold on any VDD or GVDD_X pin results in all half-bridge outputs immediately being set in the high-impedance (Hi-Z) state and FAULT being asserted low. The device automatically resumes operation when all supply voltage on the bootstrap capacitors have increased above the UVP threshold.

DEVICE RESET

Two reset pins are provided for independent control of half-bridges A/B and C/D. When RESET_AB is asserted low, all four power-stage FETs in half-bridges A and B are forced into a high-impedance (Hi-Z) state. Likewise, asserting RESET_CD low forces all four power-stage FETs in half-bridges C and D into a high-impedance state.

In full bridge and parallel full bridge configurations, to accommodate bootstrap charging prior to switching start, asserting the reset inputs low enables weak pulldown of the half-bridge outputs. In half bridge configuration, the weak pulldowns are not enabled, and it is, therefore, recommended to precharge bootstrap capacitor by providing a low pulse on the PWM inputs first when reset is asserted high.

Asserting either reset input low removes any fault information to be signaled on the FAULT output, i.e., FAULT is forced high.

A rising-edge transition on either reset input allows the device to resume operation after an overcurrent fault.

DIFFERENT MODE OPERATIONS

The DRV8402 supports three different mode operations:

1. Full bridge (FB) mode
2. Parallel full bridge (PFB) mode
3. Half bridge (HB) mode

In full bridge and half bridge modes, PWM_A controls half bridge A, PWM_B controls both half bridge B, etc. Figure 6 shows an application example for full bridge mode operation.

In parallel full bridge mode, PWM_A controls both half bridge A and B, and PWM_B controls both half bridge C and D, while PWM_C and PWM_D pins are not used (recommended to connect to ground). Bridges A and B are synchronized internally (even during CBC), and so as bridges C and D. OUT_A and OUT_B should be connected together and OUT_C and OUT_D should be connected together after a small output inductor. Figure 7 shows an example of parallel full bridge mode connection.

Mode pins are configured as CBC current limit operation in Figure 6 and Figure 7.

The DRV8402 can be also used in three phase permanent magnet synchronous motor (PMSM) applications. Because each half bridge has independent supply and ground pins, a shunt sensing resistor can be inserted between PVDD to PVDD_X or GND to GND_X. A high side shunt resistor between PVDD and PVDD_X is recommended for differential current sensing because a high bias voltage on the low side sensing could affect device operation. OCL mode is recommended for a three phase application. Figure 8 shows a three-phase application example.

A decoupling capacitor close to each supply pin is recommended for each application (not shown in diagrams).

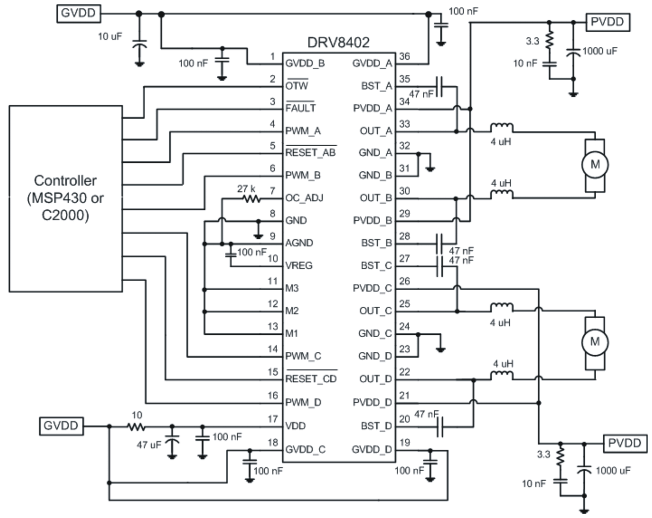
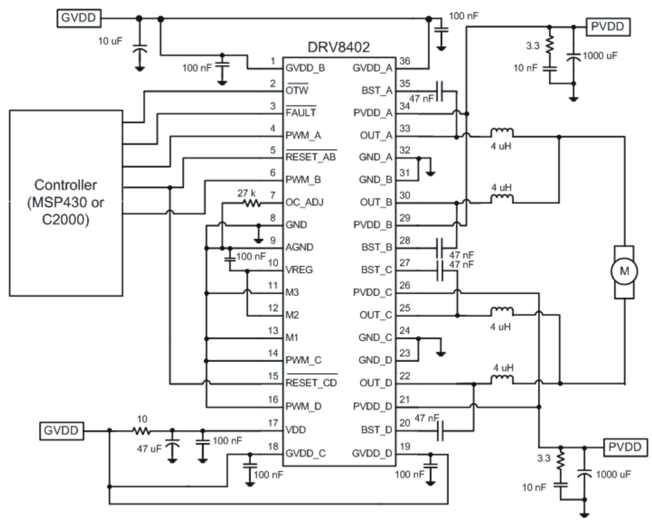


Figure 6. Application Diagram Example for Full Bridge Mode Operation



PWM_A controls OUT_A and OUT_B;
PWM_B controls OUT_C and OUT_D.

Figure 7. Application Diagram Example for Parallel Full Bridge Mode Operation

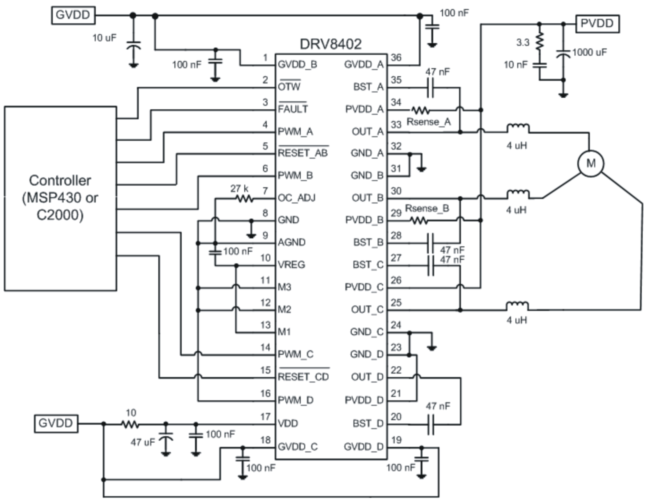


Figure 8. Application Diagram Example for Three Phase PMSM Operation

THERMAL INFORMATION

The thermally enhanced package provided with the DRV8402 is designed to interface directly to heat sink using a thermal interface compound, (e.g., Arctic Silver, TIMTronics 413, Ceramic thermal compound, etc.). The heat sink then absorbs heat from the ICs and couples it to the local air.

$R_{\theta JA}$ is a system thermal resistance from junction to ambient air. As such, it is a system parameter with the following components:

- $R_{\theta JC}$ (the thermal resistance from junction to case, or in this example the heat slug)
- Thermal grease thermal resistance
- Heat sink thermal resistance

The thermal grease thermal resistance can be calculated from the exposed heat slug area and the thermal grease manufacturer's area thermal resistance (expressed in °C-in^2/W or °C-mm^2/W). The approximate exposed heat slug size is as follows:

- DRV8402, 36-pin PSOP3 …… 0.124 in^2 (80 mm^2)

The thermal resistance of thermal pads is considered higher than a thin thermal grease layer. Thermal tape has an even higher thermal resistance and should not be used at all. Heat sink thermal resistance is predicted by the heat sink vendor, modeled using a continuous flow dynamics (CFD) model, or measured.

Thus the system $R_{\theta JA}$ = $R_{\theta JC}$ + thermal grease resistance + heat sink resistance.

See the TI application report, *IC Package Thermal Metrics* (SPRA953A), for more thermal information.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV8402DKD	NRND	HSSOP	DKD	36	29	Green (RoHS & no Sb/Br)	NIPDAU	Level-4-260C-72 HR	-40 to 85	DRV8402	
DRV8402DKDR	NRND	HSSOP	DKD	36	500	Green (RoHS & no Sb/Br)	NIPDAU	Level-4-260C-72 HR	-40 to 85	DRV8402	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

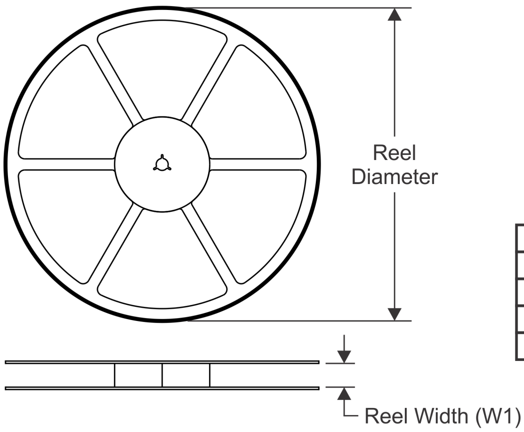
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

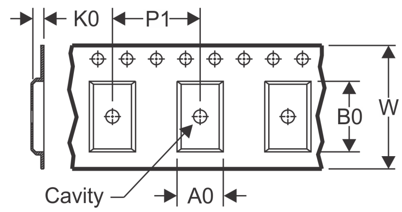
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

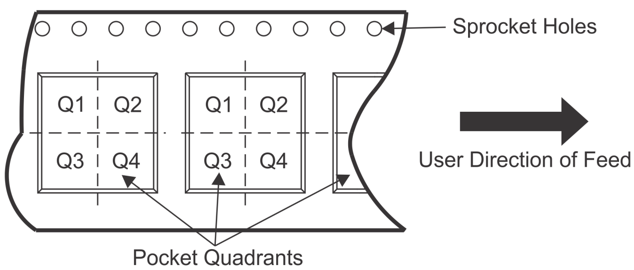


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

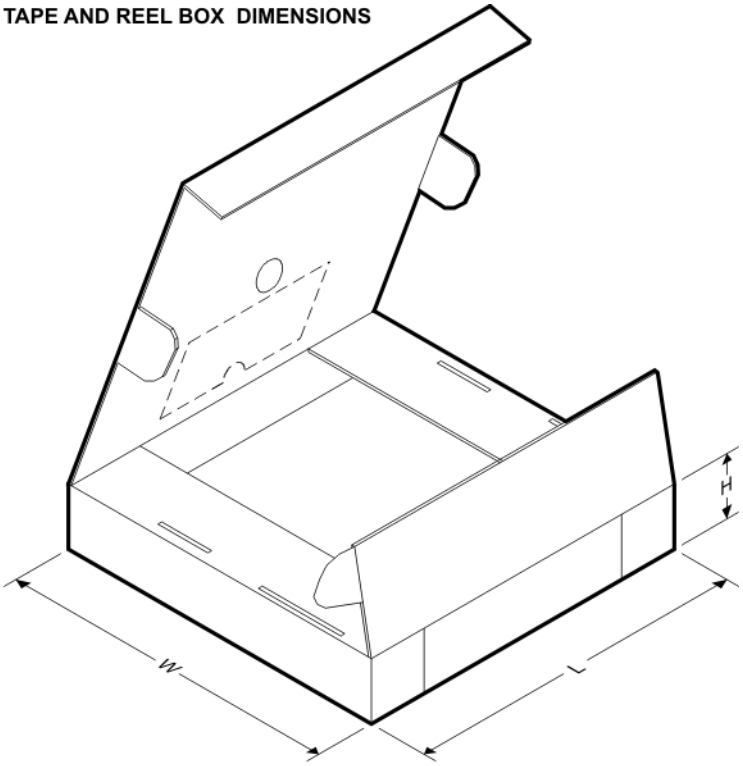
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8402DKDR	HSSOP	DKD	36	500	330.0	24.4	14.7	16.4	4.0	20.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS

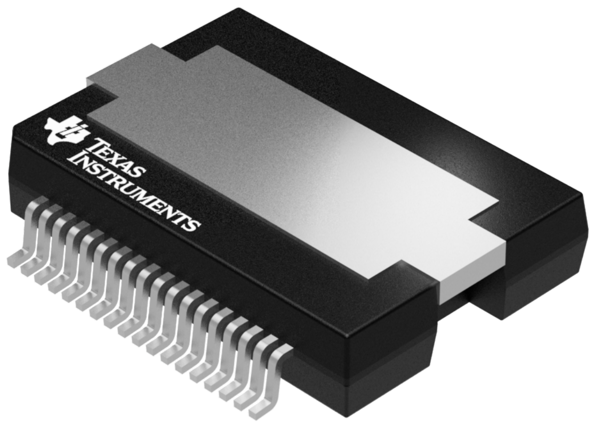


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8402DKDR	HSSOP	DKD	36	500	350.0	350.0	43.0

DKD 36 PowerPAD™ SSOP - 3.6 mm max height

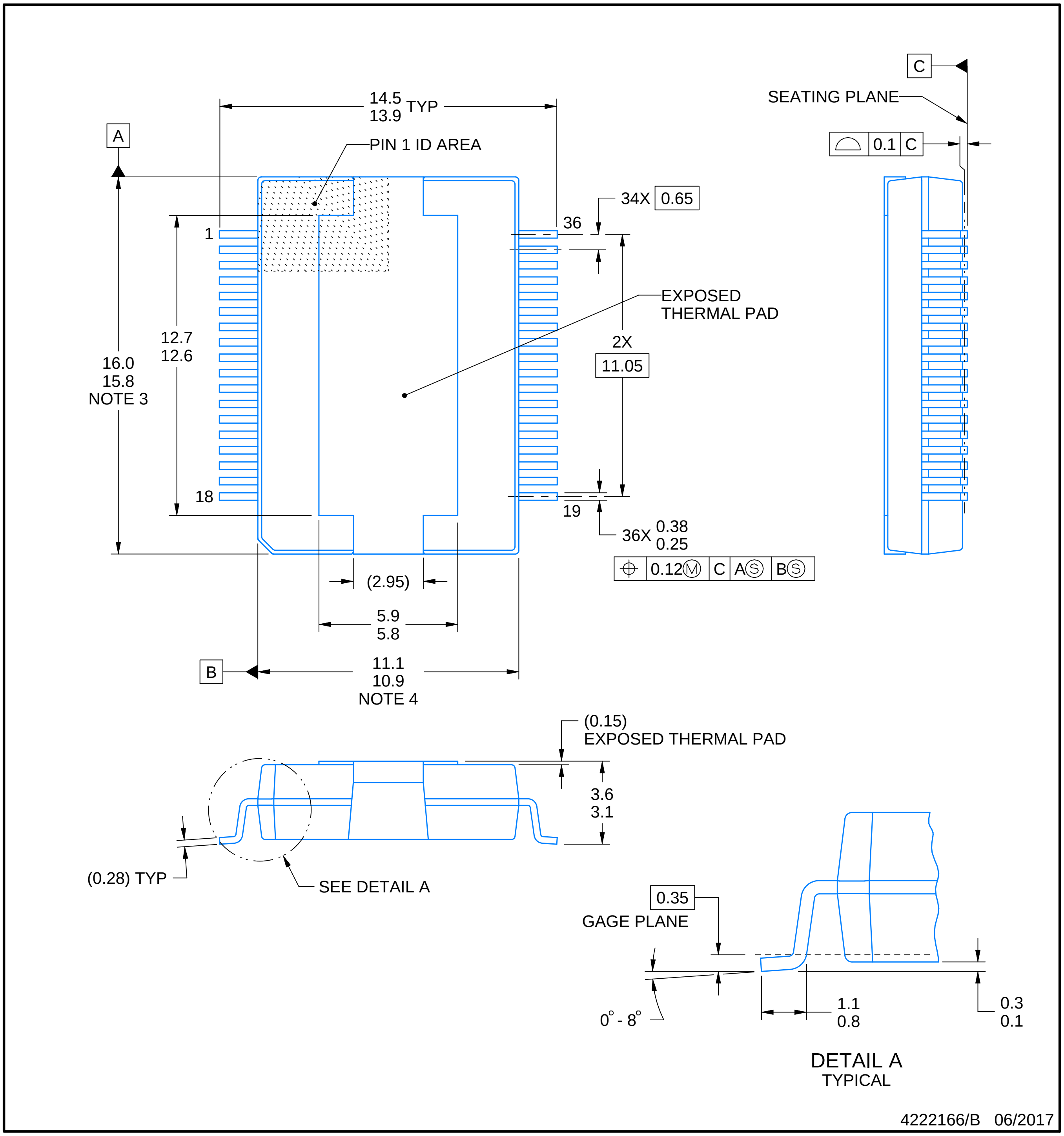
PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

PLASTIC SMALL OUTLINE

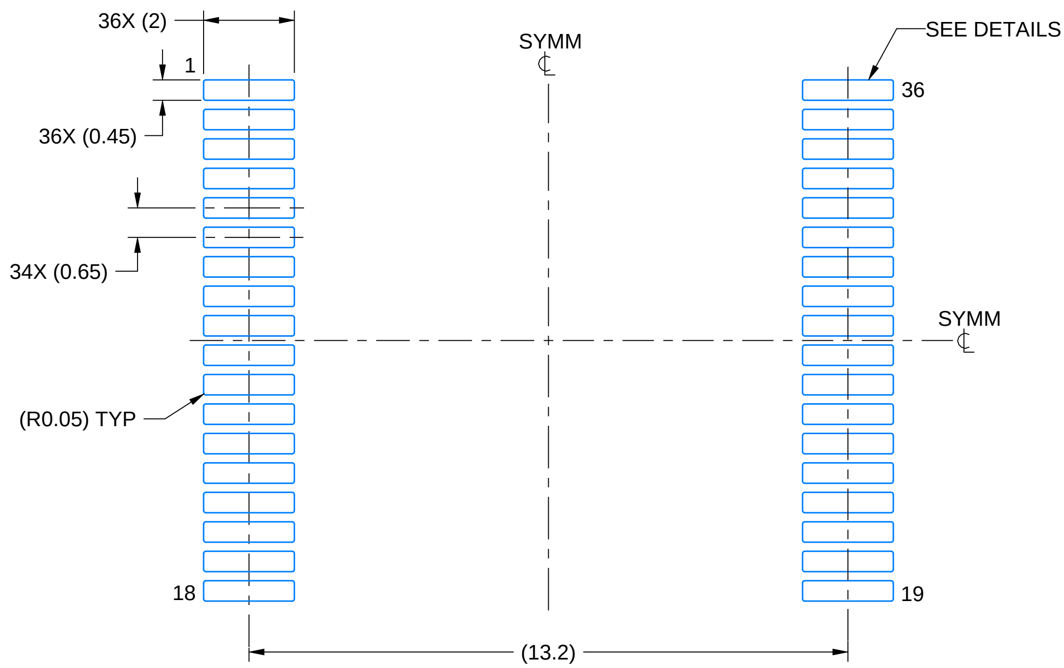


4222166/B 06/2017

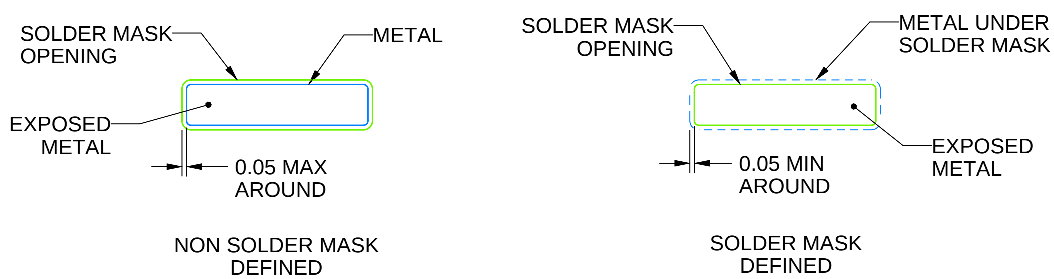
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. The exposed thermal pad is designed to be attached to an external heatsink.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X

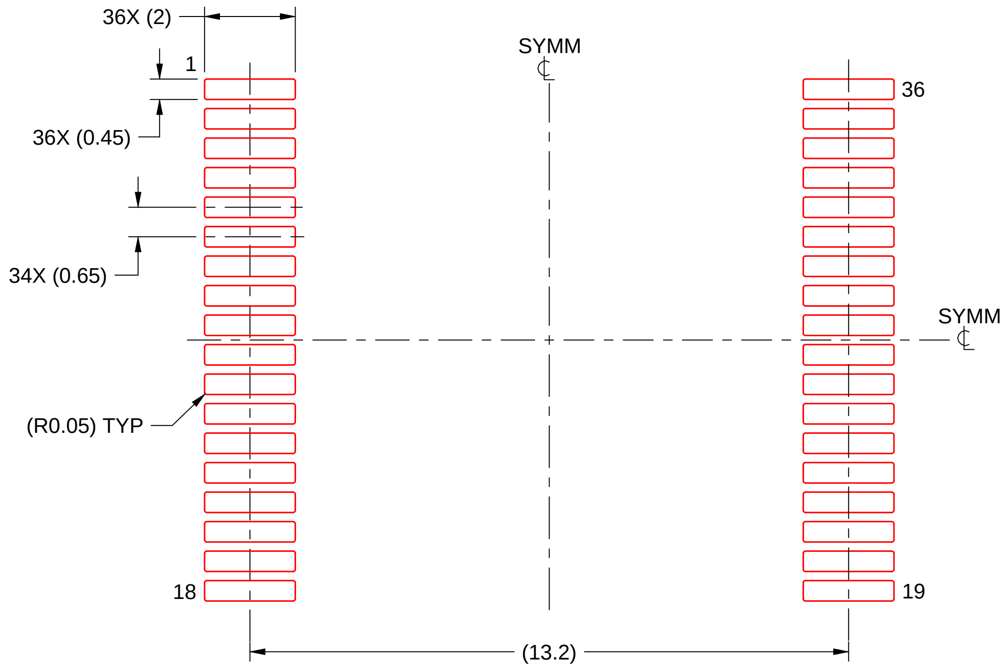


SOLDER MASK DETAILS
NOT TO SCALE

4222166/B 06/2017

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE:6X

4222166/B 06/2017

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.