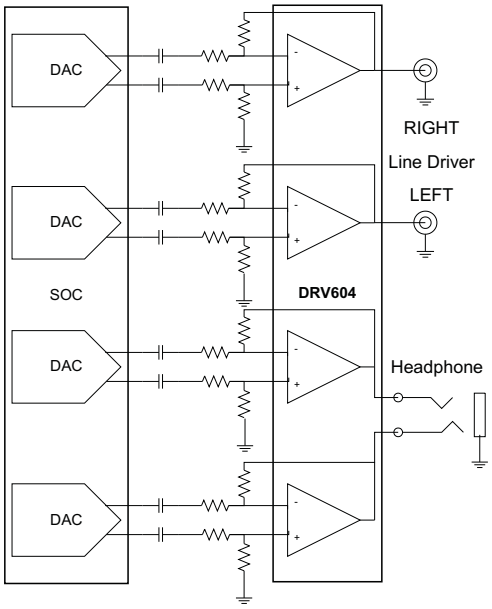
DirectPath™ 2Vrms Line Driver and HP Amp With Adjustable Gain

Check for Samples: DRV604

FEATURES

- **DirectPath™**
  - **Eliminates Pop/Clicks**
  - **Eliminate Output DC-Blocking Capacitors**
- **3.0V to 3.7V Supply Voltage**
- **Low Noise and THD**
  - **SNR > 109dB**
  - **Typical Vn < 7μVrms 20–20kHz**
  - **THD+N < 0.002% at 10kΩ**
- **Output Voltage into 5kΩ Load**
  - **2Vrms at 3.3V Supply Voltage**
- **Stereo DirectPath™ Headphone:**
  - **40mW into 32Ω at 3.3V Supply Voltage**
  - **16Ω to ∞ Ω Stable Load Range**
- **Differential Input**
- **Power Sense UVP for Brown Out Protection**
- **Short Circuit and Thermal Protection**
- **±8kV IEC ESD Protection**
- **Footprint Compatible with DRV602 and DRV603**
- **Supports Dual Line Driver Configuration**



APPLICATIONS

- **LCD and PDP TV**
- **Blu-ray Disc™, DVD Players**
- **Mini/Micro Combo Systems**
- **Soundcards**

DESCRIPTION

The DRV604 is a 2Vrms Pop-Free stereo line driver with stereo headphone output designed to allow the removal of the output DC-blocking capacitors for reduced component count and cost. The device is ideal for single supply electronics where size and cost are critical design parameters.

Designed using TI's patented DirectPath™ technology, The DRV604 is capable of driving 2 Vrms into a 5kΩ load. The headphone output can generate a clean 40mW into 32Ω load from a 3.3V supply.. The device has differential inputs and uses external gain setting resistors that supports a gain range of -1V/V to -10V/V. Headphone and line outputs have ±8kV IEC ESD protection enabling a simple ESD protection circuit. The DRV604 has built-in enable control for pop-free on/off control. DRV604 can monitor an external supply voltage using its built in comparator enabling it to shut down during a brown out condition before up stream audio DAC's can produce click and pop artifacts.

Using the DRV604 in audio products can reduce component count considerably compared to traditional methods of generating headphone output and 2Vrms output. The DRV604 does not require a power supply greater than 3.3V to generate its 5.6Vpp output, nor does it require a split rail power supply. The DRV604 integrates its own charge pump to generate a negative supply rail that provides a clean, pop-free ground biased 2Vrms output.

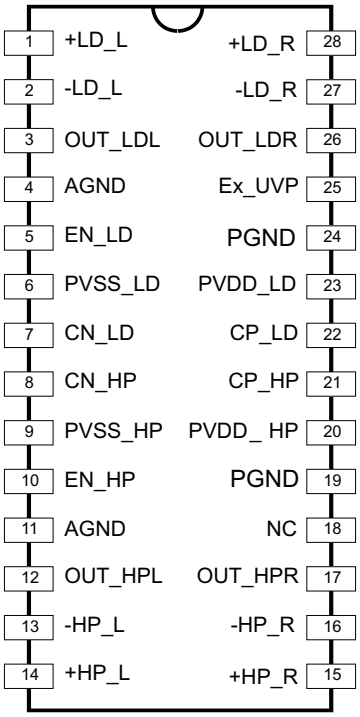
The DRV604 is available in a 28-pin HTSSOP. For a stereo line driver with no HP amp see DRV603.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DEVICE INFORMATION

PIN ASSIGNMENT

The DRV604 is available in the thermally enhanced package: 28-Pin HTSSOP package (PWP).



PIN FUNCTIONS

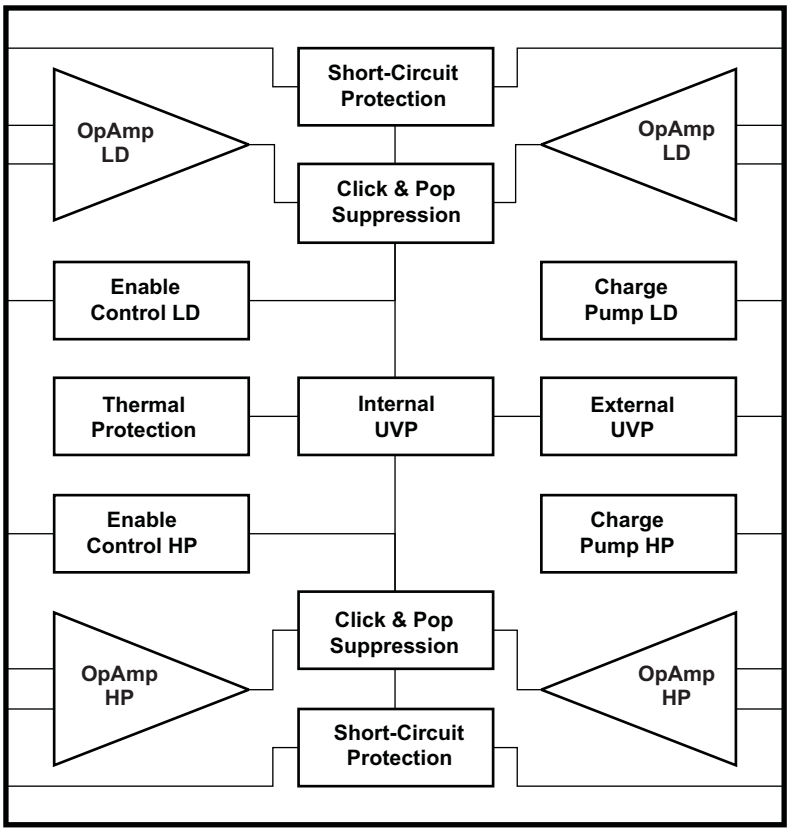
PIN		FUNCTION(1)	DESCRIPTION
NAME	PWP NO.		
+LD_L	1	I	Positive input, Line driver Left
–LD_L	2	I	Negative input, Line driver Left
OUT_LDL	3	O	Output, Line driver Left
AGND	4	P	Analog Ground
EN_LD	5	I	Enable for Line driver, active high
PVSS_LD	6	O	Charge Pump Negative Supply Voltage Output for Line Driver
CN_LD	7	I/O	Charge Pump Flying Capacitor Negative connection, Line Driver
CN_HP	8	I/O	Charge Pump Flying Capacitor Negative connection, Headphone
PVSS_HP	9	O	Headphone, Charge Pump Negative Supply Voltage Output
EN_HP	10	I	Enable for Headphone, active high
AGND	11	P	Analog Ground
OUT_HPL	12	O	Output, Headphone Left
–HP_L	13	I	Negative input, Headphone Left
+HP_L	14	I	Positive input, Headphone Left
+HP_R	15	I	Positive input, Headphone Right
–HP_R	16	I	Negative input, Headphone Right

(1) I = input, O = output, P = power

PIN FUNCTIONS (continued)

PIN		FUNCTION(1)	DESCRIPTION
NAME	PWP NO.		
OUT_HPR	17	O	Output, Headphone Right
NC	18		No connect
PGND	19	P	Charge Pump Power Ground, Headphone
PVDD_HP	20	P	Headphone Supply Voltage, connect to positive supply, internally connected to pin 23
CP_HP	21	I/O	Charge Pump Flying Capacitor Positive connection, Headphone
CP_LD	22	I/O	Charge Pump Flying Capacitor Positive connection, Line Driver
PVDD_LD	23	P	Line Driver Supply Voltage, connect to positive supply, internally connected to pin 20
PGND	24	P	Charge Pump Power Ground, Line Driver
Ex_UVP	25	I	External Under Voltage Protection
OUT_LDR	26	O	Output, Line Driver Right
–LD_R	27	I	Negative input, Line driver Right
+LD_R	28	I	Positive input, Line driver Right

SYSTEM BLOCK DIAGRAM



ORDERING INFORMATION(1)

T_A	PACKAGE	DESCRIPTION
–40°C–85°C	DRV604PWP	28-Pin

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

	DRV604PWP	UNIT
PVDD to GND	–0.3 to 4.5	V
Input voltage, V_I	PVSS–0.3 to PVDD+0.3	V
Minimum load impedance – line outputs	1000	Ω
Minimum load impedance – headphone outputs	8	Ω
EN_LD to GND	–0.3 to PVDD+0.3	V
EN_HP to GND	–0.3 to PVDD+0.3	V
Maximum operating junction temperature range, T_J	–40 to 150	°C
Storage temperature	–40 to 150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

DISSIPATION RATINGS(1)

PACKAGE	$R_{\theta JP}$(°C/W)	$R_{\theta JA}$(°C/W)	$R_{\psi JT}$(°C/W)
DRV604PWP	0.72	28	0.45

(1) PowerPAD soldered to TI recommended board.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
PVDD	Power supply	DC supply voltage	3.0	3.3	3.7	V
R_L (HP)	Load impedance		32	32		Ω
R_L (LD)			5	10		kΩ
V_{IL}	Low level input voltage	EN_LD, EN_HP	38	40	43	%PVDD
V_{IH}	High level input voltage	EN_LD, EN_HP	57	60	66	%PVDD
T_A	Free-air temperature		–40	25	85	°C

ELECTRICAL CHARACTERISTICS

PVDD_LD = PVDD_HP = 3.3 V, R_{LD} = 5 kΩ, R_{HP} = 32 Ω, R_{FB} = 20 kΩ, R_{IN} = 10 kΩ, T_A = 25°C, Charge pump: C_{CP_LD} = C_{CP_HP} = 1.0 µF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	DRV604			UNIT
			MIN	TYP	MAX	
$\|V_{os}\|$	Output offset voltage	PVDD = 3.3 V			1	mV
PSRR	Power supply rejection ratio		70	80		dB
V_{OH}	High level output voltage	PVDD = 3.3 V	3.1			V
V_{OL}	Low level output voltage	PVDD = 3.3 V			–3.05	V
V_{uvp_on}	PVDD, undervoltage detection	Internal under-voltage detection.			2.8	V
$V_{uvp\_hysteresis}$	PVDD, undervoltage detection, hysteresis			200		mV
V_{uvp}	External undervoltage detection			1.25		V
I_{Hys}	External undervoltage detection hysteresis current			5		µA
F_{cp}	Charge pump switching frequency		260		700	kHz
$\|I_{IH}\|$	High level input current	PVDD = 3.3 V, V_{IH} = PVDD, EN_HP, EN_LD			1	µA
$\|I_{IL}\|$	low level input current	PVDD = 3.3 V, V_{IL} = 0 V, EN_HP, EN_LD			1	µA
$I_{(PVDD)}$	Supply current, no load	PVDD, EN_LD, EN_HP = 3.3 V	15	25	35	mA
	Supply current, line driver, no load	PVDD, EN_LD = 3.3 V, EN_HP = GND		12		
	Supply current, headphone, no load	PVDD, EN_LD = GND, EN_HP = 3.3 V		13		
	Supply current, disabled	PVDD = 3.3 V, EN_LD, EN_HP = GND, Ex_UVP = GND		2.5	5	
T_{sd}	Thermal shutdown			150		°C
	Thermal shutdown hysteresis			15		°C

ELECTRICAL CHARACTERISTICS, LINE DRIVER

PVDD_LD = PVDD_HP = 3.3 V, R_{load} = 5 kΩ, R_{FB} = 20 kΩ, R_{IN} = 10 kΩ, T_A = 25°C, Charge pump: C_{CP_LD} = C_{CP_HP} = 1.0 µF (unless otherwise noted)

			DRV604			UNIT
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	
V_O	Output voltage, outputs in phase	1% THD+N, f = 1 kHz, 10 kΩ load		2.1		Vrms
THD+N	Total harmonic distortion plus noise	f = 1 kHz, 10 kΩ load, V_O = 2 Vrms		0.001%		
SNR	Signal-to-noise ratio	A-weighted, AES17 filter, 2 Vrms ref		109		dB
DNR	Dynamic range	A-weighted, AES17 filter, 2 Vrms ref		109		dB
V_n	Noise voltage	A-weighted, AES17 filter		7		uV
	Slew rate			4.5		V/µS
GBW	Unity gain bandwidth			8		MHz
	Crosstalk – Line L-R & R-L	10 kΩ load, V_O = 2 Vrms		-100		dB
V_{incm_pos}	Positive common-mode input voltage			+2.0		V
V_{incm_neg}	Negative common-mode input voltage			-3.0		V
I_{limit}	Current limit	PVDD = 3.3 V		60		mA
	Maximum capacitive load			220		pF

ELECTRICAL CHARACTERISTICS, HEADPHONE

PVDD_LD = PVDD_HP = 3.3 V, R_{HP} = 32 Ω, T_A = 25°C, Charge pump: C_{CP_LD} = C_{CP_HP} = 1.0 µF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	DRV604			UNIT
			MIN	TYP	MAX	
P_O	Output power, outputs in phase	THD+N = 1%, f = 1 kHz, 32 Ω load		40		mW
V_O	Output voltage, outputs in phase	THD+N = 1%, f = 1 kHz, 32 Ω load		1.45		Vrms
THD+N	Total harmonic distortion plus noise	f = 1 kHz, 32 Ω load, P_O = 40 mW		0.02%		
		f = 1 kHz, 5 kΩ load, V_O = 2 Vrms		0.001%		
SNR	Signal-to-noise ratio	A-weighted, AES17 filter, 1.45 Vrms ref (66 mW into 32 Ω)		106		dB
		A-weighted, AES17 filter, 2 Vrms ref 5 kΩ load		109		
DNR	Dynamic range	A-weighted, AES17 filter, 1.45 Vrms ref (66 mW into 32 Ω)		106		dB
		A-weighted, AES17 filter, 2 Vrms ref 5 kΩ load		109		
V_n	Noise voltage	A-weighted, AES17 filter		7		µV
	Slew rate			4.5		V/µS
GBW	Unity gain bandwidth			8		MHz
Crosstalk	Channel to channel	f = 1 kHz, R_{load} = 32 Ω, P_O = 40 mW		75		dB
V_{incm_pos}	Positive common-mode input voltage			2.0		V
V_{incm_neg}	Negative common-mode input voltage			–3.0		V
I_{limit}	Output current limit			190		mA
	Maximum capacitive load			220		pF

TYPICAL CHARACTERISTICS, LINE DRIVER

THD+N vs OUTPUT VOLTAGE

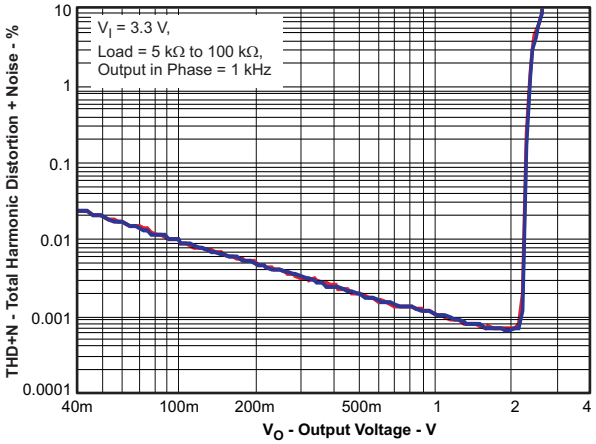


Figure 1.

THD+N vs OUTPUT VOLTAGE, LINEAR SCALE

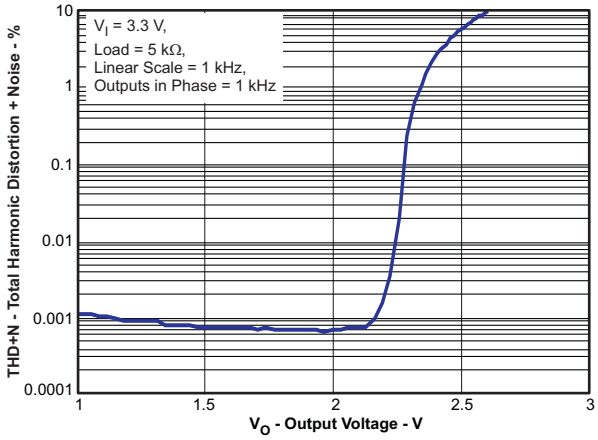


Figure 2.

THD+N vs FREQUENCY

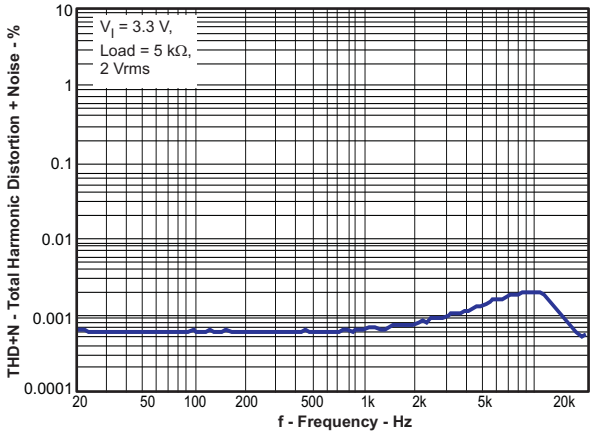


Figure 3.

CHANNEL SEPARATION

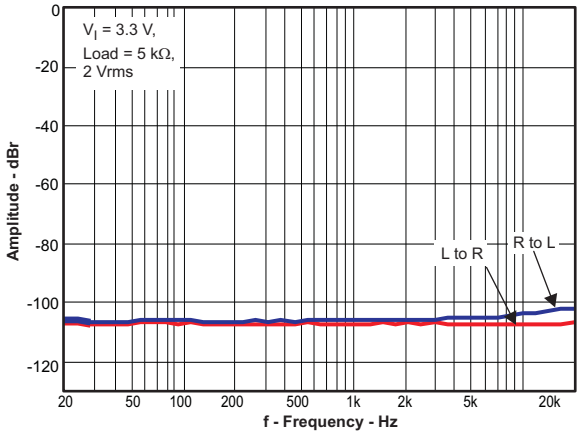


Figure 4.

HP TO LD CROSSTALK

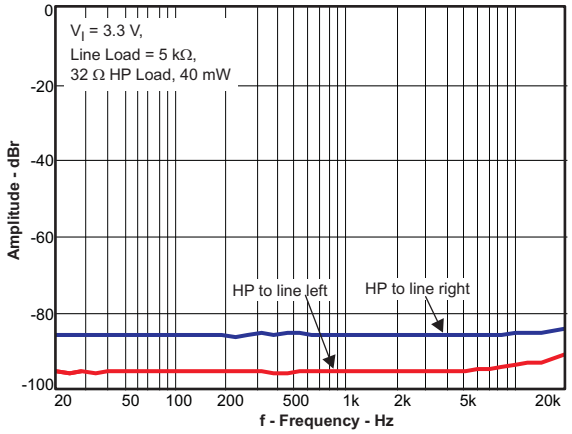


Figure 5.

AC PSRR, Ksvr

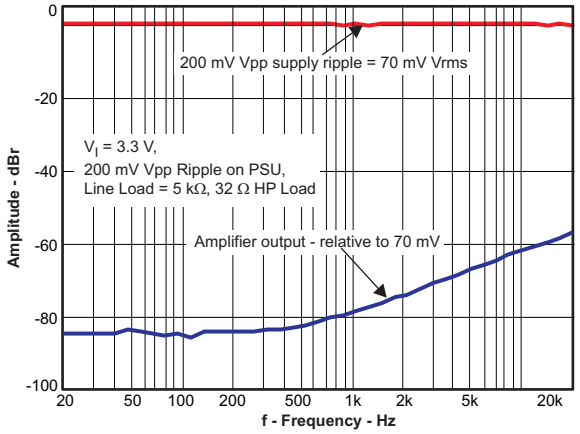


Figure 6.

TYPICAL CHARACTERISTICS, HEADPHONE

THD+N vs OUTPUT POWER

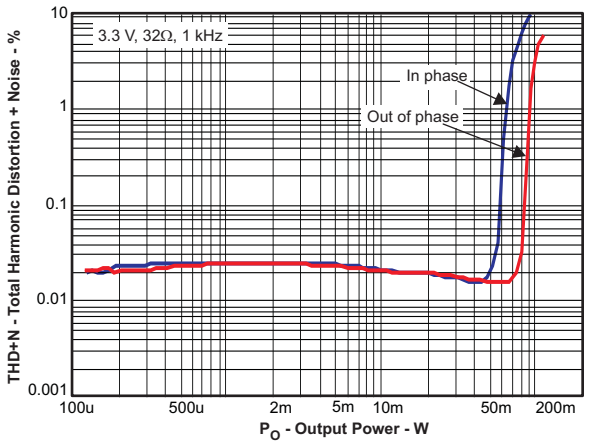


Figure 7.

THD+N vs OUTPUT POWER, LINEAR SCALE

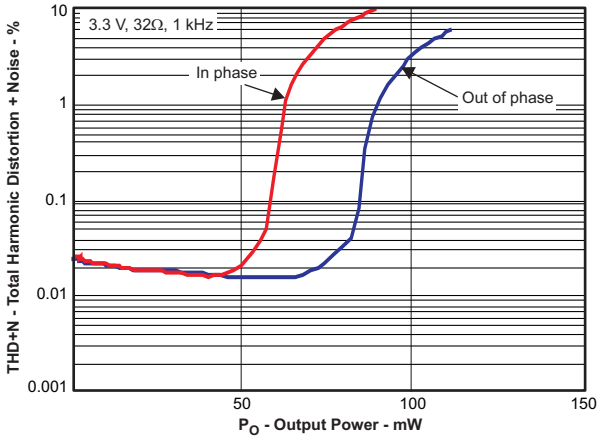


Figure 8.

CHANNEL SEPARATION

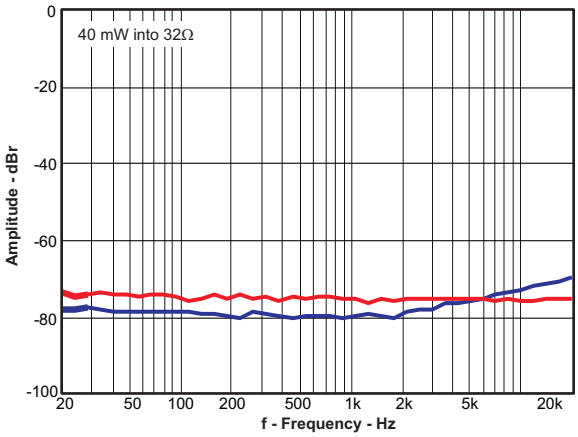


Figure 9.

LD TO HP CROSSTALK

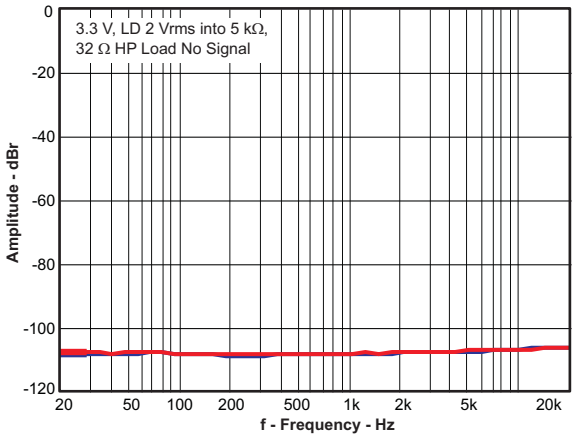


Figure 10.

START

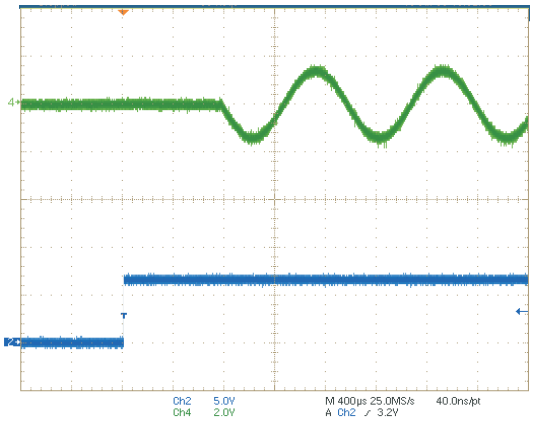


Figure 11.

STOP

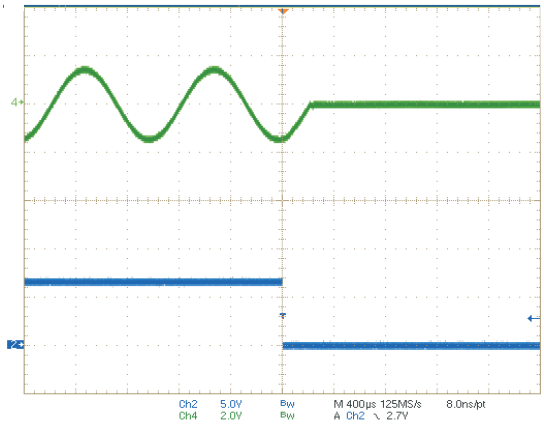


Figure 12.

APPLICATION INFORMATION

LINE DRIVER AMPLIFIERS

Single-supply headphone and line driver amplifiers typically require dc-blocking capacitors. The top drawing in Figure 13 illustrates the conventional line driver amplifier connection to the load and output signal.

DC blocking capacitors for headphone amps are often large in value, and a mute circuit is needed during power up to minimize click and pop for both headphone and line driver. The output capacitors and mute circuits consume PCB area and increase cost of assembly, and can reduce the fidelity of the audio output signal.

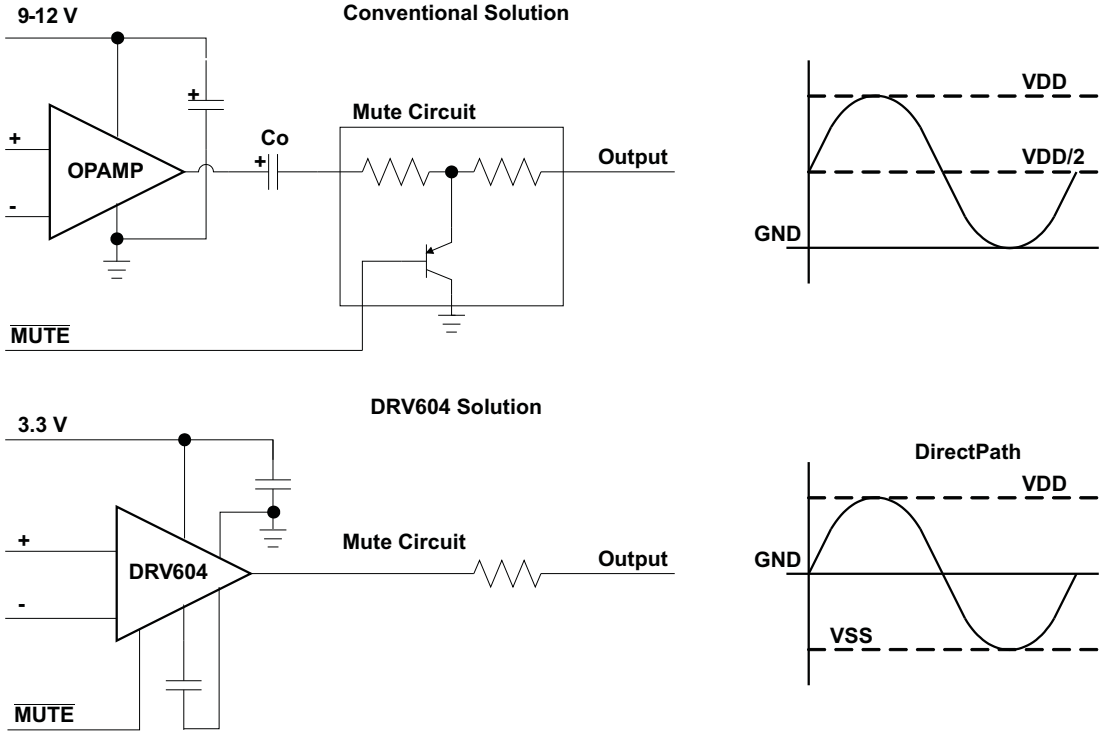


Figure 13. Conventional and DirectPath HP and Line Driver

The DirectPath™ amplifier architecture operates from a single supply but makes use of an internal charge pump to provide a negative voltage rail.

Combining the user provided positive rail and the negative rail generated by the IC, the device operates in what is effectively a split supply mode.

The output voltages are now centered at zero volts with the capability to swing to the positive rail or negative rail, combining this with the build in click and pop reduction circuit, the DirectPath™ amplifier requires no output dc blocking capacitors.

The bottom block diagram and waveform of Figure 13 illustrate the ground-referenced headphone and line driver architecture. This is the architecture of the DRV604.

COMPONENT SELECTION

Charge Pump

The charge pump flying capacitor serves to transfer charge during the generation of the negative supply voltage. The PVSS capacitor must be at least equal to the charge pump capacitor in order to allow maximum charge transfer. Low ESR capacitors are an ideal selection, and a value of 1µF is typical. Capacitor values that are smaller than 1µF can not be recommended for the HP section as it will limit the negative voltage swing in low impedance loads.

Decoupling Capacitors

The DRV604 is a DirectPath™ amplifier that requires adequate power supply decoupling to ensure that the noise and total harmonic distortion (THD) are low. A good low equivalent-series-resistance (ESR) ceramic capacitor, typically 1µF, placed as close as possible to the device PVDD leads works best. Placing this decoupling capacitor close to the DRV604 is important for the performance of the amplifier. For filtering lower frequency noise signals, a 10µF or greater capacitor placed near the audio power amplifier would also help, but it is not required in most applications because of the high PSRR of this device.

Gain Setting Resistors Ranges

The gain setting resistors, R_{in} and R_{fb}, must be chosen so that noise, stability and input capacitor size of the DRV604 is kept within acceptable limits. Voltage gain is defined as R_{fb} divided by R_{in}. Selecting values that are too low demands a large input ac-coupling capacitor, C_{IN}. Selecting values that are too high increases the noise of the amplifier. Table 1 lists the recommended resistor values for different gain settings.

Table 1. Recommended Resistor Values

INPUT RESISTOR VALUE, R_{in}	FEEDBACK RESISTOR VALUE, R_{fb}	DIFFERENTIAL INPUT GAIN	INVERTING INPUT GAIN	NON INVERTING INPUT GAIN
10 kΩ	10 kΩ	1.0 V/V	–1.0 V/V	2.0 V/V
10 kΩ	15 kΩ	1.5 V/V	–1.5 V/V	2.5 V/V
10 kΩ	20 kΩ	2.0 V/V	–2.0 V/V	3.0 V/V
4.7 kΩ	47 kΩ	10.0 V/V	–10.0 V/V	11.0 V/V

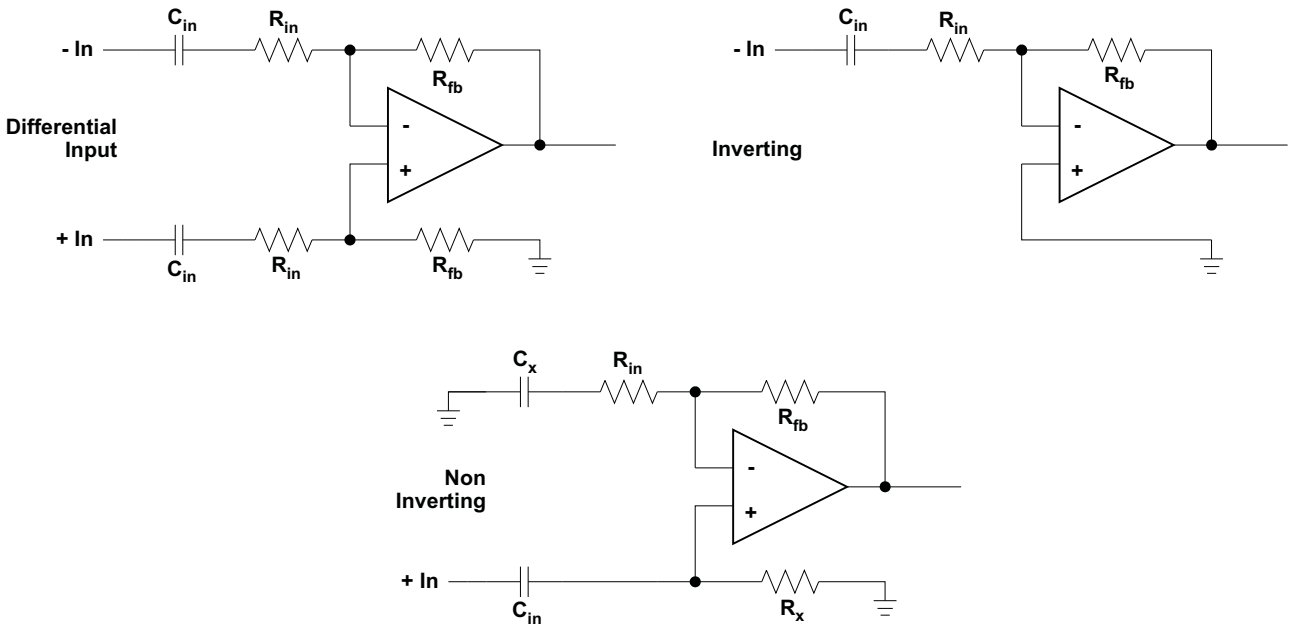
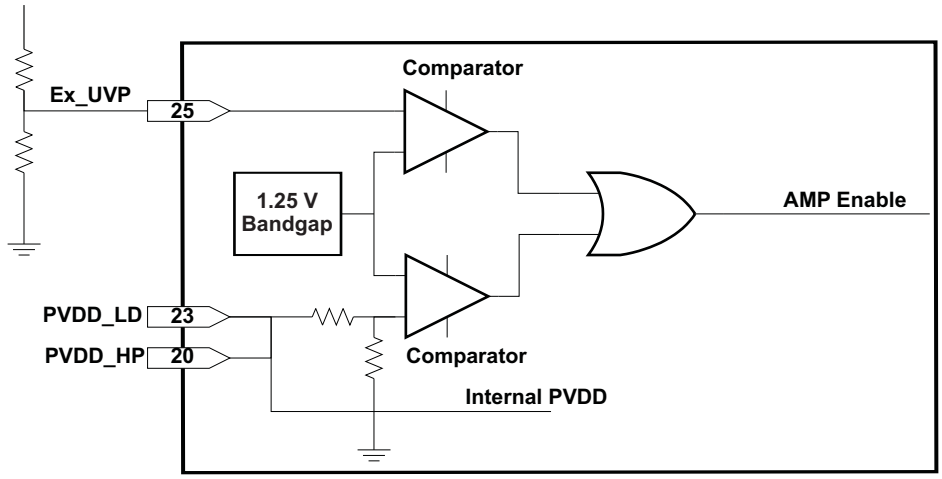


Figure 14. Differential, Inverting and Non-inverting Gain Configuration

Internal and External Under Voltage Detection and RESET Output

The DRV604 contains an internal precision band gap reference voltage and 2 comparators, one is used to monitor the supply voltages, PVDD_LD and PVDD_HP, and the other to monitor an external user selectable voltage on pin 25. The internal PVDD monitor is set at 2.8 V with 200 mV hysteresis.

The external under voltage detection can be used to shutdown the DRV604 before an input device can make a pop. The shutdown threshold at the Ex_UVP pin is 1.25 V. A resistor divider is used to obtain the shutdown threshold and hysteresis desired for the application.



The selected thresholds can be determined as follows:

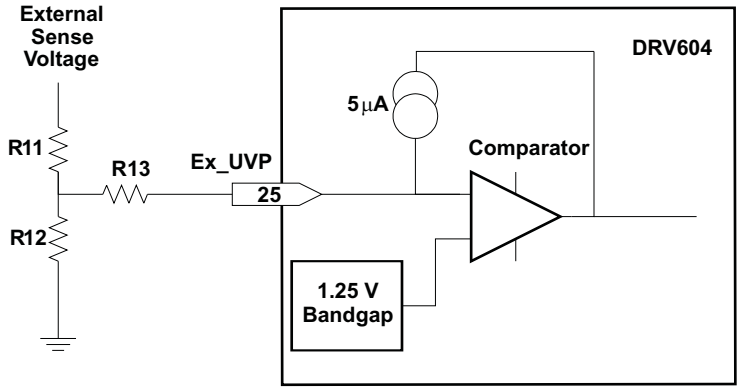
$$V_{UVP} = 1.25\ V \times \frac{(R11 + R12)}{R12} \quad (1)$$

$$V_{Hysteresis} = 5\ \mu A \times R13 \times \left(\frac{R11}{R12} + 1\right) \quad (2)$$

With the condition R13 >> R11||R12

For example, to obtain V_{UVP} = 4.5 V and 400 mV hysteresis, use R11 = 10 kΩ, R12 = 3 kΩ and R13 = 22kΩ.

To filter supply spikes and noise a capacitor across R12 can be added.



Input-Blocking Capacitors

DC input-blocking capacitors are required to be added in series with the audio signal into the input pins of the DRV604. These capacitors block the DC portion of the audio source and allow the DRV604 inputs to be properly biased to provide maximum performance. The input blocking capacitors also limit the DC gain to 1, limiting the DC-offset voltage at the output.

These capacitors form a high-pass filter with the input resistor, R_{in}. The cutoff frequency is calculated using Equation 1. For this calculation, the capacitance used is the input-blocking capacitor and the resistance is the input resistor chosen from Table 1, then the frequency and/or capacitance can be determined when one of the two values are given.

$$fc_{in} = \frac{1}{2\pi \times R_{in} \times C_{in}} \qquad C_{in} = \frac{1}{2\pi \times fc_{in} \times R_{in}} \quad (3)$$

Using the DRV604 as a 2nd order filter

Several audio DACs used today require an external low-pass filter to remove out of band noise. This is possible with the DRV604 as it can be used like a standard OPAMP. Several filter topologies can be implemented both single ended and differential. In the figure below a Multi Feed Back (MFB), with differential input and single ended input is shown.

An AC-coupling capacitor to remove dc-content from the source is shown, it serves to block any dc content from the source and lowers the dc-gain to 1 helping reducing the output dc-offset to minimum.

The component values can be calculated with the help of the TI FilterPro™ program available on the TI website at:

http://focus.ti.com/docs/toolsw/folders/print/filterpro.html

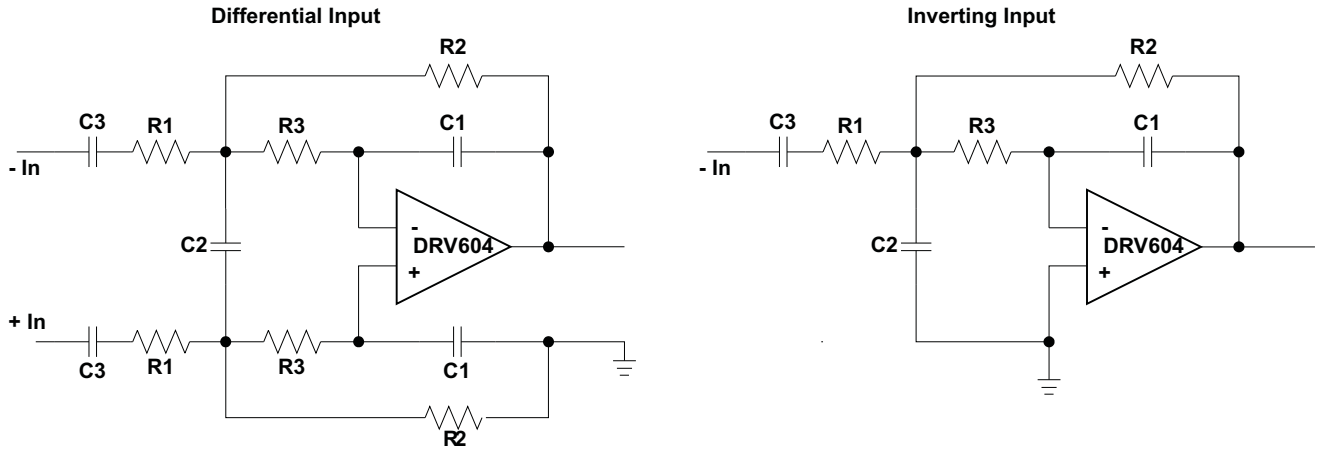


Figure 15. 2nd Order Active Low Pass Filter

The resistor values should have a low value for obtaining low noise, but should also have a high enough value to get a small size ac-coupling cap. C2 can be split in two with the midpoint connected to GND, this can increase the common-mode attenuation.

Pop-Free Power Up

Pop-free power up is ensured by keeping the EN_LD and EN_HP and/or Ex_UVP low during power supply ramp up and down. The pins should be kept low until the input AC-coupling capacitors are fully charged before asserting the EN_xx pins high, this way proper pre-charge of the ac-coupling is performed and pop-less power-up is achieved. Figure 16 illustrates the preferred sequence.

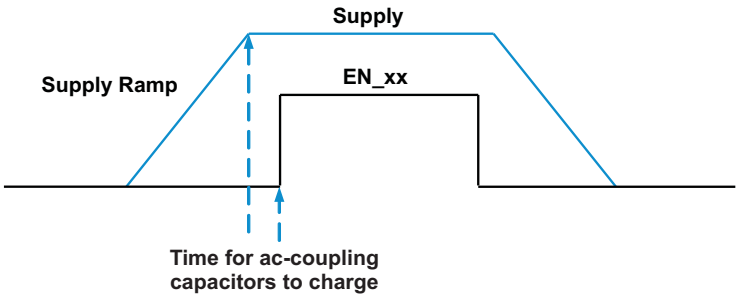


Figure 16. Power-Up/Down Sequence

Dual Stereo Line Driver

The DRV604 Headphone stereo amplifier can also be used as Line Driver and has the same high output voltage capability as the Line amp when driving 5kΩ load impedances. This makes the DRV604 ideal for applications like dual SCART outputs on LCD TV, or for multiple line outputs like in DVD or Blue-Ray players where 2x DRV604 can give a very space effective solution for a 8ch line output.

Capacitive Load

The DRV604 has the ability to drive a high capacitive load up to 220pF directly, higher capacitive loads can be accepted by adding an output series resistor of 47Ω or larger for the line driver output.

Layout Recommendations

A proposed layout for the DRV604 can be seen in the DRV604EVM user's guide, SLOU288, and the Gerber files can be downloaded on www.ti.com, open the DRV604 product folder and look in the Tools and Software folder.

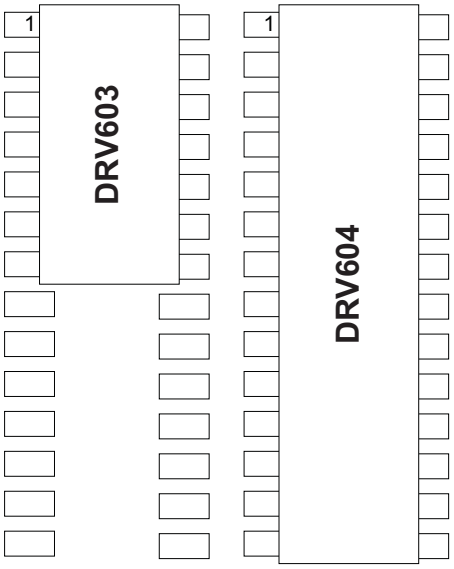
The gain setting resistors, R_{in} and R_{fb}, must be placed close to the input pins to minimize the capacitive loading on these input pins and to ensure maximum stability of the DRV604.

Ground traces are recommended to be routed as a star ground to minimize hum interference.

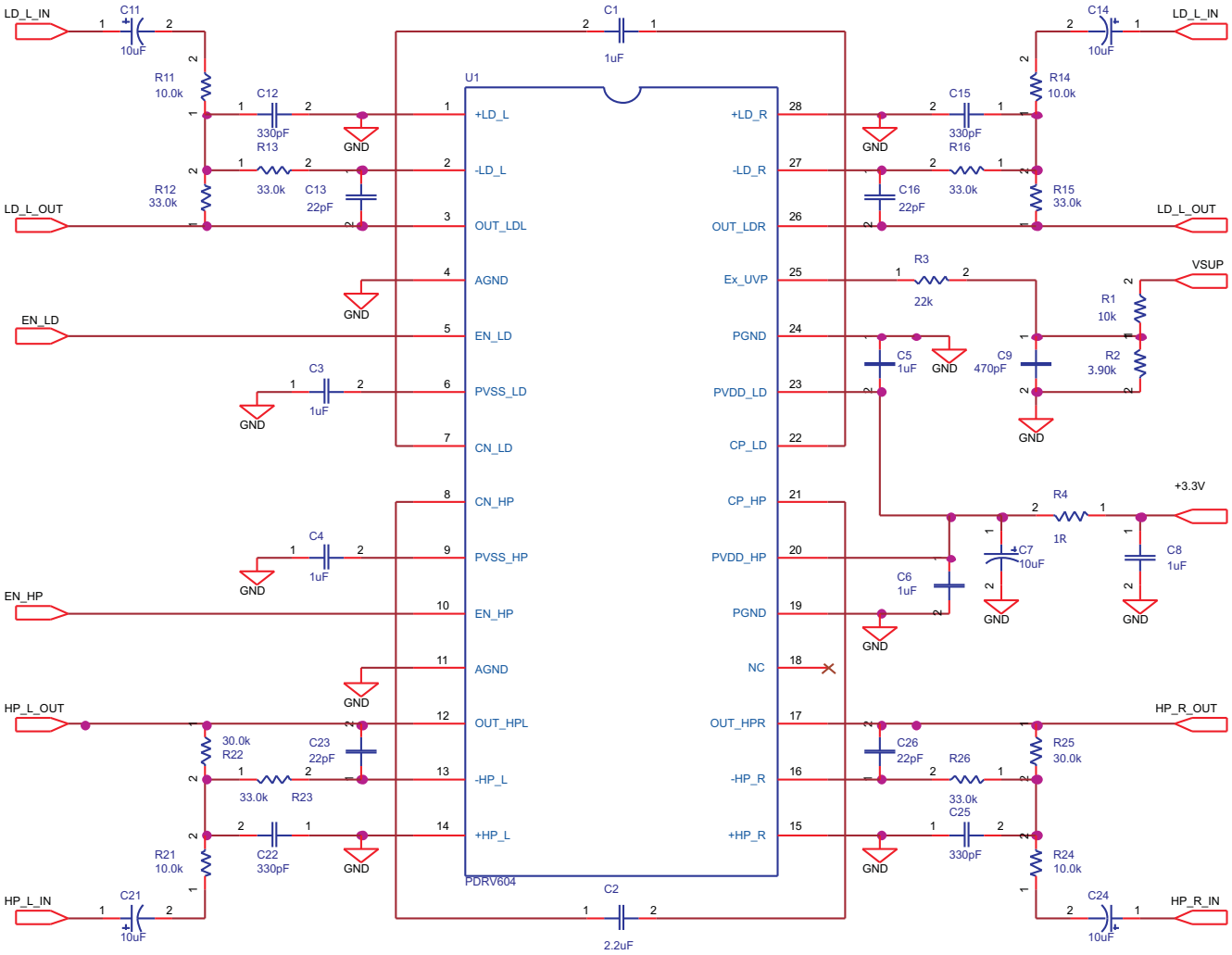
PVDD, PVSS decoupling capacitors and the charge pump capacitors should be connected with short traces.

Footprint Compatible with the DRV603

The DRV604 stereo line driver section is pin compatible with the DRV603. A single PCB layout can therefore be used with stuffing options for different output configurations.



APPLICATION CIRCUIT



Single-Ended Input and Output with 3.3x Gain in the Line Section, 3x Gain in the Headphone Section. AC-Coupling Input with a High Pass Pole of 1.6Hz, 2nd Order Low Pass Filter at 50kHz.

REVISION HISTORY

Changes from Original (January 2010) to Revision A	Page
• Changed TAS5630 to DRV604 in table heading	6

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV604PWP	ACTIVE	HTSSOP	PWP	28	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 85	DRV604	Samples
DRV604PWPR	ACTIVE	HTSSOP	PWP	28	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 85	DRV604	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

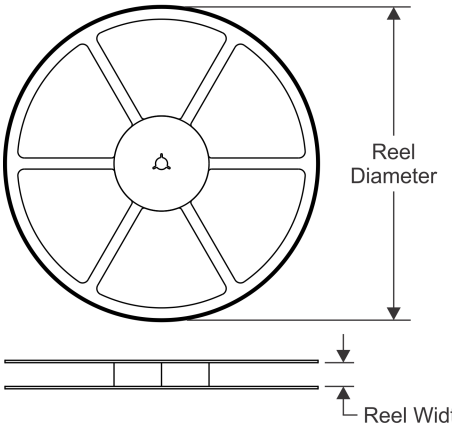
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

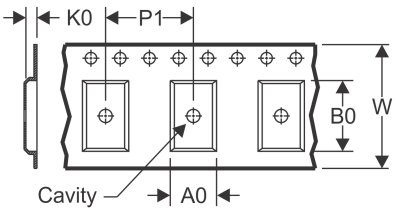
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

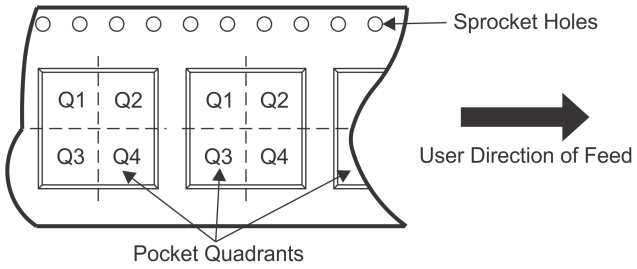


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

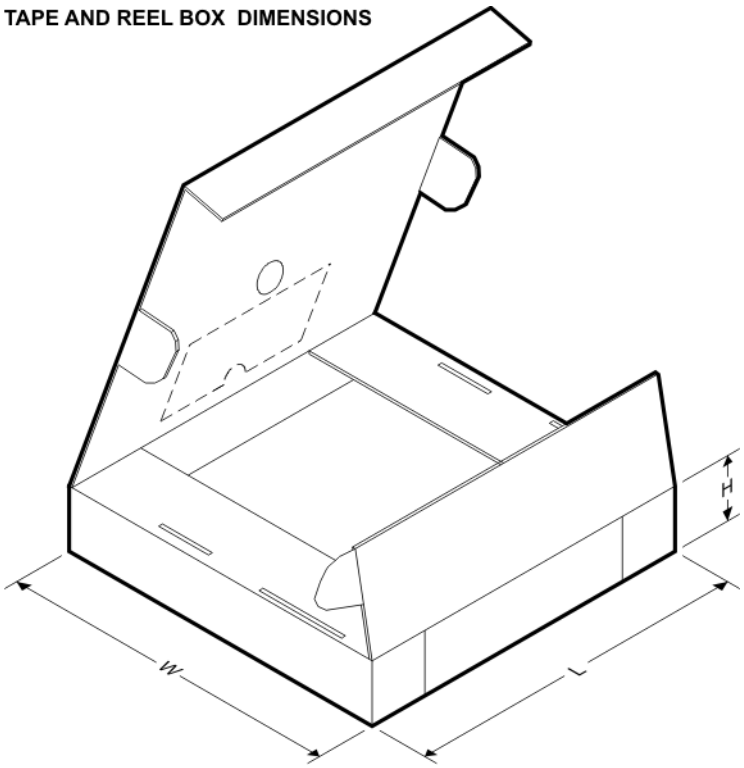
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV604PWPR	HTSSOP	PWP	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV604PWPR	HTSSOP	PWP	28	2000	350.0	350.0	43.0

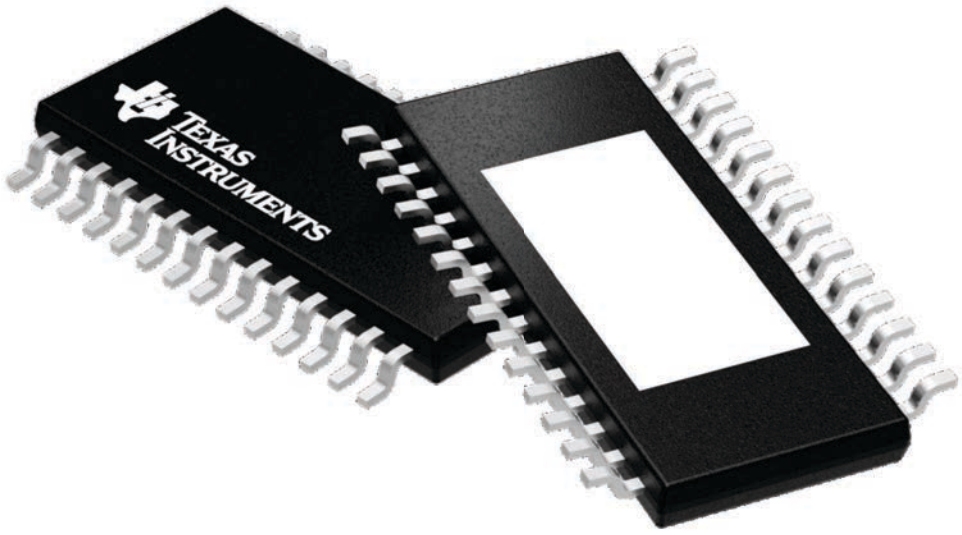
GENERIC PACKAGE VIEW

PWP 28

PowerPAD™ TSSOP - 1.2 mm max height

4.4 x 9.7, 0.65 mm pitch

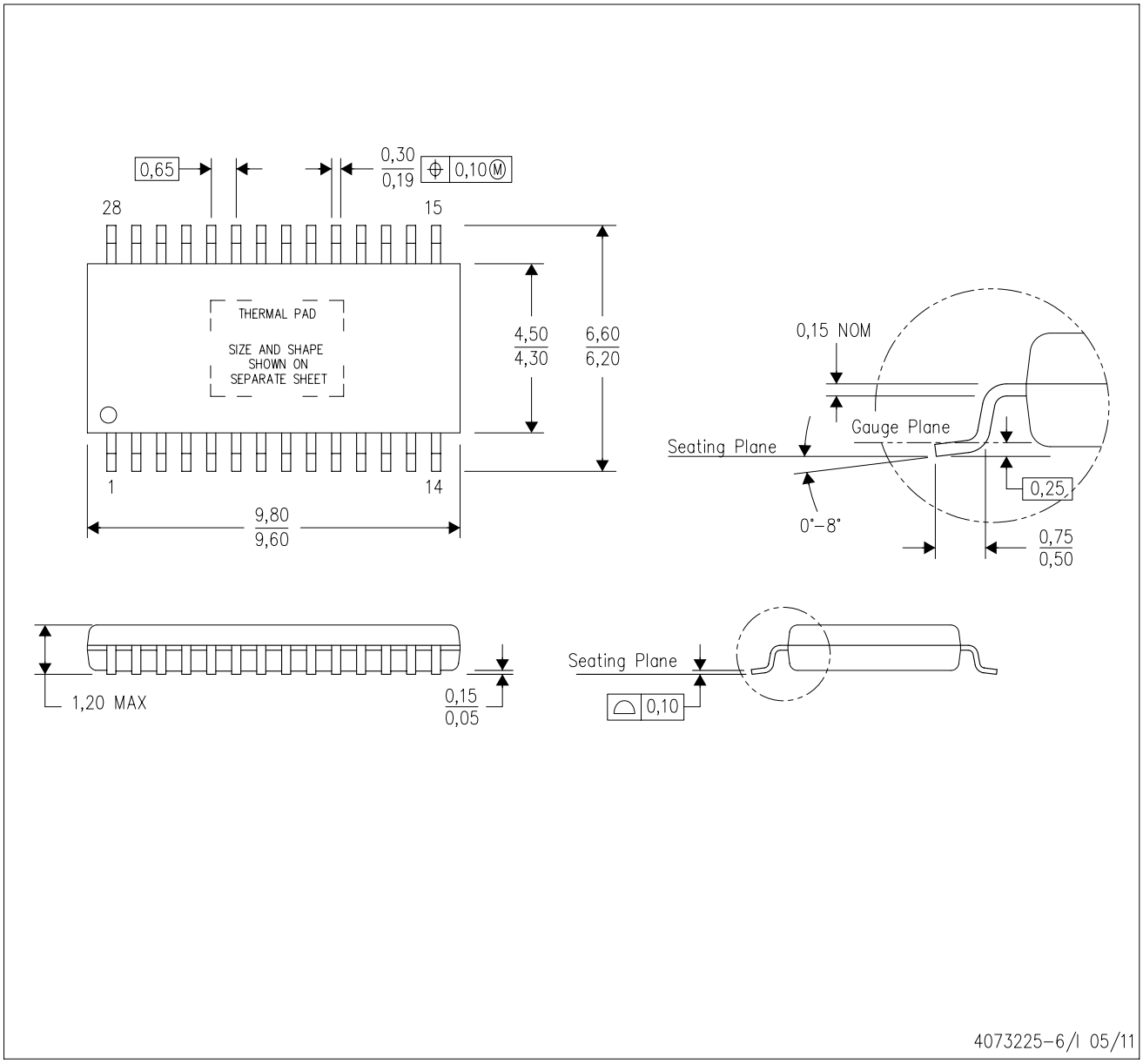
SMALL OUTLINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224765/A

PWP (R–PDSO–G28) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

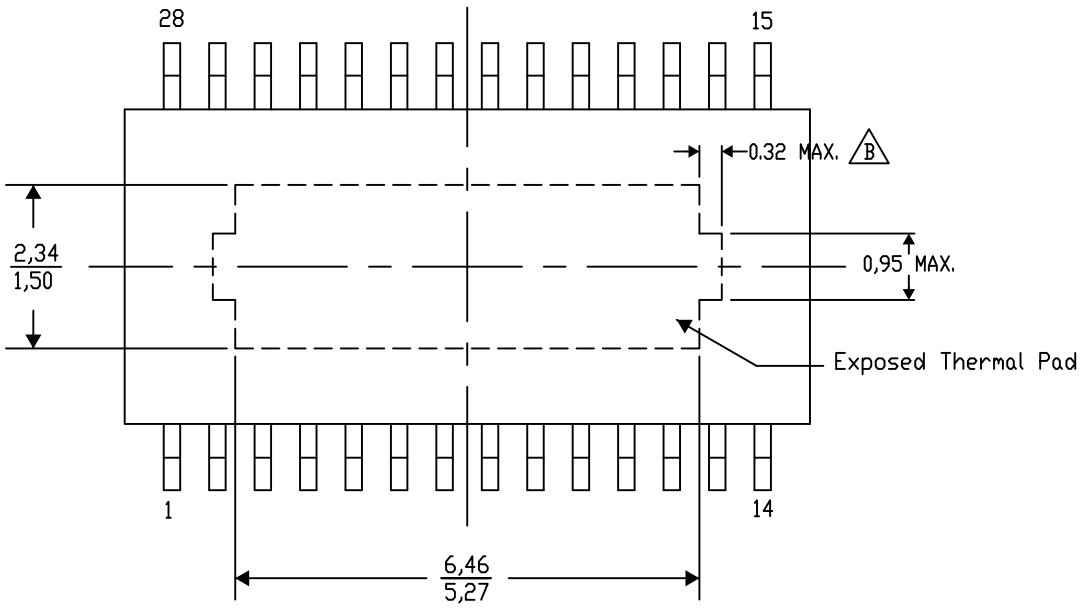
PWP (R–PDSO–G28) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

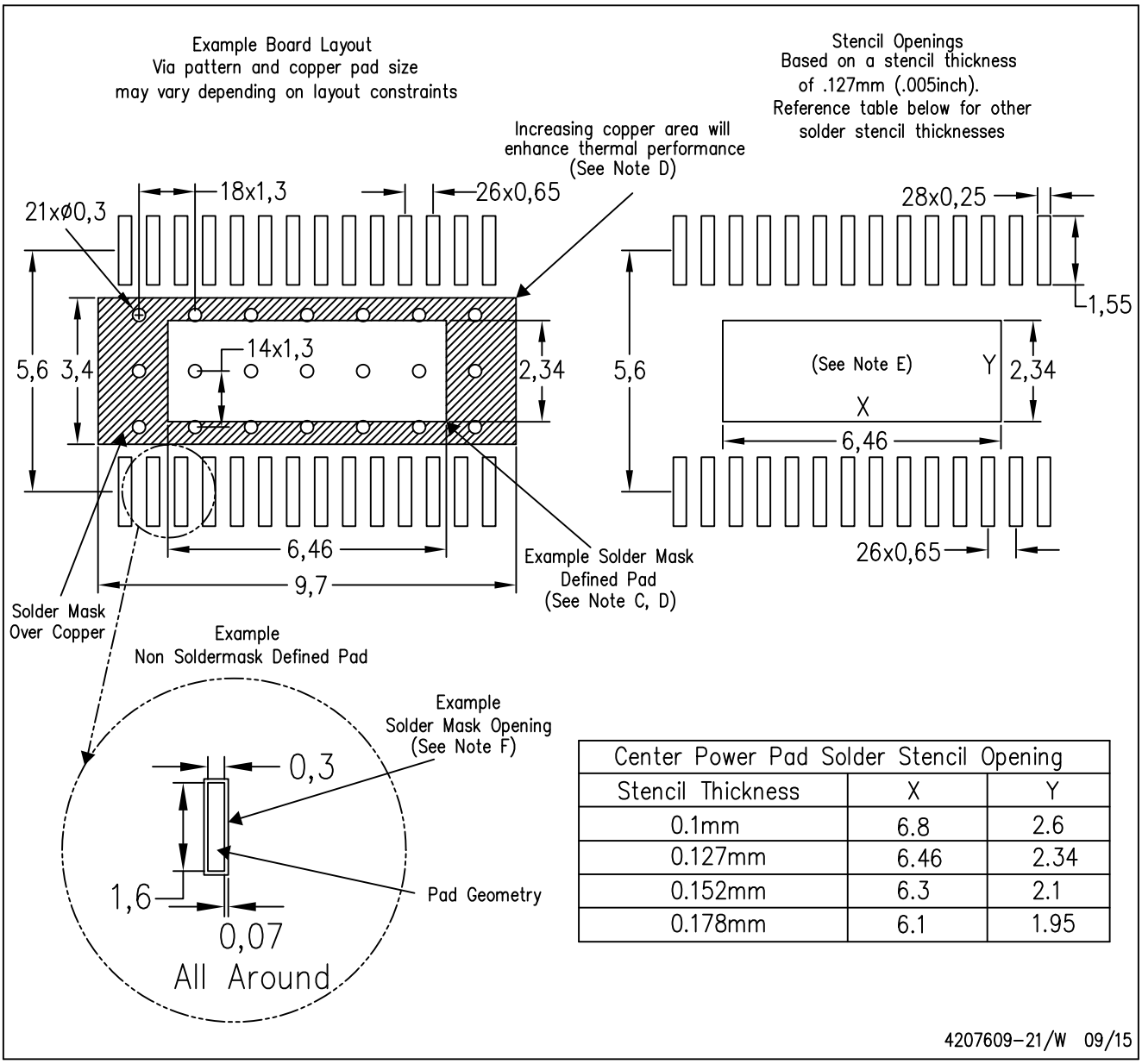
4206332–36/AO 01/16

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G28) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	6.8	2.6
0.127mm	6.46	2.34
0.152mm	6.3	2.1
0.178mm	6.1	1.95

4207609–21/W 09/15

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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