National Semiconductor

PRELIMINARY
August 1989

DP8417/NS32817, 8418/32818, 8419/32819, 8419X/ 32819X 64k, 256k Dynamic RAM Controller/Drivers

General Description

The DP8417/8418/8419/8419X represent a family of 256k DRAM Controller/Drivers which are designed to provide "No-Waitstate" CPU interface to Dynamic RAM arrays of up to 2 Mbytes and larger. Each device offers slight functional variations of the DP8419 design which are tailored for different system requirements. All family members are fabricated using National's new oxide isolated Advanced Low power Schottky (ALS) process and use design techniques which enable them to significantly out-perform all other LSI or discrete alternatives in speed, level of integration, and power consumption.

Each device integrates the following critical 256k DRAM controller functions on a single monolithic device: ultra precise delay line; 9-bit refresh counter; fall-through row, column, and bank select input latches; Row/Column address muxing logic; on-board high capacitive-load $\overline{RAS}$, $\overline{CAS}$, and Write Enable & Address output drivers; and, precise control signal timing for all the above.

There are four device options of the basic DP8419 Controller. The DP8417 is pin and function compatible with the DP8419 except that its outputs are TRI-STATE®. The DP8418 changes one pin and is specifically designed to offer an optimum interface to 32 bit microprocessors. The DP8419X is functionally identical to the DP8419, but is available in a 52-pin DIP package which is upward pin compatible with National's new DP8429D 1 Mbit DRAM Controller/ Driver.

Each device is available in plastic DIP, Ceramic DIP, and Plastic Chip Carrier (PCC) packaging. (Continued)

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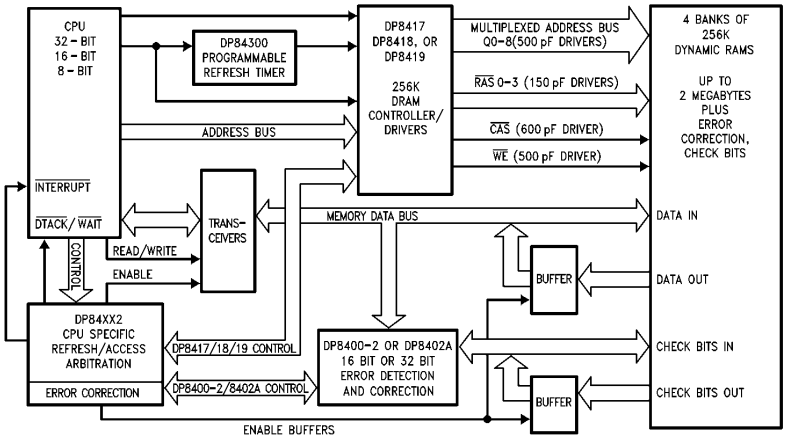
Operational Features

- Makes DRAM Interface and refresh tasks appear virtually transparent to the CPU, making DRAMs as easy to use as static RAMs
- Specifically designed to eliminate CPU wait states up to 10 MHz or beyond
- Eliminates 15 to 20 SSI/MSI components for significant board real estate reduction, system power savings and the elimination of chip-to-chip AC skewing
- On-board ultra precise delay line
- On-board high capacitive $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, and address drivers (specified driving 88 DRAMs directly)
- AC specified for directly addressing up to 8 Megabytes
- Low power/high speed bipolar oxide isolated process
- Upward pin and function compatible with new DP8428/ DP8429 1 Mbit DRAM controller drivers
- Downward pin and function compatible with DP8408A/ DP8409A 64k/256k DRAM controller/drivers
- 4 user selectable modes of operation for Access and Refresh (2 automatic, 2 external)

Contents

- System and Device Block Diagrams
- Recommended Companion Components
- Device Connection Diagrams and Pin Definitions
- Family Device Differences (DP8419 vs DP8409A, 8417, 8418, 8419X)
- Mode of Operation (Descriptions and Timing Diagrams)
- Application Description and Diagrams
- DC/AC Electrical Specifications, Timing Diagrams and Test Conditions

System Diagram



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DP8417/NS32817, 8418/32818, 8419/32819, 8419X/32819X 64k, 256k Dynamic RAM Controller/Drivers

General Description (Continued)

In order to specify each device for ''true'' worst case operating conditions, all timing parameters are guaranteed while the chip is driving the capacitive load of 88 DRAMs including trace capacitance. The chip's delay timing logic makes use of a patented new delay line technique which keeps A.C. skew to ±3 ns over the full V_{CC} range of ±10% and temperature range of −55°C to +125°C. The DP8417, DP8418, DP8419, and DP8419X guarantee a maximum $\overline{RASIN}$ to CASOUT delay of 80 ns or 70 ns even while driving a 2 Mbyte memory array with error correction check bits included. Speed selected options of these devices are shown in the switching characteristics section of this document.

With its four independent $\overline{RAS}$ outputs and nine multiplexed address outputs, the DP8419 can support up to four banks of 16k, 64k or 256k DRAMs. Two bank select pins, B1 and B0, are decoded to activate one of the $\overline{RAS}$ signals during an access, leaving the three non-selected banks in the standby mode (less than one tenth of the operating power) with data outputs in TRI-STATE.

The DP8419 has two mode-select pins, allowing for two refresh modes and two access modes. Refresh and access timing may be controlled either externally or automatically. The automatic modes require a minimum of input control signals.

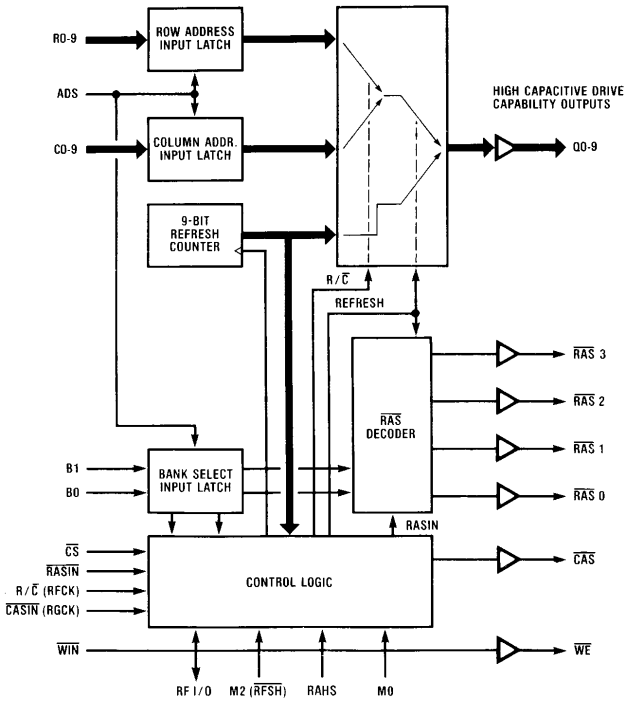
A refresh counter is on-chip and is multiplexed with the row and column inputs. Its contents appear at the address outputs of the DP8419 during any refresh, and are incremented at the completion of the refresh. Row/Column and bank address latches are also on-chip. However, if the address inputs to the DP8419 are valid throughout the duration of the access, these latches may be operated in the fall-through mode.

System Companion Components

Device #	Function
DP84300	Programmable Refresh Timer for DP84xx DRAM Controller
DP84412	NS32008/16/32 to DP8409A/17/18/19/28/29 Interface
DP84512	NS32332 to DP8417/18/19/28/29 Interface
DP84322	68000/08/10 to DP8409A/17/18/19/28/29 Interface (up to 8 MHz)
DP84422	68000/08/10 to DP8409A/17/18/19/28/29 Interface (up to 12.5 MHz)
DP84522	68020 to DP8417/18/19/28/29 Interface
DP84432	8086/88/186/188 to DP8409A/17/18/19/28/29 Interface
DP84532	80286 to DP8409A/17/18/19/28/29 Interface
DP8400-2	16-bit Expandable Error Checker/Corrector
DP8400-4	16-bit Expandable Error Checker/Corrector
DP8402A	32-bit Error Detector and Corrector (EDAC)

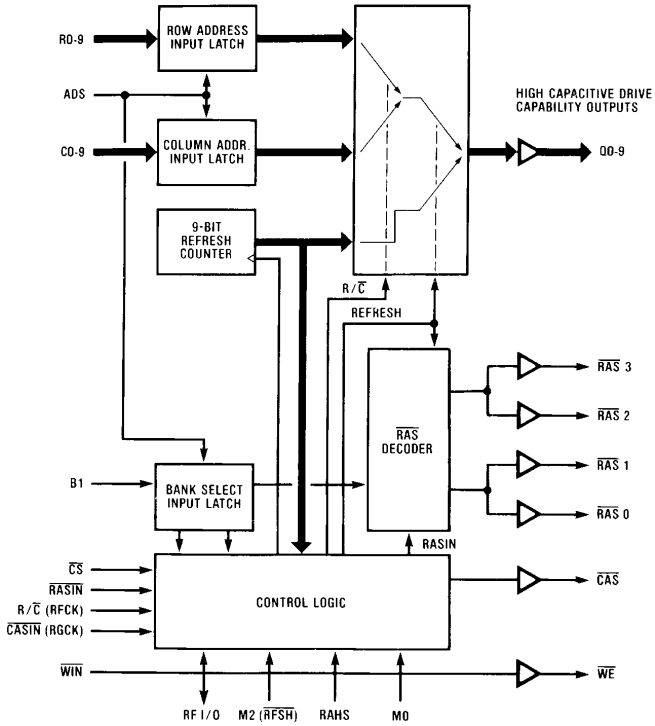
Block Diagrams

DP8417, 8419 and 8419X



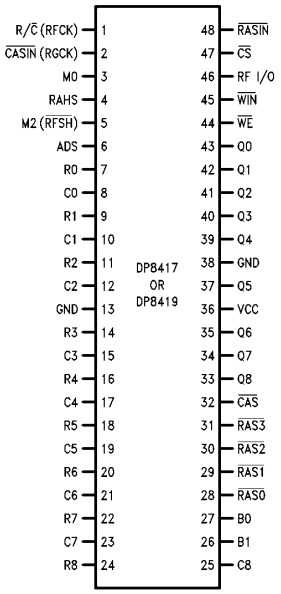
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DP8418

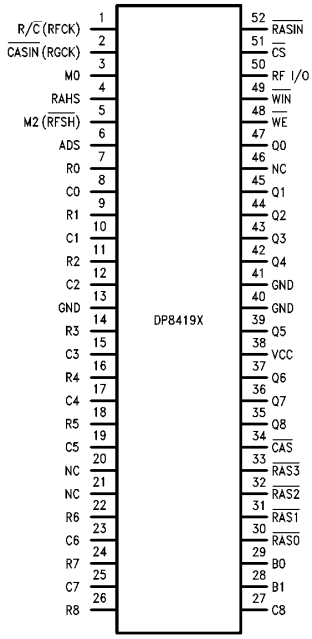


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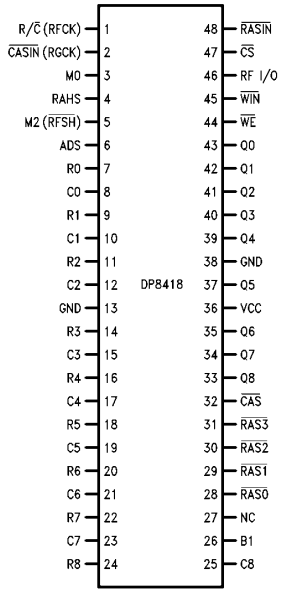
Connection Diagrams (Dual-In-Line Package)



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TL/F/8396–29

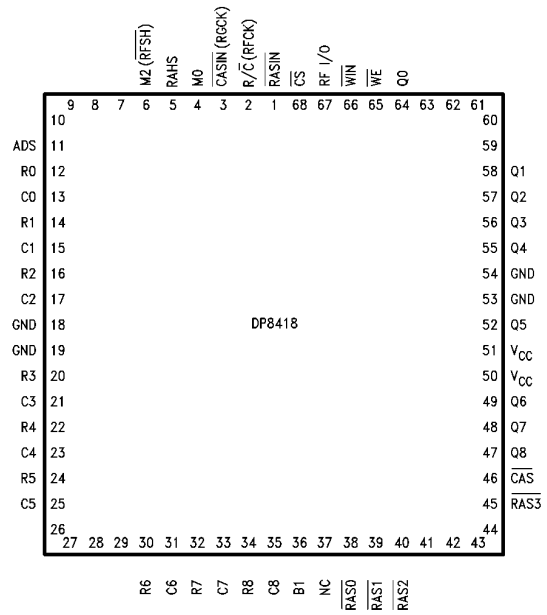


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Order Number DP8417D-70, DP8417D-80, DP8417N-70, DP8417N-80, DP8418D-70, DP8418D-80, DP8418N-70, DP8418N-80, DP8419D-70, DP8419D-80, DP8419N-70, DP8419N-80, DP8419XD-70 or DP8419XD-80.
See NS Package Number D48A, D52A, or N48A

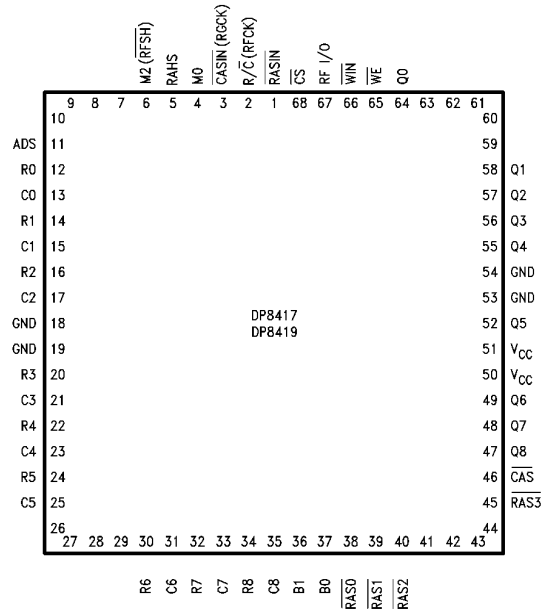
Connection Diagrams (Continued)

Plastic Chip Carrier Package



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Plastic Chip Carrier Package



TL/F/8396–32

Order Number DP8417V-70, DP8417V-80, DP8418V-70, DP8418V-80, DP8419V-70 or DP8419V-80
See NS Package Number V68A

Family Device Differences

DP8417 vs DP8419

The DP8417 is identical to the DP8419 with the exception that its $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and Q (Multiplexed Address) outputs are TRI-STATE when $\overline{CS}$ (Chip Select) is high and the chip is not in a refresh mode. This feature allows access to the same DRAM array through multiple DRAM Controller/Driver DP8417s. All AC specifications are the same as the DP8419 except t_{CSRLO} which is 34 ns for the DP8417 versus 5 ns for the DP8419. Separate delay specifications for the TRI-STATE timing paths are provided in the AC tables of this data sheet.

DP8418 vs DP8419

The DP8418 DYNAMIC RAM CONTROLLER/DRIVER is identical to the DP8419 with the exception of two functional differences incorporated to improve performance with 32-bit microprocessors.

1) Pin 26 (B1) is used to enable/disable a pair of $\overline{RAS}$ outputs, and pin 27 (B0 on the DP8419) is a no connect. When B1 is low, $\overline{RAS}$0 and $\overline{RAS}$1 are enabled such that they both go low during an access. When B1 is high, $\overline{RAS}$2 and $\overline{RAS}$3 are enabled. This feature is useful when driving words to 32 bits or more since each $\overline{RAS}$ would be driving only one half of the word. By distributing the load on each $\overline{RAS}$ line in this way, the DP8418 will meet the same AC specifications driving 2 banks of 32 DRAMs each as the DP8419 does driving 4 banks of 16 bits each.
2) The hidden refresh function available on the DP8419 has been disabled in order to reduce the amount of setup time necessary from $\overline{CS}$ going low to $\overline{RASIN}$ going low during an access of DRAM. This parameter, called t_{CSRL1}, is 5 ns for the DP8418 whereas it is 34 ns for the DP8419. The hidden refresh function only allows a very small increase in system performance, at best, at microprocessor frequencies of 10 MHz and above.

DP8419 vs DP8409A

The DP8419 High Speed DRAM Controller/Driver combines the most popular memory control features of the DP8408A/9A DRAM Controller/Driver with the high speed of bipolar oxide isolation processing.

The DP8419 retains the high capacitive-load drive capability of the DP8408A/9A as well as its most frequently used access and refresh modes, allowing it to directly replace the DP8408A/9A in applications using only modes 0, 1, 4 and 5. Thus, the DP8419 will allow most DP8408A/9A users to directly upgrade their system by replacing their old controller chip with the DP8419.

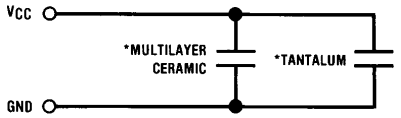
The highest priority of the DP8419 is speed. By peforming the DRAM address multiplexing, control signal timing and high-capacitive drive capability on a single chip, propagation delay skews are minimized. Emphasis has been placed on reducing delay variation over the specified supply and temperature ranges.

Except for the following, a DP8419 will operate essentially the same as a DP8409A.

1) The DP8419 has significantly faster AC performance.
2) The DP8419 can replace the DP8409A in applications which use modes 0, 1, 4, and 5. Modes 2, 3, 6, and 7 of the DP8409A are not available on the DP8419.
3) Pin 4 on the DP8419 is RAHS instead of M1, as on the DP8409A, and allows for two choices of t_{RAH} in mode 5.
4) RFI/O does not function as an end-of-count signal in Mode 0 on the DP8419 as it does on the DP8409A.
5) DP8419 address and control outputs do not TRI-STATE when $\overline{CS}$ is high as on the DP8409A. DP8419 control outputs are active high when $\overline{CS}$ is high (unless refreshing).

Pin Definitions

V_{CC}, GND, GND — V_{CC} = 5V ±10%. The three supply pins have been assigned to the center of the package to reduce voltage drops, both DC and AC. There are two ground pins to reduce the low level noise. The second ground pin is located two pins from V_{CC}, so that decoupling capacitors can be inserted directly next to these pins. It is important to adequately decouple this device, due to the high switching currents that will occur when all 9 address bits change in the same direction simultaneously. A recommended solution would be a 1 μF multilayer ceramic capacitor in parallel with a low-voltage tantalum capacitor, both connected as close as possible to V_{CC} and GND to reduce lead inductance. See Figure below.



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*Capacitor values should be chosen depending on the particular application.

R0–R8: Row Address Inputs.

C0–C8: Column Address Inputs.

Q0–Q8: Multiplexed Address Outputs - This address is selected from the Row Address Input Latch, the Column Address Input Latch or the Refresh Counter.

$\overline{RASIN}$: Row Address Strobe Input - $\overline{RASIN}$ directly controls the selected $\overline{RAS}$ output when in an access mode and all $\overline{RAS}$ outputs during hidden or external refresh.

R/$\overline{C}$ (RFCK) - In the auto-modes this pin is the external refresh clock input; one refresh cycle should be performed each clock period. In the external access mode it is Row/Column Select Input which enables either the row or column address input latch onto the output bus.

$\overline{CASIN}$ (RGCK) - In the auto-modes this pin is the $\overline{RAS}$ Generator Clock input. In external access mode it is the Column Address Strobe input which controls $\overline{CAS}$ directly once columns are enabled on the address outputs.

ADS: Address (Latch) Strobe Input - Row Address, Column Address, and Bank Select Latches are fall-through with ADS high; latching occurs on high-to-low transition of ADS.

$\overline{CS}$: Chip Select Input - When high, $\overline{CS}$ disables all accesses. Refreshing, however, in both modes 0 and 1 is not affected by this pin.

M0, M2 ($\overline{RFSH}$): Mode Control Inputs - These pins select one of the four available operational modes of the DP8419 (see Table III).

RFI/O: Refresh Input/Output - In the auto-modes this pin is the Refresh Request Output. It goes low following RFCK

Pin Definitions (Continued)

indicating that no hidden refresh was performed while RFCK was high. When this pin is set low by an external gate the on-chip refresh counter is reset to all zeroes.

$\overline{WIN}$: Write Enable Input.

$\overline{WE}$: Write Enable Output - $\overline{WE}$ follows $\overline{WIN}$ unconditionally.

RAHS: Row Address Hold Time Select - Selects the t_{RAH} to be generated by the DP8419 delay line to allow use with fast or slow DRAMs.

$\overline{CAS}$: Column Address Strobe Output - In mode 5 and in mode 4 with $\overline{CASIN}$ low before R/$\overline{C}$ goes low, $\overline{CAS}$ goes low automatically after the column address is valid on the address outputs. In mode 4 $\overline{CAS}$ follows $\overline{CASIN}$ directly after R/$\overline{C}$ goes low, allowing for nibble accessing. $\overline{CAS}$ is always high during refresh.

$\overline{RAS}$ 0–3: Row Address Strobe Outputs - The enabled $\overline{RAS}$ output (see Table II) follows $\overline{RASIN}$ directly during an access. During refresh, all $\overline{RAS}$ outputs are enabled.

B0, B1: Bank Select Inputs - These pins are decoded to enable one of the four $\overline{RAS}$ outputs during an access (see Table I and Table II).

TABLE I. DP8417, DP8419, DP8419X Memory Bank Decode

Bank Select (Strobed by ADS)		Enabled $\overline{RAS}_n$
B1	B0	
0	0	$\overline{RAS}_0$
0	1	$\overline{RAS}_1$
1	0	$\overline{RAS}_2$
1	1	$\overline{RAS}_3$

TABLE II. DP8418 Memory Bank Decode

Bank Select (Strobed by ADS)		Enabled $\overline{RAS}_n$
B1	NC	
0	X	$\overline{RAS}_0$ and $\overline{RAS}_1$
1	X	$\overline{RAS}_2$ and $\overline{RAS}_3$

Conditions for All Modes

INPUT ADDRESSING

The address block consists of a row-address latch, a column-address latch, and a resettable refresh counter. The address latches are fall-through when ADS is high and latch when ADS goes low. If the address bus contains valid addresses until after $\overline{CAS}$ goes low at the end of the memory cycle, ADS can be permanently high. Otherwise ADS must go low while the addresses are still valid.

DRIVE CAPABILITY

The DP8419 has timing parameters that are specified driving the typical capacitance (including traces) of 88, 5V-only DRAMs. Since there are 4 $\overline{RAS}$ outputs, each is specified driving one-fourth of the total memory. $\overline{CAS}$, $\overline{WE}$ and the address outputs are specified driving all 88 DRAMs.

The graph in *Figure 10* may be used to determine the slight variations in timing parameters, due to loading conditions other than 88 DRAMs.

Because of distributed trace capacitance and inductance and DRAM input capacitance, current spikes can be created, causing overshoots and undershoots at the DRAM inputs that can change the contents of the DRAMs or even destroy them. To reduce these spikes, a damping resistor (low inductance, carbon) should be inserted between the DP8419 outputs and the DRAMs, as close as possible to the DP8419. The damping resistor values may differ depending on how heavily an output is loaded. These resistors should be determined by the first prototypes (not wire-wrapped due to the larger distributed capacitance and inductance). Resistors should be chosen such that the transition on the control outputs is critically damped. Typical values will be from 15Ω to 100Ω, with the lower values being used with the larger memory arrays. Note that AC parameters are specified with 15Ω damping resistors. For more information see AN-305 ''Precautions to Take When Driving Memories''.

DP8419 DRIVING ANY 16k, 64k or 256k DRAMs

The DP8419 can drive any 16k, 64k or 256k DRAMs. All 16k DRAMs use basically the same configuration, including the 5V-only version. Hence, in most applications, different manufacturers' DRAMs are interchangeable (for the same supply-rail chips), and the DP8419 can drive them all (see *Figure 1a*).

There are three basic configurations for the 5V-only 64k DRAMs: a 128-row by 512-column array with an on-RAM refresh counter, a 128-row by 512-column array with no on-RAM refresh counter, and a 256-row by 256-column array with no on-RAM refresh counter. The DP8419 can drive all three configurations, and allows them all to be interchangeable (as shown in *Figures 1b* and *1c*), providing maximum flexibility in the choice of DRAMs. Since the 9-bit on-chip refresh counter can be used as a 7-bit refresh counter for the 128-row configuration, or as an 8-bit refresh counter for the 256-row configuration, the on-RAM refresh counter, if present, is never used.

256k DRAMs require all 18 of the DP8419's address inputs to select one memory location within the DRAM. $\overline{RAS}$-only refreshing with the nine-bit refresh-counter on the DP8419 makes $\overline{CAS}$ before $\overline{RAS}$ refreshing, available on 256k DRAMs, unnecessary.

READ, WRITE AND READ-MODIFY-WRITE CYCLES

The output signal, $\overline{WE}$, determines what type of memory access cycle the memory will perform. If $\overline{WE}$ is kept high while $\overline{CAS}$ goes low, a read cycle occurs. If $\overline{WE}$ goes low before $\overline{CAS}$ goes low, a write cycle occurs and data at DI (DRAM input data) is written into the DRAM as $\overline{CAS}$ goes low. If $\overline{WE}$ goes low later than t_{CWD} after $\overline{CAS}$ goes low, first a read occurs and DO (DRAM output data) becomes valid, then data DI is written into the same address in the DRAM as $\overline{WE}$ goes low. In this read-modify-write case, DI and DO cannot be linked together. $\overline{WE}$ always follows $\overline{WIN}$ directly to determine the type of access to be performed.

POWER-UP INITIALIZE

When V_{CC} is first applied to the DP8419, an initialize pulse clears the refresh counter and the internal control flip-flops.

Mode Features Summary

- 4 modes of operation: 2 access and 2 refresh
- Automatic or external control selected by the user
- Auto access mode provides $\overline{RAS}$, row to column change, and then $\overline{CAS}$ automatically
- Choice between two different values of t_{RAH} in auto-access mode
- $\overline{CAS}$ controlled independently in external control mode, allowing for nibble mode accessing
- Automatic refreshing can make refreshes transparent to the system
- $\overline{CAS}$ is inhibited during refresh cycles

DP8419 Mode Descriptions

MODE 0–EXTERNALLY CONTROLLED REFRESH

Figure 2 shows the Externally Controlled Refresh timing. In this mode the refresh counter contents are multiplexed to the address outputs. All $\overline{RAS}$ outputs are enabled to follow $\overline{RASIN}$ so that the row address indicated by the refresh counter is refreshed in all DRAM banks when $\overline{RASIN}$ goes low. The refresh counter increments when $\overline{RASIN}$ goes high. $\overline{RFSH}$ should be held low at least until $\overline{RASIN}$ goes high (they may go high simultaneously) so that the refresh address remains valid and all $\overline{RAS}$ outputs remain enabled throughout the refresh.

A burst refresh may be performed by holding $\overline{RFSH}$ low and toggling $\overline{RASIN}$ until all rows are refreshed. It may be useful in this case to reset the refresh counter just prior to beginning the refresh. The refresh counter resets to all zeroes when RFI/O is pulled low by an external gate. The refresh counter always counts to 511 before rolling over to zero. If there are 128 or 256 rows being refreshed then Q7 or Q8, respectively, going high may be used as an end-of-burst indicator.

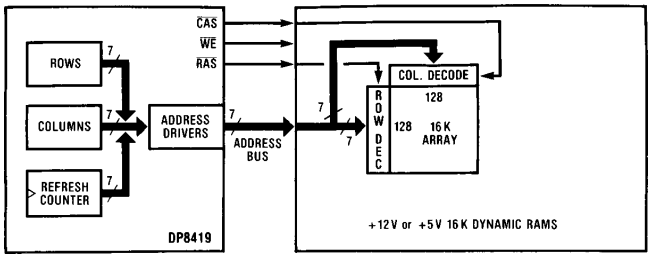
In order that the refresh address is valid on the address outputs prior to the $\overline{RAS}$ lines going low, $\overline{RFSH}$ must go low before $\overline{RASIN}$. The setup time required is given by t_{RFLRL} in the Switching Characteristics. This parameter may be adjusted using *Figure 10* for loading conditions other than those specified.

TABLE III. DP8419 Mode Select Options

Mode	($\overline{RFSH}$) M2	M0	Mode of Operation
0	0	0	Externally Controlled Refresh
1	0	1	Auto Refresh–Forced
4	1	0	Externally Controlled Access
5	1	1	Auto Access (Hidden Refresh)

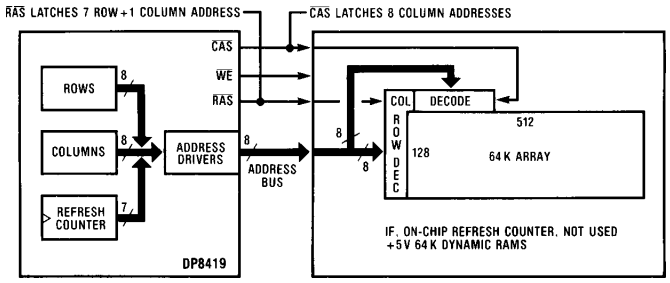
DP8419 Mode Descriptions (Continued)

DP8419 Interface Between System & DRAM Banks



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FIGURE 1a. DP8419 with any 16k DRAMS

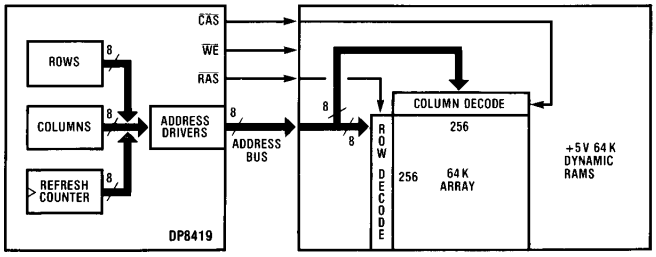


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Only LS 7 Bits of Refresh Counter used for the 7 Row Addresses.

MSB not used but can toggle.

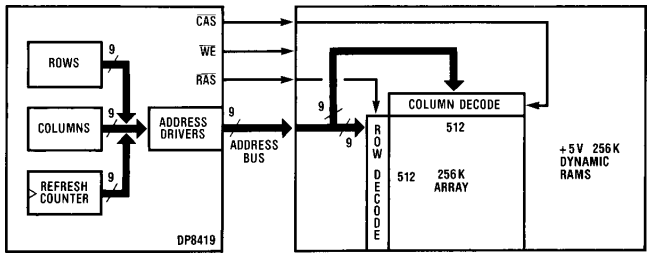
FIGURE 1b. DP8419 with 128 Row x 512 Column 64k DRAM



8 Bits of Refresh Counter Used

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FIGURE 1c. DP8419 with 256 Row x 256 Column 64k DRAM

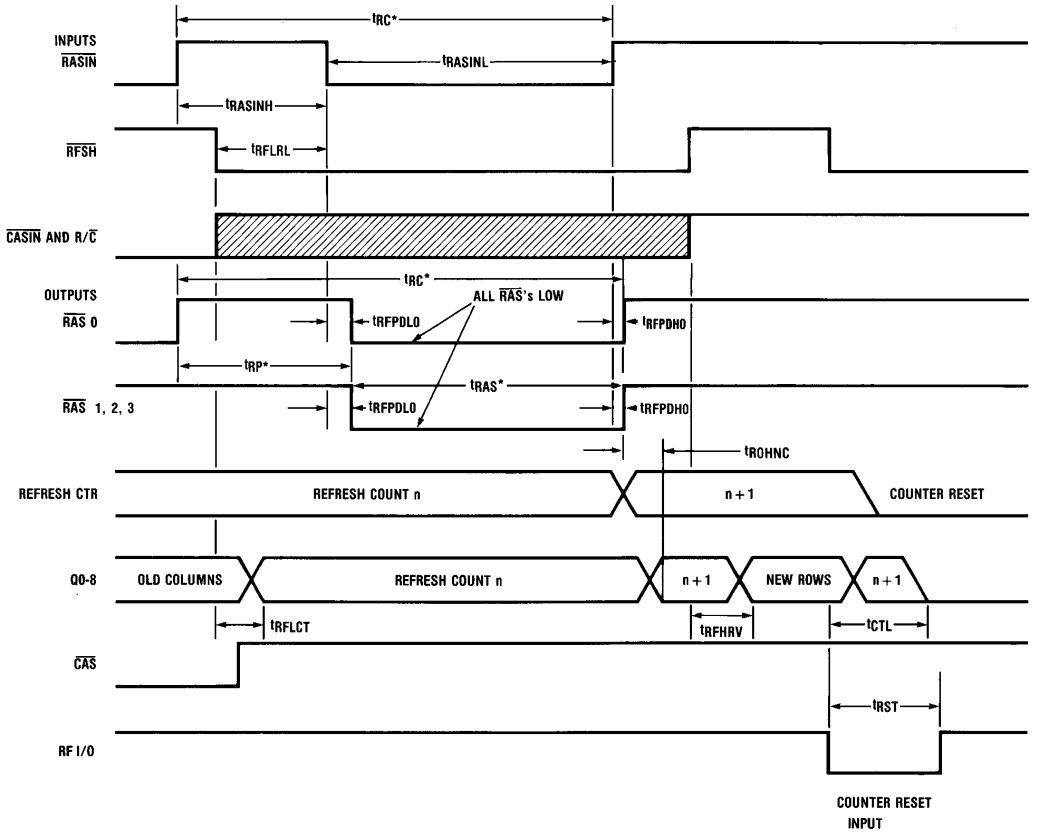


All 9 Bits of Refresh Counter Used

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FIGURE 1d. DP8419 with 256k DRAMs

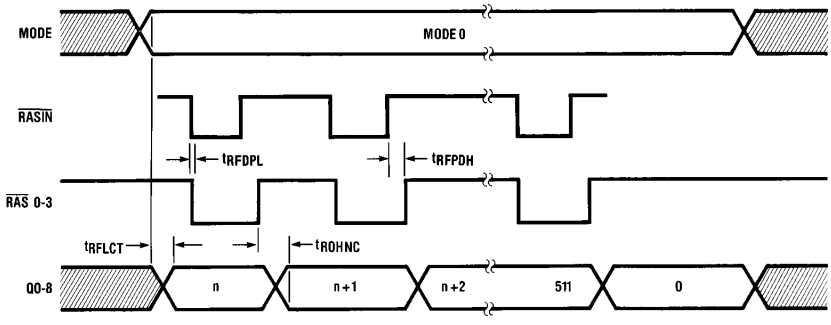
DP8419 Mode Descriptions (Continued)



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*Indicates Dynamic RAM Parameters

FIGURE 2a. External Control Refresh Cycle (Mode 0)



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FIGURE 2b. Burst Refresh Mode 0

DP8419 Mode Descriptions (Continued)

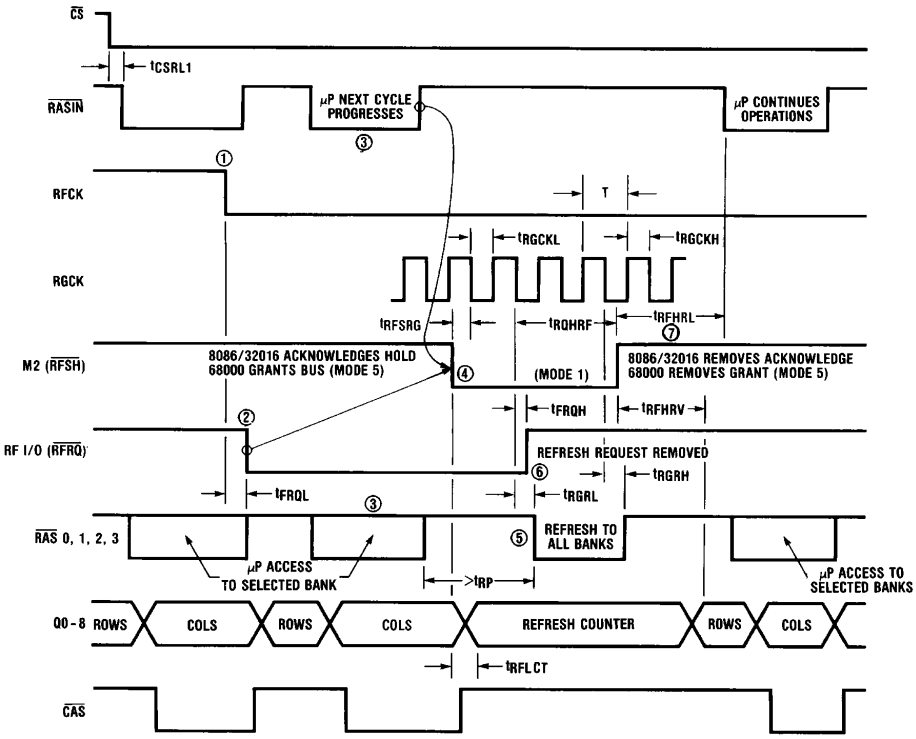
MODE 1–AUTOMATIC FORCED REFRESH

In Mode 1 the R/$\overline{C}$ (RFCK) pin becomes RFCK (refresh cycle clock) and the $\overline{CASIN}$ (RGCK) pin becomes RGCK ($\overline{RAS}$ generator clock). If RFCK is high and Mode 1 is entered then the chip operates as if in MODE 0 (externally controlled refresh), with all $\overline{RAS}$ outputs following $\overline{RASIN}$. This feature of Mode 1 may be useful for those who want to use Mode 5 (automatic access) with externally controlled refresh. By holding RFCK permanently high one need only toggle M2 ($\overline{RFSH}$) to switch from Mode 5 to external refresh. As with Mode 0, RFI/O may be pulled low by an external gate to reset the refresh counter.

When using Mode 1 as automatic refresh, RFCK must be an input clock signal. One refresh should occur each period of RFCK. If no refresh is performed while RFCK is high, then when RFCK goes low RFI/O immediately goes low to indicate that a refresh is requested. (RFI/O may still be used to reset the refresh counter even though it is also used as a refresh request pin, however, an open-collector gate should be used to reset the counter in this case since RFI/O is forced low internally for a request).

After receiving the refresh request the system must allow a forced refresh to take place while RFCK is low. External logic can monitor $\overline{RFRQ}$ (RFI/O) so that when $\overline{RFRQ}$ goes low this logic will wait for the access currently in progress to be completed before pulling M2 ($\overline{RFSH}$) low to put the DP8419 in mode 1. If no access is taking place when $\overline{RFRQ}$ occurs, then M2 may immediately go low. Once M2 is low, the refresh counter contents appear at the address outputs and $\overline{RAS}$ is generated to perform the refresh.

An external clock on RGCK is required to derive the refresh $\overline{RAS}$ signals. On the second falling edge of RGCK after M2 is low, all $\overline{RAS}$ lines go low. They remain low until two more falling edges of RGCK. Thus $\overline{RAS}$ remains high for one to two periods of RGCK after M2 goes low, and stays low for two periods. In order to obtain the minimum delay from M2 going low to $\overline{RAS}$ going low, M2 should go low t_{RFSRG} before the falling edge of RGCK.



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① RFCK goes low
② $\overline{RFRQ}$ goes low if no hidden refresh occurred while RFCK was high
③ Next $\overline{RASIN}$ starts next access
④ µP acknowledges refresh request
⑤ Forced refresh $\overline{RAS}$ starts after > T (> t_{RP})
⑥ Forced refresh $\overline{RAS}$ ends $\overline{RFRQ}$
⑦ µP removes refresh acknowledge

FIGURE 3. DP8419 Performing a Forced Refresh (Mode 5 ⟶ 1 ⟶ 5) with Various Microprocessors

DP8419 Mode Descriptions (Continued)

The Refresh Request on RFI/O is terminated as $\overline{RAS}$ goes low. This signal may be used to end the refresh earlier than it normally would as described above. If M2 is pulled high while the $\overline{RAS}$ lines are low, then the $\overline{RAS}$s go high t_{RFRH} later. The designer must be careful, however, not to violate the minimum $\overline{RAS}$ low time of the DRAMs. He must also guarantee that the minimum $\overline{RAS}$ precharge time is not violated during a transition from mode 1 to mode 5 when an access is desired immediately following a refresh.

If the processor tries to access memory while the DP8419 is in mode 1, WAIT states should be inserted into the processor cycles until the DP8419 is back in mode 5 and the desired access has been accomplished (see *Figure 9*).

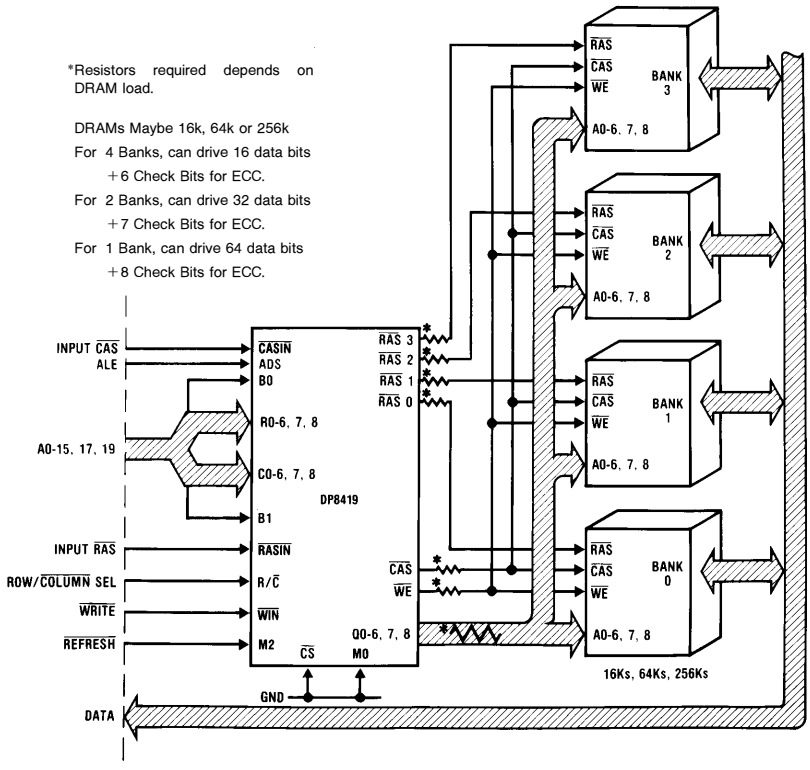
Instead of using WAIT states to delay accesses when refreshing, HOLD states could be used as follows. $\overline{RFRQ}$ could be connected to a HOLD or Bus Request input to the system. When convenient, the system acknowledges the $\overline{HOLD}$ or Bus Request by pulling M2 low. Using this scheme, $\overline{HOLD}$ will end as the $\overline{RAS}$ lines go low (RFI/O goes high). Thus, there must be sufficient delay from the time $\overline{HOLD}$ goes high to the DP8419 returning to mode 5, so that the $\overline{RAS}$ low time of the DRAMs isn't violated as described earlier (see *Figure 3* for mode 1 refresh with Hold states).

To perform a forced refresh the system will be inactive for about four periods of RGCK. For a frequency of 10 MHz, this is 400 ns. To refresh 128 rows every 2 ms an average of about one refresh per 16 μs is required. With a RFCK period of 16 μs and RGCK period of 100 ns, DRAM accesses are delayed due to refresh only 2.5% of the time. If using the Hidden Refresh available in mode 5 (refreshing with RFCK high) this percentage will be even lower.

MODE 4 - EXTERNALLY CONTROLLED ACCESS

In this mode all control signal outputs can be controlled directly by the corresponding control input. The enabled $\overline{RAS}$ output follows $\overline{RASIN}$, $\overline{CAS}$ follows $\overline{CASIN}$ (with R/$\overline{C}$ low), $\overline{WE}$ follows $\overline{WIN}$ and R/$\overline{C}$ determines whether the row or the column inputs are enabled to the address outputs (see *Figure 4*).

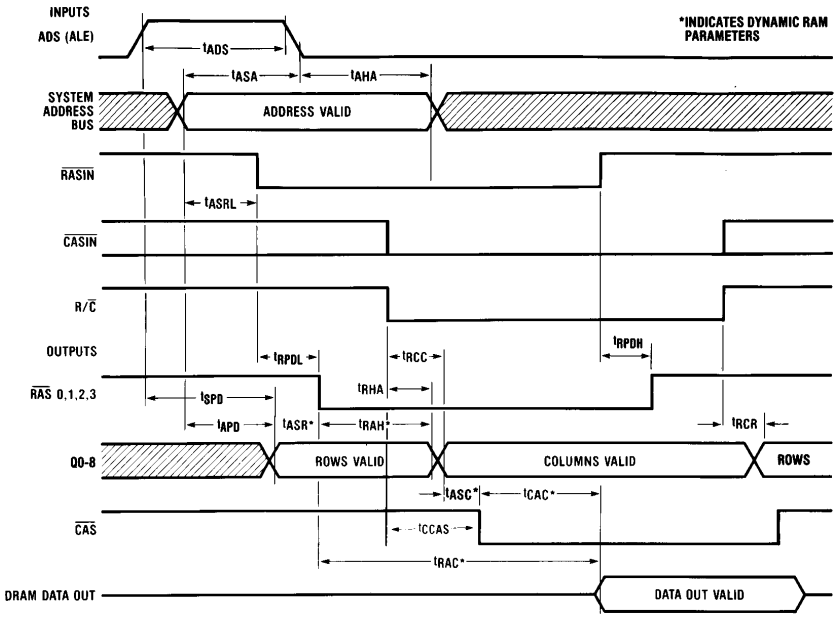
With R/$\overline{C}$ high, the row address latch contents are enabled onto the address bus. $\overline{RAS}$ going low strobes the row address into the DRAMs. After waiting to allow for sufficient row-address hold time (t_{RAH}) after $\overline{RAS}$ goes low, R/$\overline{C}$ can go low to enable the column address latch contents onto the address bus. When the column address is valid, $\overline{CAS}$ going low will strobe it into the DRAMs. $\overline{WIN}$ determines whether the cycle is a read, write or read-modify-write access. Refer to *Figures 5a* and *5b* for typical Read and Write timing using mode 4.



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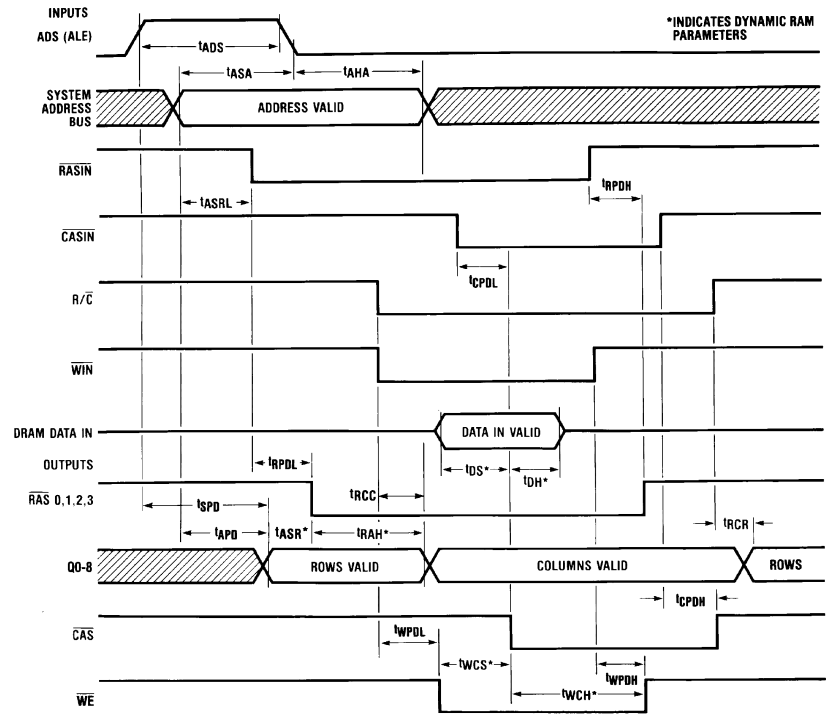
FIGURE 4. Typical Application of DP8419 Using External Control Access and Refresh in Modes 0 and 4

DP8419 Mode Descriptions (Continued)



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FIGURE 5a. Read Cycle Timing (Mode 4)



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FIGURE 5b. Write Cycle Timing (Mode 4)

DP8419 Mode Descriptions (Continued)

Page or Nibble mode may be performed by toggling $\overline{CASIN}$ once the initial access has been completed. In the case of page mode the column address must be changed before $\overline{CASIN}$ goes low to access a new memory location (see *Figure 5c*). Parameter t_{CPdif} has been specified in order that users may easily determine minimum $\overline{CAS}$ pulse widths when $\overline{CASIN}$ is toggling.

AUTOMATIC $\overline{CAS}$ GENERATION

$\overline{CAS}$ is held high when R/$\overline{C}$ is high even if $\overline{CASIN}$ is low. If $\overline{CASIN}$ is low when R/$\overline{C}$ goes low, $\overline{CAS}$ goes low automatically, t_{ASC} after the column address is valid. This feature eliminates the need for an externally derived $\overline{CASIN}$ signal to control $\overline{CAS}$ when performing a simple access (*Figure 5a* demonstrates Auto-$\overline{CAS}$ generation in mode 4). Page or nibble accessing may be performed as shown in *Figure 5c* even if $\overline{CAS}$ is generated automatically for the initial access.

FASTEST MEMORY ACCESS

The fastest mode 4 access is achieved by using the automatic $\overline{CAS}$ feature and external delay line to generate the required delay between $\overline{RASIN}$ and R/$\overline{C}$. The amount of delay required depends on the minimum t_{RAH} of the DRAMs being used. The DP8419 parameter t_{DIF1} has been specified in order that the delay between $\overline{RASIN}$ and R/$\overline{C}$ may be minimized.

$$t_{DIF1} = \text{MAXIMUM } (t_{RPDL} - t_{RHA})$$

where t_{RPDL} = $\overline{RASIN}$ to $\overline{RAS}$ delay

and t_{RHA} = row address held from R/$\overline{C}$ going low.

The delay between $\overline{RASIN}$ and R/$\overline{C}$ that guarantees the specified DRAM t_{RAH} is given by

$$\text{MINIMUM } \overline{RASIN} \text{ to R/}\overline{C} = t_{DIF1} + t_{RAH}.$$

Example

In an application using DRAMs that require a minimum t_{RAH} of 15 ns, the following demonstrates how the maximum $\overline{RASIN}$ to $\overline{CAS}$ time is determined.

With t_{DIF1} (from Switching Characteristics) = 7 ns,

$\overline{RASIN}$ to R/$\overline{C}$ delay = 7 ns + 15 ns = 22 ns.

A delay line of 25 ns will be sufficient.

With Auto-$\overline{CAS}$ generation, the maximum delay from R/$\overline{C}$ to $\overline{CAS}$ (loaded with 600 pF) is 46 ns. Thus the maximum $\overline{RASIN}$ to $\overline{CAS}$ time is 71 ns, under the given conditions.

With a maximum $\overline{RASIN}$ to $\overline{RAS}$ time (t_{RPDL}) of 20 ns, the maximum $\overline{RAS}$ to $\overline{CAS}$ time is about 51 ns. Most DRAMs with a 15 ns minimum t_{RAH} have a maximum t_{RCD} of about 60 ns. Thus, memory accesses are likely to be $\overline{RAS}$ limited instead of $\overline{CAS}$ limited. In other words, memory access time is limited by DRAM performance, not controller performance.

REFRESHING IN CONJUNCTION WITH MODE 4

If using mode 4 to access memory, mode 0 (externally controlled refresh) must be used for all refreshing.

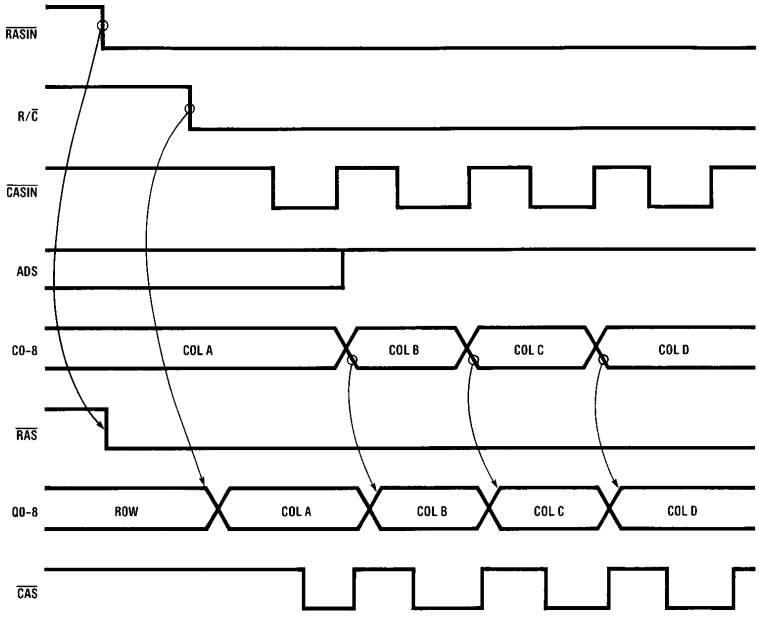
MODE 5 – AUTOMATIC ACCESS WITH HIDDEN REFRESHING CAPABILITY

Automatic-Access has two advantages over the externally controlled access (mode 4). First, $\overline{RAS}$, $\overline{CAS}$ and the row to column change are all derived internally from one input signal, $\overline{RASIN}$. Thus the need for an external delay line (see mode 4) is eliminated.

Secondly, since R/$\overline{C}$ and $\overline{CASIN}$ are not needed to generate the row to column change and $\overline{CAS}$, these pins can be used for the automatic refreshing function.

AUTOMATIC ACCESS CONTROL

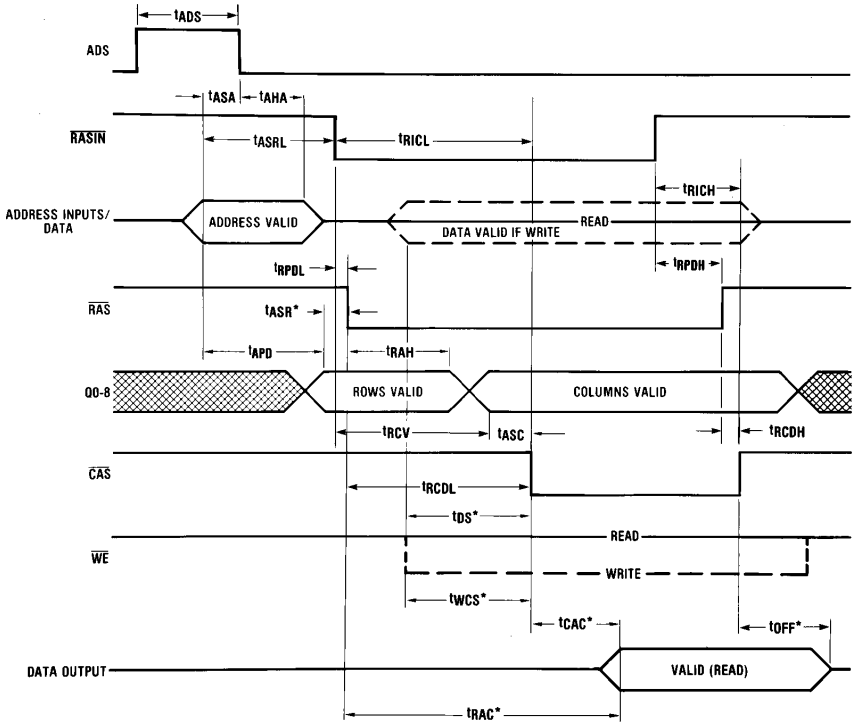
Mode 5 of the DP8419 makes accessing Dynamic RAM nearly as easy as accessing static RAM. Once row and column addresses are valid (latched on the DP8419 if necessary), $\overline{RASIN}$ going low is all that is required to perform the memory access.



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FIGURE 5c. Page or Nibble Access in Mode 4

DP8419 Mode Descriptions (Continued)



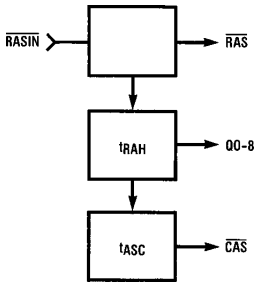
*Indicates Dynamic RAM Parameters

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FIGURE 6. Mode 5 Timing

(Refer to *Figure 6*) In mode 5 the selected $\overline{RAS}$ follows $\overline{RASIN}$ immediately, as in mode 4, to strobe the row address into the DRAMs. The row address remains valid on the DP8419 address outputs long enough to meet the t_{RAH} requirement of the DRAMs (pin 4, RAHS, of the DP8419 allows the user two choices of t_{RAH}). Next, the column address replaces the row address on the address outputs and $\overline{CAS}$ goes low to strobe the columns into the DRAMs. $\overline{WIN}$ determines whether a read, write or read-modify-write is done.

The diagram below illustrates mode 5 automatic control signal generation.



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REFRESHING IN CONJUNCTION WITH MODE 5

When using mode 5 to perform memory accesses, refreshing may be accomplished:

(a) externally (in mode 0 or mode 1)

(b) by a combination of mode 5 (hidden refresh) and mode 1 (auto-refresh)

or (c) by a combination of mode 5 and mode 0

(a) Externally Controlled Refreshing in Mode 0 or Mode 1

All refreshing may be accomplished using external refreshes in either mode 0 or mode 1 with R/$\overline{C}$ (RFCK) tied high (see mode 0 and mode 1 descriptions). If this is desired, the system determines when a refresh will be performed, puts the DP8419 in the appropriate mode, and controls the $\overline{RAS}$ signals directly with $\overline{RASIN}$. The on-chip refresh counter is enabled to the address outputs of the DP8419 when the refresh mode is entered, and increments when $\overline{RASIN}$ goes high at the completion of the refresh.

(b) Mode 5 Refreshing (hidden) with Mode 1 refreshing (auto)

(Refer to *Figure 7a*) If RFCK is tied to a clock (see mode 1 description), RFI/O becomes a refresh request output and goes low following RFCK going low if no refresh occurred while RFCK was high. Refreshes may be performed in mode 5 when the DP8419 is not selected for access ($\overline{CS}$ is high) and RFCK is high. If these conditions exist the refresh counter contents appear on the DP8419 address outputs and all $\overline{RAS}$ lines follow $\overline{RASIN}$ so that if $\overline{RASIN}$ goes low (an access other than through the DP8419 occurs), all $\overline{RAS}$ lines go low to perform the refresh. The DP8419 allows only one refresh of this type for each period of RFCK, since RFCK should be fast enough such that one refresh per period is sufficient to meet the DRAM refresh requirement.

DP8419 Mode Descriptions (Continued)

Once it is started, a hidden refresh will continue even if RFCK goes low. However, $\overline{CS}$ must be high throughout the refresh (until $\overline{RASIN}$ goes high).

These hidden refreshes are valuable in that they do not delay accesses. When determining the duty cycle of RFCK, the high time should be maximized in order to maximize the probability of hidden refreshes. If a hidden refresh doesn't happen, then a refresh request will occur on RFI/O when RFCK goes low. After receiving the request, the system must perform a refresh while RFCK is low. This may be done by going to mode 1 and allowing an automatic refresh (see mode 1 description). This refresh must be completed while RFCK is low, thus the RFCK low time is determined by the worst-case time required by the system to respond to a refresh request.

(c) Mode 5 Refresh (Hidden Refresh) with mode 0 Refresh (External Refresh)

This refresh scheme is identical to that in (b) except that after receiving a refresh request, mode 0 is entered to do the refresh (see mode 0 description). The refresh request is terminated (RFI/O goes high) as soon as mode 0 is entered. This method requires more control than using mode 1 (auto-refresh), however, it may be desirable if the mode 1 refresh time is considered to be excessive.

Example

Figure 7b demonstrates how a system designer would use the DP8419 in mode 5 based on certain characteristics of his system.

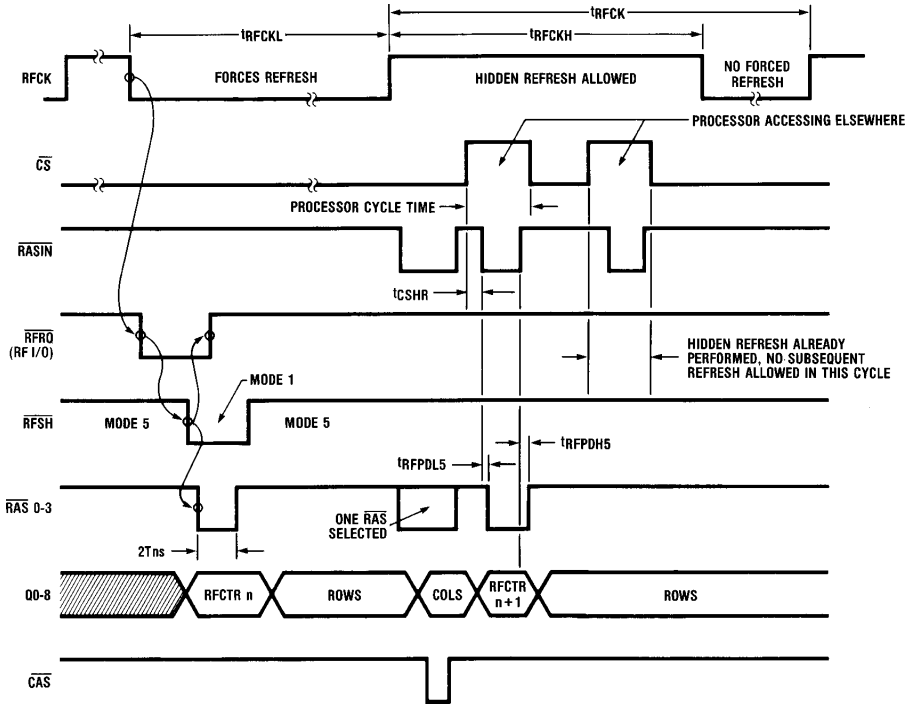
System Characteristics:

1) DRAM used has min t_{RAH} requirement of 15 ns and min t_{ASR} of 0 ns
2) DRAM address is valid from time T_V to the end of the memory cycle
3) four banks of twenty-two 256K memory chips each are being driven

Using the DP8419 (see *Figure 7b*):

1) Tie pin 4 (RAHS) high to guarantee a 15 ns minimum t_{RAH} which is sufficient for the DRAMs being used
2) Generate $\overline{RASIN}$ no earlier than time $T_V + t_{ASRL}$ (see switching characteristics), so that the row address is valid on the DRAM address inputs before $\overline{RAS}$ occurs
3) Tie ADS high since latching the DRAM address on the DP8419 is not necessary
4) Connect the first 18 system address bits to R0-R8 and C0-C8, and bits 19 and 20 to B0 and B1
5) Connect each $\overline{RAS}$ output of the DP8419 to the $\overline{RAS}$ inputs of the DRAMs of one bank of the memory array; connect Q0-Q8 of the DP8419 to A0-A8 of all DRAMs; connect $\overline{CAS}$ of the DP8419 to $\overline{CAS}$ of all the DRAMs

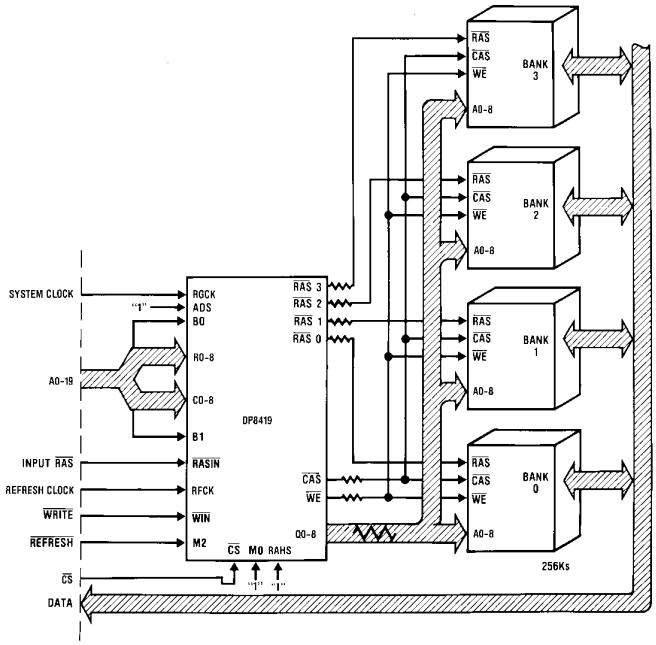
Figure 7c illustrates a similar example using the DP8418 to drive two 32-bit banks.



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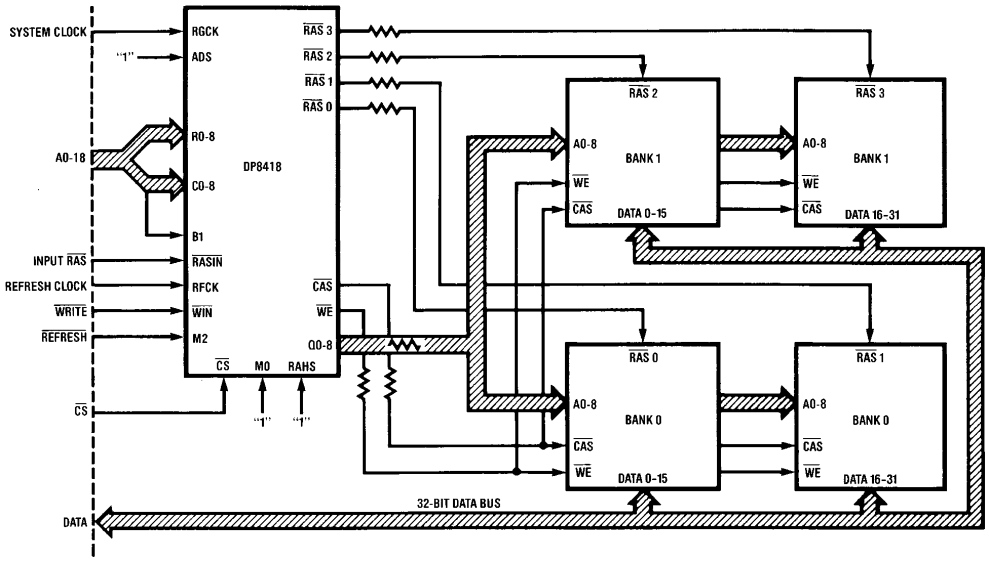
FIGURE 7a. Hidden Refreshing (Mode 5) and Forced Refreshing (Mode 1) Timing

DP8419 Mode Descriptions (Continued)



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FIGURE 7b. Typical Application of DP8419 Using Modes 5 and 1



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FIGURE 7c. Typical Application of DP8418 Using Modes 5 and 1

Applications

If one desires a memory interface containing the DP8419 that minimizes the number of external components required, modes 5 and 1 should be used. These two modes provide:

1) Automatic access to memory (in mode 5 only one signal, $\overline{RASIN}$, is required in order to access memory)
2) Hidden refresh capability (refreshes are performed automatically while in mode 5 when non-local accesses are taking place, as determined by $\overline{CS}$)
3) Refresh request capability (if no hidden refresh took place while RFCK was high, a refresh request is generated at the RFI/O pin when RFCK goes high)
4) Automatic forced refresh (If a refresh request is generated while in mode 5, as described above, external logic should switch the DP8419 into mode 1 to do an automatic forced refresh. No other external control signals need be issued. WAIT states can be inserted into the processor machine cycles if the system tries to access memory while the DP8419 is in mode 1 doing a forced refresh).

Some items to be considered when integrating the DP8419 into a system design are:

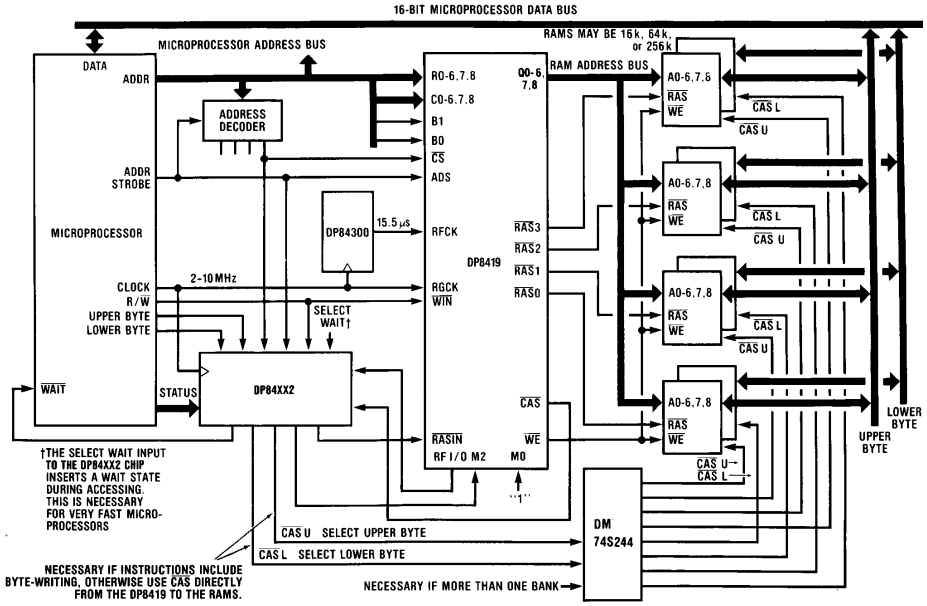
1) The system designer should ensure that a DRAM access not be in progress when a refresh mode is entered. Similarly, one should not attempt to start an access while a refresh is in progress. The parameter $t_{\overline{RFH}RL}$ specifies the minimum time from $\overline{RFSH}$ high to $\overline{RASIN}$ going low to initiate an access.
2) One should always guarantee that the DP8419 is enabled for access prior to initiating the access (see t_{CSRL1}).
3) One should bring $\overline{RASIN}$ low even during non-local access cycles when in mode 5 in order to maximize the chance of a hidden refresh occurring.
4) At lower frequencies (under 10 Mhz), it becomes increasingly important to differentiate between READ and WRITE cycles. $\overline{RASIN}$ generation during READ cycles can take place as soon as one knows that a processor READ access cycle has started. WRITE cycles, on the other hand, cannot start until one knows that the data to be written at the DRAM inputs will be valid a setup time before $\overline{CAS}$ (column address strobe) goes true at the DRAM inputs. Therefore, in general, READ cycles can be initiated earlier than WRITE cycles.
5) Many times it is possible to only add WAIT states during READ cycles and have no WAIT states during WRITE cycles. This is because it generally takes less time to write data into memory than to read data from memory.

The DP84XX2 family of inexpensive preprogrammed medium Programmable Array Logic devices (PALs) have been developed to provide an easy interface between various microprocessors and the DP84XX family of DRAM controller/drivers. These PALs interface to all the necessary control signals of the particular processor and the DP8419. The PAL controls the operation of the DP8419 in modes 5 and 1, while meeting all the critical timing considerations discussed above. The refresh clock, RFCK, may be divided down from the processor clock using an IC counter such as the DM74LS393 or the DP84300 programmable refresh timer. The DP84300 can provide RFCK periods ranging from 15.4 μs to 15.6 μs based on an input clock of 2 to 10 MHz. *Figure 8* shows a general block diagram for a system using the DP8419 in modes 1 and 5. *Figure 9* shows possible timing diagrams for such a system (using $\overline{WAIT}$ to prohibit access when refreshing). Although the DP84XX2 PALs are offered as standard peripheral devices for the DP84XX DRAM controller/drivers, the programming equations for these devices are provided so the user may make minor modification, for unique system requirements.

ADVANTAGES OF DP8419 OVER A DISCRETE DYNAMIC RAM CONTROLLER

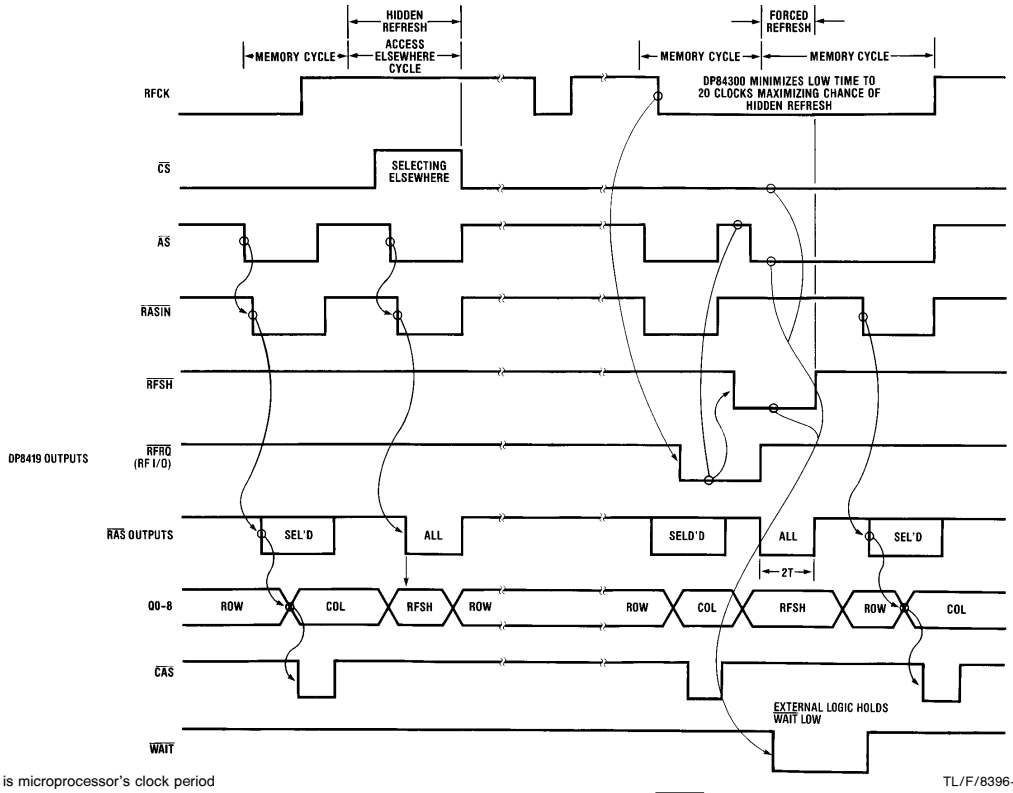
1) The DP8419 system solution takes up much less board space because everything is on one chip (latches, refresh counter, control logic, multiplexers, drivers, and internal delay lines).
2) Less effort is needed to design a memory system. The DP8419 has automatic modes (1 and 5) which require a minimum of external control logic. Also programmable array logic devices (PALs) have been designed which allow an easy interface to most popular microprocessors (Motorola 68000 family, National Semiconductor 32032 family, Intel 8086 family, and the Zilog Z8000 family).
3) Less skew in memory timing parameters because all critical components are on one chip (many discrete drivers specify a minimum on-chip skew under worst-case conditions, but this cannot be used if more then one driver is needed, such as would be the case in driving a large dynamic RAM array).
4) Our switching characteristics give the designer the critical timing specifications based on TTL output levels (low = 0.8V, high = 2.4V) at a specified load capacitance. All timing parameters are specified on the DP8419:
   A) driving 88 DRAM's over a temperature range of 0–70 degrees centigrade (no extra drivers are needed).
   B) under worst-case driving conditions with all outputs switching simultaneously (most discrete drivers on the market specify worst-case conditions with only one output switching at a time; this is not a true worst-case condition!).

Applications (Continued)



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FIGURE 8. Connecting the DP8419 Between the 16-bit Microprocessor and Memory



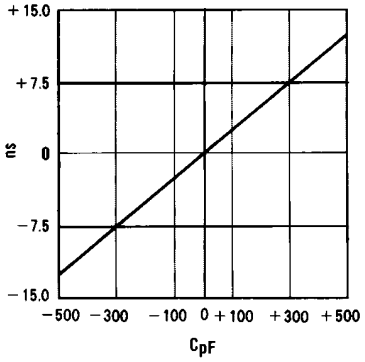
*T is microprocessor's clock period

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FIGURE 9. DP8419 Auto Refresh, Access with $\overline{\text{WAIT}}$ States

Switching Characteristics

All AC parameters are specified with the equivalent load capacitances, including traces, of 88 DRAMs organized as 4 banks of 22 DRAMs each. Maximums are based on worst-case conditions including all outputs switching simultaneously. This, in many cases, results in the AC values shown in the DP84XX DRAM controller data sheet being much looser than true worst case (maximum) AC delays. The system designer should estimate the DP8419 load in his/her application, and modify the appropriate AC parameters using the graph in *Figure 10*. Two example calculations are provided below.



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FIGURE 10. Change in Propagation Delay Relative to "True" (Application) Load Minus AC Specified Data Sheet Load

2 Examples

#1) A mode 4 user driving 2 16-bit banks of DRAM has the following approximate "true" loading conditions:

$\overline{CAS}$ - 300 pF

Q0-Q8 - 250 pF

$\overline{RAS}$ - 150 pF

max t_{RPDL} = 20 ns − 0 ns = 20 ns (since $\overline{RAS}$ loading is the same as that which is spec'ed)

max t_{CPDL} = 32 ns − 7 ns = 25 ns

max t_{CCAS} = 46 ns − 7 ns = 39 ns

max t_{RCC} = 41 ns − 6 ns = 35 ns

min t_{RHA} is not significantly effected since it does not involve an output transition

Other parameters are adjusted in a similar manner.

#2) A mode 5 user driving one 16-bit bank of DRAM has the following approximate "true" loading conditions:

$\overline{CAS}$ - 120 pF

Q0-Q8 - 100 pF

$\overline{RAS}$ - 120 pF

A. C. parameters should be adjusted as follows:

with RAHS = "1",

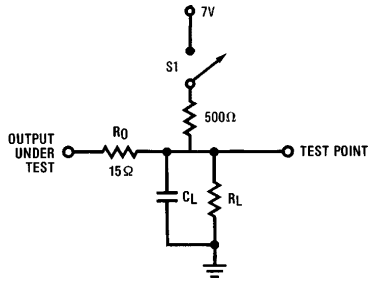
max t_{RICL} = 70 ns − 11 ns = 59 ns

max t_{RCDL} = 55 ns + 1 ns − 11 ns = 45 ns

(the + 1 ns is due to lighter $\overline{RAS}$ loading; the − 11 ns is due to lighter $\overline{CAS}$ loading)

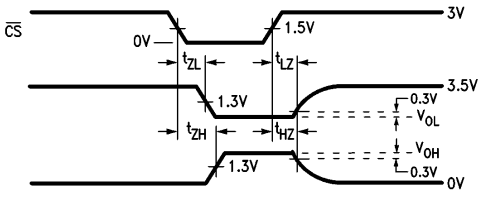
min t_{RAH} = 15 ns + 1 ns = 16 ns

The additional 1 ns is due to the fact that the $\overline{RAS}$ line is driving less (switching faster) than the load to which the 15 ns spec applies. The row address will remain valid for about the same time irregardless of address loading since it is considered to be not valid at the beginning of its transition.



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FIGURE 11a. Output Load Circuit



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FIGURE 11b. DP8417 TRI-STATE Waveforms

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply voltage, V_{CC}	7.0V
Storage Temperature Range	−65°C to +150°C
Input Voltage	5.5V
Output Current	150 mA
Lead Temp. (Soldering, 10 seconds)	300°C

Operating Conditions

		Min	Max	Units
V_{CC}	Supply Voltage	4.50	5.50	V
T_A	Ambient Temperature	0	+70	°C

Electrical Characteristics V_{CC} = 5.0V ±10%, 0°C ≤ T_A ≤ 70°C unless otherwise noted (Note 2)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_C	Input Clamp Voltage	V_{CC} = Min, I_C = − 12 mA		− 0.8	− 1.2	V
I_{IH}	Input High Current for all Inputs	V_{IN} = 2.5V		2.0	100	μA
I_I RSI	Output Load Current for RFI/O	V_{IN} = 0.5V, Output high		−0.7	−1.5	mA
I_{IL_1}	Input Low Current for all Inputs**	V_{IN} = 0.5V		−0.02	−0.25	mA
I_{IL2}	ADS, R/$\overline{C}$, $\overline{CS}$, M2, $\overline{RASIN}$	V_{IN} = 0.5V		−0.05	−0.5	mA
V_{IL}	Input Low Threshold				0.8	V
V_{IH}	Input High Threshold		2.0			V
V_{OL1}	Output Low Voltage*	I_{OL} = 20 mA		0.3	0.5	V
V_{OL2}	Output Low Voltage for RFI/O	I_{OL} = 8 mA		0.3	0.5	V
V_{OH1}	Output High Voltage*	I_{OH} = − 1 mA	2.4	3.5		V
V_{OH2}	Output High Voltage for RFI/O	I_{OH} = − 100 μA	2.4	3.5		V
I_{1D}	Output High Drive Current*	V_{OUT} = 0.8V (Note 3)	−50	− 200		mA
I_{0D}	Output Low Drive Current*	V_{OUT} = 2.4V (Note 3)	50	200		mA
I_{CC}	Supply Current	V_{CC} = Max		150	240	mA

*Except RFI/O

**Except RFI/O, ADS, R/$\overline{C}$, $\overline{CS}$, M2, $\overline{RASIN}$

Switching Characteristics: DP8417, DP8418, DP8419, DP8419X

V_{CC} = 5.0V ±10%, 0°C ≤ T_A ≤ 70°C unless otherwise noted (Notes 2, 4, 5), the output load capacitance is typical for 4 banks of 22 DRAMs each or 88 DRAMs, including trace capacitance.

*** These values are Q0-Q8, C_L = 500 pF; $\overline{RAS}$0–$\overline{RAS}$3, C_L = 150 pF; $\overline{WE}$, C_L = 500 pF; $\overline{CAS}$, C_L = 600 pF; RL = 500Ω unless otherwise noted. See *Figure 11a* for test load. S1 is open unless otherwise noted. Maximum propagation delays are specified with all outputs switching.**

** **Preliminary**

Symbol	Parameter	Condition	*CL		**All C_L = 50 pF		Units
			Min	Max	Min	Max	
ACCESS							
t_{RICL0}	$\overline{RASIN}$ to $\overline{CAS}$ Low Delay (RAHS = 0)	*Figure 6* DP8417, 18, 19-80	57	97	42	85	ns
t_{RICL0}	$\overline{RASIN}$ to $\overline{CAS}$ Low Delay (RAHS = 0)	*Figure 6* DP8417, 18, 19-70	57	87	42	75	ns
t_{RICL1}	$\overline{RASIN}$ to $\overline{CAS}$ Low Delay (RAHS = 1)	*Figure 6* DP8417, 18, 19-80	48	80	35	68	ns
t_{RICL1}	$\overline{RASIN}$ to $\overline{CAS}$ Low Delay (RAHS = 1)	*Figure 6* DP8417, 18, 19-70	48	70	35	58	ns
t_{RICH}	$\overline{RASIN}$ to $\overline{CAS}$ High Delay	*Figure 6*		37			ns
t_{RCDL0}	$\overline{RAS}$ to $\overline{CAS}$ Low Delay (RAHS = 0)	*Figure 6* DP8417, 18, 19-80	43	80			ns
t_{RCDL0}	$\overline{RAS}$ to $\overline{CAS}$ Low Delay (RAHS = 0)	*Figure 6* DP8417, 18, 19-70	43	72			ns
t_{RCDL1}	$\overline{RAS}$ to $\overline{CAS}$ Low Delay (RAHS = 1)	*Figure 6* DP8417, 18, 19-80	34	63			ns
t_{RCDL1}	$\overline{RAS}$ to $\overline{CAS}$ Low Delay (RAHS = 1)	*Figure 6* DP8417, 18, 19-70	34	55			ns
t_{RCDH}	$\overline{RAS}$ to $\overline{CAS}$ High Delay	*Figure 6*		22			ns
t_{RAH0}	Row Address Hold Time (RAHS = 0, Mode 5)	*Figure 6*	25		25		ns
t_{RAH1}	Row Address Hold Time (RAHS = 1, Mode 5)	*Figure 6*	15		15		ns
t_{ASC}	Column Address Set-up Time (Mode 5)	*Figure 6*	0		0		ns

Switching Characteristics: DP8417, DP8418, DP8419, DP8419X (Continued)

V_{CC} = 5.0V ±10%, 0°C ≤ T_A ≤ 70°C unless otherwise noted (Notes 2, 4, 5). The output load capacitance is typical for 4 banks of 22 DRAMs each or 88 DRAMs, including trace capacitance.

* **These values are Q0-Q8, C_L = 500 pF; $\overline{RAS}$0–$\overline{RAS}$3, C_L = 150 pF; $\overline{WE}$, C_L = 500 pF; $\overline{CAS}$, C_L = 600 pF; RL = 500Ω unless otherwise noted. See *Figure 11a* for test load. S1 is open unless otherwise specified. Maximum propagation delays are specified with all outputs switching.**

** **Preliminary**

Symbol	Parameter	Condition	*CL		**All C_L = 50 pF		Units
			Min	Max	Min	Max	
ACCESS (Continued)							
t_{RCV0}	$\overline{RASIN}$ to Column Address Valid (RAHS = 0, Mode 5)	*Figure 6* DP8417, 18, 19-80		94			ns
t_{RCV0}	$\overline{RASIN}$ to Column Address Valid (RAHS = 0, Mode 5)	*Figure 6* DP8417, 18, 19-70		85			ns
t_{RCV1}	$\overline{RASIN}$ to Column Address Valid (RAHS = 1, Mode 5)	*Figure 6* DP8417, 18, 19-80		76			ns
t_{RCV1}	$\overline{RASIN}$ to Column Address Valid (RAHS = 1, Mode 5)	*Figure 6* DP8417, 18, 19-70		68			ns
t_{RPDL}	$\overline{RASIN}$ to $\overline{RAS}$ Low Delay	*Figures 5a, 5b, 6*		21		18	ns
t_{RPDH}	$\overline{RASIN}$ to $\overline{RAS}$ High Delay	*Figures 5a, 5b, 6*		20		17	ns
t_{ASRL}	Address Set-up to $\overline{RASIN}$ low	*Figures 5a, 5b, 6*	13				ns
t_{APD}	Address Input to Output Delay	*Figures 5a, 5b, 6*		36		25	ns
t_{SPD}	Address Strobe High to Address Output Valid	*Figures 5a, 5b*		48			ns
t_{ASA}	Address Set-up Time to ADS	*Figures 5a, 5b, 6*	5				ns
t_{AHA}	Address Hold Time from ADS	*Figures 5a, 5b, 6*	10				ns
t_{ADS}	Address Strobe Pulse Width	*Figures 5a, 5b, 6*	26				ns
t_{WPD}	$\overline{WIN}$ to $\overline{WE}$ Output Delay	*Figure 5b*		28			ns
t_{CPDL}	$\overline{CASIN}$ to $\overline{CAS}$ Low Delay (R/$\overline{C}$ low, Mode 4)	*Figure 5b*	17	33			ns
t_{CPDH}	$\overline{CASIN}$ to $\overline{CAS}$ High Delay (R/$\overline{C}$ low, Mode 4)	*Figure 5b*	13	33			ns
t_{CPdif}	t_{CPDL} - t_{CPDH}	See Mode 4 Description		13			ns
t_{RCC}	Column Select to Column Address Valid	*Figure 5a*		41			ns
t_{RCR}	Row Select to Row Address Valid	*Figures 5a, 5b*		45			ns
t_{RHA}	Row Address Held from Column Select	*Figure 5a*	7				ns
t_{CCAS}	R/$\overline{C}$ Low to $\overline{CAS}$ Low Delay ($\overline{CASIN}$ Low, Mode 4)	*Figure 5a* DP8417, 18, 19-80		50			ns
t	R/$\overline{C}$ Low to $\overline{CAS}$ Low Delay ($\overline{CASIN}$ Low, Mode 4)	*Figure 5a* DP8417, 18, 19-70		46			ns
t_{DIF1}	Maximum (t_{RPDL} - t_{RHA})	See Mode 4 Description		7			ns
t_{DIF2}	Maximum (t_{RCC} - t_{CPDL})			13			ns
REFRESH							
t_{RC}	Refresh Cycle Period	*Figure 2a*	100				ns
$t_{RASINL,H}$	Pulse Width of $\overline{RASIN}$ during Refresh	*Figure 2a*	50				ns
t_{RFPDL0}	$\overline{RASIN}$ to $\overline{RAS}$ Low Delay during Refresh (Mode 0)	*Figure 2a*		28			ns

Switching Characteristics: DP8417, DP8418, DP8419, DP8419X (Continued)

V_{CC} = 5.0V ±10%, 0°C ≤ T_A ≤ 70°C unless otherwise noted (Notes 2, 4, 5). The output load capacitance is typical for 4 banks of 22 DRAMs each or 88 DRAMs, including trace capacitance.

*** These values are Q0-Q8, C_L = 500 pF; $\overline{RAS}$0–$\overline{RAS}$3, C_L = 150 pF; $\overline{WE}$, C_L = 500 pF; $\overline{CAS}$, C_L = 600 pF; RL = 500Ω unless otherwise noted. See *Figure 11a* for test load. S1 is open unless otherwise specified. Maximum propagation delays are specified with all outputs switching.**

Symbol	Parameter	Condition	*CL		All C_L = 50 pF		Units
			Min	Max	Min	Max	
REFRESH (Continued)							
t_{RFPDL5}	$\overline{RASIN}$ to $\overline{RAS}$ Low Delay during Hidden Refresh	*Figure 7*		38			ns
t_{RFPDH0}	$\overline{RASIN}$ to $\overline{RAS}$ High Delay during Refresh (Mode 0)	*Figure 2a*		35			ns
t_{RFPDH5}	$\overline{RASIN}$ to $\overline{RAS}$ High Delay during Hidden Refresh	*Figure 7*		44			ns
t_{RFLCT}	$\overline{RFSH}$ Low to Counter Address Valid	*Figures 2a, 3* $\overline{CS}$ = X		38			ns
t_{RFLRL}	$\overline{RFSH}$ Low Set-up to $\overline{RASIN}$ Low (Mode 0), to get Minimum t_{ASR} = 0	*Figure 2a*	12				ns
t_{RFHRL}	$\overline{RFSH}$ High Setup to Access $\overline{RASIN}$ Low	*Figure 3*	25				ns
t_{RFHRV}	$\overline{RFSH}$ High to Row Address Valid	*Figure 3*		43			ns
t_{ROHNC}	$\overline{RAS}$ High to New Count Valid	*Figure 2a*		42			ns
t_{RST}	Counter Reset Pulse Width	*Figure 2a*	60				ns
t_{CTL}	RFI/O Low to Counter Outputs All Low	*Figure 2a*		100			ns
$t_{RFCKL,H}$	Minimum Pulse Width of RFCK	*Figure 7*	100				ns
T	Period of $\overline{RAS}$ Generator Clock	*Figure 3*	30				ns
t_{RGCKL}	Minimum Pulse Width Low of RGCK	*Figure 3*	15				ns
t_{RGCKH}	Minimum Pulse Width High of RGCK	*Figure 3*	15				ns
t_{FRQL}	RFCK Low to Forced $\overline{RFRQ}$ (RFI/O) Low	*Figure 3* C_L = 50 pF RL = 35k		66			ns
t_{FRQH}	RGCK Low to Forced $\overline{RFRQ}$ High	*Figure 3* C_L = 50 pF RL = 35k		55			ns
t_{RGRL}	RGCK Low to $\overline{RAS}$ Low	*Figure 3*	20	41			ns
t_{RGRH}	RGCK Low to $\overline{RAS}$ High	*Figure 3*	20	48			ns

Switching Characteristics: DP8417, DP8418, DP8419, DP8419X (Continued)

V_{CC} = 5.0V ±10%, 0°C ≤ T_A ≤ 70°C unless otherwise noted (Notes 2, 4, 5). The output load capacitance is typical for 4 banks of 22 DRAMs each or 88 DRAMs, including trace capacitance.

*** These values are Q0-Q8, C_L = 500 pF; $\overline{RAS0}$–$\overline{RAS3}$, C_L = 150 pF; $\overline{WE}$, C_L = 500 pF; $\overline{CAS}$, C_L = 600 pF; RL = 500Ω unless otherwise noted. See *Figure 11a* for test load. S1 is open unless otherwise specified. Maximum propagation delays are specified with all outputs switching.**

Symbol	Parameter	Condition	*CL		All C_L = 50 pF		Units
			Min	Max	Min	Max	
REFRESH (Continued)							
t_{RQHRF}	$\overline{RFSH}$ Hold Time from RGCK	*Figure 3*	2T				ns
t_{RFRH}	$\overline{RFSH}$ High to $\overline{RAS}$ High (Ending Forced Refresh early)	(See Mode 1 Description)		42			ns
t_{RFSRG}	$\overline{RFSH}$ Low Set-up to RGCK Low (Mode 1)	(See Mode 1 Description) *Figure 3*	12				ns
t_{CSHR}	$\overline{CS}$ High to $\overline{RASIN}$ Low for Hidden Refresh	*Figure 7*	10				ns
t_{RKRL}	RFCK High to $\overline{RASIN}$ low for hidden Refresh		50				ns
DP8419, DP8419X ONLY							
t_{CSRL1}	$\overline{CS}$ Low to Access $\overline{RASIN}$ Low (Using Mode 5 with Auto Refresh Mode)	*Figure 3*	34				ns
t_{CSRL0}	$\overline{CS}$ Low to Access $\overline{RASIN}$ Low (Using Modes 4 or 5 with externally controlled Refresh)	(See Mode 5 Description)	5				ns
DP8418 ONLY							
t_{CSRL1}	$\overline{CS}$ Low to Access $\overline{RASIN}$ Low (Using Mode 5 with Auto Refresh Mode)	*Figure 3*	5				ns
t_{CSRL0}	$\overline{CS}$ Low to Access $\overline{RASIN}$ Low (Using Modes 4 or 5 with externally controlled Refresh)	(See Mode 5 Description)	5				ns
DP8417 ONLY — PRELIMINARY							
t_{CSRL1}	$\overline{CS}$ Low to Access $\overline{RASIN}$ Low (Using Mode 5 with Auto Refresh Mode)	*Figure 3*	34				ns
t_{CSRL0}	$\overline{CS}$ Low to Access $\overline{RASIN}$ Low (Using Modes 4 or 5 with externally controlled Refresh)	(See Mode 5 Description)	34				ns
TRI-STATE (DP8417 ONLY)							
t_{ZH}	$\overline{CS}$ Low to Output High from Hi-Z	S1 Open *Figure 11b*		50			ns
t_{HZ}	$\overline{CS}$ High to Output Hi-Z from High	S1 Open, Q, $\overline{WE}$ *Figure 11b*				50	ns
t_{HZ}	$\overline{CS}$ High to Output Hi-Z from High	S1 Open, $\overline{RAS}$0-3 $\overline{CAS}$0-3 *Figure 11b*				95	ns
t_{ZL}	$\overline{CS}$ Low to Output Low from Hi-Z	S1 Closed *Figure 11b*		50			ns
t_{LZ}	$\overline{CS}$ High to Output Hi-Z from Low	S1 Closed *Figure 11b*				50	ns

Input Capacitance T_A = 25°C (Note 2)

Symbol	Parameter	Condition	Min	Typ	Max	Units
C_{IN}	Input Capacitance ADS, R/$\overline{C}$, $\overline{CS}$, M2, $\overline{RASIN}$			8		pF
C_{IN}	Input Capacitance All Other Inputs			5		pF

Note 1: ''Absolute Maximum Ratings'' are the values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of ''Electrical Characteristics'' provides conditions for actual device operation.

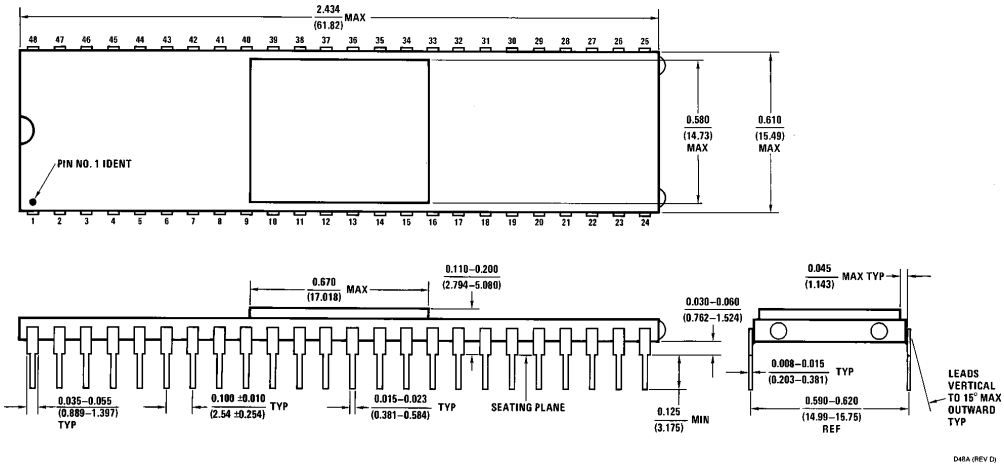
Note 2: All typical values are for $T_A = 25°C$ and $V_{CC} = 5.0V$.

Note 3: This test is provided as a monitor of Driver output source and sink current capability. Caution should be exercised in testing this parameter. In testing these parameters, a 15Ω resistor should be placed in series with each output under test. One output should be tested at a time and test time should not exceed 1 second.

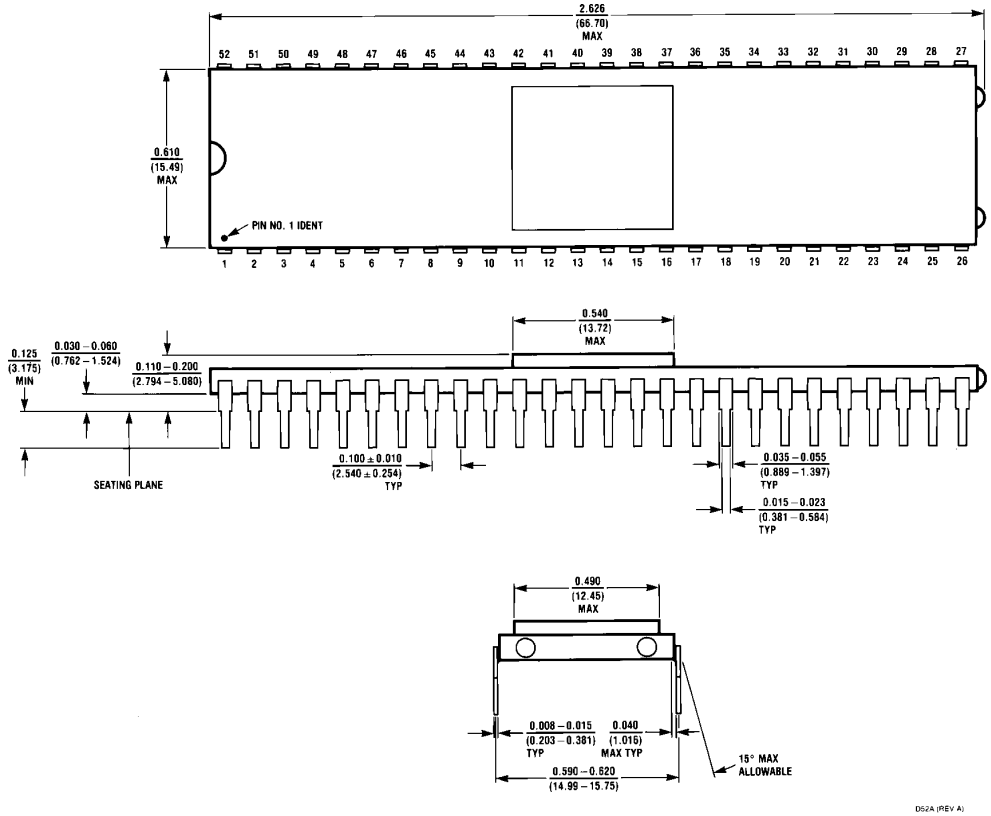
Note 4: Input pulse 0V to 3.0V, $t_R = t_F = 2.5$ ns, f = 2.5 MHz, $t_{PW} = 200$ ns. Input reference point on AC measurements is 1.5V Output reference points are 2.4V for High and 0.8V for Low.

Note 5: The load capacitance on RF I/O should not exceed 50 pF.

Physical Dimensions inches (millimeters)

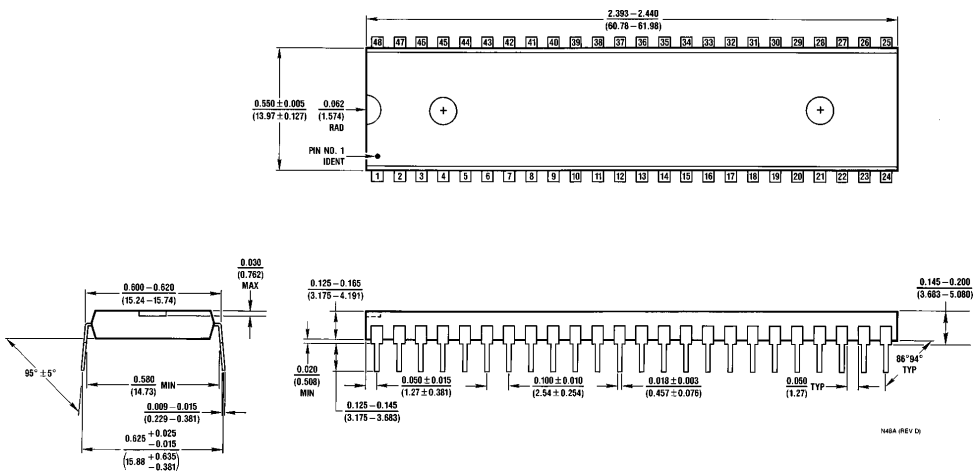


Hermetic Dual-in-Line Package (D)
Order Number DP8417D-70 or DP8417D-80; DP8418D-70
or DP8418D-80; or DP8419D-70 or DP8419D-80
NS Package Number D48A



Hermetic Dual-in-Line Package (D)
Order Number DP8419XD-80 or DP8419XD-70
NS Package Number D52A

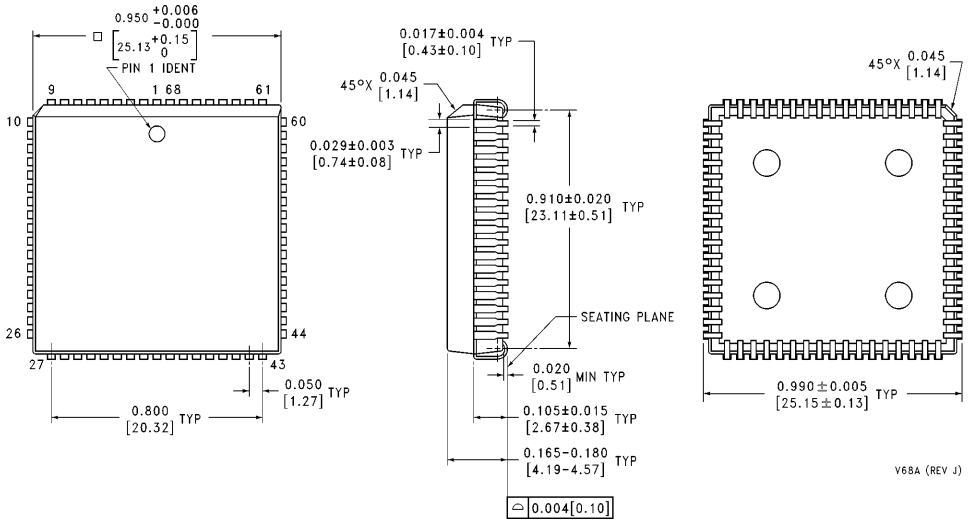
Physical Dimensions inches (millimeters) (Continued)



Molded Dual-in-Line Package (N)
Order Number DP8417N-70 or DP8417N-80; or DP8418N-70
or DP8418N-80; or DP8419N-70 or DP8419N-80
NS Package Number N48A

Physical Dimensions inches (millimeters) (Continued)

Lit. # 103070



Plastic Chip Carrier (V)
Order Number DP8417V-70 or DP8417V-80; or DP8418V-70 or DP8418V-80; or DP8419V-70 or DP8419V-80
NS Package Number V68A

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