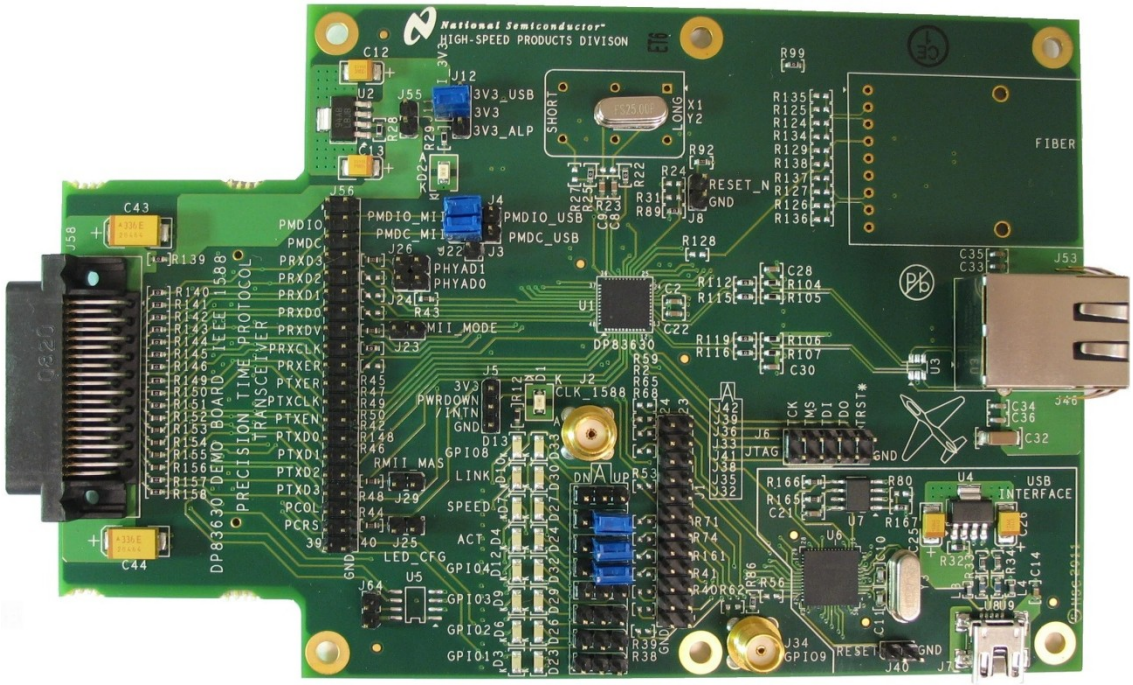
National Semiconductor

The Sight & Sound of Information

10/100 Mb/s Ethernet Products

DP83630
Ethernet Physical Layer Transceiver
Demo Board User Guide



Interface Division

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National Semiconductor

The Sight & Sound of Information

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1 General Description

The purpose of the DP83630 Demo Board is to provide National Semiconductor Corp.'s customers with a vehicle to quickly design and market systems containing the DP83630. Customers are encouraged to copy EVK components to expedite their design process.

The EVK contains:

- DP83630 Demo Board
- USB cable
- Cover letter
- DP83630 Demo licensing agreement

Links to the EVK design files and this User Guide can be found via the DP83630 product folder on the National Semiconductor website (www.national.com).

2 Quick Start

The DP83630 Demo Board is fully assembled and factory tested. Follow the instructions below to set up the hardware platform for the measurement of interest.

2.1 Power Connection

The DP83630 Demo Board provides several options for supplying power to the board. Power can be supplied by way of the MII interface at 3.3 V or 5.0 V, USB interface, or directly from an external supply.

2.1.1 MII Interface (Default)

To allow the board to be supplied by the MII interface a 0 ohm resistor must be inserted at R139. Placing the jumper between J11 and pin 2 of J12 will connect the 3.3 V power plane to the MII 3.3V supply. In the case of an MII interface that supplies 5.0 V, an on board 3.3 V regulator is provided and no jumper should be placed on J55. For a 3.3 V MII supply, a jumper should be placed on J55 to bypass the regulator. In both cases, LED D2 will illuminate if a voltage is available at J11. The following image shows the default jumper configuration.

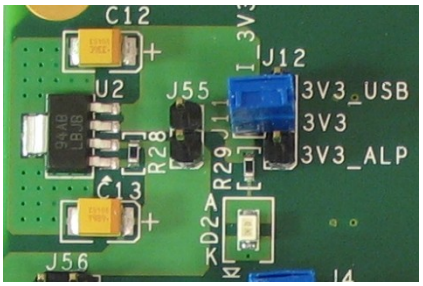


Figure 1. Default Power Supply Connection

2.1.2 USB Interface

To supply the device using the USB interface, a jumper should be placed between pins 2 and 3 of J12.

2.1.3 External Supply

The board can be supplied from an external supply by removing the jumper on J12 and connecting the external 3.3 V supply directly to pin 2 of J12. Ground can be connected to one of the GND pins on the board.

2.2 Address Setting

The PHY address can be set by placing jumpers in J24 and J26 as indicated in Table 1. Placing 2.2k ohm resistors in R47, R49, and R50 will pull PHYAD2, PHYAD3, and PHYAD4 high allowing for PHY addresses greater than 3. The default address is 1 (no jumpers or resistors placed).

Table 1. PHY Address Settings

PHYAD1 (J26)	PHYAD0 (J24)	PHY Address
Open	Jumpered	0
Open	Open	1 (Default)
Jumpered	Jumpered	2
Jumpered	Open	3

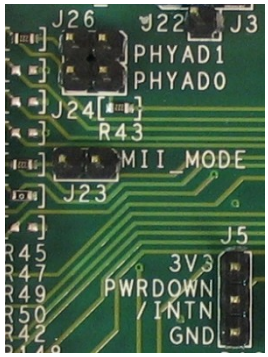


Figure 2. Default PHY Address Setting

2.3 Device Register Access

2.3.1 Access MDIO Through MII

To access the device registers through the MII interface jumpers should be placed between pins 1 and 2 of J3 and J4. Figure 3 shows the default jumper settings for the MDIO/MDC access via the MII interface.



Figure 3. Default MDIO/MDC Connection

2.3.2 Access MDIO Through USB

To access the device registers through the USB interface jumpers should be placed between pins 2 and 3 of J3 and J4.

2.3.3 Access MDIO Through Parallel Port

To access the device registers through the parallel port of the PC, the jumpers on J3 and J4 must be removed. Figure 4 shows the connection between the parallel port and the device signals: MDIO (J4, 2), MDC (J3, 2), and GND (J22, 1).

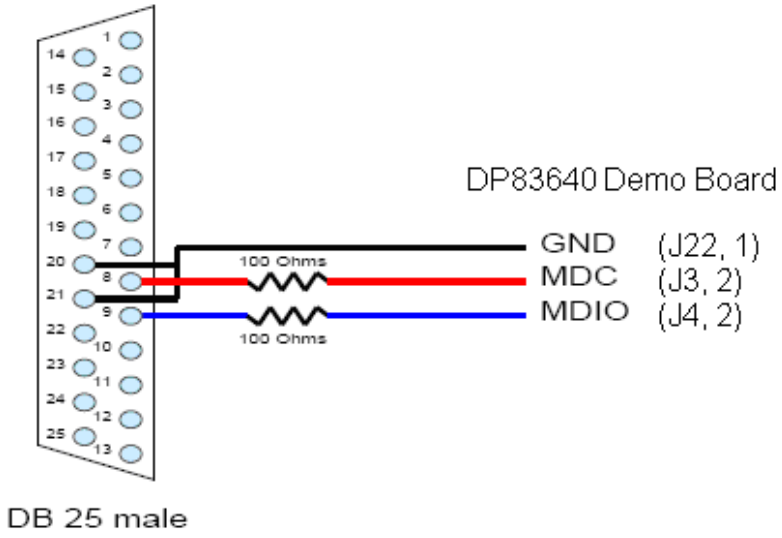


Figure 4. Direct Connect Cable with Line Resistors

2.4 Clock Sources

The board can be configured to operate with either a crystal or an external oscillator.

2.4.1 Crystal (Default)

The board comes with a 25 MHz crystal for use in the MII configuration. A surface mount device using the pads provided on the bottom side of the board can replace the through-hole part.

2.4.2 Oscillator

To use the board with a 25 MHz oscillator, remove the crystal (Y2) and resistors R22 and R25, populate the oscillator (X1) and R27 with a 0 ohm resistor. The board will accept oscillators in both full and half can package sizes.

For Reduced MII mode, two modes of operation are supported (RMII Master Mode and RMII Slave Mode). For RMII Master Mode, the DP83630 internally generates the 50 MHz RMII reference clock from the 25 MHz XTAL. For RMII Slave Mode operation, an external 50 MHz oscillator must provide the reference to the X1 input of the DP83630. Refer to the DP83630 datasheet for details on configuring the device for RMII Master and Slave Modes.

2.5 Straps

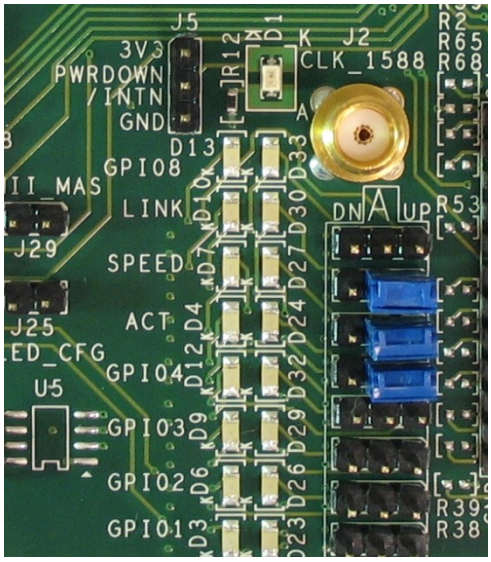
The DP83630 Demo Board provides a combination of jumpers and resistors to configure the strap options for the device. The following table summarizes the straps and the default settings.

Table 2. Strap Settings

Jumper	Signal Name	IC Pin Name	Function	Default Setting
J23	MII_MODE	RX_DV	MII Mode Select	Open
J29	RMII_MAS	TXD_3	RMII Master Enable	Open
J25	LED_CFG	CRS/CRS_DV	LED Configuration	Open
J32	CLK_OUT_EN	GPIO1	CLK_OUT Enable	Open
J35	PCF_EN	GPIO2	PHY Control Frame Enable	Open
J33	ACT	LED_ACT	Sets Mode in Auto Negotiation	High
J36	SPEED	LED_SPEED	Sets Mode in Auto Negotiation	High
J39	LINK	LED_LINK	Auto-Negotiation Enable	High
R46	FX_EN_Z	RX_ER	Fiber Mode Enable	Open
PHY Address				
J24	PHYAD0	COL	PHY Address Bit 0	Open
J26	PHYAD1	RXD_3	PHY Address Bit 1	Open
R47	PHYAD2	RXD_2	PHY Address Bit 2	Open
R49	PHYAD3	RXD_1	PHY Address Bit 3	Open
R50	PHYAD4	RXD_0	PHY Address Bit 4	Open

Refer to the DP83630 datasheet for specific details related to each strap option. The position of the default strap settings are indicated below for each version of the board.

Figure 5. Default Strap Locations



2.6 LEDs

Various LEDs are provided to assist the user in determining the state of operation of the board. Table 3 and Figure 6 clarify the relationship between the LEDs and Jumpers.

Table 3. List of LEDs with Jumpers

LED	Associated Jumper	Function
D1		Interrupt Indication
D2		MII Power Supply Indication
D13 / D33	J42	GPIO8
D10 / D30	J39	Link (GPIO7)
D7 / D27	J36	Speed (GPIO6)
D4 / D24	J33	Activity (GPIO5)
D12 / D32	J41	GPIO4
D9 / D29	J38	GPIO3
D6 / D26	J35	GPIO2
D3 / D23	J32	GPIO1

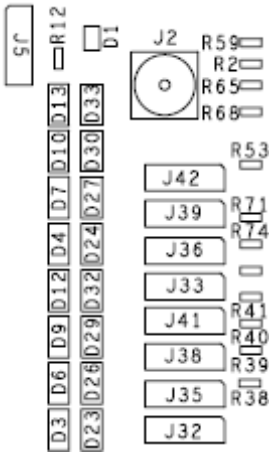


Figure 6. LED/Jumper Order

LEDs D3 through D33 can be used to indicate the state of GPIOs 1 through 8. When it is desired that the LED is “ON” when the GPIO is “LOW”, the associated jumper should be set to the “UP” state. With this setting a GREEN LED will be illuminated. When it is desired that the LED is “ON” when the GPIO is “HIGH”, the associated jumper should be set to the “DN” state. In this case, an AMBER LED has been incorporated in the circuit. **Care should be taken when selecting the LED polarity of the GPIO which also function as strap inputs.**

For additional information about the functionality of pins connected to the LEDs (with the exception of D2), refer to the DP83630 datasheet.

2.7 SMA Connectors

For convenience, two SMA connectors are provided (J2 and J34). J2 can be connected to the CLK_OUT pin by placing a 0 ohm resistor at R1. Similarly, J34 can be connected to GPIO9 by placing a 0 ohm resistor at R86. 50 ohm resistors can be placed at R2 and R62 to provide a terminating impedance for test equipment, if desired.

2.8 Table of Jumpers

Table 4. List of Jumpers

Jumper	Name	Function	Default Setting
Power			
J11/J12		Selects device 3.3 V source (Default MII_3V3)	
J55	MII 5V/3V3	Bypasses 3.3 V regulator for 3.3 V MII supply	Open
MDIO/MDC Access			
J3	MDC_SEL	Allows selection between USB, MII or parallel port MDC source	Jumper to PMDC_MII
J4	MDIO_SEL	Allows selection between USB, MII or parallel port MDIO source	Jumper to PMDIO_MII
J22	GND	Ground for parallel port source	Open
Address			
J24	PHYAD0	PHY address strap pin	Open
J26	PHYAD1	PHY address strap pin	Open
Auto-Negotiation			
J33	ACT	Force/Advertised operation mode in auto-negotiation	Pulled High
J36	SPEED	Force/Advertised operation mode in auto-negotiation	Pulled High
J39	LINK	Enable/Disable auto-negotiation	Pulled High
Reset			
J8	RESET_N	Allows reset of DP83630	Open
J40	/RESET	Allows reset of USB interface device	Open
Function			
J5	PWRDOWN/INTN	Allows for powerdown and interrupt modes	Open
J23	MII_MODE	Allows for MII_MODE strap option. Placing the jumper forces the unit into RMII mode.	Open
J25	LED_CFG	Allows for LED configuration strap option	Open
J29	RMII_MAS	Allows for RMII_MAS strap option. Placing the jumper forces the unit into RMII Master mode when MII_MODE (J23) is strapped.	Open
J32	GPIO1	Allows GPIO1 LED connection and CLK_OUT_EN strap option	Open
J35	GPIO2	Allows GPIO2 LED connection and PCF_EN strap option	Open
J38	GPIO3	Allows GPIO3 LED connection	Open
J41	GPIO4	Allows GPIO4 LED connection	Open
J42	GPIO8	Allows GPIO8 LED connection	Open
J64		ALP EEPROM write control (Internal Use)	Open

Interface			
J1	GPIO Header	Allows access to GPIO pins	
J2	CLK_1588	Allows access to CLK_OUT signal	
J6	JTAG	JTAG interface for DP83630	
J7	USB	USB Mini B connector	
J34	GPIO9	SMA Connector to GPIO9	
J46	Connector	RJ-45 connector	
J53	FX Transceiver	HP FX transceiver (AFBR5803Z) - Not stuffed in copper configuration	
J56	MII Header	Allow connection to MII pins	
J58	MII Male Connector	Smartbits Interface	
J60	ALP Connector	Internal Use – Not placed on Customer Demo Boards	

2.9 Modification for Fiber Operation

Provisions have been made to allow for the evaluation board to be configured for fiber mode operation. To modify the board for fiber operation, the components on Sheet 7 of the schematic should be placed, with R113, R114, R117, R118, and R128 all 0 ohm resistors. A 2.2k ohm resistor should also be placed in R46 to strap the device into fiber mode. Resistors R112, R115, R116, and R119 should be removed.

2.10 Register Access Software

Access to the device registers is available with the use of National's Analog LaunchPAD software. Refer to the DP83630 datasheet for detailed information on specific registers and to the National Semiconductor website (www.national.com) for the most recent version of the Analog LaunchPAD programming software.

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