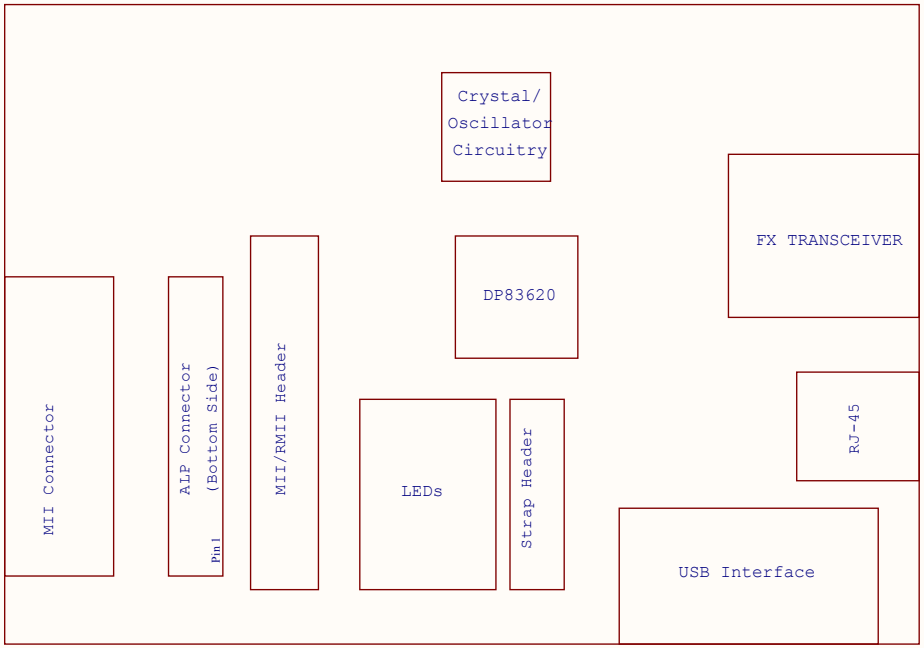


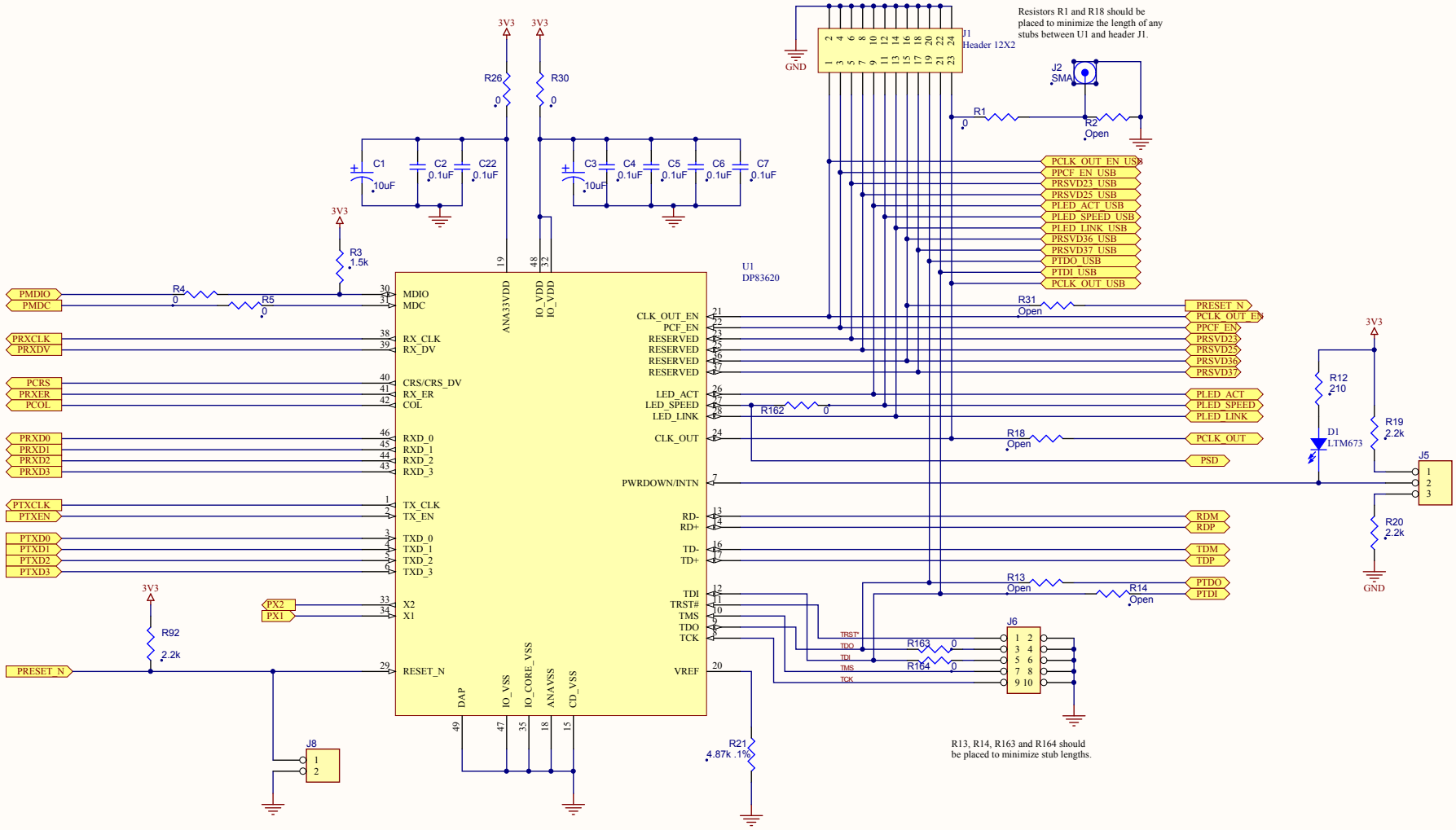
AN_EN	AN1	AN0	AUTO-NEG FORCED MODES	
0	0	0	10BASE-T	HALF-DUPLEX
0	0	1	10BASE-T	FULL-DUPLEX
0	1	0	100BASE-TX	HALF-DUPLEX
0	1	1	100BASE-TX	FULL-DUPLEX

AN_EN	AN1	AN0	AUTO-NEG ADVERTISED MODES	
1	0	0	10BASE-T	HALF/FULL-DUPLEX
1	0	1	100BASE-TX	HALF/FULL-DUPLEX
1	1	0	100BASE-TX	FULL-DUPLEX
1	1	1	10BASE-T 100BASE-TX	HALF/FULL-DUPLEX HALF/FULL-DUPLEX

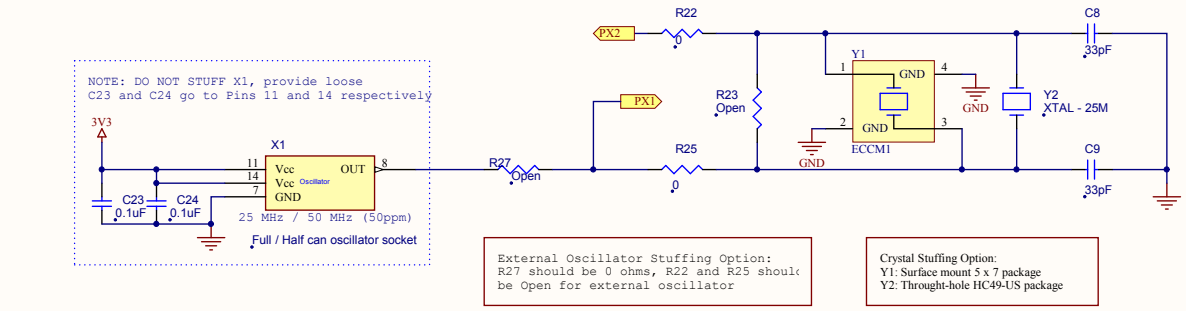
Title: DP83620 TP&FX Demo Board - Cover

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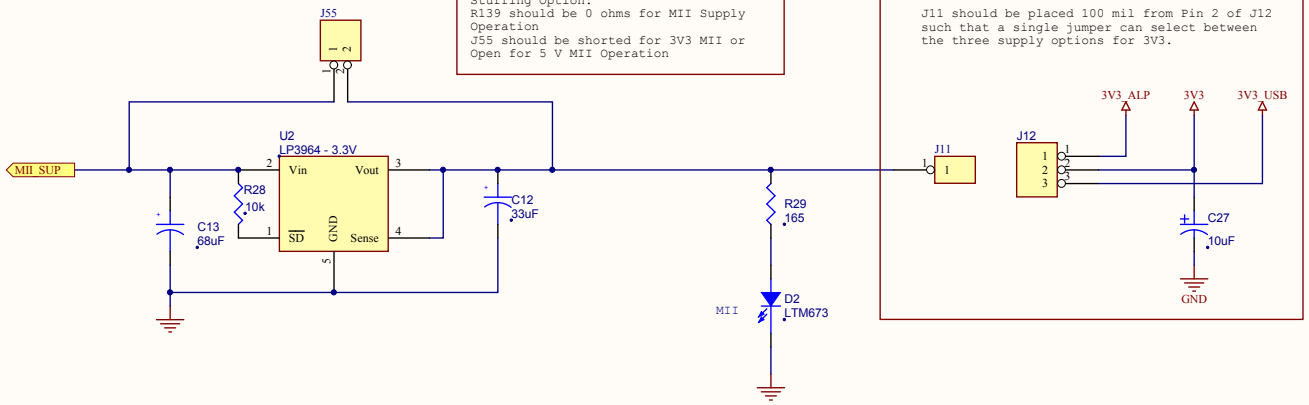


Title	DP83620 TP&FX Demo Board - Ethernet PHY Page
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External Oscillator Stuffing Option:
R27 should be 0 ohms, R22 and R25 should be Open for external oscillator

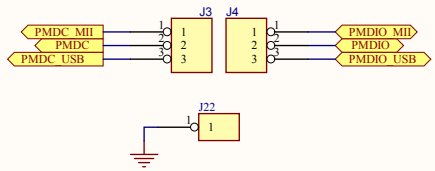
Crystal Stuffing Option:
Y1: Surface mount 5 x 7 package
Y2: Throught-hole HC49-US package



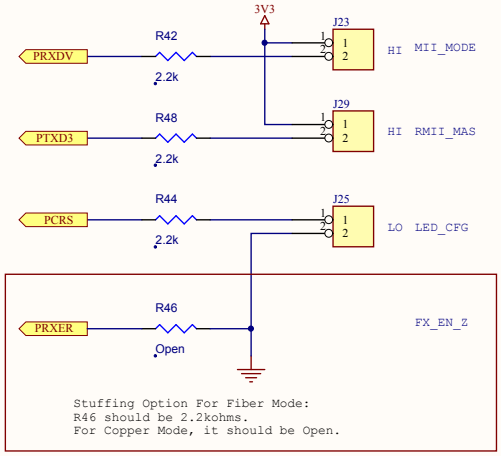
Stuffing Option:
R139 should be 0 ohms for MII Supply Operation
J55 should be shorted for 3V3 MII or Open for 5 V MII Operation

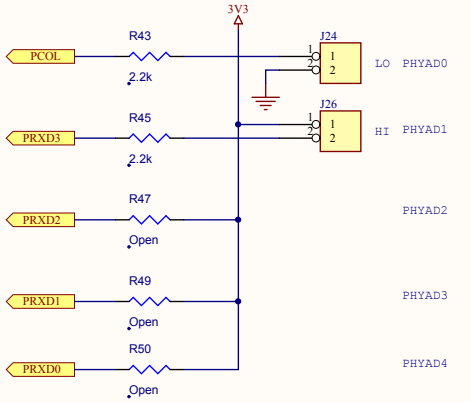
J11 should be placed 100 mil from Pin 2 of J12 such that a single jumper can select between the three supply options for 3V3.

J3 and J4 should be placed 100 mil apart. J22 should be placed 100 mil from Pin 2 of J3 such that a three wire MDIO/MDC interface can be used.



Title: DP83620 TP&FX Demo Board - Power, Clock, MDIO Page		
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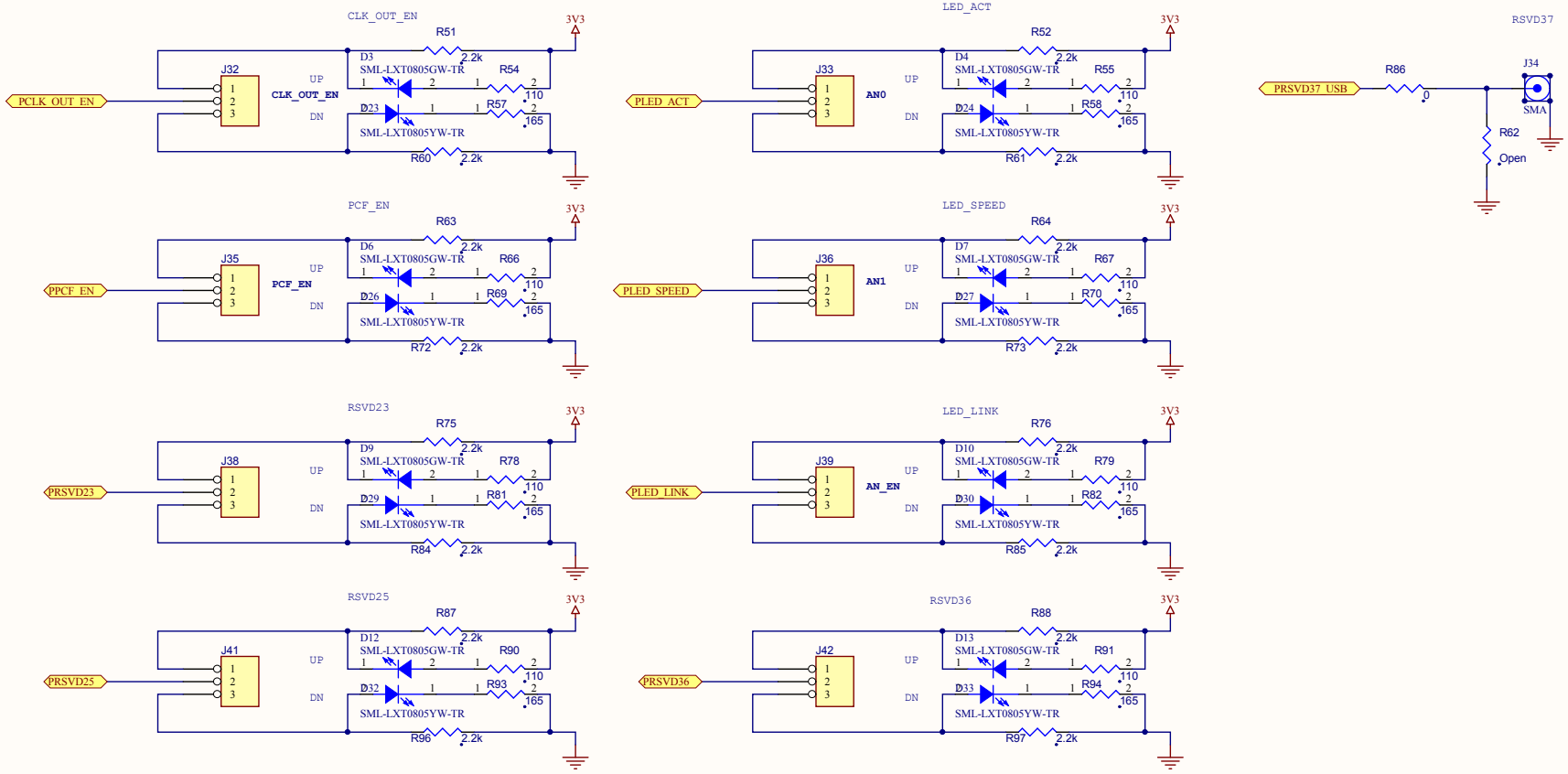


Phy Address Straps:

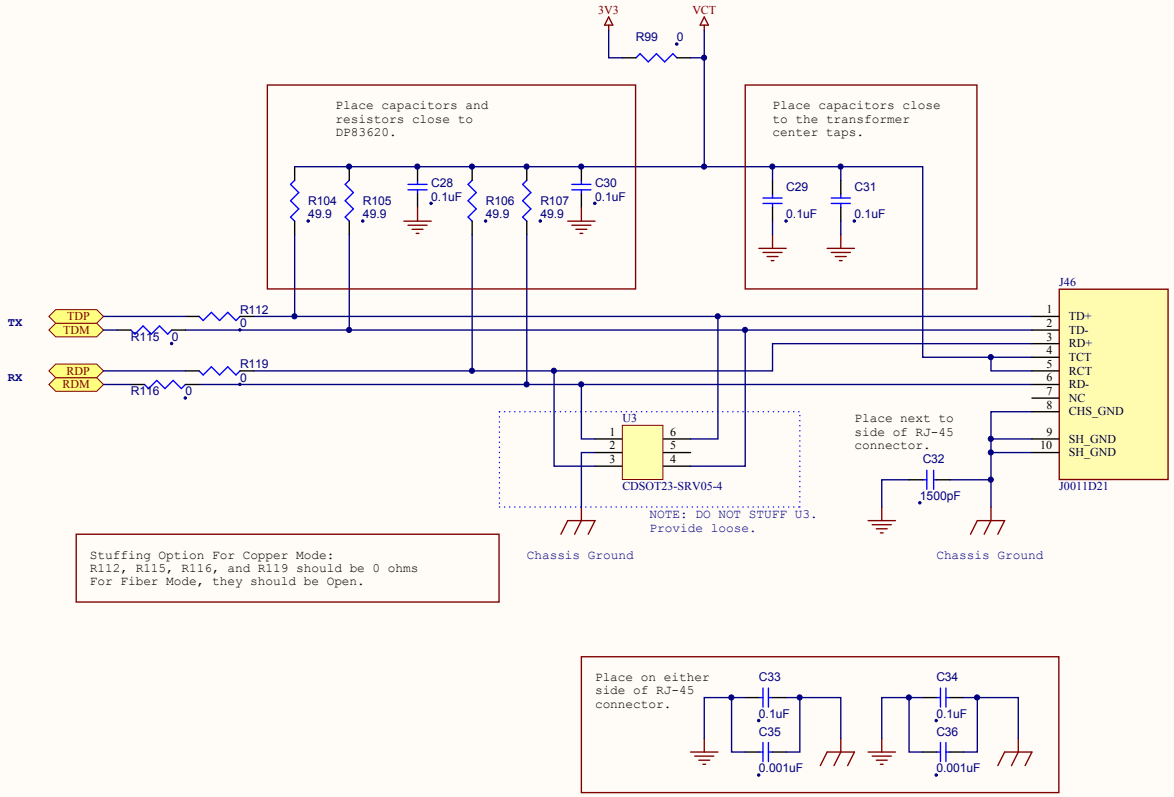
PHYAD1	PHYAD0	ADDRESS
0	0	0
0	1	1 (Default)
1	0	2
1	1	3

PHYAD2, PHYAD3 and PHYAD4 are internally strapped to 0.
R47, R49 and R50 can be stuffed with 2.2kohm to allow selection of Phy addresses above 3.

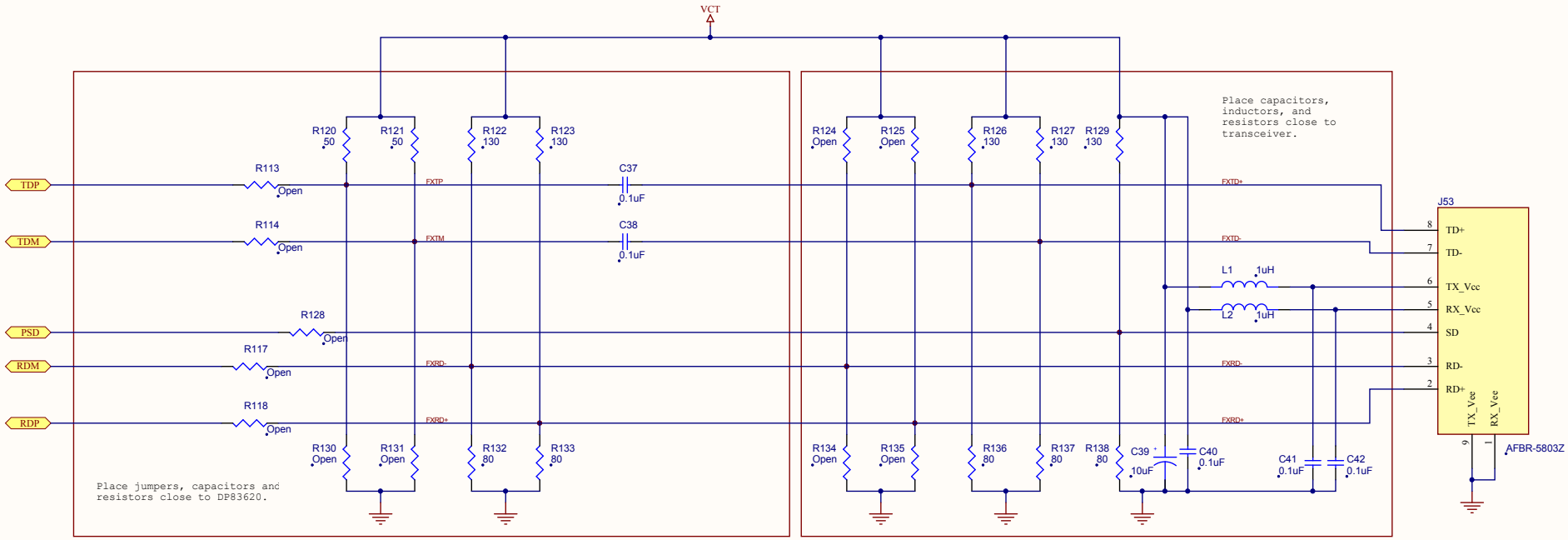
Title: DP83620 TP&FX Demo Board - Strap Options Page 1		
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Title	DP83620 TP&FX Demo Board - Strap Options Page 2	
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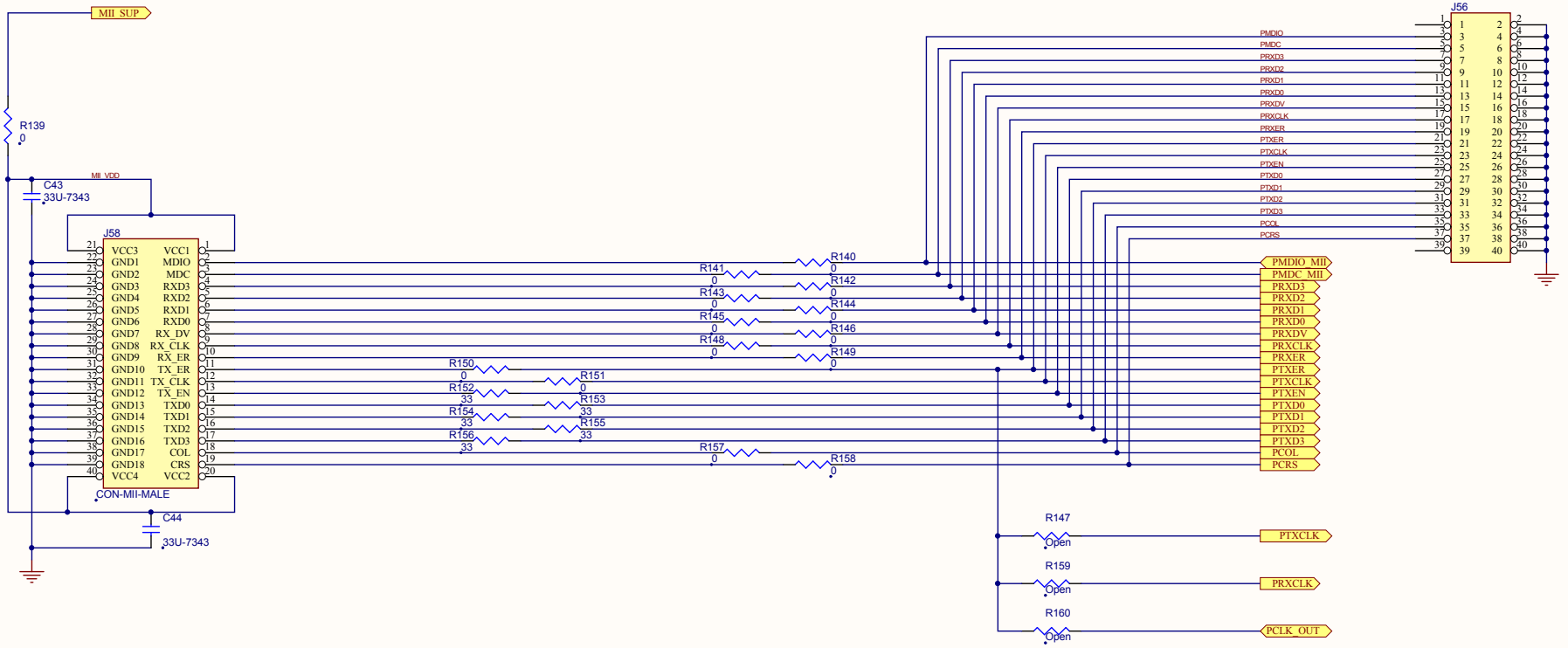
Title	DP83620 TP&FX Demo Board - TP Page		
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Important note:
- R112, R115, R116, R119 are to be routed on top.
- R113, R114, R117, R118 are to be routed on bottom.

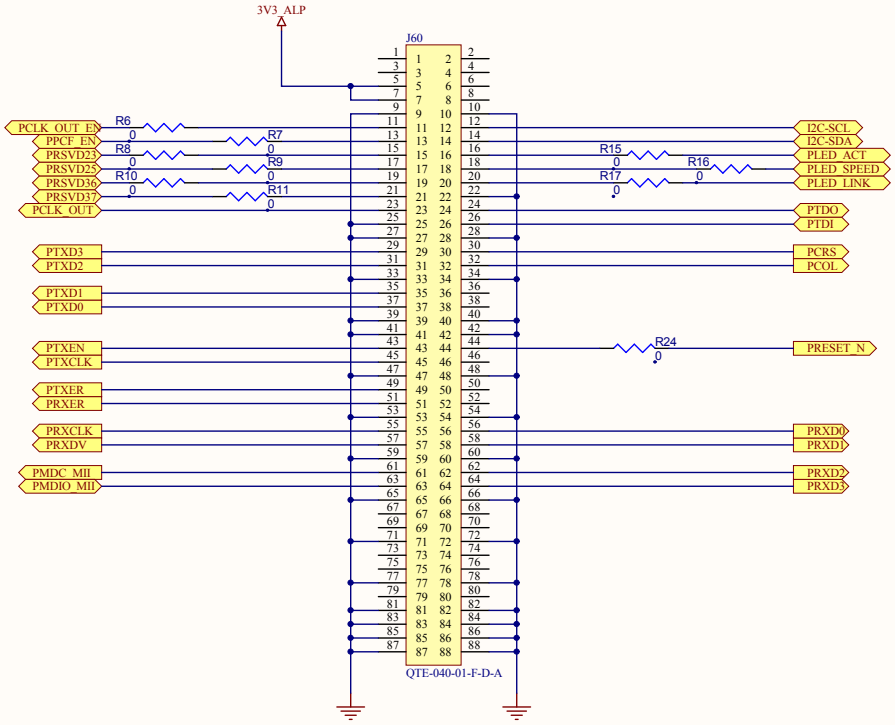
Stuffing option:
For Copper Stuff: R112, R115, R116, R119
For Fiber Stuff: R113, R114, R117, R118, R128

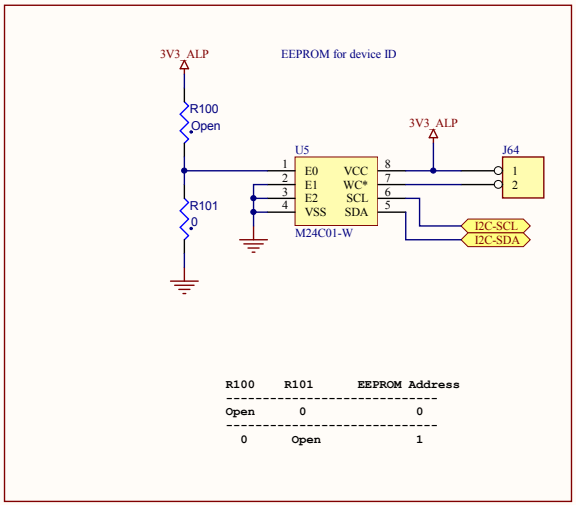
Title: DP83620 TP&FX Demo Board - FX Page		
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Resistor R147, R159 and R160 should be placed close to each other.

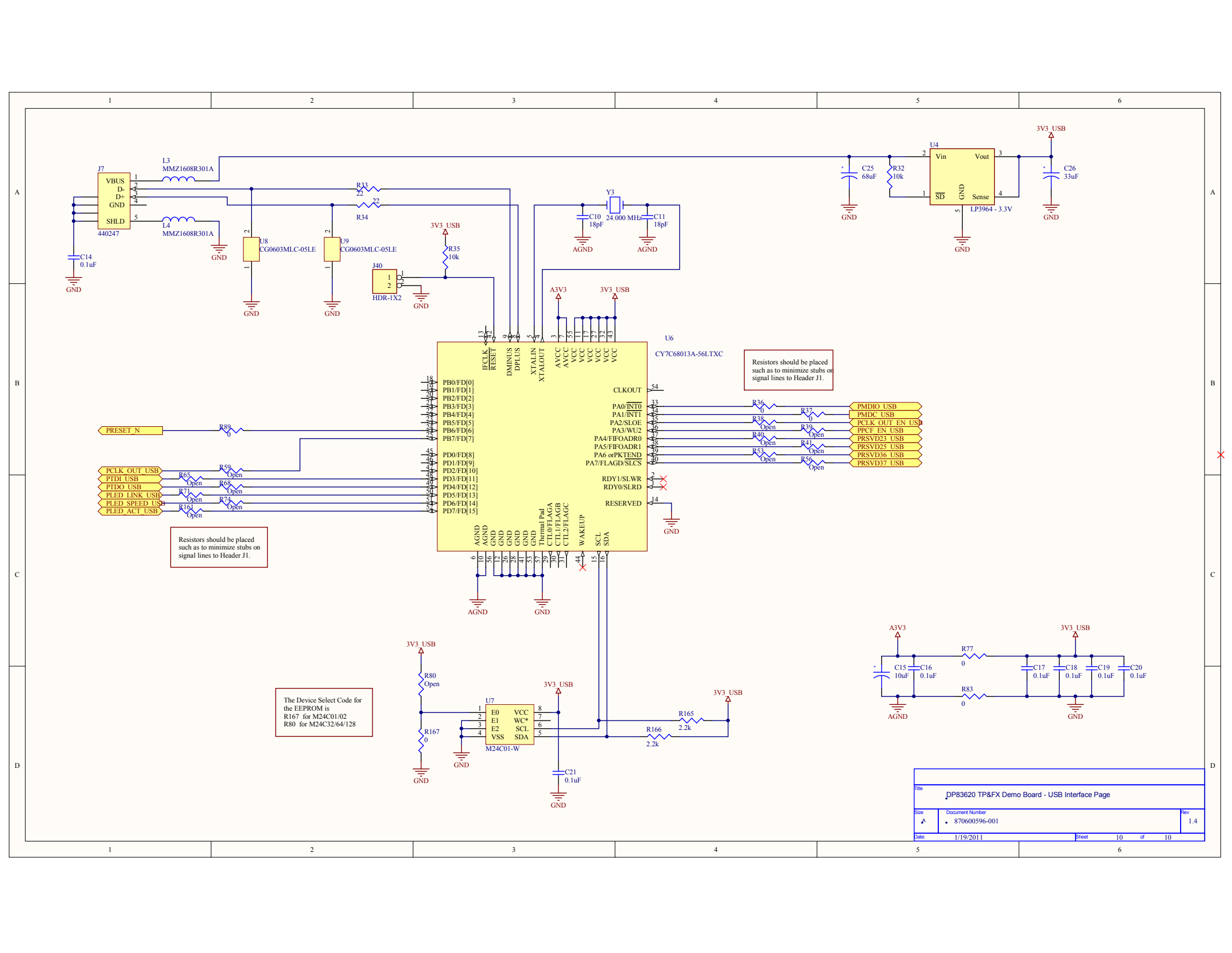
Title	DP83620 TP&FX Demo Board - MII Page	
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R100	R101	EEPROM Address
Open	0	0
0	Open	1

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J7
VBUS
D-
D+
GND
SHLD
440247
L3
MMZ1608R301A
L4
MMZ1608R301A
C14
0.1uF
R33
22
R34
22
U8
CG0603MLC-05LE
U9
CG0603MLC-05LE
J40
HDR-1X2
R35
10k
Y3
24.000 MHz
C10
18pF
C11
18pF
U4
Vin
Vout
SD
GND
Sense
LP3964 - 3.3V
C25
68uF
R32
10k
C26
33uF
3V3_USB
A3V3
AGND
GND
U6
CY7C68013A-56LTXC
IFCLK
RESET
DMINUS
DPLUS
XTALIN
XTALOUT
AVCC
VCC
CLKOUT
PB0/FD[0]
PB1/FD[1]
PB2/FD[2]
PB3/FD[3]
PB4/FD[4]
PB5/FD[5]
PB6/FD[6]
PB7/FD[7]
PA0/INT0
PA1/INT1
PA2/SLOE
PA3/WU2
PA4/FIFOADR0
PA5/FIFOADR1
PA6 orPKTEND
PA7/FLAGD/SLCS
PD0/FD[8]
PD1/FD[9]
PD2/FD[10]
PD3/FD[11]
PD4/FD[12]
PD5/FD[13]
PD6/FD[14]
PD7/FD[15]
RDY1/SLWR
RDY0/SLRD
RESERVED
Thermal Pad
CTL0/FLAGA
CTL1/FLAGB
CTL2/FLAGC
WAKEUP
SCL
SDA
PRESET_N
R89
0
PCLK_OUT_USB
PTDI_USB
PTDO_USB
PLED_LINK_USB
PLED_SPEED_USB
PLED_ACT_USB
R59
R65
R68
R71
R74
R161
Open
R36
R37
R38
R39
R40
R41
R53
R56
PMDIO_USB
PMDC_USB
PCLK_OUT_EN_USB
PPCF_EN_USB
PRSVD23_USB
PRSVD25_USB
PRSVD36_USB
PRSVD37_USB
Resistors should be placed such as to minimize stubs on signal lines to Header J1.
Resistors should be placed such as to minimize stubs on signal lines to Header J1.
R80
R167
R165
R166
2.2k
U7
E0
E1
E2
VSS
VCC
WC*
SCL
SDA
M24C01-W
C21
0.1uF
The Device Select Code for the EEPROM is
R167 for M24C01/02
R80 for M24C32/64/128
C15
10uF
C16
C17
C18
C19
C20
0.1uF
R77
R83
0
Title
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