DP141RLJ Evaluation Module

This document describes how to use the DP141RLJ EVM. Throughout this user's guide, the abbreviation EVM and the term *evaluation module* are synonymous with the DP141RLJEVM, unless otherwise noted.

Contents

1 What is the DP141RLJ DFP EVM? 1
2 DP141RLJ EVM Features 3
2.1 Power 3
2.2 Connectors 3
2.3 EQ/Gain Test Config Headers 4

List of Figures

1 DP141RLJ Block Diagram 2
2 DP141RLJ EVM 2
3 DP141RLJ EVM Between Notebook and DP Monitor 3
4 DP141RLJ Between Dock and DP Monitor 3

1 What is the DP141RLJ DFP EVM?

The DP141RLJ EVM is designed to evaluate the DP141RLJ device at a system level using a standard DisplayPort connection. The EVM provides standard DP connectors which can be utilized to connect to a DisplayPort source or sink systems to evaluate DP141RLJ settings. PCB design files can be provided, upon request, to aid PCB design with the DP141RLJ. The layout files can be used as a guideline to implement the DP141RLJ with illustrations of the routing and placement rules. Note that the EVM design may include test components for evaluation purposes but not applicable for production.

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Figure 1 illustrates the EVM block diagram.

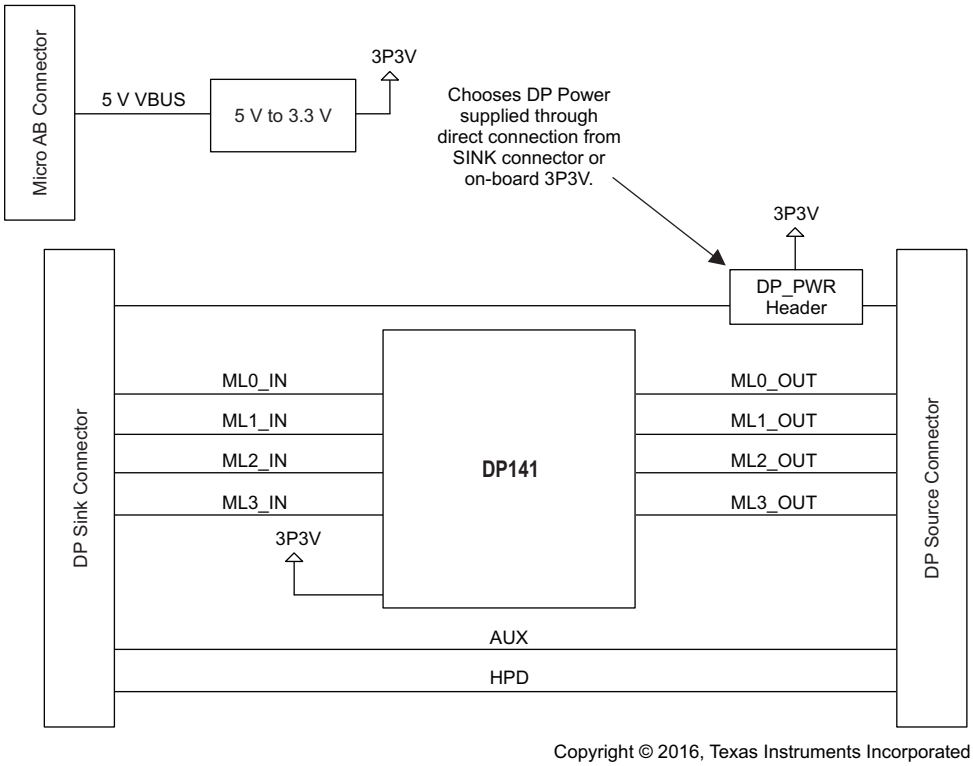


Figure 1. DP141RLJ Block Diagram

The EVM can be configured to operate either in GPIO or I²C mode. In GPIO mode, test headers are provided to configure the input pins for EQ gain and VOD settings. In I²C mode, the I²C can be accessed through a 2 × 5 test header pinned out to match the Total Phase™ Aardvark™ I²C programming module.

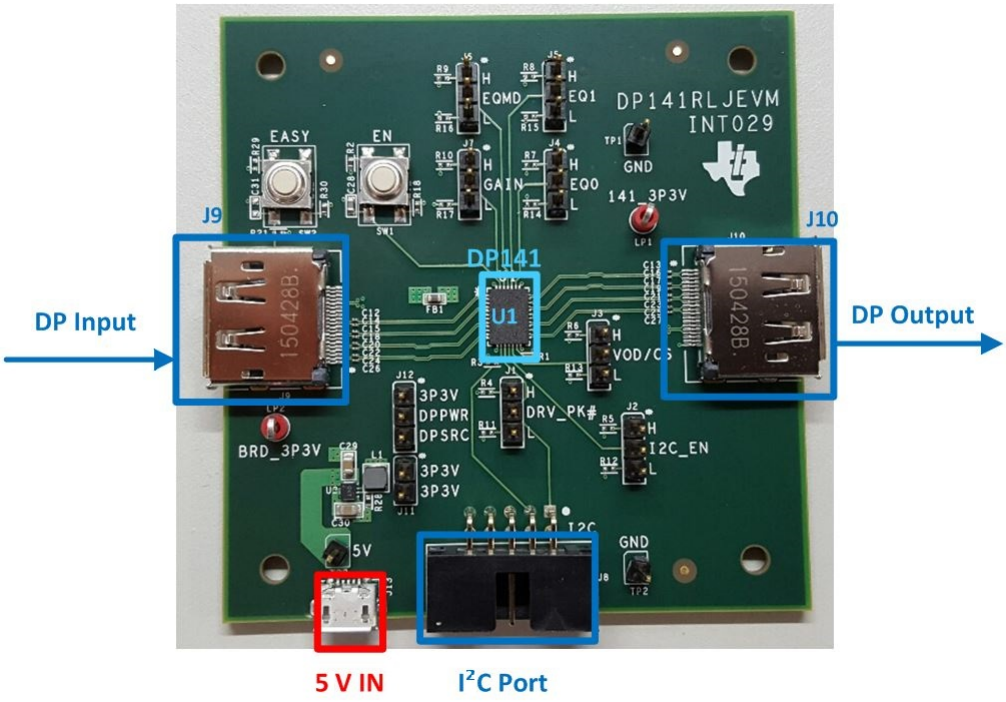


Figure 2. DP141RLJ EVM

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2 DP141RLJ EVM Features

2.1 Power

2.1.1 Board Power

The EVM operates from the 5 V VBUS from Micro AB USB connection (J13). If using a non-USB external power supply is desired, either 5 V or 3.3 V can be provided via test headers provided on board: 5 V via TP3, 3.3 V via J11. It is important that only one power source is used, do not connect multiple sources at the same time.

2.1.2 DP PWR

The DP power can be passed through from the DP input connected via J9 or tied directly to 3P3V on the board. See Table 1 for DP PWR configuration via J12.

Table 1. Board Power Configuration

Ref #	Name	Default Config	Description
J11	3P3V	Open	Provided in case power is to be provided externally
J12	DP_PWR	Pin 2-3	Configures source for DP_PWR. Default is to use the DP_PWR input from J9.

2.2 Connectors

The EVM has two standard DisplayPort connectors: J9 and J10. J9 is intended to be connected to a DP source, J10 to a DP sink. Example configurations are illustrated in Figure 3 and Figure 4.

Note that the connection between DP Source and DP Branch/Dock does not have to be through a DisplayPort cable but other cable connections such as USB Type-C™.

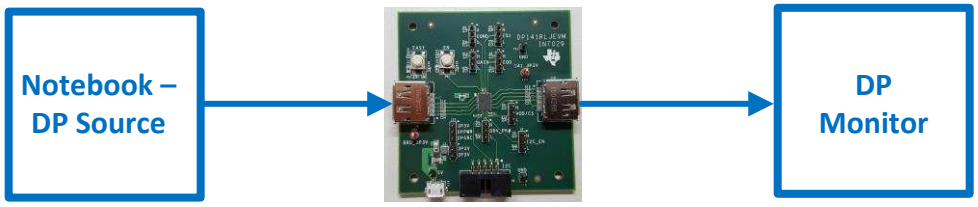


Figure 3. DP141RLJ EVM Between Notebook and DP Monitor

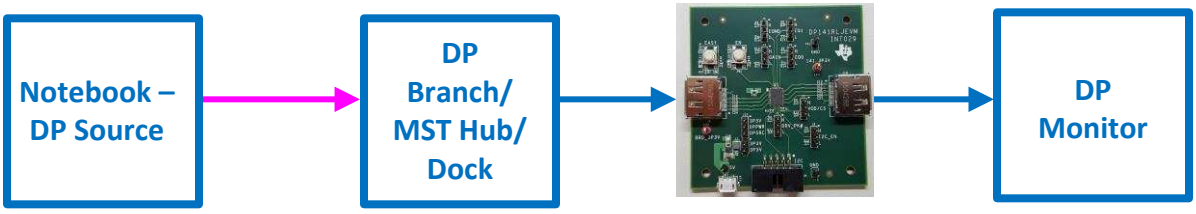


Figure 4. DP141RLJ Between Dock and DP Monitor

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2.3 EQ/Gain Test Config Headers

The DP141RLJ settings are configurable through the test configuration headers provided on the board. Table 2 summarizes the configuration setting. Refer to the SN65DP141 datasheet (SLLSES6) for the details on the device operation in different settings.

Table 2. EQ/Gain Configuration

Ref #	Signal Name	Default Config	Description
J1	DRV_PK#	Low - Enable DRV	Disable/Enable Driver peaking
J2	I2C_EN	Open - GPIO Mode	Configures device to operate in I^2C or GPIO mode
J3	VOD	High - High VOD	Configures VOD mode - High or Low
J4	EQ0	Configurable	See datasheet for details
J5	EQ1	Configurable	See datasheet for details
J6	EQ_MODE	Open - Cable mode	Configures device to operate in Cable or Trace mode
J7	GAIN	Low or Open- See data sheet	Work with EQ0 and EQ1 to set total EQ gain

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