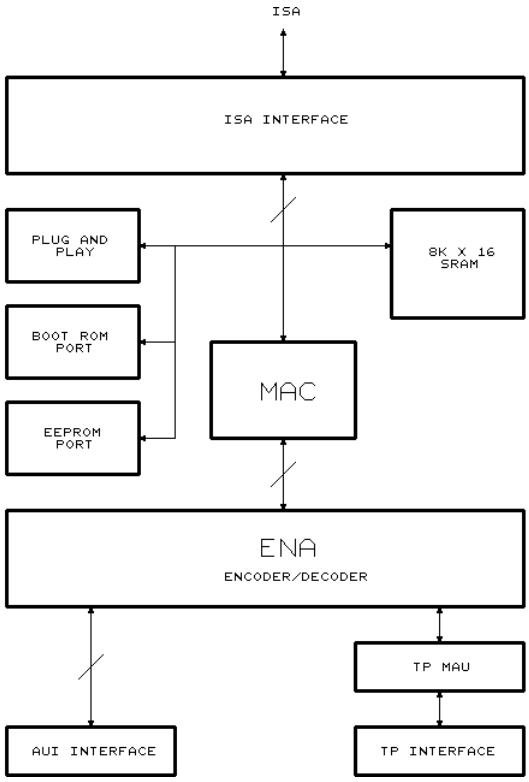
General Description

The DM9008 Ethernet controller is a highly integrated design that provides all Medial Access Control (MAC) and Encode-Decode (ENDEC) functions in accordance with the IEEE 802.3 standard. Network interfaces include 10BASE5 or 10BASE2 Ethernet via the AUI port and 10BASE-T via the Twisted-pair. The DM9008 Ethernet controller can interface directly to the PC-AT ISA bus without any external device. The interface to PC-AT ISA bus is fully compatible with NE2000 Ethernet adapter cards, so all software programs designed for NE2000 can run on the DM9008 card without any modification.
Microsoft's Plug and Play and the jumperless software configuration function are both supported. The capability of the PnP and Non-PnP mode auto-switch function allows users to configure network card. No jumpers or switches are needed to set when using either the PC or PnP function. The integrated 8Kx16 SRAM and 10BASE-T transceiver make DM9008 more cost-effective.

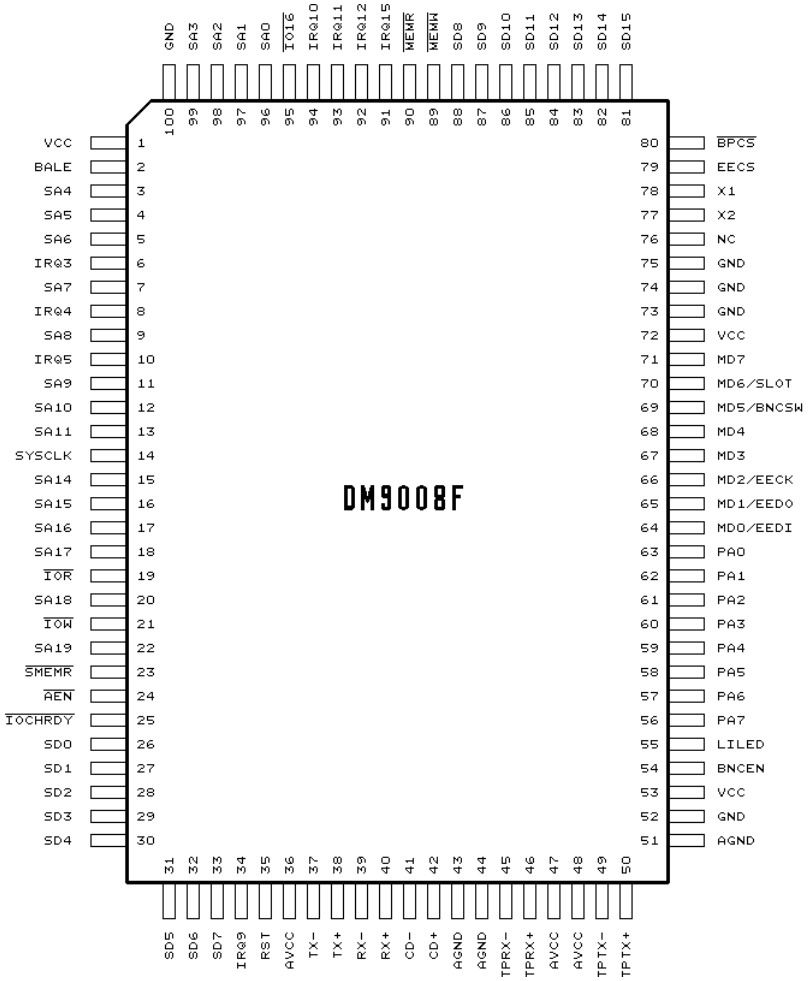
Block Diagram



Features

- Single chip solution for IEEE 802.3, 10BASE-T, 10BASE2 and 10BASE5
- Integrated ISA interface, 8Kx16 SRAM, Media Access Control, ENDEC and 10BASE-T transceiver
- Supports ISA Plug and Play configuration
- Software-compatible with NOVELL NE2000
- Supports PnP and Non-PnP Auto-switching
- PnP, Non-PnP and Auto-switch mode software selectable
- 8 interrupt lines selectable
- Auto-Polarity detection and correction
- Selectable 8 and 16-bit slot mode
- Provides auto-detection/auto-switching for 10BASE-T Transceiver and Attachment Unit Interface (AUI)
- External EEPROM programmable
- Supports BOOT-ROM page mode
- Loopback capability for diagnostics
- Receiver and collision squelch circuit to reduce noise
- Low-power CMOS process with single 5V power supply
- Built-in pre-distortion resisters for 10BASE-T application
- 100-pin QFP package

Pin Configuration



Absolute Maximum Ratings*

Supply Voltage (VCC) . . . . . -0.5V to +7.0V
DC Input Voltage (Vin) . . . . . -0.5V to VCC +0.5V
DC Output Voltage (Vout) . . . . . -0.5V to VCC +0.5V
Storage Temperature Range (Tstg) . . . -65°C to + 150°C
Power Dissipation (PD) . . . . . 500 mW
Lead Temp. (TL) (Soldering, 10 sec.) . . . . . 235°C
Case Temp. (Tc) . . . . . 0°C to 85°C
ESD rating (Rzap = 1.5k, Czap = 120 pF) 4000V
Differential Input Voltage . . . . . -5.5V to 16V
Differential Output Voltage . . . . . 0V to 16V

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (VCC = 5V ± 5%, Tc= 0°C to 85°C, unless otherwise specified)

Symbol	Parameter	Min.	Max.	Unit	Conditions
Voh	High Level Output Voltage (Notes 1, 2)	VCC - 0.1 3.5		V V	Ioh = -20μA Ioh = -2.0mA
Vol	Low Level Output Voltage (Notes 1, 2)		0.1 0.4	V V	Iol = 20μA Iol = 2.0mA
Vih	High Level Input Voltage (Note 6)	3.0		V	
Vil	Low Level Input Voltage (Note 6)		0.8	V	
Iin	Input Current	-1.0	+1.0	μA	Vi = VCC or GND
Ioz	Tri-state Output Leakage Current	-10	+10	μA	Vout = VCC or GND
Icco	Operating VCC + AVCC Supply Current (Note 3)		120	mA	X1 = 20 Mhz Iout = 0μA Vin = VCC or GND
Iccs	Standby VCC + AVCC Supply Current (Note 4)		110	mA	
Differential Pins (TX+/TX-, RX+/RX-, CD+/CD)					
V_{OD}	Differential Output Voltage (TX±)	+550	+1200	mV	78 ohm termination and 270 ohms from each to GND
V_{OB}	Differential Output Voltage Imbalance (TX±)		40	mV	78 ohm termination and 270 ohms from each to GND
V_U	Undershoot Voltage (TX±)		100	mV	78 ohm termination and 270 ohms from each to GND

DC Electrical Characteristics (continued)

Symbol	Parameter	Min.	Max.	Unit	Conditions
VDS	Differential Squelch Threshold (RX± and CD±)	-175 (Note 5)	-300	mV	
VCM	Differential Input Common Mode Voltage (RX± and CD±) (Note 5)	0	5.5	V	
Twisted Pair Interface Pins (TPTX+/TPTX-)					
Vtidf	TP input voltage	.350	2.0	V	-
 Vil Vih	LI: low high	 - 2.4	 0.8 -	 V V	 - -

Note 1: These levels are tested dynamically using a limited number of functional test patterns. Refer to AC Test Load.
Note 2: The low drive CMOS compatible Voh and Vol limits are not tested directly. Detailed device characterization verifies that this specification can be guaranteed by testing the high drive TTL compatibl e Vol and Voh specifications.
Note 3: This measurement is made while the DM9008 is undergoing transmission, reception, and collision. The value is not measured instantaneously, but is averaged over a span of several milliseconds.
Note 4: This measurement is made while the DM9008 is sitting idle of transmission. This measurement is described in note 1.
Note 5: This parameter is guaranteed by design and is not tested.
Note 6: Except RST, IORB, IOWB which are Schmitt trigger with Vil = 1.0V, Vih = 2.8V.

Pin Description

Pin No.	Symbol	I/O	Description
PC ISA BUS INTERFACE PINS			
96 - 99 3 - 5 7 9 11 - 13 15 - 18 20, 22	SA0 - SA3 SA4 - SA6 SA7 SA8 SA9 - SA11 SA14 - SA17 SA18, SA19	I	SYSTEM ADDRESS: These signals are connected to the address bus of the PC I/O slot. They are used to select the DM9008 I/O ports or the boot ROM address
26 - 33 88 - 81	SD0 - SD7 SD8 - SD15	I/O, Z	SYSTEM DATA: These signals are connected to the data bus of the PC I/O bus slot. They are used to transfer data between the PC and the DM9008
2	BALE	I	ADDRESS LATCH ENABLE: PC ISA bus BALE signal; used only to define the timing of IOCHRDY in Remote DMA This pin is not used if the value of biteA of CRB is 0, and tie to high to prevent floating.
14	SYSCLK	I	SYSTEM CLOCK: PC ISA bus system clock This pin is not used if the value of biteA of CRB is 0, and tie to high to prevent floating.
19	$\overline{\text{IOR}}$	I	I/O READ: An active low signal used to read data from the DM9008
21	$\overline{\text{IOW}}$	I	I/O WRITE: An active low signal used to write data to the DM9008
23	$\overline{\text{SMEMR}}$	I	MEMORY READ: An active low signal used to read boot ROM data
35	RST	I	RESET: An active high signal used to power-on reset the DM9008
24	$\overline{\text{AEN}}$	I	ADDRESS ENABLE: This is an active low signal used to enable the system address for the DM9008
25	$\overline{\text{IOCHRDY}}$	O I, Z	I/O CHANNEL READY: The DM9008 sets this signal low to insert wait states into the PC ISA bus
89	$\overline{\text{MEMW}}$	I	MEMORY WRITE: PC ISA bus memory write signal This pin is not used if the value of biteA of CRB is 0, and tie to high to prevent floating.
90	$\overline{\text{MEMR}}$	I	MEMORY READ: PC ISA bus memory read signal This pin is not used if the value of biteA of CRB is 0, and tie to high to prevent floating.
95	$\overline{\text{IO16}}$	O, Z	16-BIT I/O: This signal goes low when the data transfer between the DM9008 and the PC ISA bus is word wide

6 8 10 34 94 - 92 91	IRQ3 IRQ4 IRQ5 IRQ9 IRQ10-12 IRQ15	O, Z	INTERRUPT REQUESTS: These are 8 interrupt request pins. Only one pin, which is decoded from Configuration Register A, can be activated; the other pins are left floating. The activated pin will go high when an interrupt request is generated from the ENC module of the DM9008
MEMORY INTERFACE PINS			
79	EECS	O	EEPROM CHIP SELECT: This signal goes high when the EEPROM is selected by the DM9008
80	$\overline{\text{BPCS}}$	O	BOOT ROM CHIP SELECT: This signal goes low when the PC reads the boot ROM data
64 - 71 (64) (65) (66) (66) (69) (70)	MD0 - MD7 (EEDI) (EEDO) (EECK) (LEDSW) (BNCSW) (SLOT)	I/O, Z	MEMORY DATA BUS: These are the memory data signals for the boot ROM When the EEPROM is loaded or written, MD0, 1, 2 are used as the EEPROM signals * EEPROM DATA IN: This pin is used as the serial input data signal from the EEPROM * EEPROM DATA OUT: This pin is used as the serial output data signal to the EEPROM * EEPROM CLOCK: This pin is used as the EEPROM clock signal These memory data pins can also be used as switches when the DM9008 is in reset state. There is an approximately 100K pull-low resistor on each pin, and a 10K pull-high resistor can be connected to a pin when it is switched to logic high LED mode switch: see page 67 for details. * When this pin pulled high upon reset, pin 54 outputs 312.5KHz * SLOT SELECTION: When this pin is pulled to high, the DM9008 is in NE2000 16-bit mode
63 - 56	PA0 - PA7	O	BOOT ROM PAGE ADDRESS. When the boot ROM is accessed, PA0-PA7 are used as the page address of the boot ROM
NETWORK INTERFACE PINS			
37 38	TX- TX+	O	TRANSMIT OUTPUT: Differential line driver which sends the encoded data to the transceiver. The outputs are source followers which require 270 ohm pull-down resistors
54	BNCEN	O	BNC OUTPUT ENABLE: This pin goes high if the value of the Configuration Register B bit 1 is low and bit 0 is high. Typically, this pin is used to control the DC-DC converter to enable or disable the UM9092A (Coaxial Transceiver Interface) * Output 312.5KHz clock: when the 69 pin (BNCSW) is pulled high, this pin output 312.5KHz clock
78	X1	O	CRYSTAL FEEDBACK OUTPUT: Used in crystal connection only. Connect to ground when using an external clock
77	X2	I	CRYSTAL or EXTERNAL CLOCK INPUT

Pin Description (continued)

Pin No.	Symbol	I/O	Description
NETWORK INTERFACE PINS			
39 40	RX- RX+	I	RECEIVE INPUT: Differential receive input pair from the transceiver
41 42	CD- CD+	I	COLLISION INPUT: Differential collision input pair from the transceiver
50 49	TPTX+ TPTX-	O	TP Driver Outputs. These two outputs provide the TP drivers with pre-distortion capability
46 45	TPRX+ TPRX-	I	TP Receive Input. A differential receiver tie to the receive transformer pair of the twisted-pair wire. The receive pair of the twisted-pair medium is driven with 10 Mbits/s Manchester-encoded data
5	LILED	OPEN DRAIN	LINK and Traffic LED Driver: If TP is LINK-pass, this pin outputs low. This pin will go low for 80ms and then into high impedance state for 50ms to indicate the presence of traffic on the network
76	NC		No connection
POWER SUPPLY PINS			
36, 47, 48	AVCC		+5V DC power supply for analog CKT. A decoupling capacitor should be connected between these pins and GND for analog CKT
43, 44, 51	AGND		GND for analog CKT
1, 53, 72	VCC		+5V DC power supply for digital CKT. A decoupling capacitor should be connected between these pins and GND for digital CKT
52, 73, 74, 75, 100	GND		GND for digital CKT

ENC Register Address Assignments

Page 0 (PS1 = 0, PS0 = 0)

SA0-SA3	RD	WR
00H	Command (CR)	Command (CR)
01H	Current Local DMA Address 0 (CLDA0)	Page Start Register (PSTART)
02H	Current Local DMA Address 1 (CLDA1)	Page Stop Register (PSTOP)
03H	Boundary Pointer (BNRY)	Boundary Pointer(BNRY)
04H	Transmit Status Register (TSR)	Transmit Page Start Address (TPSR)
05H	Number of Collisions Register (NCR)	Transmit Byte Count Register 0 (TBCR0)
06H	FIFO	Transmit Byte Count Register 1 (TBCR1)
07H	Interrupt Status Register (ISR)	Interrupt Status Register (ISR)
08H	Current Remote DMA Address 0 (CRDA0)	Remote Start Address Register 0 (RSAR0)
09H	Current Remote DMA Address 1 (CRDA1)	Remote Start Address Register 1 (RSAR1)
0AH	Configuration Register A	Remote Byte Count Register 0 (RBCR0)
0BH	Configuration Register B	Remote Byte Count Register 1 (RBCR1)
0CH	Receive Status Register (RSR)	Receive Configura-tion Register (RCR)
0DH	Tally Counter 0 (Frame AlignmentÞ Errors) (CNTR0)	Transmit Configuration Register (TCR)
0EH	Tally Counter 1 (CRC Errors) (CNTR1)	Data Configuration Register (DCR)
0FH	Tally Counter 2 (Missed Packet Errors) (CNTR2)	Interrupt Mask Register (IMR)

Page 1 (PS1 = 0, PS0 = 1)

SA0-SA3	RD	WR
00H	Command (CR)	Command (CR)
01H	Physical Address Register 0 (PAR0)	Physical Address Register 0 (PAR0)
02H	Physical Address Register 1 (PAR1)	Physical Address Register 1 (PAR1)
03H	Physical Address Register 2 (PAR2)	Physical Address Register 2 (PAR2)
04H	Physical Address Register 3 (PAR3)	Physical Address Register 3 (PAR3)
05H	Physical Address Register 4 (PAR4)	Physical Address Register 4 (PAR4)
06H	Physical Address Register 5 (PAR5)	Physical Address Register 5 (PAR5)
07H	Current Page Register (CURR)	Current Page Register (CURR)
08H	Multicast Address Register 0 (MAR0)	Register 0 (MAR0)Multicast Address
09H	Multicast Address Register 1 (MAR1)	Multicast Address Register 1 (MAR1)
0AH	Multicast Address Register 2 (MAR2)	Multicast Address Register 2 (MAR2)
0BH	Multicast Address Register 3 (MAR3)	Multicast Address Register 3 (MAR3)
0CH	Multicast Address Register 4 (MAR4)	Multicast Address Register 4 (MAR4)
0DH	Multicast Address Register 5 (MAR5)	Multicast Address Register 5 (MAR5)
0EH	Multicast Address Register 6 (MAR6)	Multicast Address Register 6 (MAR6)
0FH	Multicast Address Register 7 (MAR7)	Multicast Address Register 7 (MAR7)

Register Address Assignments (continued)

Page 2 (PS1 = 1, PS0 = 0)

SA0-SA3	RD	WR
00H	Command (CR)	Command (CR)
01H [3]	Page Start Register (PSTART)	Current Local DMA Address 0 (CLDA0)
02H	Page Stop Register (PSTOP)	Current Local DMA Address 1 (CLDA1)
03H	Remote Next Packet Pointer	Remote Next Packet Pointer
04H	Transmit Page Start Address	----
05H	Local Next Packet	Local Next Packet
06H	Address Counter (Upper)	Address Counter (Upper)
07H	Address Counter (Lower)	Address Counter (Lower)
08H	----	----
09H	Interrupt Lines Status Register	Interrupt Lines Pull-Down Register
0AH	Boot ROM Page Register	Boot ROM Page Register
0BH	Configuration Register C	Configuration Register C
0CH	Receive Configuration Register (RCR)	----
0DH	Transmit Configuration Register (TCR)	----
0EH	Data Configuration Register (DCR)	----
0FH	Interrupt Mask Register (IMR)	----

Page3 (PS1=1, PS0=1)

SA0-SA3	RD	WR
00H	Command (CR)	Command (CR)
01H-06H	----	----
07H	Configuration Register D	Configuration Register D
08H-0FH	----	----

Register Descriptions

Configuration Register A (CRA)

Configuration Register A can be read at address 0AH in Page 0 of ENC, and can be written by following a read to address 0AH with a write to address 0AH. If address 0AH is written without a previous read to 0AH, the write will be regarded as a write to register RBCR0 of ENC.

7	6	5	4	3	2	1	0
FREAD	INT2	INT1	INT0	IOAD3	IOAD2	IOAD1	IOAD0

Bit	Symbol	Description
0 - 3	IOAD0 IOAD1 IOAD2 IOAD3	I/O Address: These three bits determine the base I/O address of DM9008 within the PC system's I/O map bit3 bit2 bit1 bit0 I/O base 0 0 0 0 300H 0 0 0 1 320H 0 0 1 0 340H 0 0 1 1 360H 0 1 0 0 380H 0 1 0 1 3A0H 0 1 1 0 3C0H 0 1 1 1 3E0H bit3 bit2 bit1 bit0 I/O base 1 0 0 0 200H 1 0 0 1 220H 1 0 1 0 240H 1 0 1 1 260H 1 1 0 0 280H 1 1 0 1 2A0H 1 1 1 0 2C0H 1 1 1 1 2E0H
4 - 6	INT0 INT1 INT2	Interrupt Pin Mapping: Only one interrupt output pin will be driven active when a valid interrupt condition occurs bit5 bit4 bit3 Interrupt 0 0 0 IRQ3 0 0 1 IRQ4 0 1 0 IRQ5 0 1 1 IRQ9 1 0 0 IRQ10 1 0 1 IRQ11 1 1 0 IRQ12 1 1 1 IRQ15
7	FREAD	Fast Read: In the remote DMA read mode. When this bit is set high, the DM9008 will begin the next port fetch before the current $\overline{IOR}$ is completed

Configuration Register B (CRB)

Configuration Register B can be read at address 0BH in Page 0 of ENC, and can be written by following a read to address 0BH with a write to address 0BH. If a write to address 0BH is performed without a previous read to 0BH, it will be regarded as a write to register RBCR1 of ENC.

7	6	5	4	3	2	1	0
--	--	BUSERR	CHRDY	--	GDLINK	PHYS1	PHYS0

Bit	Symbol	Description
0, 1	PHYS0 PHYS1	Physical Media Interfaces: These two bits determine which type of physical interface the DM9008 is using, as shown below: bit1 bit0 Interface 0 0 Set to 10BASE-T; BNCEN = low 0 1 Set to 10BASE2; BNCEN = high 1 0 Set to 10BASE5; BNCEN = low 1 1 Auto-detection media
2	GDLINK	Read: Link status. One indicates Link OK; zero indicates Link Fail
3	--	Reserved
4	CHRDY	IOCHRDY from $\overline{IOR}$ or $\overline{IOW}$ or from BALE: When low, DM9008 will pull IOCHRDY low after the command strobe. If high, IOCHRDY will be pulled low after BALE goes high
5	BUSERR	Bus Error: This bit shows that DM9008 has detected an ISA bus error. This bit will be high if DM9008 inserts wait states into a system access and the system terminates the cycle without inserting wait states
6	--	Reserved
7	--	Reserved

Configuration Register C (CONFIG.C)

This register is configured during RESET and EEPROM read states.
CONFIG.C can be read from address 0BH of page 2 of ENC.

7	6	5	4	3	2	1	0
--	PnP	--	--	BPS3	BPS2	BPS1	BPS0

Bit	Symbol	Description
0 - 3	BPS0 BPS1 BPS2 BPS3	BOOT PROM Select: Selects address at which boot ROM begins and size of boot ROM bit3 bit2 bit1 bit0 Address Size 0 0 0 X X No boot ROM 0 0 1 0 C0000H 16K 0 0 1 1 C4000H 16K 0 1 0 0 C8000H 16K 0 1 0 1 CC000H 16K 0 1 1 0 D0000H 16K 0 1 1 1 D4000H 16K 1 0 0 0 D8000H 16K 1 0 0 1 DC000H 16K 1 0 1 0 C0000H 32K 1 0 1 1 C8000H 32K 1 1 0 0 D0000H 32K 1 1 0 1 D8000H 32K 1 1 1 0 C0000H 64K 1 1 1 1 D0000H 64K These four bits can be updated by writing new values to this register
4 - 5	--	Reserved
6	PnP	DM9008 is in PnP state when this bit is set
7	--	Reserved

Configuration Register D (CONFIG. D)

This register can be read or written at register 07H of ENC Page 3. All bits of this register are power-on low.

7	6	5	4	3	2	1	0
EEMODE	--	--	CLK-REF	EECS	EECK	EEDO	EEDI

Bit	Symbol	Description
0	EEDI	EEPROM DATA IN: This bit reflects the state of the DM9008 MD0 pin
1	EEDO	EEPROM DATA OUT: When EEMODE is high, this bit reflects the state of the DM9008 MD1 pin
2	EECK	EEPROM CLOCK: When EEMODE is high, this bit reflects the state of the DM9008 MD2 pin
3	EECS	EEPROM CHIP SELECT: When EEMODE is high, this bit reflects the state of the DM9008 EECS pin
4	CLK-REF	When EEMODE is high, this bit is toggled every 12μs
5, 6	--	Reserved. Must be set to zero
7	EEMODE	EEPROM MODE: If this bit is set high, the EEPROM can be programmed with the values of EECS, EECK and EEDO in this register

Interrupt Line Status Register

The logic value of DM9008's eight interrupt pins can be read in register 09H of ENC, page 2.

7	6	5	4	3	2	1	0
IRQ15	IRQ12	IRQ11	IRQ10	IRQ9	IRQ5	IRQ4	IRQ3

Bit	Symbol	Description
0 - 7	IRQ3-15	INTERRUPT LINE STATUS: The logic values of interrupt pins IRQ3-15

Interrupt Line Pull-Down Register

When any one of the eight bits in register 09H of ENC page 2 is set to one, the corresponding interrupt line will be pulled down to GND with a resistor whose value is approximately 1K. All bits of this register are power-on low.

7	6	5	4	3	2	1	0
IRQPD15	IRQPD12	IRQPD11	IRQPD10	IRQPD9	IRQPD5	IRQPD4	IRQPD3

Bit	Symbol	Description
0 - 7	IRQPD3-15	INTERRUPT LINE PULL-DOWN: When one, enables the interrupt line to be pulled down with 1K resistor

Boot ROM Page Register

The boot ROM page register can be read or written in register 0AH of ENC page 2.
All bits of this register are power-on low.

7	6	5	4	3	2	1	0
XMA8	XMA7	XMA6	XMA5	XMA4	XMA3	XMA2	XMA1

Bit	Symbol	Description
0 - 7	XMA1-8	BOOT ROM PAGE ADDRESS: When boot ROM is read by host, the value of this register will be indicated by MEMORY ADDRESS PA0-7

Command Register (CR)

The Command Register is used to initiate transmissions, enable or disable Remote DMA operations, and select register pages. To issue a command, the microprocessor sets the corresponding bit(s) (RD2, RD1, RD0, TXP). Further commands may be overlapped, but with the following rules: (1) If a transmit command overlaps a remote DMA operation, bits RD0, RD1, and RD2 must be maintained for the remote DMA command when the TXP bit is set. Note that if a remote DMA command is re-issued when the transmit command is given, the DMA will be completed immediately if the remote byte count register has not been reinitialized. (2) If a remote DMA operation overlaps a transmission, RD0, RD1, and RD2 may be written with the desired values and a "0" may be written to the TXP bit. Writing a "0" to this bit has no effect. (3) A remote write DMA may not overlap a remote read operation or vice versa. Either of these operations must either be completed or be aborted before the other operation may start. Bits PS1, PS0, RD2 and STP may be set at any time.

7	6	5	4	3	2	1	0
PS1	PS0	RD2	RD1	RD0	TXP	STA	STP

Bit	Symbol	Description
D0	STP	STOP: Software reset command. Takes the controller off-line, and no packets will be received or transmitted. Any reception or transmission in progress will continue to completion before the reset state is entered. To exit this state, the STP bit must be reset. The software reset is executed only when indicated by the RST bit in the ISR being set to a "1." STP powers up high
D1	STA	Start mode
D2	TXP	Transmit Packet: This bit must be set to initiate transmission of a packet. TXP is internally reset after the transmission is either completed or aborted. This bit should be set only after the Transmit Byte Count and Transmit Page Start registers have been programmed. TXP powers up low
D3 D4 D5	RD0 RD1 RD2	Remote DMA Command: These three encoded bits control operation of the Remote DMA channel. RD2 can be set to abort any Remote DMA command in progress. The Remote Byte Count Registers should be cleared when a Remote DMA has been aborted. The Remote Start Addresses are not restored to the starting address if the Remote DMA is aborted. RD2 powers up high RD2 RD1 RD0 0 0 0 Not Allowed 0 0 1 Remote Read 0 1 0 Remote Write 0 1 1 Send Packet 1 X X Abort/Complete Remote DMA
D6 D7	PS0 PS1	Page Select: These two encoded bits select which register page is to be accessed with addresses SA0-3 PS1 PS0 0 0 Register Page 0 0 1 Register Page 1 1 0 Register Page 2 1 1 Register Page 3

Data Configure Register (DCR)

This register is used to program the DM9008 for the 8 or 16-bit memory interface, select byte ordering in 16-bit applications, and establish FIFO thresholds. The DCR must be initialized prior to loading the Remote Byte Count Registers. LAS is set on power up.

7	6	5	4	3	2	1	0
--	FT1	FT0	ARM	LS	LAS	BOS	WTS

Bit	Symbol	Description
D0	WTS	Word Transfer Select 0: Selects 8-bit DMA transfers 1: Selects 16-bit DMA transfers
D1	BOS	Byte Order Select 0: MS byte placed on SD15-SD8 and LS byte on SD7-SD0 (32000, 8086) 1: MS byte placed on SD7-SD0 and LS byte on SD15-SD8 (68000) Ignored when byte-wide DMA operation is chosen Note: Byte Order Select mode is not supported in the current version of the DM9008, so this bit should be cleared in the application
D2	LAS	Long Address Select 0: Dual 16-bit DMA mode 1: Single 32-bit DMA mode Note: Single 32-bit DMA mode is not supported in the current version of the DM9008, so this bit should be cleared in the application
D3	LS	Loopback Select 0: Loopback mode selected. Bits D1, D2 of the TCR must also be programmed for Loopback mode selected 1: Normal Operation
D4	ARM	Auto-initialize Remote 0: Send Command not executed, all packets removed from Buffer Ring under program control 1: Send Command executed, Remote DMA auto-initialized to remove packets from Buffer Ring
D5 D6	FT0 FT1	FIFO Threshold Select: Encoded FIFO threshold. During reception, the FIFO threshold indicates the number of bytes (or words) filled into the FIFO serially from the network before received data are written to the buffer RAM Receive Thresholds FT1 FT0 Word Wide Byte Wide 0 0 1 Word 2 Bytes 0 1 2 Words 4 Bytes 1 0 4 Words 8 Bytes 1 1 6 Words 12 Bytes During transmission, the FIFO threshold indicates the number of bytes (or words filled into the FIFO from the Local DMA before transmitted data are read from the buffer RAM. Thus, the transmission threshold is 16 bytes less than the receive threshold
D7	--	Reserved

Transmit Configuration Register (TCR)

The transmit configuration register determines the actions of the transmitter section of the DM9008 during transmission of a packet on the network. LB1 and LB0 power up as 0.

7	6	5	4	3	2	1	0
--	--	--	OFST	ATD	LB1	LB0	CRC

Bit	Symbol	Description
D0	CRC	Inhibit CRC 0: CRC appended by transmitter 1: CRC inhibited by transmitter
D1 D2	LB0 LB1	Encoded Loopback Control: These encoded configuration bits set the type of loopback that is to be performed. Note that loopback in mode 2 sets the ENA in loopback mode and that D3 of the DCR must be set to zero for loopback operation LB1 LB0 Mode 0 0 0 Normal Operation Mode 1 0 1 ENC module Loopback Mode 2 1 0 ENA module Loopback Mode 3 1 1 Loopback to Coax
D3	ATD	Auto Transmit Disable: This bit allows another station to disable the DM9008 transmitter by transmission of a particular multicast packet. The transmitter can be re-enabled by resetting this bit or by reception of a second particular multicast packet 0: Normal Operation 1: Reception of multicast address hashing to bit 62 disables transmitter; reception of multicast address hashing to bit 63 enables transmitter
D4	OFST	Collision Offset Enable: This bit modifies the backoff algorithm to allow propitiation of nodes 0: Backoff Logic implements normal algorithm 1: Forces Backoff algorithm modification to 0 to $2^{\min(3+n,10)}$ slot times for first three collisions, then follows standard backoff. (For first three collisions, station has higher average backoff delay, resulting in a low priority mode.)
D5	--	Reserve must be set to zero
D6	--	Reserved
D7	--	Reserved

Transmit Status Register (TSR)

This register records events that occur on the media during transmission of a packet. It is cleared when the next transmission is initiated by the host.
All bits remain low unless the event that corresponds to a particular bit occurs during transmission. Each transmission should be followed by a read of this register. The contents of this register are not specified until after the first transmission.

7	6	5	4	3	2	1	0
OWC	CDH	FU	CRS	ABT	COL	--	PTX

Bit	Symbol	Description
D0	PTX	Packet Transmitted: Indicates transmission without error (no excessive colli-sions or FIFO underrun) (ABT ="0", FU ="0")
D1	--	Reserved
D2	COL	Transmit Collided: Indicates that transmission collided at least once with another station on the network. The number of collisions is recorded in the Number of Colli-sions Register (NCR)
D3	ABT	Transmit Aborted: Indicates the DM9008 aborted transmission because of excessive collisions (total number of transmissions including original transmission attempt equals 16)
D4	CRS	Carrier Sense Lost: This bit is set when carrier is lost during transmission of the packet. Carrier Sense is monitored from the end of Preamble/Synch until the end of transmission. Transmission is not aborted on loss of carrier
D5	FU	FIFO Underrun: If the ENC cannot gain access to the bus before the FIF empties, this bit is set. Transmission of the packet will be aborted
D6	CDH	CD Heartbeat: Failure of the transceiver to transmit a collision signal after transmission of a packet will set this bit. The Collision Detect (CD) heartbeat signal must commence during the first 6.4μs of the interframe gap followinga transmission. In certain collisions, the CD heartbeat bit will be set even though the transceiver is not performing the CD heartbeat test
D7	OWC	Out of Window Collision: Indicates that a collision occurred after a slot time (51.2μs). Transmissions are rescheduled as in normal collisions

Receive Configuration Register (RCR)

This register determines the operation of the NIC during reception of a packet, and is used to program what types of packets to accept.

7	6	5	4	3	2	1	0
--	--	MON	PRO	AM	ABP	ARP	SEP

Bit	Symbol	Description
D0	SEP	Save Errored Packets 0: Packets with receive errors are rejected 1: Packets with receive errors are accepted. Receive errors are CRC and Frame Alignment errors
D1	ARP	Accept Runt Packets 0: Packets with fewer than 64 bytes rejected 1: Packets with fewer than 64 bytes accepted
D2	ABP	Accept Broadcast 0: Packets with all 1's broadcast destination address rejected 1: Packets with all 1's broadcast destination address accepted
D3	AM	Accept Multicast 0: Packets with multicast destination address not checked 1: Packets with multicast destination address checked
D4	PRO	Promiscuous Physical 0: Physical address of node must match the station address programmed in PARO-PAR5 (physical address checked) 1: All packets with physical address accepted (physical address not checked)
D5	MON	Monitor Mode: Enables the receiver to check addresses and CRC on incoming packets without buffering to memory. The Missed Packet Tally counter will be incremented for each recognized packet 0: Packets buffered to memory 1: Packets checked for address match, good CRC and Frame Alignment, but not buffered to memory
D6	--	Reserve: must be set to zero
D7	--	Reserved
Note: D2 and D3 are "OR'd" together, i.e., if D2 and D3 are set, DM9008 will accept broadcast and multicast addresses, as well as its own physical address. To establish full promiscuous mode, bits D2, D3, and D4 should be set. In addition, the multicast hashing array must be set to all 1's to accept all multicast addresses		

Receive Status Register (RSR)

This register records the status of the received packet, including information on errors and the type of address match, either physical or multicast. The contents of this register are written to buffer memory by the DMA after reception of a good packet. If packets with errors are to be saved, the receive status is written to memory at the head of the erroneous packet if an erroneous packet is received.

If packets with errors are to be rejected, the RSR will not be written to memory. The contents will be cleared when the next packet arrives. CRC errors, frame alignment errors and missed packets are counted internally by DM9008, which releases the host from reading the RSR in real time to record errors for network management functions. The contents of this register are not specified until after the first reception.

7	6	5	4	3	2	1	0
DFR	DIS	PHY	MPA	FO	FAE	CRC	PRX

Bit	Symbol	Description
D0	PRX	Packet Received Intact: lndicates packet received without error. (Bits CRC, FAE, FO, and MPA are zero for the received packet.)
D1	CRC	CRC Error: Indicates packet received with CRC error. Increments Tally Counter (CNTR1). This bit will also be set for Frame Alignment errors
D2	FAE	Frame Alignment Error: Indicates that the incoming packet did not end on a byte boundary and the CRC did not match at last byte boundary. Increments Tally counter (CNTRO)
D3	FO	FIFO Overrun: This bit is set when the FIFO is not serviced, causing overflow during reception. Reception of the packet will be aborted
D4	MPA	Missed Packet: Set when packet intended for node cannot be accepted by the DM9008 because of a lack of receive buffers, or when the controller is in monitor mode and did not buffer the packet to memory. Increments Tally Counter (CNTR2)
D5	PHY	Physical/Multicast Address: Indicates whether received packet had a physical or multicast address type 0: Physical Address Match 1: Multicast/Broadcast Address Match
D6	DIS	Receiver Disabled: Set when receiver is disabled by entering Monitor mode Reset when receiver is re-enabled while exiting Monitor mode
D7	DFR	Deferring: Set when the carrier or collision signal is detected by ENC. If the transceiver has asserted the CD line as a result of the jabber, this bit will stay set, indicating the jabber condition

Note: The following coding applies to CRC and FAE bits:

FAE	CRC	Type of Error
0	0	No error (Good CRC and <6 Dribble Bits)
0	1	CRC ERROR
1	0	Illegal, will not occur
1	1	Frame Alignment Error and CRC Error

Interrupt Mask Register (IMR)

The Interrupt Mask Register is used to mask interrupts. Each interrupt mask bit corresponds to a bit in the Interrupt Status Register (ISR). If an interrupt mask bit is set, an interrupt will be issued whenever the corresponding bit in the ISR is set. If any bit in the IMR is set low, an interrupt will not occur when the bit in the ISR is set. The IMR powers up all zeroes.

7	6	5	4	3	2	1	0
--	RDCE	CNTE	OVWE	TXEE	RXEE	PTXE	PRXE

Bit	Symbol	Description
D0	PRXE	PACKET RECEIVED INTERRUPT ENABLE Enables interrupt when packet is received
D1	PTXE	PACKET TRANSMITTED INTERRUPT ENABLE Enables interrupt when packet is transmitted
D2	RXEE	RECEIVE ERROR INTERRUPT ENABLE Enables interrupt when packet is received with error
D3	TXEE	TRANSMIT ERROR INTERRUPT ENABLE Enables interrupt when packet transmission results in error
D4	OVWE	OVERWRITE WARNING INTERRUPT ENABLE Enables interrupt when Buffer Management Logic lacks sufficient buffers to store incoming packet
D5	CNTE	COUNTER OVERFLOW INTERRUPT ENABLE Enables interrupt when MSB of one or more of the Network Tally counters has been set
D6	RDCE	DMA COMPLETE INTERRUPT ENABLE Enables interrupt when Remote DMA transfer has been completed
D7	--	Reserved

Interrupt Status Register (ISR)

This register is accessed to determine the cause of an interrupt. Any interrupt can be masked in the interrupt Mask Register (IMR). Individual interrupt bits are cleared by writing a 1 to the corresponding bit of the ISR.

The IRQ signal is active as long as any unmasked signal is set, and will not go low until all unmasked bits in this register have been cleared.
The ISR must be cleared after power up by writing it with all 1's.

7	6	5	4	3	2	1	0
RST	RDC	CNT	OVW	TXE	RXE	PTX	PRX

Bit	Symbol	Description
D0	PRX	Packet Received: Indicates packet received with no errors
D1	PTX	Packet Transmitted: Indicates packet transmitted with no errors
D2	RXE	Receive Error: Indicates that a packet was received with one or more of the following errors: -- CRC Error -- Frame Alignment Error -- FIFO Overrun -- Missed Packet
D3	TXE	Transmit Error: Set when packet is transmitted with one or more of the following errors: -- Excessive Collisions -- FIFO Underrun
D4	OVW	Overwrite Warning: Set when receive buffer ring storage resources have been exhausted. (Local DMA has reached Boundary Pointer.)
D5	CNT	Counter Overflow: Set when MSB of one or more of the Network Tally Counters has been set
D6	RDC	Remote DMA Complete: Set when Remote DMA operation has been completed
D7	RST	Reset Status: A status indicator (no interrupt generated): -- Set when ENC enters reset state and cleared when a start command is issued. -- Set when a Receive Buffer Ring overflows and cleared when overflow status ends Writing to this bit has no effect. The bit powers up high

Network Tally Counter Registers (CNTR)

Three 8-bit counters are provided for monitoring the number of CRC errors, Frame Alignment Errors and Missed Packets. The maximum count reached by any counter is 192 (C0H). These registers will be cleared when read by the CPU. The count is recorded in binary in CT0-CT7 of each Tally Register.

CNTR0: Monitors the number of Frame Alignment errors

7	6	5	4	3	2	1	0
CT7	CT6	CT5	CT4	CT3	CT2	CT1	CT0

CNTR1: Monitors the number of CRC errors

7	6	5	4	3	2	1	0
CT7	CT6	CT5	CT4	CT3	CT2	CT1	CT0

CNTR2: Monitors the number of Missed Packets

7	6	5	4	3	2	1	0
CT7	CT6	CT5	CT4	CT3	CT2	CT1	CT0

Number of Collisions Register (NCR)

This register contains the number of collisions a node experiences when attempting to transmit a packet. If no collisions are experienced during a transmission attempt, the COL bit of the TSR will not be set and the contents of NCR will be zero. If there are excessive collisions, the ABT bit in the TSR will be set and the contents of NCR will be zero. NCR is cleared after TXP in CR is set.

	7	6	5	4	3	2	1	0
NCR	0	0	0	0	NC3	NC2	NC1	NC0

FIFO Register (FIFO)

This is an 8-bit register that allows the CPU to examine the contents of the FIFO after loopback. The FIFO will contain the last 8 data bytes transmitted in the loopback packet. Sequential reads from the FIFO will advance a pointer in the FIFO and allow reading of all 8 bytes. Note that the FIFO should only be read when DM9008 has been programmed in loopback mode.

7	6	5	4	3	2	1	0
DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

Physical Address Register (PAR0-PAR5)

The Physical Address Registers are used to compare the destination addresses of incoming packets to be rejected or accepted. Comparisons are performed on a byte-wide basis. The bit assignment shown below relates the sequence in PAR0-PAR5 to the bit sequence of the received packet.

. .	Syn	Syn	DA0	DA1	DA2	DA3	DA4	DA5	DA6	DA7	. .

Destination Address → Sou

	D7	D6	D5	D4	D3	D2	D1	D0
PAR0	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
PAR1	DA15	DA14	DA13	DA12	DA11	DA10	DA9	DA8
PAR2	DA23	DA22	DA21	DA20	DA19	DA18	DA17	DA16
PAR3	DA31	DA30	DA29	DA28	DA27	DA26	DA25	DA24
PAR4	DA39	DA38	DA37	DA36	DA35	DA34	DA33	DA32
PAR5	DA47	DA46	DA45	DA44	DA43	DA42	DA41	DA40

Multicast Address Registers (MAR0-MAR7)

The Multicast Address Registers provide filtering of multicast addresses hashed by the CRC logic. All destination addresses are fed through the CRC logic. When the last bit of the destination address enters the CRC, the 6 most significant bits of the CRC generator are latched. These 6 bits are then decoded by a 1 of 64 decode to index a unique filter bit (FB0-63) in the multicast address registers. If the filter bit selected is set, the multicast packet is accepted. The system designer uses a program to determine which filter bits to set in the multicast registers. If an address is found to hash to the value 50(32H), then FB50 in MAR6 should be initialized to 1. All multicast filter bits that correspond to the multicast address accepted by the node are then set to one. To accept all multicast packets, all of the registers are set to all ones.

	D7	D6	D5	D4	D3	D2	D1	D0
MAR0	FB7	FB6	FB5	FB4	FB3	FB2	FB1	FB0
MAR1	FB15	FB14	FB13	FB12	FB11	FB10	FB9	FB8
MAR2	FB23	FB22	FB21	FB20	FB19	FB18	FB17	FB16
MAR3	FB31	FB30	FB29	FB28	FB27	FB26	FB25	FB24
MAR4	FB39	FB38	FB37	FB36	FB35	FB34	FB33	FB32
MAR5	FB47	FB46	FB45	FB44	FB43	FB42	FB41	FB40
MAR6	FB55	FB54	FB53	FB52	FB51	FB50	FB49	FB48
MAR7	FB63	FB62	FB61	FB60	FB59	FB58	FB57	FB56

DMA Registers

Local DMA Transmit Registers

	15 – 8	7 – 0
(TPSR)	PAGE START	
(TBCR0,1)	TRANSMIT BYTE COUNT	

Local DMA Receive Registers

	15 – 8	7 – 0
(PSTART)	PAGE START	
(PSTOP)	PAGE STOP	
(CURR)	CURRENT	
(BRNY)	BOUNDARY	
(CLDA0,1)	CURRENT LOCAL DMA ADDRESS	

Remote DMA Registers

	15 – 8	7 – 0
(RSAR0,1)	START ADDRESS	
(RBCR0,1)	BYTE COUNT	
(CRAD0,1)	CURRENT REMOTE DMA ADDRESS	

(i) Local DMA Transmit Registers

Transmit Page Start Register (TPSR)
This register points to the assembled packet to be transmitted. Since all transmit packets are assembled on 256-byte page boundaries, only the eight higher order addresses are specified.

7	6	5	4	3	2	1	0
A15	A14	A13	A12	A11	A10	A9	A8

Transmit Byte Counter Register 0,1 (TBCR0,TBCR1)
These two registers indicate the length of the packet to be transmitted in bytes. The maximum number of transmit bytes allowed is 64K bytes. The DM9008 will not truncate transmissions longer than 1500 bytes.

	7	6	5	4	3	2	1	0
TBCR1	L15	L14	L13	L12	L11	L10	L9	L8
TBCR0	L7	L6	L5	L4	L3	L2	L1	L0

(ii) Local DMA Receive Registers
Page Start, Stop Registers (PSTART, PSTOP)
The Page Start and Page Stop Registers program the starting and stopping page of the Receive Buffer RAM. Since the DM9008 uses fixed 256-byte buffers aligned on page boundaries, only the upper eight bits of the start and stop address are specified.

	7	6	5	4	3	2	1	0
PSTART PSTOP	A15	A14	A13	A12	A11	A10	A9	A8

Boundary Register (BNRY)

This register is used to prevent overflow of the Receive Buffer Ring. Buffer management compares the contents of this register to the next buffer address when linking buffers together. If the contents of this register match the next buffer address, the local DMA operation is aborted.

	7	6	5	4	3	2	1	0
BNRY	A15	A14	A13	A12	A11	A10	A9	A8

Current Page Register (CURR)

This register is used internally by the Buffer Management Logic as a backup register for reception. CURR contains the address of the first buffer to be used for a packet reception, and is used to restore DMA pointers in the event of receive errors. This register is initialized to the same value as PSTART, and should not be written to again unless the controller is reset.

	7	6	5	4	3	2	1	0
CURR	A15	A14	A13	A12	A11	A10	A9	A8

Current Local DMA Register 0, 1 (CLDA0, 1)

These two registers can be accessed to determine the current Local DMA Address.

	7	6	5	4	3	2	1	0
CLDA 1	A15	A14	A13	A12	A11	A10	A9	A8

	7	6	5	4	3	2	1	0
CLDA 0	A7	A6	A5	A4	A3	A2	A1	A0

(iii) Remote DMA Registers

Remote Start Address Registers (RSAR0, 1)
Remote Byte Count Registers (RBCR0, 1)
Remote DMA operations are programmed via the Remote Start Address (RSAR0, 1) and Remote Byte Count registers (RBCR0, 1). The Remote Start Address is used to point to the start of the block of data to be transferred. The Remote Byte Count is used to indicate the length of the block (in bytes).

	7	6	5	4	3	2	1	0
RSAR1	A15	A14	A13	A12	A11	A10	A9	A8

	7	6	5	4	3	2	1	0
RSAR0	A7	A6	A5	A4	A3	A2	A1	A0

	7	6	5	4	3	2	1	0
RBCR1	BC15	BC14	BC13	BC12	BC11	BC10	BC9	BC8

3

	7	6	5	4	3	2	1	0
RBCR0	BC7	BC6	BC5	BC4	BC3	BC2	BC1	BC0

Current Remote DMA Address Registers (CRDA0, 1)
The Current Remote DMA Registers contain the current address of the Remote DMA. The bit assignments are shown below:

	7	6	5	4	3	2	1	0
CRDA1	A15	A14	A13	A12	A11	A10	A9	A8

	7	6	5	4	3	2	1	0
CRDA0	A7	A6	A5	A4	A3	A2	A1	A0

Functional Description

Plug and Play (PnP) Module

Auto-configuration Ports

Three 8-bit I/O ports are defined for the PnP read/write operations. They are called "Auto-configuration ports", and are listed below.

Port Name	Type	Location
ADDRESS	W	279H (Printer status port)
WRITE DATA	W	A79H (Printer status prot + 800H)
READ DATA	R	Relocatable in range 203H to 3FFH

The Plug and Play registers are accessed by first writing the address of the desired register, which is called the "Register Index". This can be followed by any number of WRITE_DATA or READ_DATA accesses to the same indexed register without any need to write to the ADDRESS port before each access.

The Address port is also the write destination of the initiation key, which will be described later.

Plug and Play Registers

The Plug and Play registers may be divided into two groups: card registers and logical device registers. According to the Plug and Play specification, for each additional device contained in a PnP card, there should be a corresponding copy of the logical device register. However, because the DM9008 contains only one logical device, the card registers and logical device registers are unique for each card. Those PnP registers or bits not defined in the following table are all read with value = 0.

Card Control Registers

Index	Name	Type	Definition
00H	Set RD_DATA port	W	The location of the READ_DATA port is determined by writing to this register. Bits[7:0] become ISA I/O read port address bits[9:2]. Address bits[1:0] of the READ_DATA port are always1
01H	Serial Isolation	R	A read to this register causes a PnP card in the Isolation state to compare one bit of the card's serial ID. This process is described in more detail on page 34
02H	Config Control	W	Bit[0] - Reset command Setting this bit will reset all logical devices and restore configuration registers to their power-up values The CSN is preserved Bit[1] - Wait for Key command Setting this bit makes the PnP card return to the Wait for Key state. The CSN is preserved Bit[2] - PnP Reset CSN command Setting this bit will reset the card's CSN to 0 Note that the hardware will automatically clear the bits without any need for software to clear them
03H	Wake[CSN]	W	A write to this register will cause all cards that have a CSN that matches the write data[7:0] to go from the Sleep state to either the 1) Isolation state if the write data for this command is zero, or 2) Config state if the write data is not zero
04H	Resource Data	R	A read from this register reads the next byte of resource data. The Status register must be polled until bit[0] is set before this register may be read
05H	Status	R	Bit[0], when set, indicates it is O.K. to read the next data byte from the Resource Data register
06H	Card Select Numbe (CSN)	R/W	A write to this register sets a card's CSN. The CSN's value is uniquely assigned to each ISA PnP card after the serial identification process so that each card may be individually selected during a Wake[CSN] command
07H	Logical Device	R	00H (Only one logical device in DM9008)

Logical Device Control Registers

Index	Name	Type	Definition
30H	Activate	R/W	For each logical device, there is one Activate register that controls whether or not the device is active on the ISA bus. Bit[0], if set, activates the logical device. Before a logical device is activated, I/O range check must be disabled
31H	I/O Range Check	R/W	This register is used to perform a conflict check on the I/O port range programmed for use by a logical device Bit[1] - This bit, when set, enables I/O range check I/O range check is only valid when the logical device is inactive Bit[0] - If set, this bit forces logical device to respond to I/O reads within logical device's assigned I/O range with a55H when I/O range check is in operation. If clear, the logical device drives AAH

Logical Device Configuration Registers

Memory Configuration Registers

Index	Name	Type	Definition
40H	BROM base address bits[23:16]	R/W	Bits[23:20] and bit[17] are read only when their values = 0. All other bits are read/write bits
41H	BROM base address bits[15:0]	R/W	Bits[13:8] are read only when their values = 0. All other bits are read/write bits
42H	Memory Control	R	00H (Only 8-bit operation is supported for BROM)

I/O Configuration Registers

Index	Name	Type	Definition
60H	I/O base address bits[15:8]	R/W	Bits[15:10] are read-only with undetermined values. Bit[9] is read only, and is always 1. All other bits are read/write bits
61H	I/O base address bits[7:0]	R/W	Bits[4:0] are read only when their values = 0. All other bits are read/write bits

Interrupt Configuration Registers

Index	Name	Type	Definition
70H	IRQ level	R/W	Read/write value indicating a selected interrupt level. Bits[3:0] select which ISA interrupt level is used. A value of 1 selects IRQ1, 15 selects IRQ15, etc. IRQ0 is not a valid interrupt selection
71H	IRQ type bits[7:0]	R	Read/write value indicating which type of interrupt is used for the IRQ selected above. Bit[1] - Level, 1 = high, 0 = low Bit[0] - Type, 1= level, 0 = edge For DM9008, this register is read only, with a value of 02H

DMA Configuration Registers

Index	Name	Type	Definition
74H	DMA channel select 0	R	04H (indicating no DMA channel is needed)
75H	DMA channel select 1	R	04H (indicating no DMA channel is needed)

Vendor Defined Registers

Index	Name	Type	Definition
F0H	CONFIG A	R	Direct mapping of CONFIG A register, page 0
F1H	CONFIG B	R	Direct mapping of CONFIG B register, page 0
F2H	CONFIG C	R	Direct mapping of the CONFIG C register, page 2
F4H	RESET CSN	W	Writing bit 2 to 1 will reset DM9008 CSN to 0

Initial Values of CONFIG.A-D after PC Hardware Reset

CONFIG A

Mode	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	FREAD	**INT2**	**INT1**	**INT0**	**IOAD3**	**IOAD2**	**IOAD1**	**IOAD0**
DM Jumperless Plug and Play	9346	9346	9346	9346	9346	9346	9346	9346

CONFIG B

Mode	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	--	**--**	**BUSERR**	**CHRDY**	**--**	**GDLINK**	**PHYS1**	**PHYS0**
DM Jumperless Plug and Play	0	0	Read only	9346	0	Read only	9346	9346

CONFIG C

Mode	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	--	**PnP-B**	**--**	**--**	**BPS3**	**BPS2**	**BPS1**	**BPS0**
DM Jumperless Plug and Play	9346	0	0	0	9346	9346	9346	9346

CONFIG D

Mode	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 Ý
	EEMODE	**--**	**--**	**CLK-REF**	**EECS**	**EECK**	**EEDO**	**EEDI**
DM Jumperless Plug and Play	0	0	0	0	0	0	0	0

The Initial Key for Plug and Play (PnP)

The Plug and Play logical is quiescent on power up and must be enabled by software. This accomplished with a predefined sequence of indices (32 I/O writes) to the Address port. This sequence is called the Initiation Key. The write sequence is decoded by DM9008. If the proper series of I/O writes is detected, then the Plug and Play auto-configuration ports are enabled. The write sequence will be reset, and must be issued from the beginning if any data mismatch occurs. The exact sequence for the Initiation Key is listed below in hexadecimal notation.

PnP Initiation Key

6A, B5, DA, ED, F6, FB, 7D, BE, DF, 6F, 37, 1B, 0D, 86, C3, 61, B0, 58, 2C, 16, 8B, 45, A2, D1, E8, 74, 3A, 9D, CE, E7, 73, 39

DM Initiation Key

2A, 95, CA, E5, F2, F9, FC, 7E, BF, 5F, 2F, 17, 0B, 05, 82, C1, E0, 70, 38, 1C, 0E, 87, 43, 21, 90, 48, 24, 12, 89, C4, 62, B1

Isolation Protocol

A simple algorithm is used to isolate each Plug and Play card. This algorithm uses the signals on the ISA bus. It requires lock-step operation between the Plug and Play hardware and the isolation software.

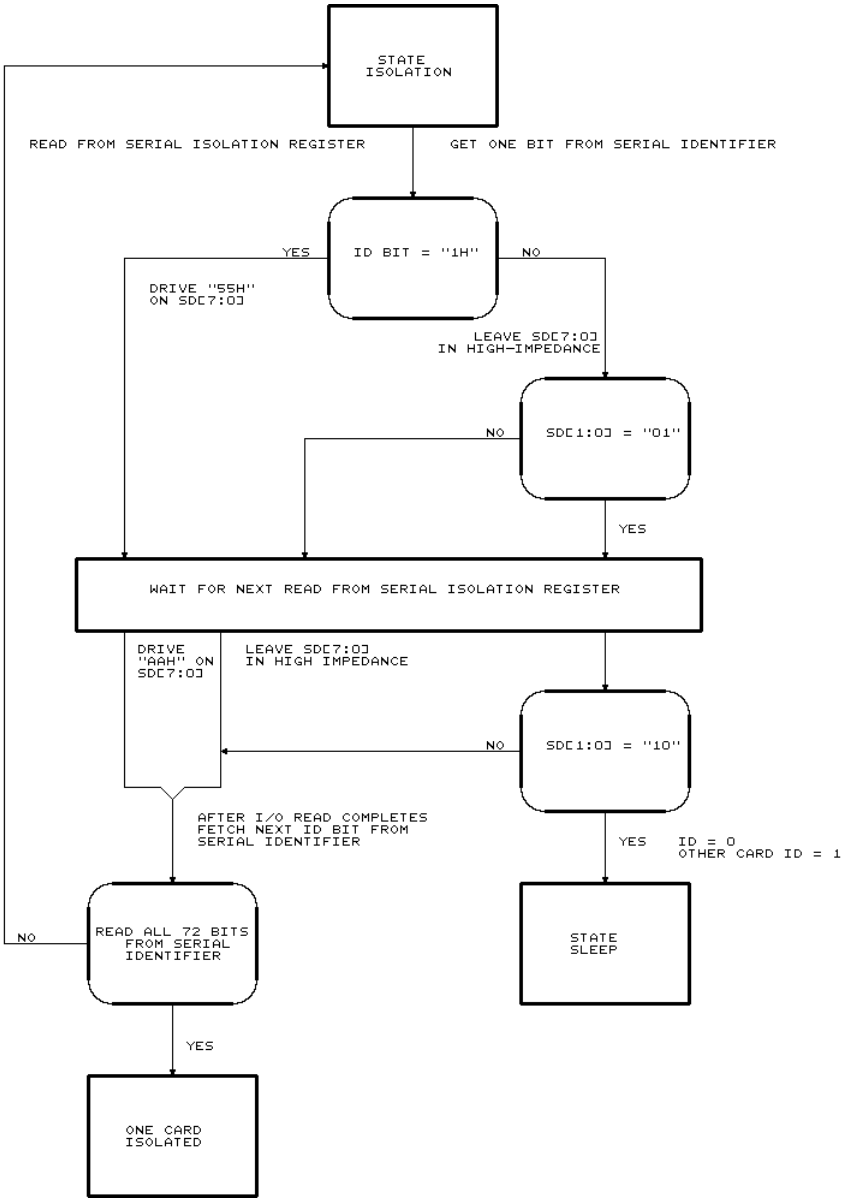


Figure 1. Plug and Play ISA Card Isolation Algorithm

Serial Identifier

The key element of the Plug and Play isolation protocol is that each card contains a unique number called a serial identifier. The serial identifier is a 72-bit unique, non-zero number composed of two 32-bit fields and 8-bit checksum. The first 32-bit field is a vendor identifier. The other 32 bits can be any value, such as a serial number, part of a LAN address or a static number, as long as no two cards in a single system have the same 64-bit number. The serial identifier is accessed bit-serially by isolation logic, and is used to differentiate the cards.

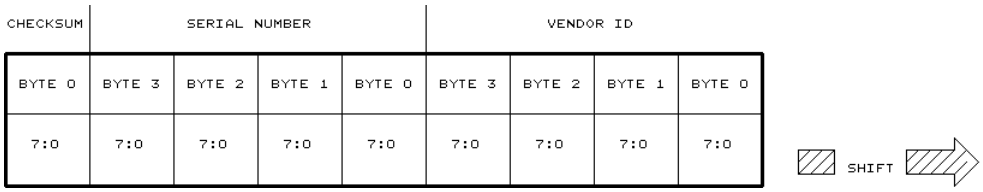


Figure 2. Shifting of Serial Identifier

The shift order for all Plug and Play serial isolation and resource data is defined as bit[0], bit[1], and so on through bit[7].

Hardware Protocol

The isolation protocol can be invoked by the Plug and Play software at any time. The previously described Initiation Key puts all cards into configuration mode. The hardware for each card expects 72 pairs of I/O read accesses to the READ_DATA port. The card's response to these reads depends on the value for each bit of the serial identifier, which is examined one bit at a time, as shown in Figure 1.

If the current bit of the serial identifier is a "1", then the card will drive the data bus to 55H to complete the first I/O read cycle. If the bit is "0", then the card puts its data bus driver into high impedance. All cards in high impedance will check the data bus during the I/O read cycle to sense if another card is driving SD[1:0] to "01". During the second I/O read, the card(s) that drove the 55H will now drive a AAH. All high impedance cards will check the data bus to sense if another card is driving SD[1:0] to "10".

If a high impedance card senses another card driving the data bus with the appropriate data during both cycles, it ceases to participate in the current iteration of card isolation. Such cards, which lose out, will participate in future iterat-ions of the isolation protocol.

NOTE: During each read cycle, the Plug and Play hardware drives the entire 8-bit data bus, but checks only the lower 2 bits.

If a card is driving the bus or is in high impedance state and does not sense another card driving the bus, then it should prepare for the next pair of I/O reads. The card shifts the serial identifier by one bit, using the shifted bit to decide its response. The above sequence is repeated for the entire 72-bit serial identifier.

At the end of this process, one card remains. This card is assigned a handle, referred to as the Card Select Number (CSN), that will be used later to select the card. Cards which have been assigned a CSN will not participate in subsequent iterations of the isolation protocol. Cards must be assigned a CSN before they will respond to the other PnP commands.

Software Protocol

The Plug and Play software sends the initiation Key to all Plug and Play cards to place them into configuration mode. The software is then ready to perform the isolation protocol.

The Plug and Play software generates 72 pairs of I/O read cycles from the READ_DATA port. The software checks the data returned from each pair of I/O reads for the 55H or AAH driven by the hardware. If either 55H or AAH are read back, then the software assumes that the hardware has a 1 bit in that position. All other bits are assumed to be 0.

During the first 64 bits, software generates a checksum using the received data. The checksum is compared with the checksum read back in the last 8 bits of the sequence.
There are two other special considerations for software protocol. During an iteration, it is possible that the 55H and AAH combination is never detected. It is also possible that the checksum does not match. If either of these cases occurs on the first iteration, it must be assumed that the READ_DATA port is in conflict. If a conflict is detected, then the READ_DATA port is relocated. The above process is repeated until a non-conflicting location for the READ_DATA port is found. The entire range between 200H and 3FFH is available; however, in practice it is expected that only a few locations will be tried before software determines that no Plug and Play cards are present.

During subsequent iterations, the occurrence of either of these two special cases should be interpreted as the absence of any further Plug and Play cards (i.e. the last card was found in the previous iteration). This terminates the isolation protocol.

NOTE: The software must delay 1 msec prior to starting the first pair of isolation reads, and must wait 250µsec between each subsequent pair of isolation reads. This delay gives the ISA card time to access information from very slow storage devices.

On power up, all PnP cards detect RSTDRV, set their CSNs to 0, and enter the Wait fo Key state. There is a required 2 msec delay from either a RSTDRV or PnP Reset command to any Plug and Play port access. This allows a card to load initial configuration information from a non-volatile device, which is "9346" for DM9008.

Cards in the Wait for Key state do notacknowlege any access to their auto-configuration ports until the Initiation Key is detected, ignoring all ISA access to their Plug and Play interface. When the cards have received the initiation key, they enter the Sleep state. In this state, the cards listen for a Wake[CSN] command with the write data set to 00H. This wake[CSN] command will send all cards to the Isolation state and reset the serial identifier/resource data pointer to the beginning.

The first time the cards enter the Isolation state, it is necessary to set the READ_DATA port address using the Set RD_DATA port command. The software should then use isolation protocol to check whether the selected READ_DATA port address is in conflict with any other device.

Next, 72 pairs of reads are performed to the Serial Isolation register to isolate a card, as previously described. If the checksum read from the card is valid, then one card has been isolated. The isolated card remains in the Isolation state, while all other cards failing the isolation protocol are returned to Sleep state. The CSN on the isolated card is set to a unique number, causing this card to change to the Config state. Sending a Wake[0] command causes this card to change back to Sleep state, and all cards with a CSN value of zero to change to the Isolation state. This entire process is repeated until no Plug and Play cards are detected.

Reading Resource Data

Each PnP card supports a resource data structure stored in a non-volatile device (e.g. 9346) that describes the resources requested by the card. The Plug and Play resource management software will arbitrate resources and set up the logical device configuration registers according to the resource data.

Card resource data may only be read from cards in the Config state. A card may get to the Config state by one of two different methods:.1) A card enters the Config state in response to the card "winning" the serial isolation protocol and having a CSN assigned, or 2) the card receives a Wake[CSN] command that matches the card's CSN.

As described above, all Plug and Play cards function as if their serial identifier and their resource data both come from the same serial device. As also stated above, the pointer to the serial device is reset in response to any Wake[CSN] command. This implies that if a card enters the Config state directly from sleep state in response to a Wake[CSN] command, the 9-byte serial identifier must first be read before the card resource data is accessed. The Vendor ID and Unique Serial Number are valid; however, the checksum byte, when read in this way, is not valid. For a card that enters the Config state from the isolation state, the first read of the resource Data register will return resource data.

Card resource data is read by first polling the Status register and waiting for bit[0] to be set. When this bit is set, one byte of resource data is ready to be read from the Resource data register. After the Resource Data register is read, the Status register must be polled before reading the next byte of resource data. This process is repeated until all resource data is read.

The above operation implies that the hardware is responsible for accumulating 8 bits of data in the Resource Data register. When this operation is complete, the status bit[0] is set. When a read is performed on the Resource Data register, status bit[0] is cleared, eight more bits are shifted into the Resource Data register, and
the status bit[0] is set again.

Contents of EEPROM (93C46) in DM9008

Word	High Byte	Low Byte
00H	Ethernet Addr. 1	Ethernet Addr. 0
01H	Ethernet Addr. 3	Ethernet Addr. 2
02H	Ethernet Addr. 5	Ethernet Addr. 4
03H | 06H	: : :	: : :
07H	57H	57H
08H	42H	42H
09H | 0DH	: : :	: : :
0EH	Config. Reg. B	Config. Reg. A
0FH	Operation Mode *1	Config. Reg. C
10H	Vendor ID byte 1	Vendor ID byte 0
11H	Vendor ID byte 3	Vendor ID byte 2
12H	Serial # byte 1	Serial # byte 0
13H	Serial # byte 3	Serial # byte 2
14H	Resource Data 0	Checksum
15H | 3FH	Plug and Play Resource Data *2	

PS: *1. Operation mode to meet the different reqirement, DM9008 offers three operation mode:
1. Auto-Detection (default): any value except 0X4A and 0X50.
2. Jumpless mode: 0X4A ("J")
3. PnP mode: 0X50 ("P")

*2. For more information on the PnP resource data format, please refer to the Plug and Play ISA sepcification v1.0a.

ENA Module

Oscillator

The oscillator is controlled by a 20 Mhz parallel resonant crystal connected between X1 and X2. The 20 MHz output of the oscillator is divided by 2 to generate the 10 MHz transmit clock for the ENC. The oscillator also provides internal clock signals to the encoding and decoding circuits. It is recommended that a crystal meeting the following specifications be used:

Resonant Frequency . . . . . 20 MHz
Tolerance . . . . . ±0.001% at 25°C
Stability . . . . . ±0.005% at 0°C to 70°C
Type . . . . . AT CUT
Circuit . . . . . Series or Parallel Resonance

An external 20MHz oscillator may be applied to pin X2 while pin X1 is connected to ground.

Manchester Encoder

The Manchester encoder accepts NRZ data from the controller, encodes the data to Manchester format, and transmits it differentially to the transceiver through the differential transmit driver.

The differential transmit pair from the secondary of the isolation transformer drives up to 50 meters of wisted pair AUI cable. These outputs are source followers which require two 270 ohm pull-down resistors to ground.

Manchester Decoder

The decoder consists of a slicer circuit and a PLL circuit to recover the receiver clock and data. The differential input must be externally terminated with two 39 ohm resistors connected in series if the standard 78 ohm transceiver drop cable is used. In thin Ethernet applications, these resistors are optional.

To prevent noise from falsely triggering the decoder, a squelch circuit at the input rejects signals with pulse width of less than 30 ns at -300 mV, or signals with levels of less than -175 mV. Signals more negative than -300 mV with a duration of greater than 30 ns are decoded. Data become valid typically within 5 bit times. The ENA may tolerate bit jitter of up to 20ns in the received data. The decoder detects the end of a frame when no more midbit transitions are detected.

Collision Detector

A transceiver detects collisions on the network and generates a 10 Mhz signal at the CD± input. When these inputs exceed the squelch requirements (same as the receiver/decoder), DM9008 uses this signal to back off its current transmission and reschedule another one.

Loopback Function

When loopback mode 2 is set, the ENA redirects its transmitted data back into its receive path. This feature provides a convenient method for testing the whole chip and system level integrity. The transmit driver and receive input circuit are disabled in loopback mode.

Traffic LED Driver

DM9008 provides an LED driver in pin 55. When the DM9008 is in transmission or receive mode, this pin will go low for 80ms, then into high impedance state for 50ms to indicate the presence of traffic on the network. In idle state, it is in high impedance state.

ENC Module

Transmit Parallel/Serial

At the beginning of each transmission, the preamble and synch generators append 62 bits of 1, 0 preamble and 1, 1 synch pattern. The parallel data from the FIFO are then serialized for transmission. The serial data are also shifted into the CRC generator. After the last data byte has been serialized, the 32-bit FCS field is shifted directly out of the CRC generator.

Receive Serial/Parallel

When the RX± input signal from ENA becomes active, the incoming serial data are shifted into the shift register. The receiver will detect the SFD to establish where byte boundaries are located. The serial data are also routed to the CRC checker. After every eight receive clocks, the byte-wide data are transferred to the FIFO, and the receive byte count is incremented.

Address Recognition Logic

There are three types of address recognition logic. The first 6-byte destination address field of the received packet is compared to the physical address registers. The packet will be rejected if the field and registers do not match. Multicast destination addresses are filtered using a hashing technique. The packet is accepted only if the multicast address indexes a bit that has been set in the filter bit array of the multicast address registers. Each destination address is also checked for all 1's, which is the reserved broadcast address.

16-Byte FIFO

Through local DMA operation, parallel data can be transferred to or from the 16-byte FIFO during transmission and reception. The DMA begins a bus access and writes/reads data to/from the FIFO before a FIFO underrun/overrun occurs. Because the DM9008 must buffer the address field of an incoming packet to make a decision, the first local DMA transfer does not occur until 8 bytes have accumulated in the FIFO. The FIFO logic will flag a FIFO overrun when the 13th byte is written to the FIFO.

CRC Generator/Checker

During transmission, the CRC encodes all fields after the synch bits to generate a local CRC field. The CRC is shifted out MSB first following the transmit byte. During reception, the CRC logic generates a CRC field from the incoming packet. This local CRC is serially compared to the incoming CRC to check whether the incoming packet is correct.

DMA Registers and Control Logic

Two 16-bit DMA channels are provided. The local DMA stores received packets in a receive buffer ring during reception and transfers a packet from local buffer memory to the FIFO during transmission. The remote DMA is used to transfer data between the local buffer memory and the host system. Both are internally arbitrated, with the local DMA channel having highest priority. External arbitration is performed with a standard bus request, bus acknowledge handshake protocol.

Protocol Control Logic

The protocol control logic implements the IEEE 802.3 protocol, including collision recovery with random backoff. The protocol control logic also formats packets during transmission, as well as strips preamble and synch during reception.

Direct Memory Access Control (DMA)

DM9008 provides DMA capabilities to simplify buffer data transfer. The local DMA channel transfers data between the FIFO and buffer. On reception, packets are transferred from the FIFO to the receive buffer ring in bursts. During transmission, the packets are transferred in the opposite direction from the buffer to the FIFO.

A remote DMA channel is provided to accomplish transfers between buffer memory and system memory. TheENC's local DMA channel performs burst transfers between the buffer memory and DM9008's FIFO. The remote DMA transfers data between the buffer memory and the host memory via bidirectional latches. The DM9008 allows local and remote DMA operations to be interleaved.

Remote DMA

The Remote DMA channel is used both to assemble packets for transmission and to remove received packets from the Receive Buffer Ring. It may also be used as a general purpose slave DMA channel for moving blocks of data or commands between host memory and local buffer memory. There are three modes of operation: Remote Write, Remote Read and Send Packet. Two register pairs are used to control the Remote DMA: Remote Start Address (RSAR0, RSAR1) and Remote Byte Count (RBCR0, RBCR1). The Start Address Register pair points to the beginning of the block to be moved, while the Byte Count Register pair is used to indicate the number of bytes to be transferred. Full handshake logic is provided to move data between local buffer memory and a bidirectional I/O port.

Remote Write

A Remote Write transfer is used to move a block of data from the host into local buffer memory. The Remote DMA will read data from the I/O port and sequentially write it to local buffer memory beginning at the Remote Start Address. The DMA Address will be incremented and the Byte Counter will be decremented after each transfer. The DMA is terminated when the Remote Byte Count Register reaches a count of zero.

Remote Read

A Remote Read transfer is used to move a block of data from local buffer memory to the host. The Remote DMA will sequentially read data from the local buffer memory, beginning at the Remote Start Address, and write data to the I/O port. The DMA Address will be incremented and the Byte Counter will be decremented after each transfer. The DMA is terminated when the Remote Byte Count Register reaches zero.

Send Packet Command

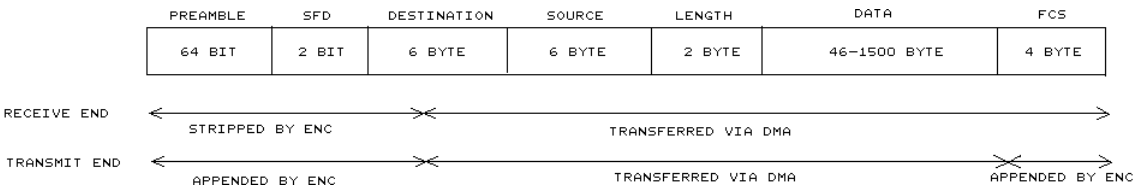
The Remote DMA channel can be automatically initialized to transfer a single packet from the Receive Buffer Ring. The CPU begins this transfer by issuing a "Send Packet" Command. The DMA will be initialized to the value of the Boundary Pointer Register, and the Remote Byte Count Register pair (RBCR0, RBCR1) will be initialized to the value of the Receive Byte Count fields found in the Buffer Header of each packet. After the data are transferred, the Boundary Pointer is advanced to allow the buffers to be used for new receive packets. The Remote Read will terminate when the Byte Count equals zero. The Remote DMA is then prepared to read the next packet from the Receive Buffer Ring. If the DMA pointer crosses the Page Stop Register, it is reset to the Page Start Address. This allows the Remote DMA to remove packets that have wrapped around to the top of the Receive Buffer Ring.

Note 1: In order for DM9008 to correctly execute the Send Packet Command, the upper Remote Byte Count Register (RBCR1) must first be loaded with 0FH.

Note 2: The Send Packet command cannot be used with 68000-type processors.

Packet Encapsulation/Decapsulation

A standard IEEE 802.3 packet consists of the following fields: preamble, Start of Frame Delimiter (SFD), destination address, source address, length, data and Frame Check Sequence (FCS). The typical format is shown on the following page. The packets areManchester encoded and decoded by the ENA and transferred serially to the ENC using NRZ data with a clock. All fields are of fixed length except for the data field. DM9008 generates and appends the preamble, SFD and FCS fields during transmission. The Preamble and SFD fields are stripped during reception. (The CRC is passed through to buffer
memory during reception.)



IEEE 802.3 Packet Format

Preamble and Start of Frame

Delimiter (SFD)

The Manchester encoded alternating 1, 0 preamble field is used by the ENA to acquire bit synchronization with an incoming packet. When transmitted, each packet contains 62 bits of alternating 1, 0 preamble. Some of this preamble will be lost as the packet travels through the network. The preamble field is stripped by the ENC. Byte alignment is performed with the Start of Frame Delimiter (SFD) pattern, which consists of two consecutive 1's. The ENC does not treat the SFD pattern as a byte; it detects only the two-bit pattern. This allows any preceding preamble within the SFD to be used for phase locking.

Destination Address

The destination address indicates the destination of the packet on the network, and is used to filter unwanted packets from reaching a node. Three types of address formats are supported by the DM9008: physical, multicast and broadcast. The physical address is a unique address that corresponds to only a single node. All physical addresses have an MSB of "0." These addresses are compared to the internally stored physical address registers. Each bit in the destination address must match the corresponding address of the address register in order for DM9008 to accept the packet. Multicast addresses begin with an MSB of "1." The DM9008 filters multicast addresses using a standard hashing algorithm that maps all multicast addresses into a 6-bit value. This 6-bit value indexes a 64-bit array that filters the value. If the address consists of all 1's, it is a broadcast address, indicating that the packet is intende for all nodes. Promiscuous mode allows reception of all packets: the destination address is not required to match any filters. Physical, broadcast, multicast, and promis-cuous address modes can be selected.

Source Address

The source address is the physical address of the node that sent the packet. Source addresses cannot be multicast or broadcast addresses. This field is simply passed to buffer memory.

Length Field

The 2-byte length field indicates the number of bytes that are contained in the data field of the packet. This field is not interpreted by the ENC.

Data Field

The data field consists of anywhere from 46 to 1500 bytes. Messages longer than 1500 bytes need to be broken into multiple packets. Messages shorter than 46 bytes will require padding to bring the data field to the minimum length of 46 bytes. If the data field is padded, the number of valid data bytes is indicated in the length.

FCS Field

The Frame Check Sequence (FCS) is a 32-bit CRC field calculated and appended to a packet during transmission to allow detection of errors when a packet is received. During reception, error-free packets result in a specific pattern in the CRC generator. Packets with improper CRC will be rejected. The AUTODIN II ($X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X^1 + 1$) polynomial is used for CRC calculations.

Packet Reception

The local DMA receive channel uses a Buffer Ring Structure comprised of a series of contiguous fixed length 256-byte (128-word) buffers for storage of received packets. The location of the Receive Buffer Ring is programmed in two registers: Page Start and Page Stop. An ethernet packet consists of a distribution of shorter link control packets and longer data packets. The 256 byte buffer length provides a good compromise between short packets and longer packets for using memory most efficiently. In addition, these buffers provide memory resources for storage of back-to-back packets in loaded networks. The assignment of buffers for storing packets is controlled by DM9008's Buffer Management Logic, which provides three basic functions: linking of receive buffers for long packets, recovery of buffers when a packet is rejected, and recirculation of buffer pages that have been read by the host. At initialization, a portion of the 64K byte (or 32K word) address space is reserved for the receive buffer ring. For applications, DM9008 should be programmed to 16K byte (or 8K word) address space (4000H-7FFFH) in NE2000 16-bit mode, and 8K byte address space (4000-H-5FFFH) in NE2000 8-bit mode. Two eight-bit registers, the Page Start Address Register (PSTART) and the Page Stop Address Register (PSTOP), define the physical boundaries where the buffers reside. DM9008 treats the list of buffers as a logical ring. Whenever the DMA address reaches the Page Stop Address, the DMA is reset to the Page Start Address.

Initialization of the Buffer Ring

Two static registers and two working registers control the operation of the Buffer Ring. These are the Page Start Register, the Page Stop Register (both described previously), the Current Page Register (CURR) and the Boundary Pointer Register (BNRY). The Current Page Register points to the first buffer used to store a packet, and is used to restore the DMA to Buffer Ring writing status. It also restores the DMA address in the event of a Runt Packet, a CRC or Frame Alignment error. The Boundary Register points to the first packet in the Ring not yet read by the host If the local DMA address reaches the boundary, reception is aborted. The Boundary Pointer is also used to initialize the Remote DMA for removing a packet, and is incremented when a packet is removed. A simple analogy for remembering the function of these registers is that the Current Page Register acts as a Write Pointer, whereas the Boundary Pointer acts as a Read Pointer.

Beginning of Reception

When the first packet arrives, DM9008 begins storing the packet at the location pointed to by CURR. An offset of 4 bytes is saved in this first buffer to store the packet's corresponding receive status.

Linking Receive Buffer Pages

If the length of the packet exhausts the first 256-byte buffer, the DMA performs a forward link to the next buffer to store the remainder of the packet. For a maximum length packet, the buffer logic will link six buffers to store the entire packet. Buffers cannot be skipped when linking; a packet will always be stored in contiguous buffers. Before the next buffer can be linked, the Buffer Management Logic performs two comparisons. The first comparison tests for equalit between the DMA address of the next buffer and the contents of PSTOP. If the buffer address equals PSTOP, the buffer management logic will restore the DMA to the first buffer in the Receive Buffer Ring value programmed in PSTART. The second comparison tests for equality between the DMA address of the next buffer address and the contents of BNRY. If the two values are equal, the reception is aborted. BNRY can be used to protect against overwriting any area in the receive buffer ring that has not yet been read. When linking buffers, buffer management will never cross this pointer, effectively avoiding any overwrites. If the buffer address does not match either BNRY or PSTOP, the link to the next buffer is performed.

Linking Buffers

Before the DMA can enter the next contiguous 256-byte buffer, the address is checked for equality to PSTOP and to BNRY. If neither is reached, the DMA is allowed to use the next buffer.

Buffer Ring Overflow

If the Buffer Ring has been filled and the DMA reaches the Boundary Pointer Address, reception of the incoming packet will be aborted by the ENC. Thus, the packets previously received and still contained in the Ring will not be erased.

In a heavily loaded network environment, the local DMA may be disabled, preventing the DM9008 from buffering packets from the network. To guarantee this will not happen, a software reset must be issued during all Receive Buffer Ring overflows (indicated by the OVW bit in the ISR). The following procedure is used to recover from a Receiver Buffer Ring Overflow.

1. Issue the STOP mode command (Command Register=21H). DM9008 may not immediately enter the STOP mode. If it is currently processing a packet, ENC will enter STOP mode only after finishing the packet. DM9008 indicates that it has entered STOP mode by setting the RST bit in theInterrupt Status Register.

2. Clear the Remote Byte Counter Registers (RBCR0, RBCR1). The DM9008 requires these registers to be cleared before it sets the RST bit.

3. Poll the Interrupt Status Register for the RST bit. When set, the ENC is in Stop mode.

4. Place DM9008 in LOOPBACK (mode 1 or 2) by writing 02H or 04H to the Transmit Configuration Register. This step is required to properly enable DM9008 to be used on an active network.

5. Issue the START mode command (Command Register=22H). The local receive DMA is still inactive because DM9008 is in LOOPBACK.

6. Remove at least one packet from the Receive Buffer Ring to accommodate additional incoming packets.

7. Take DM9008 out of LOOPBACK by programming the Transmit Configuration Register to its original and resume normal operation.

Note: If the Remote DMA channel is not used, step 6 may be eliminated and packets can be removed from the Receive Buffer Ring after step 1. This will reduce or eliminate the polling time incurred in step 3.

End of Packet Operations

At the end of the packet, DM9008 determines whether the received packet is to be accepted or rejected. It branches either to a routine to store Buffer Header, or to another routine that recovers the buffers used to store the packet.

Successful Reception

If the packet is successfully received, the DMA is restored to the first buffer used to store the packet (pointed to by CURR). The DMA then stores the Receive Status, a pointer indicating where the next packet will be stored, and the number of received bytes. Note that the remaining bytes in the last buffer are discarded and reception of the next packet begins on the next empty 256 byte buffer boundary. CURR is then initialized to the next available buffer in the Buffer Ring.

Buffer Recovery for Rejected Packets

If the packet is a runt packet or contains CRC or Frame Alignment errors, it is rejected. The buffer management logic resets the DMA back to the first buffer page used to store the packet (pointed to by CURR), recovering all buffers that had been used to store the rejected packet. This operation will not be performed if DM9008 is programmed to accept either runt packets or packets with CRC or Frame Alignment errors. The received CRC is always stored in buffer memory after the last byte of data for the packet is received.

Error Recovery

If the packet is rejected, DM9008 resotres DMA by reprogramming the DMA starting address pointed to by CURR.

Removing Packets from the Ring

Packets are removed from the ring using either the Remote DMA or an external device. When the Remote DMA is used, the Send Packet command can be used. This programs the Remote DMA to automatically remove the received packet pointed to by the Boundary Pointer. At the end of the transfer, DM9008 moves the Boundary Pointer, freeing additional buffers for reception. The Boundary Pointer can also be moved manually by programming BNRY. Care should be taken to keep BNRY at least one buffer behind CURR.

Storage Format for Received Packets

The following diagrams describe the format used by the local DMA channel for placing received packets into memory. These modes are selected in the Data Configuration Register (DCR).

D15 D8 D7 D0

Next Packet Pointer	Receive Status
Receive Byte Count 1	Receive Byte Count 0
Byte 2	Byte 1

BOS=0, WTS=1 in DCR
This format is used with Series 32000 808X-type processors.

D15 D8 D7 D0

Next Packet Pointer	Receive Status
Receive Byte Count 0	Receive Byte Count 1
Byte 1	Byte 2

BOS=1, WTS=1 in DCR
This format is used with 68000-type processors.

D7 D0

Receive status
Next Packet Pointer
Receive Byte Count 0
Receive Byte Count 1
Byte 1
Byte 2

BOS=0, WTS=0 in DCR
This format is used with general 8-bit CPUs.
For compatibility with the NE2000 and NE1000, it is essential to program DCR with BOS=0.

Packet Transmission

The local DMA is also used during transmission of a packet. Three registers control the DMA transfer during transmission: a Transmit Page Start Address Register (TPSR) and the Transmit Byte Count Registers (TBCR0, 1). When the DM9008 receives a command to transmit the packet pointed to by these registers, buffer memory data will be moved into the FIFO as required during transmission. DM9008 will generate and append the preamble, Synch and CRC fields.

Transmit Packet Assembly

DM9008 requires a contiguous assembled packet with the format shown. The transmit byte count includes the Destination Address, Source Address, Length of Field and Data. It does not include preamble and CRC. When fewer than 46 bytes are transmitted, the packet must be padded to the minimum size of 64 bytes. The programmer is responsible for adding and stripping pad bytes.

DESTINATION ADDRESS	6 bytes
SOURCE ADDRESS	6 bytes
TYPE LENGTH	2 bytes
DATA	≥ 64 bytes
PAD (IF DATA < 46 BYTES)	

Prior to transmission, TPSR and TBCR0, TBCR1 must be initialized. To initiate transmission of the packet, the TXP bit in the Command Register is set. The Transmit Status Register (TSR) is cleared and DM9008 begins to transmit data from memory (unless the ENC is currently receiving). If the interframe gap has timed out, ENC will begin transmission.

Collision Recovery

During transmission, Buffer Management logic monitors the transmit circuitry to determine whether a collision has occurred. If a collision is detected, the Buffer Management logic will reset the FIFO and restore the Transmit DMA pointers for retransmission of the packet. The COL bit will be set in TSR and NCR (Number of Collisions Register) will be incremented. If 15 successive retransmissions each result in a collision, the transmission will be aborted and the ABT bit in TSR will be set.

Note: NCR reads as all zeroes if excessive collisions are encountered.

Transmit Packet Assembly Format

The following diagrams describe the format for assembling packets prior to transmission for different byte ordering schemes. The various formats are selected in the DCR.

D15 D8 D7 D0

DA1	DA0
DA3	DA2
DA5	DA4
SA1	SA0
SA3	SA2
SA5	SA4
T/L1	T/L0
DATA1	DATA0

BOS=0, WTS=1 in DCR
This format is used with Series 32000 808X-type processors.

D15 D8 D7 D0

DA0	DA1
DA2	DA3
DA4	DA5
SA0	SA1
SA2	SA3
SA4	SA5
T/L0	T/L1
DATA0	DATA1

BOS =1, WTS = 1 in DCR
This format is used with 68000-type processors.

D7 D0

DA0
DA1
DA2
DA3
DA4
DA5
SA0
SA1

BOS = 0, WTS = 0 in DCR
This format is used with general 8-bit CPUs.

Loopback Diagnostics

Three forms of local loopback are provided on the DM9008. The user has the ability to loop back through the deserializer on the ENC, through the ENA, and to the co-ax to check the link via the transceiver circuitry. Because of the half duplex architecture of DM9008, loopback testing is a special mode of operation.

Restrictions During Loopback

The FIFO is split into two halves. The first half is used for transmission, the second for reception. Because only 8-bit fields can be fetched from memory, two tests are required for 16-bit systems to verify the integrity of the entire data path. Only the last 8 bytes of the loopback packet are retained in the FIFO. These 8 bytes can be read through the FIFO register, which will advance through the FIFO to allow the receive packet to be read sequentially.

When DM9008 is in word-wide mode with Byte Order Select set, the loopback packet must be assembled in the even byte locations, as shown below. (The loopback only operates with byte wide transfers.)

LS BYTE	MS BYTE
	DESTINATION
	SOURCE
	LENGTH
	DATA
	CRC

WTS = 1 BOS=1 in DCR

When the device is in word-wide mode with Byte Order Select low, the following format must be used for loopback.

LS BYTE	MS BYTE
DESTINATION	
SOURCE	
LENGTH	
DATA	
CRC	

WTS = 1 BOS=0 in DCR

Note: When loopback is used in word mode, 2n bytes must be programmed in TBCRO, 1, where n=actual number of bytes assembled in even or odd locations.

To initiate a loopback, the user first assembles the loopback packet, then selects the type of loopback using TCR bits LB0, LB1. TCR must also be set to enable or disable CRC generation during transmission. The user then issues a normal transmit command to send the packet. During loopback, the receiver checks for an address match. If the CRC bit in the TCR is set, the receiver will also check the CRC. The last 8 bytes of the loopback packet are buffered and can be read out of the FIFO using the FIFO read port.

Loopback Modes

Mode 1: Loopback through the controller (LB1 = 0, LB0 =1).

If the loopback is through the ENC, the serializer is simply linked to the deserializer, and the receive clock is derived from the transmit clock.

Mode 2:Loopback through the ENA (LB1 = 1, LB0 = 0).

Mode 3: Loopback to Coax (LB1 = 1, LB0 =1).

Packets can be transmitted to the co-ax in loopback mode to check all of the transmit and receive paths, as well as the co-ax itself.

Note:It is not possible to switch directly between the loopback modes, necessitating return to normal operation (00H) in order to change modes.

Reading the Loopback Packet

The last eight bytes of a received packet can be examined by 8 consecutive reads of the FIFO register. The FIFO pointer is incremented after the rising edge of the PC read strobe by internally synchronizing and advancing. If the pointer has not been incremented by the time the PC reads the FIFO register again, DM9008 will insert wait states.

Alignment of the Received Packet in the FIFO

Reception of the packet in the FIFO begins at location zero. After the FIFO pointer reaches the last location in the FIFO, the pointer wraps to the top of the FIFO, overwriting the previously received data. This process continues until the last byte is received. The ENC then appends the received byte count in the next two locations of the FIFO. The value of the next FIFO location is 0. The number of bytes used in the loopback packet determines the alignment of the packet in the FIFO. The alignment for a 64-byte packet is shown below.

FIFO LOCATION	FIFO CONTENTS
0	LOWER BYTE COUNT
1	UPPER BYTE COUNT
2	0
3	LAST BYTE
4	CRC1
5	CRC2
6	CRC3
7	CRC4

For the following alignment in the FIFO, the packet length should be (N x 8) + 5 bytes. Note that if the CRC bit in TCR is set, CRC will not be appended by the transmitter. If CRC is appended by the transmitter, the last four bytes, bytes N-3 to N, will correspond to the CRC.

FIFO LOCATION	FIFO CONTENTS
0	BYTE N-4
1	BYTE N-3 (CRC1)
2	BYTE N-3 (CRC2)
3	BYTE N-3 (CRC3)
4	BYTE N (CRC4)
5	LOWER BYTE COUNT
6	UPPER BYTE COUNT
7	0

Bus Arbitration and Timing

DM9008 powers up as a bus slave in the Reset state, in which the receiver and transmitter are both disabled. The reset state can be reentered under three conditions: soft reset (Stop Command) hard reset (RST input or PC RESET por command), or an error that shuts down the receiver or transmitter (FIFO underflow or overflow, receive buffer ring overflow). After initialization of registers, DM9008 is issued a Start Command, causing it to enter idle state. Until the DMA is required, DM9008 remains idle. Idle state is exited by a request from FIFO in the case of a receive, transmit or a request from the remote DMA in the case of a remote DMA operation.

After the remote or local DMA transfer is completed, DM9008 again enters the idle state.

FIFO Burst Control

All local DMA transfers are burst transfers. Once the DMA is activated, it will transfer an exact burst of bytes programmed in the DCR. If there are remaining bytes in the FIFO, the next burst will not be initiated until the FIFO threshold is exceeded.

Interleaved Local Operation

If a remote DMA transfer is initiated or in progress when a packet is being received or transmitted, the remote DMA transfer will be interrupted for higher priority local DMA transfers. When the local DMA transfer is completed, the remote DMA will rearbitrate for the bus and continue its transfers. Note that if the FIFO requires service while a remote DMA is in progress, the local DMA burst is appended to the remote transfer.

Remote Read Timing

1) The DMA reads a byte/word from local buffer memory and writes the byte/word into the latch, increments the DMA address, and decrements the byte count (RBCR0, 1).
2) If the byte from local buffer memory is not available, IOCHRDY will be pulled low to insert wait states to the PC. The IOCHRDY is inactive when the byte is available.
3) When the system reads the port, the read strobe ($\overline{IOR}$) is used as an acknowledge by the remote DMA.

Steps 1-3 are repeated until the remote DMA is finished.

Note that if a local DMA is in progress, the remote DMA is held off until the local DMA is finished.

Remote Write Timing

A Remote Write operation transfers data from the I/O port to the local buffer RAM. The system transfers a byte/word to the latch via $\overline{IOW}$, and this write strobe is detected by the ENC. The remote DMA then holds off further transfers into the latch until the current byte/word has been transferred from the latch, after which the next transfer can begin.

1) The system writes a byte/word into the latch. If DM9008 is not ready to accept the byte/word, IOCHRDY will be pulled low to insert wait states into the PC. IOCHRDY is inactive when the byte/word is accepted by DM9008.
2) The remote DMA reads the contents of the port and writes the byte/word to local buffer memory, increments the address, and decrements the byte count (RBCR0, 1).

Steps 1-2 are repeated until the remote DMA is finished.

Slave Mode Timing

When the PC reads or writes any internal registers of DM9008, DM9008 becomes a bus slave. All register accesses are byte-wide. The PC accesses internal registers with four address lines, SA0-SA3, and $\overline{IOR}$ and $\overline{IOW}$ strobes. Since DM9008 may be a local bus master when the PC attempts to read or write to DM9008, or attempts to read Boot-ROM data, IOCHRDY will be pulled low to hold off the PC until DM9008 leaves master mode.

Boot-ROM Data Read

The Boot-ROM data pins are connected to Memory Data pins MD0-7. DM9008 transfers these data to SD0-7 if the PC activates a memory read operation with the address in the range of the Boot-ROM address space.

Hardware Reset

DM9008 will be reset if RST is high. The ENC module can also be reset when the PC reads the RESET port, followed by an IOW operation.

The following bits will be cleared or set when DM9008 is reset.

Register	Reset Bits	Set Bits
CR	TXP, STA	RD2, STP
ISR		RST
IMR	D0 - D6	
DCR		LAS
TCR	LB1, LB0	

Functional Description

TPMAU Function

TPMAU receives transmit data and transfers the data to the TP network. The input must be transformer-coupled to the AUI circuit. The receiver is able to pass differential signals as small as 300 mV peak and as large as 1315 mV. DC biasing is provided with internal common mode, set to nominal 2.5V. An internal analog delay line is used to generate the pre-distortion signals. A delay lock loop, referencing the CLOCK INPUT, is used to generate the internal delay line. All TP output driver pins are driven low in response to any of the following: there is an AUI IDL pulse of at least 200ns duration; the output driver is jabbered; there is a link failure; or an IDL pulse is not detected at the end of a packet and the input does not exceed the detection threshold of 500±100ns. When the driver detects that it has finished sending an IDL pulse to the TP, a timer of not more than 500ns is activated.

Receive Function

The TP receiver is connected to a band-limiting filter whose input is transformer-coupled to the twisted-pair TPRX+/TPRX pins. The receiver is able to resolve differential signals as small as 350mV peak. Common mode input voltage is provided with internal common mode, with the common mode set to nominal 2.5V. The receiver squelch circuit prevents noise on the twisted-pair cable from falsely triggering the receiver in the absence of true data. The receiver will not be activated for signals when the buffer input has a peak amplitude below 300mV, a continuous frequency below 2 MHz, or a single cycle duration within the pass band of the receive filter. The current through the load results in an output voltage between ±0.6V and ±1.2V, measured differentially between the two pins. When the driver detects that it has finished sending an IDL pulse to the AUI, a timer of not more than 500ns is activated. While this timer is active, activity on the TPRX+/TPRX- inputs is ignored, and the AUI driver discharges the current stored in the inductive load.

Collision Function

A collision state exists whenever valid inputs to the TPMAU from the network and from the DTE are received simultaneously, and the device is not in a link-integrity failure state. The TPMAU reports collisions to the AUI by sending a 10 Mhz signal. The collision report signal is sent out no more than 9 bit times (BT) after the chip detects a collision. If TPRX+/TPRX- become active while there is activity on the transmission pair, the loopback data on TPRX+/TPRX- switches from transmit mode to receive mode within 13±3BT. If a collision condition exists with TPRX+/TPRX- having gone idle while transmission pair is still active, SQE continues for 7±2BT. If a collision condition exists with a transmission pair having gone idle while TPRX+/TPRX are still active, SQE may continue for up to 9 BT.

Jabber Function

Jabber is a self-interrupt function that keeps a damaged node from continuously transmitting to the network. The chip contains a nominal window of 50 ms, during which time a normal data link frame can be transmitted. If a frame length exceeds this duration, the jabber function inhibits transmission and sends a collision signal over the collision pair. When activity on the transmission pair has ceased, the chip continues to present the CS0 signal to the collision pair for 0.5s±0.25s. The transmission of link-integrity pulses from the TP drivers is not inhibited when the TPMAU is jabbed and the link integrity function is enabled.

SQE Test Function

When the TPMAU transmission pair has gone idle after a successful transmission and the heartbeat function is enabled, the chip presents the CS0 signal to the collision pair. After a successful transmission to the network media, the chip presents the CS0 signal within 11±5BT of the time activity on the transmission pair has ceased. The CS0 signal is presented for 10±5BT, after which the chip presents an IDL on the collision pair and returns to the idle state.

Link Integrity Function

In the absence of receive traffic, the twisted-pair receiver on the chip can detect periodic link-integrity pulses. A link-integrity pulse is a 100ns high signal with pre-distortion followed by a return to idle. The chip provides a link-integrit reception window, during which a link pulse is expected in the absence of receive traffic. The link-integrity window nominally opens 6.5ms after the receipt of either a link-integrity pulse or the end of a data frame. The window closes nominally 104ms after the receipt of either a link-integrity pulse or the end of a data frame. If a link pulse is received before the link-integrity reception window opens, it is ignored. If no link-integrity pulse is received while the link-integrity reception window is open, a link failure occurs. The chip's transmit, loopback, and receive functions are disabled. If a link-integrity pulse or receive traffic is received while the link-integrity reception window is open, the timers involved are reset. Once the TPMAU has detected a link failure, one of two events must occur before TPMAU re-enables transmission and reception of data:

1) Reception of two consecutive link-integrity pulses that both fall within the link-integrity reception window and are separated by at least a nominal 6.5ms.
2) Reception of a data packet from the twisted pair. With either of these events, TPMAU enters a wait state and continues to disable loopback, transmit and receive functions.

This continues until TPMAU determines that there is no traffic going in either the transmit or receive direction, at which time it enters the idle state. TPMAU also transmits link-integrity pulses to the transmit twisted-pair link. In the absence of transmission traffic, a link-integrity pulse is transmitted at a nominal rate of once per 16ms. Link-integrity pulses continue to be transmitted when part of the chip is jabbed by the watchdog timer, or when there is link-integrity failure.

Auto-Polarity Detection and Correction Functions

TPMAU can determine if the twisted-pair receiver has been wired with polarity reversal. If so, TPMAU automatically corrects for this error condition when the correction function is enabled. When enabled and in the normal state, TPMAU activates this function to determine if the receive wires are reversed. TPMAU examines either an IDL pulse at the end of each receive packet or a link pulse when the link integrity function is enabled. It uses this information to sense the polarity. If TPMAU determines that the incoming IDL pulse is of the proper polarity, it remains in the normal state. If TPMAU detects two consecutive reverse IDL pulses or four reverse link pulses, it enters the reverse state. If TPMAU determines that the polarity of the link is reversed, it internally corrects for the polarity, ensuring that all subsequent packets sent to the AUI have the correct polarity.

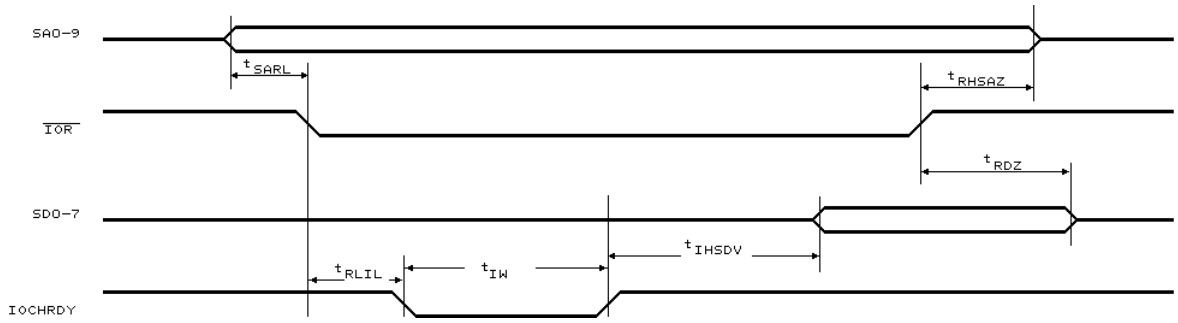
Automatic AUI and RJ45 Connector Selection Functions

The chip provides the designer of a 10BASE-T Ethernet interface card the ability to design a card without having to provide a switch or jumper array that alternates between the AUI and twisted-pair connections. The TPMAU provides automatic changeover whenever the external cable connection is changed.

Power-Down Mode Function

The power-down function is ideal for embedded laptop computer applications. In power-down mode, i.e., when TPMAU is not selected, it pulls within 10μA. When the device is reactivated from power-down mode, normal transceiver operation will resume after the 3.2ms calibration sequence is completed.

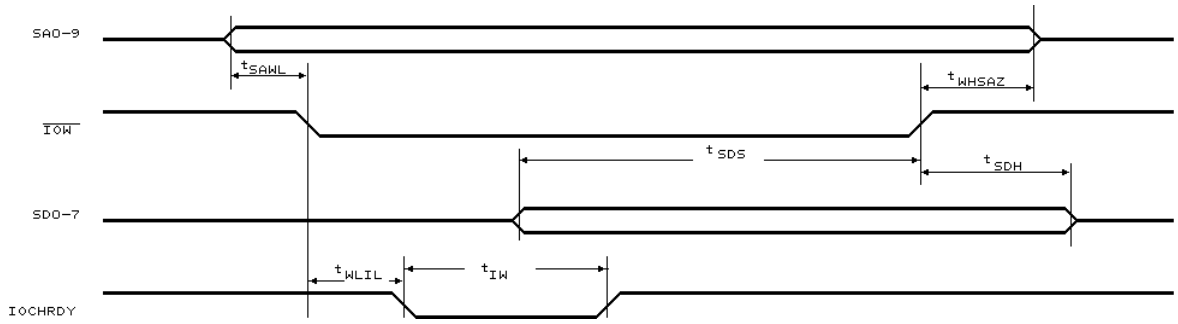
Timing Specifications:



Register Read Timing

Register Read Timing

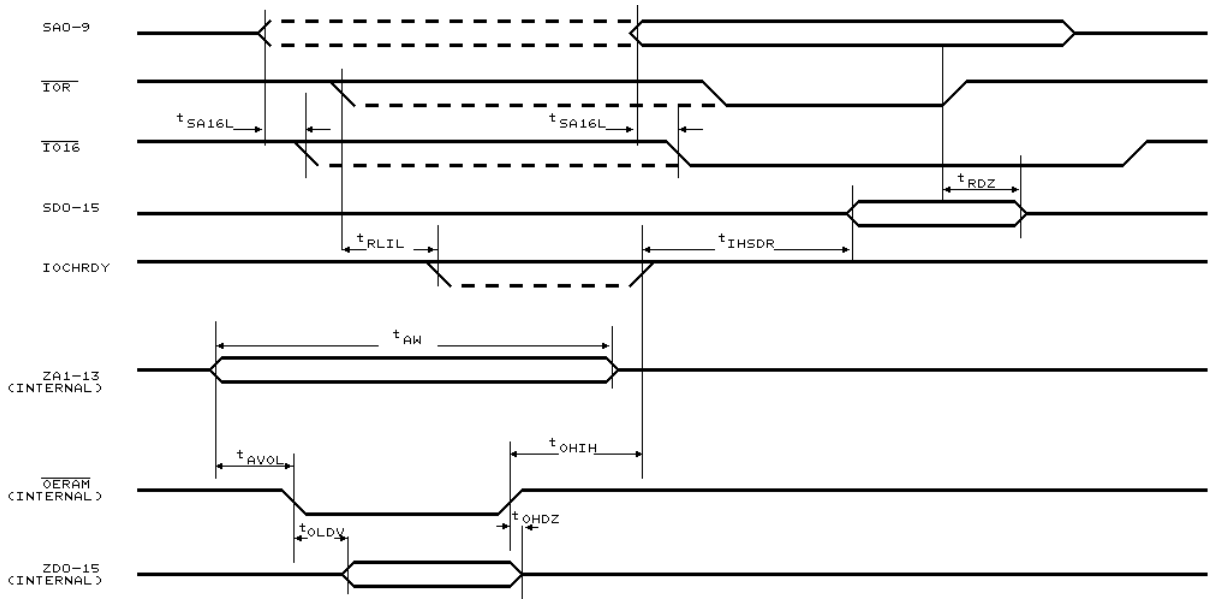
Symbol	Parameter	Min.	Max.	Unit
t_{SARL}	System Address Valid to $\overline{IOR}$ Low	20		ns
t_{RLIL}	$\overline{IOR}$ Low to IOCHRDY Low		20	ns
t_{IW}	IOCHRDY Width	25		ns
t_{IHSDV}	IOCHRDY High to System Data Valid		15	ns
t_{RDZ}	$\overline{IOR}$ High to System Data Tristate	15	70	ns
t_{RHSAZ}	$\overline{IOR}$ High to System Address Invalid	0		ns



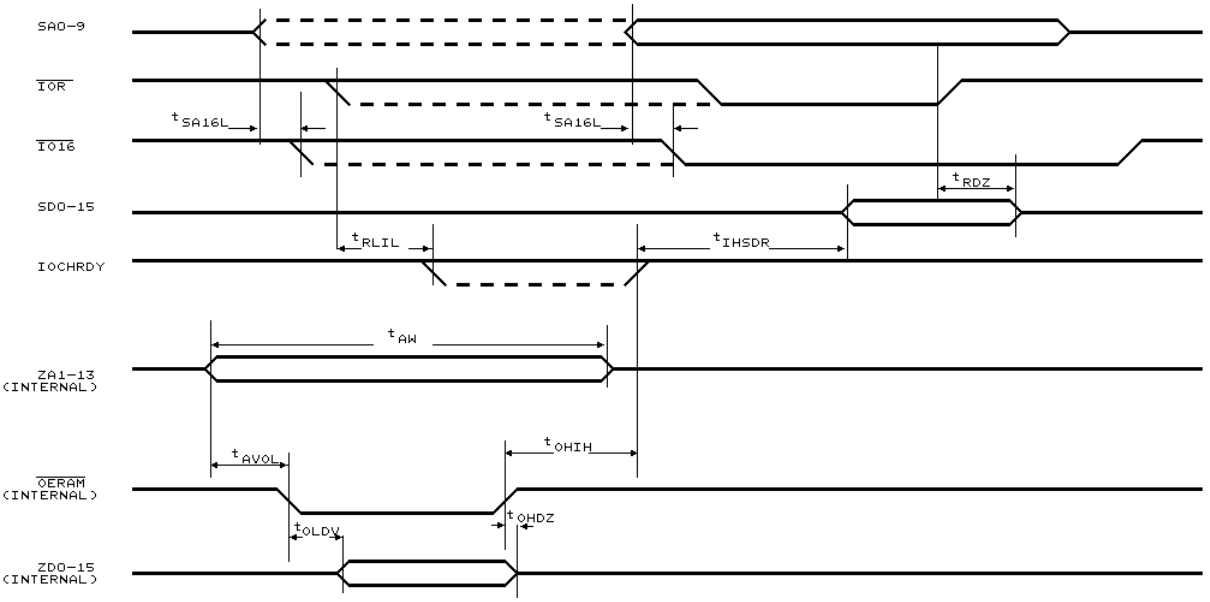
Register Write Timing

Register Write Timing

Symbol	Parameter	Min.	Max.	Unit
t_{SAWL}	System Address Valid to $\overline{IOW}$ Low	20		ns
t_{WLIL}	$\overline{IOW}$ Low to IOCHRDY Low		20	ns
t_{IW}	IOCHRDY Width	25		ns
t_{SDS}	System Data Setup	50		ns
t_{SDH}	System Data Hold	0		ns
t_{WHSAZ}	$\overline{IOW}$ High to System Address Invalid	0		ns



Internal Remote DMA Buffer Memory Read Timing



Internal Remote DMA Buffer Memory Write Timing

Internal Remote DMA Memory Read Timing

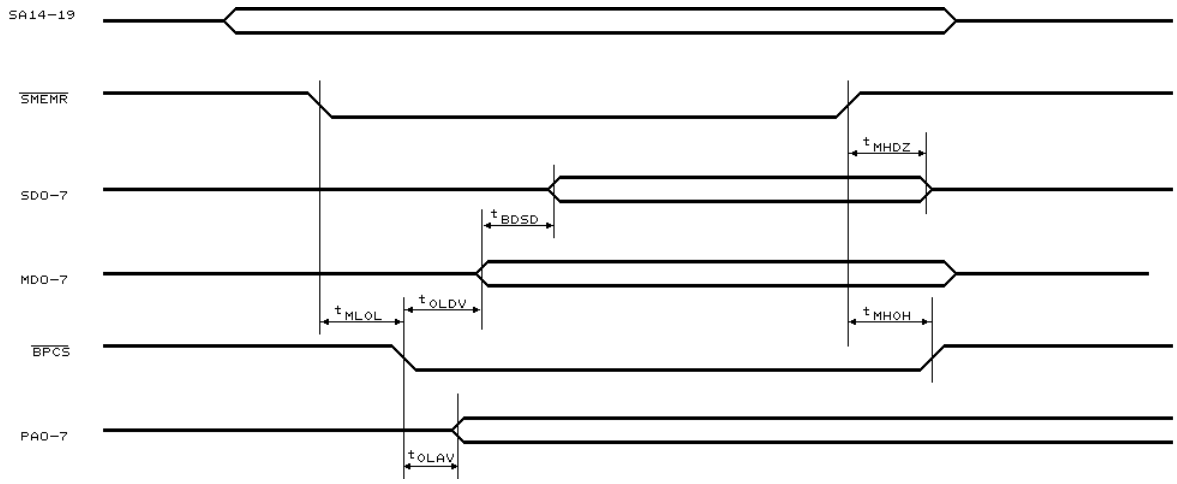
Symbol	Parameter	Min.	Max.	Unit
t_{SA16L}	System Address Valid to $\overline{IO16}$ Low		20	ns
t_{RDZ}	$\overline{IOR}$ High to System Data Tristate	20		ns
t_{IHSDR}	IOCHRDY High to System Data Valid		10	ns
t_{RLIL}	$\overline{IOR}$ Low to IOCHRDY Low (Note 1)		15	ns
t_{OHIH}	$\overline{OERAM}$ High to IOCHRDY High		25	ns
t_{OLDV}	$\overline{OERAM}$ Low to RAM Data Valid		50	ns
t_{OHDZ}	$\overline{OERAM}$ High to RAM Data Tristate	5		ns
t_{OWD}	$\overline{OERAM}$ Width	95	105	ns
t_{AW}	RAM Address Width	195	205	ns
t_{AVOL}	RAM Address Valid to $\overline{OERAM}$ Low		50	ns

Note 1: IOCHRDY will be pulled low if the $\overline{IOR}$ command of the remote DMA is active before DM9008 internal remote DMA read operation is ready.

Internal Remote DMA Memory Write Timing

Symbol	Parameter	Min.	Max.	Unit
t_{SA16L}	System Address Valid to $\overline{IO16}$ Low		20	ns
t_{SDS}	System Data Setup	50		ns
t_{SDH}	System Data Hold	30		ns
t_{WLIL}	IOW Low to IOCHRDY Low (Note 1)		15	ns
t_{IHWL}	IOCHRDY High to $\overline{WERAM}$ Low		25	ns
t_{RDS}	RAM Data Setup	40		ns
t_{RDH}	RAM Data Hold	5		ns
t_{WWD}	$\overline{WERAM}$ Width	95	105	ns
t_{AW}	RAM Address Width	195	205	ns
t_{AVWL}	RAM Address Valid to $\overline{WERAM}$ Low		50	ns

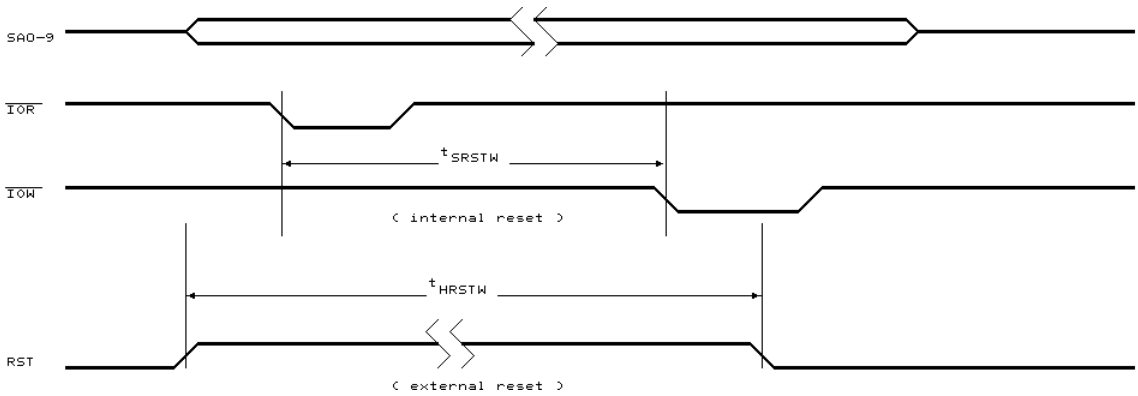
Note 1: IOCHRDY will be pulled low if the $\overline{IOW}$ command of the remote DMA is active before DM9008 internal remot DMA write operation is ready.



Boot-ROM Read Timing

Boot-ROM Read Timing

Symbol	Parameter	Min.	Max.	Unit
t_{MLOL}	$\overline{SMEMR}$ Low to $\overline{BPCS}$ Low		15	ns
t_{MHOH}	$\overline{SMEMR}$ High to $\overline{BPCS}$ High		15	ns
t_{MHDZ}	$\overline{SMEMR}$ High to System Data Tristate		40	ns
t_{BDSD}	Boot-ROM Data to System Data Valid		20	ns
t_{OLDV}	$\overline{BPCS}$ Low to Boot-ROM Data Valid		35	ns
t_{OLAV}	$\overline{BPCS}$ Low to Page Address Valid		10	ns



Reset Timing

Reset Timing

Symbol	Parameter	Min.	Max.	Unit
t_{SRSTW}	Software Reset Pulse Width	1500		ns
t_{HRSTW}	Hardware Reset Pulse Width	205		µs

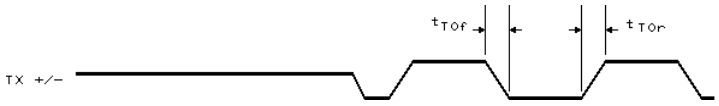
AC Characteristics

Oscillator Specifications

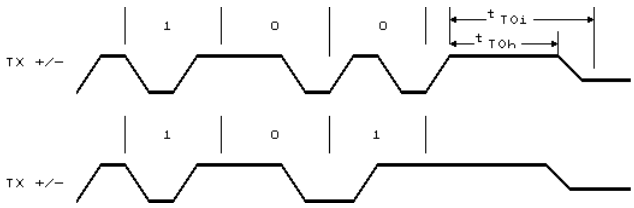
Symbol	Parameter	Min.	Max.	Unit
t_{XTH}	X1 to Transmit Clock High	5		ns
t_{XTL}	X1 to Transmit Clock Low	5		ns

Transmit Specifications (Start of Packet)

Symbol	Parameter	Min.	Max.	Unit
t_{TOr}	Transmit Output Rise Time (20% to 80%)		8	ns
t_{TOf}	Transmit Output Fall Time (80% to 20%)		8	ns
t_{TOj}	Transmit Output Jitter		2	ns
t_{TOh}	Transmit Output High Before Idle (Half Step)		200	ns
t_{TOi}	Transmit Output Idle Time (Half Step)		8000	ns



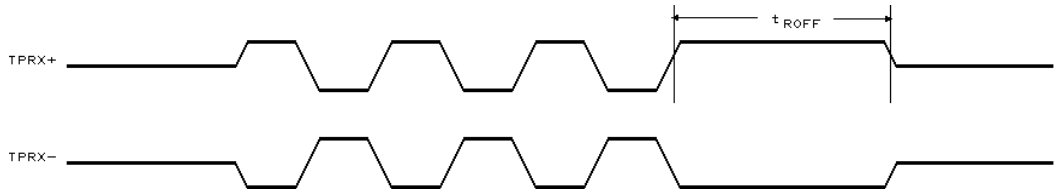
Transmit Start Timing



Transmit End Timing

AC Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
Receive Timing					
t_{ROFF}	TPRX+ high to idle time	200			ns
Link Integrity Timing					
t_{LP}	Transmitted link integrity pulse period	8	16	24	ms
t_{LPWD}	Link integrity pulse width for TPTX±	40	50	60	ns



Receive Timing

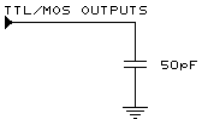


Transmitted Link Integrity Pulse Timing

AC Timing Test Conditions

All specifications are valid only if mandatory isolation is employed and all differential signals are taken to be at the AUI side of the pulse tranformer.

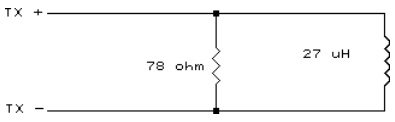
Input pulse level . . . . . GND to 3V
Input rise and fall time 5ns
Input and output reference level (TTL/MOS) 1.3V
Input and output reference level (Diff.) . . . . . .
. . . . . 50% of the differential



Load for Digital Output Pins

Capacitance Ta = 25°C, f = 1MHz

Parameter	Symbol	Typ.	Unit
Input Capacitance	Cin	7	pF
Output Capacitance	Cout	7	pF

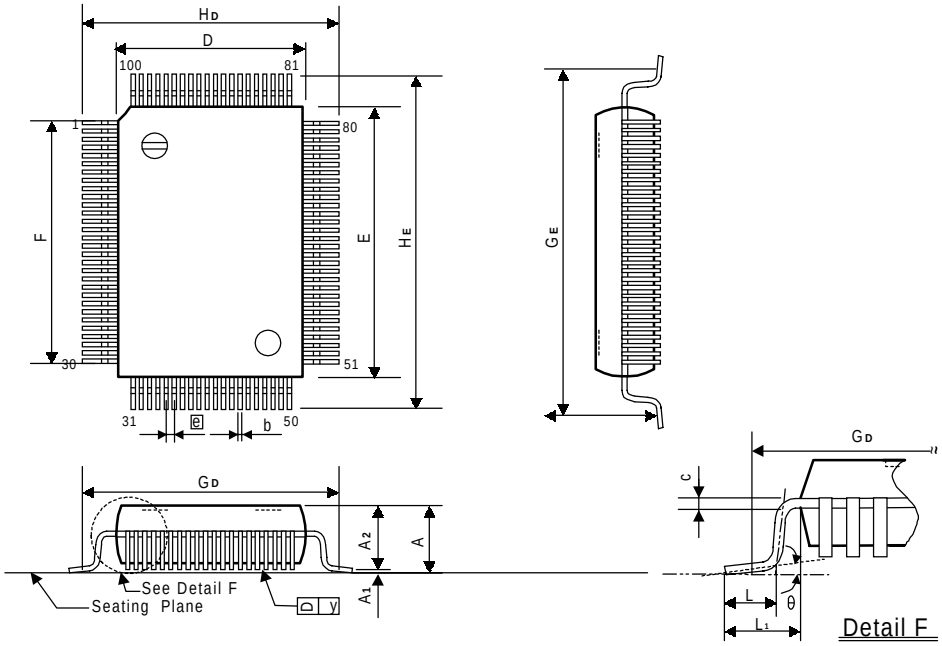


Load for TX± Pins

Package Information

QFP 100L Outline Dimensions

unit: inches/mm

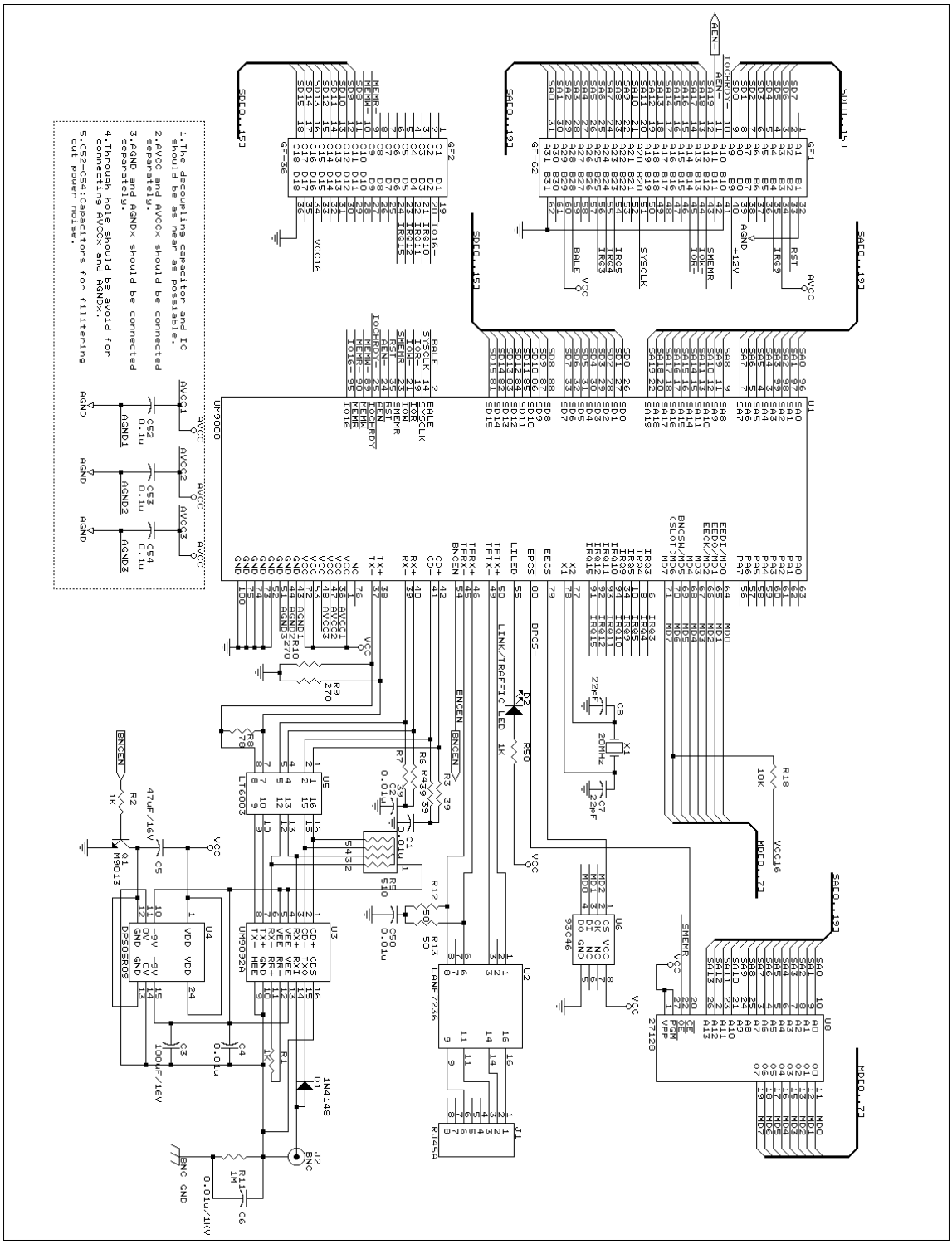


Symbol	Dimensions in inches	Dimensions in mm
A	0.130 Max.	3.30 Max.
A_1	0.004 Min.	0.10 Min.
A_2	0.112 ± 0.005	2.85 ± 0.13
b	0.012 $^{+0.004}_{-0.002}$	0.31 $^{+0.10}_{-0.05}$
c	0.006 $^{+0.004}_{-0.002}$	0.15 $^{+0.10}_{-0.05}$
D	0.551 ± 0.005	14.00 ± 0.13
E	0.787 ± 0.005	20.00 ± 0.13
□ e	0.026 ± 0.006	0.65 ± 0.15
F	0.742 NOM.	18.85 NOM.
G_D	0.693 NOM.	17.60 NOM.
G_E	0.929 NOM.	23.60 NOM.
H_D	0.740 ± 0.012	18.80 ± 0.31
H_E	0.976 ± 0.012	24.79 ± 0.31
L	0.047 ± 0.008	1.19 ± 0.20
L_1	0.095 ± 0.008	2.41 ± 0.20
y	0.006 Max.	0.15 Max.
θ	0° ~ 12°	0° ~ 12°

Notes:
1. Dimensions D&E do not include resin fins.
2. Dimensions G_D & G_E are for PC Board surface mount pad pitch design reference only.

APPENDIX A

1. Application Circuit (for reference only)



2. Oscillator

The oscillator is controlled by a 20 Mhz parallel resonant crystal connected between X1 and X2 or by an external clock on X2. The 20 Mhz output of the oscillator is divided by 2 to generate the 10 MHz transmit clock for the controller. The oscillator also provides internal clock signals to the encoding and decoding circuits.
Note:When X2 is being driven by an external oscillator, X1 MUST be grounded.

Crystal Specifications

Resonant Frequency	20 MHz
Tolerance	±0.001% at 25°C
Stability	±0.0005% at 0°C - 70°C
Type	AT Cut
Circuit	Parallel Resonance
Max. ESR	20Ω
Crystal Load Capacitor	20 pF

The 20 Mhz crystal connection to DM9008 requires special care. The IEEE 802.3 standard requires the transmitted signal frequency to be accurate within ±0.01%. Stray capacitance can shift the crystal's frequency out of range and cause transmitted frequency to exceed its 0.01% tolerance. The frequency marked on the crystal is usually measured with a fixed load capacitance specified in the crystal's data sheet, typically 20 pF.

In order to prevent distortion on the transmitted frequency, the total capacitance seen by the crystal should equal the total load capacitance. For a standard parallel setup, as shown in the diagram below, the 2 load caps C1 and C2 should equal 2(C1) minus any stay capacitances. 2(C1) is equal to the specific load capacity acting in series. Thus the trim capacitors required can be calculated as follows:

C1 = 2XC1 - (Cb1 + Cd1), where Cb1 = Board cap on X1 and Cd1 = X1 dev cap
C2 = 2XC1 - (Cb2 + Cd2), where Cb2 = Board cap on X2 and Cd2 = X2 dev cap

The values of STNIC pins X1 and X2are the region of 5 pF.

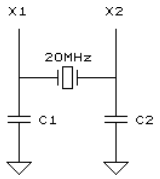


Figure 1.

3. PC Board Layout Considerations

The DM9008 pinout configuration is arranged in accordance with the pin configuration of the ISA-Bus. At the same time, the PC board optimizes layout trace with the larger ground.

Analog Trace Routing

The cardinal rule of analog trace routing is to keep the area enclosed by a circuit loop as small as possible to minimize the incidence of magnetic coupling. This can conflict, however, with the general rule of keeping trace lengths short. For example, if circuit components are positioned along three sides of a square, the best return route is back along the same three sides of the square, NOT directly back along the fourth side. This rule must be adhered to strictly. Furthermore, there should never be an unnecessary via of feed-through inside the circuit loop. This also implies that the circuit loop should never encircle the power/ground planes (i.e., part of the circuit loop above and part below these planes). This concept is illustrated in Figure 2.

A simple case of this guideline applies to differential signal pairs. The two traces of the pair should always be routed in adjacent channels. To reduce capacitive coupling, each circuit loop should be separated from the others. Circuit loops can be separated either by physical space (if located on the same signal layer) or by placement on signal layers on opposite sides of the power/ground planes. The following items should be isolated from each other.

- Receiver path
- Transmit path
- Collision path

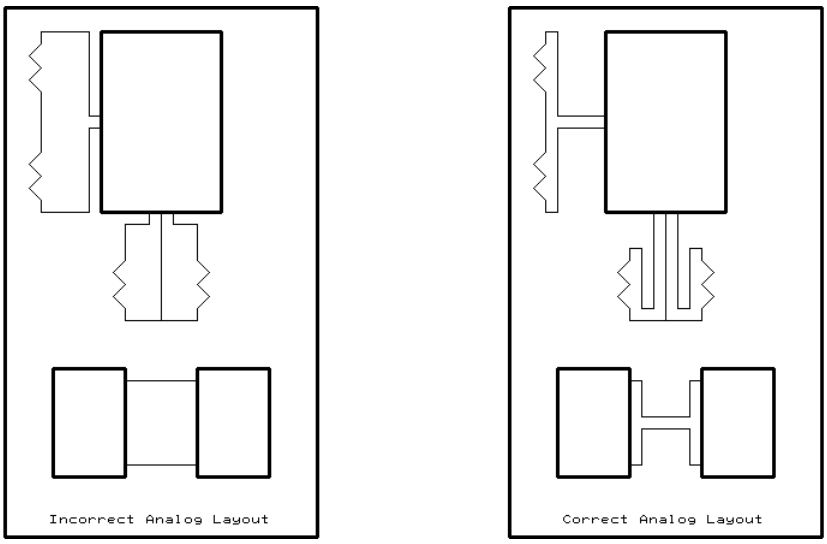
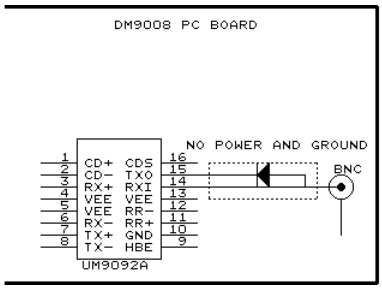


Figure 2.

To protect the transceiver from the environment and to achieve optimum performance, the only layout restriction for the transmitter circuit is that the longest current path from the TXO pin (U3, pin 15) to the coaxial cable's center conductor must be no longer than 4 inches. The layout of the receiver circuit (U3, pin 14), however, is critical to minimize parasitic capacitance that can degrade the received signal. The external receiver circuit should be isolated from power and ground planes.



Digital Trace Routing

Placement of digital components and routing of digital traces should follow standard common-sense digital layout techniques, such as minimizing trace lengths, daisy-chaining bus signals, etc.

APPENDIX B

Plug and Play Function Descriptions

DM9008 Configuration Modes

DM9008 is power-on in jumperless mode.

DM9008's resource configuration information, such as I/O base address, BROM memory base address, interrupt request line, etc., are stored in the CONFIGA-D registers, as well as in the PnP logical device configuration registers. Their power-up default values may come from the contents of 9346 in PnP and DM jumperless modes. Their values can be modified by software via the logical device configuration registers in DM Jumpless and PnP modes. The update values will also be recorded to the CONFIGA-D registers. This new configuration is only valid temporarily, and will be lost after an active PC Hardware Reset. Permanent changes to the configuration must be done by either changing the jumper state or the contents of 9346. Note that the BROM size cannot be modified temporarily.

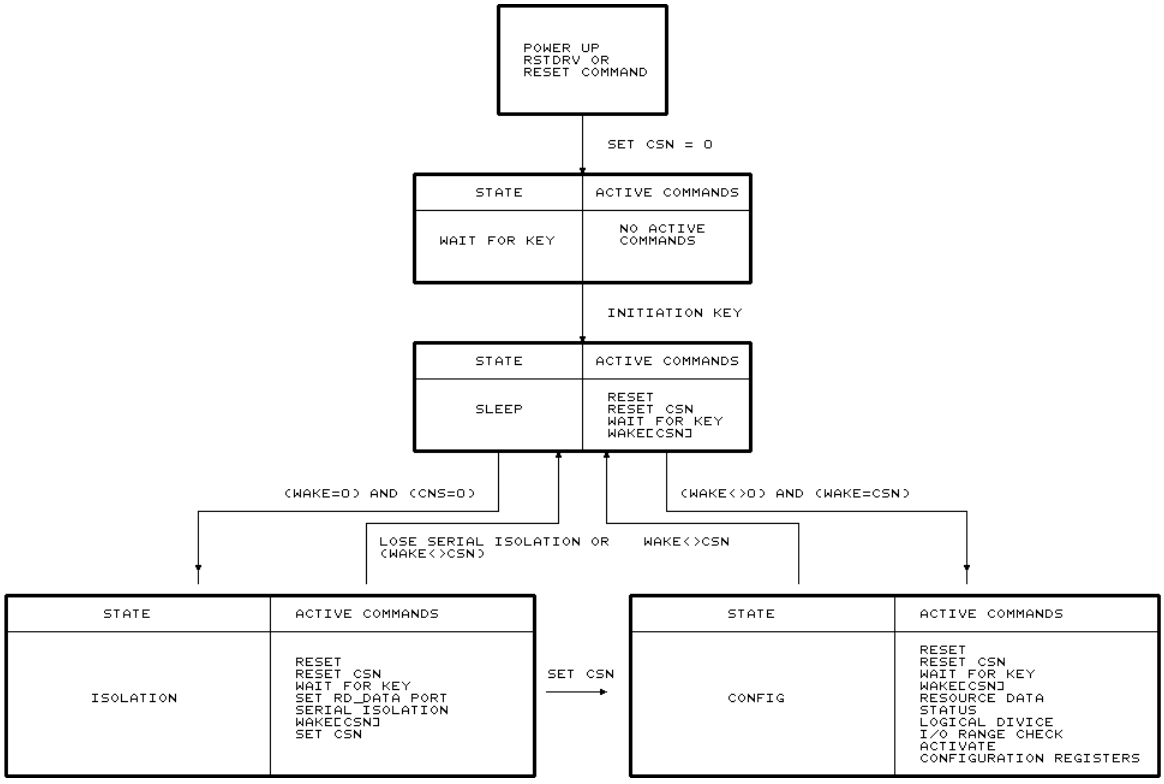
The Plug and Play logic can work in both configuration modes if using a DM, instead of the PnP, Initiation Key. In other words, the DM Initiation Key is supported in all configuration modes, whereas the PnP Initiation key is only supported in PnP mode. By using the DM Initiation Key, the software can put DM9008 in the PnP Config state and access the logical device configuration registers even if DM9008 is in Jumpless mode.

The differences between the 2 configuration modes are shown in the following table.

Configuration Mode	Resource of Power-up Value	Supported Initiation Key
DM Jumperless	9346	DM Initiation Key
Plug and Play	9346	DM and PnP Initiation Key

Plug and Play Isolation Sequence

The Plug and Play isolation sequence is divided into four states: Wait for Key, Sleep, Isolation, and Config states. The state transitions for the Plug and Play ISA card are shown below:



Notes:
1. CSN = Card Select Number.
2. RSTDRV causes a state transition from the current state to Wait for Key and sets all CSNs to zero.
3. The Wait for Key command causes a state transition from the current state to Wait for Key.
4. The Reset CSN commands include PnP Reset, CSN and DM Reset CSN commands.
   The former sets all CSNs of ISA PnP cards to zero, while the latter only sets CSNs of DM9008 PnP cards to zero.
   Neither command will cause a state transition.

Figure 3. Plug and Play ISA Card State Transitions

Contents of EEPROM (93C46) in DM9008

Word	High Byte	Low Byte
00H	Ethernet Addr. 1	Ethernet Addr. 0
01H	Ethernet Addr. 3	Ethernet Addr. 2
02H	Ethernet Addr. 5	Ethernet Addr. 4
03H | 06H	: : :	: : :
07H	57H	57H
08H	42H	42H
09H | 0DH	: : :	: : :
0EH	Config. Reg. B	Config. Reg. A Ý
0FH	Operation Mode *1	Config. Reg. C
10H	Vendor ID byte 1	Vendor ID byte 0
11H	Vendor ID byte 3	Vendor ID byte 2
12H	Serial # byte 1	Serial # byte 0
13H	Serial # byte 3	Serial # byte 2
14H	Resource Data 0	Checksum
15H | 3FH	Plug and Play Resource Data *2	

PS: *1. Operation mode to meet the different reqirement, DM9008 offers three operation mode:
1. Auto-Detection (default): any value except 0X4A and 0X50.
2. Jumpless mode: 0X4A ("J")
3. PnP mode: 0X50 ("P")

*2. For more information on the PnP resource data format, please refer to the Plug and Play ISA sepcification v1.0a.

Introduction to the Plug&Play Function of DM9008

The Plug&Play is a mechanism to provide automatic configuration ability to ISA card in the PC. About the Plug&Play Specification, please reference to "Plug and Play ISA Specification" issued by Intel Corporation and Microsoft Corporation. The DM9008 follows this industry standard to allow Plug&Paly software to program its configuration. The Plug&Play Software includes Windows 95, Intel Plug&Play unilities, Plug&Paly BIOS and etc. For the PC without Plug&Play environment, DM9008 also supports Plug&Play auto-detection facility to solve the configuration disabled problem. So, the DM9008 can work properly in both Plug&Play and Non-Plug&Play computer.

Three Mode Supported by DM9008

To meet the different requirements, DM9008 offers three operation modes. Those modes can be programmed in EEPROM. DM9008 will change the operation mode only when the hardware reset is occurred. Those will be described as follows:

1. Auto-detection mode: DM9008 will detect the PC environment automatically. If the environment without Plug&Play Software executed, DM9008 will set itself to be jumperless mode and the initial configuration is set by EEPROM Otherwise, the DM9008 configuration is programmed by Plug&Play software.

2. Jumperless mode: In this mode, the DM9008 configuration cannot be programmed by Plug&Play software and only decided by EEPROM.

3. Plug&Play mode: The initial configuration for DM9008 is disabled. It needs the Plug&Play Software to program its configuration.

Two Initial Key Software by DM9008

The Initial Key is provided by DM9008 to drive the Plug&Play logic to accept the command. The Initial Key defined by Plug&Play Spec is called as PnP Initial Key. Another Initial Key only defined by DM9008 is called as DM Initial Key. Both of them include a series of writing (32 I/O writes) to the Address Port. The PnP Initial Key will drive all Plug&Play ISA card. The DM Initial Key will effects the DM9008 adapter only.

In the DM9008 design, 2 LED applications may be used.
If 1 LED is used, it will meet the link and traffic LED driver. If TP is link-pass, the pin outputs low for 80ms and then goes into a high impedance state for 50ms to indicate the presence of traffic on the network.
If 2 to 4 LEDS are used, 10K must be connected to pin 67 (MD3) and pull-high.

LED	Pin 55	Pin 56	Pin 57	Pin 58	Notes
1	LINK/TRAFFIC	--	--	--	--
4	LINK	COLLISION	RX	TX	Needs MD3 Pull-high

Ordering Information

Part Number	Pin Count	Package
DM9008F	100	QFP

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