DLPC350 Programmer’s Guide

User's Guide

Literature Number: DLPU010G
May 2013–Revised July 2018

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Read This First

About This Manual

This document specifies the command and control interface to the DLP4500 and DLP4500NIR chipsets. The document defines all applicable commands, default settings, and control register bit definitions to communicate with the DLP4500 and DLP4500NIR chipsets.

Related Documents from Texas Instruments

- DLPC350 Data Sheet: DLP® Digital Controller for DLP4500 and DLP4500NIR DMDs, DLPS029
- DLP4500 Data Sheet: DLP4500 0.45 WXGA DMD, DLPS028
- DLP4500NIR Data Sheet: DLP4500NIR 0.45 WXGA Near-Infrared DMD, DLPS032
- DLPC350 Configuration and Support Firmware, DLPR350

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Interface Protocol

This chapter describes the interface protocol between the DLPC350 and a host processor. The DLPC350 supports two host interface protocols: I²C and USB 1.1 slave interfaces.

1.1 I²C Interface

The DLPC350 controller uses the I²C protocol to exchange commands and data with a host processor. The I²C protocol is a two-wire serial data bus that conforms to the NXP I²C specification, up to 400 kHz(See application note SLVA689 about optimizing I²C bus speed). One wire (SCL) serves as a serial clock, while the second wire (SDA) serves as serial data. Several different devices can be connected together in an I²C bus. Each device is software addressable by a unique address. Communication between devices occurs in a simple master-to-slave relationship.

1.1.1 I²C Transaction Structure

All I²C transactions are composed of a number of bytes, combined in the following order:

START Condition, Slave Address Byte + R/W Bit, Subaddress Byte, N-Data Bytes, STOP Condition

where N in "N-Data Bytes" varies based on the subaddress.

1.1.1.1 I²C START Condition

All I²C transactions begin with a START condition. A START condition is defined by a high-to-low transition on the SDA line, while the SCL line is high.

1.1.1.2 DLPC350 I²C Slave Address

The DLPC350 offers two different 7-bit I²C slave addresses based on the power-up state of the I2C_ADDR_SEL pin. If the I2C_ADDR_SEL pin is low, then the DLPC350 slave address is 0x1A. If the I2C_ADDR_SEL pin is high, then the DLPC350 slave address is 0x1D (
Fixed binary/hex mislabel in Section 2.4.3.4.1).

Table 1-1. I²C Slave Address

PIN	STATE	DLPC350 7-BIT I²C SLAVE ADDRESS
I2C_ADDR_SEL	Low	0x1A
	High	0x1D

The first 8-bit I2C packet includes the 7-bit slave address followed by a read/write bit. A read command to the DLPC350 concatenates the slave address with a 1. A write command to the DLPC350 concatenates the slave address with a 0. Thus, when I2C_ADDR_SEL is low, the first byte packet of an I²C command to the DLPC350 is 0x34 for write and 0x35 for read. When I2C_ADDR_SEL is high, the first byte packet of an I²C command is 0x3A for write and 0x3B for read (
Fixed example in Section 4.4).

Table 1-2. First 8-Bit I2C Packet

7-BIT I²C SLAVE ADDRESS	READ/WRITE BIT	FIRST 8-BIT I²C PACKET	TRANSACTION
0x1A	0	0x34	Write
0x1A	1	0x35	Read

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Table 1-2. First 8-Bit I2C Packet (continued)

7-BIT I²C SLAVE ADDRESS	READ/WRITE BIT	FIRST 8-BIT I²C PACKET	TRANSACTION
0x1D	0	0x3A	Write
0x1D	1	0x3B	Read

1.1.1.3 DLPC350 I²C Subaddress and Data Bytes

The DLPC350 subaddress corresponds to the byte address of the DLPC350 registers shown in Appendix A. Each register address requires a certain number of data bytes, typically four. Thus, a register address is followed by variable length data. These bytes contain the value read or written into this register, with the most significant byte first.

The DLPC350 subaddress contains a read/write bit in the most significant bit position. For read functions, bit 7 is set to 0. For write functions, bit 7 is set to 1. As an example, to read from register 0x06 in the DLPC350, the most significant bit is cleared, resulting in the read subaddress 0x06. To write to register 0x06 in the DLPC350, the most significant bit must be set, resulting in the write subaddress 0x86 (Fixed binary/hex mislabel in Section 2.4.3.4.2).

Table 1-3. Read/Write Subaddressing Example With Register 0x06

TRANSACTION	SUBADDRESS	DATA
Write	0x86	Byte (N-1), Byte (N-2), … , Byte 0
Read	0x06	

1.1.1.4 I²C STOP Condition

All I²C transactions end with a STOP condition. A STOP condition is defined by a low-to-high transition on the SDA line while the SCL line is high.

1.1.2 I²C Read Transaction Sequence

To issue a command to read a DLPC350 value, the host must perform the following steps:

1. Host sends a START condition (shown as S in Figure 1-1) followed by the DLPC350 address with the I²C read/write bit cleared (0x34 or 0x3A).
2. Host sends a subaddress byte that contains the command of the desired DLPC350 function.
3. Host sends a STOP (shown as P in Figure 1-1) condition.
4. Host sends another I²C START condition followed by the DLPC350 address with the I²C read/write bit set (0x35 or 0x3B).
5. Host reads a status byte and checks that bit zero is set. If bit zero is not set, the read transaction repeats until bit zero is set. If bit one is also set, an error occurred. Successful command requests only have bit zero set.
6. Host reads the required bytes for each command.
7. Host issues a STOP condition to terminate the command read access.

1.1.2.1 Example Read Transaction Sequence

An example of a host reading DLPC350's register 4h whose contents are 00h, shown in Figure 1-1, would follow this sequence:

S 34 04 P

S 35 01 00 P

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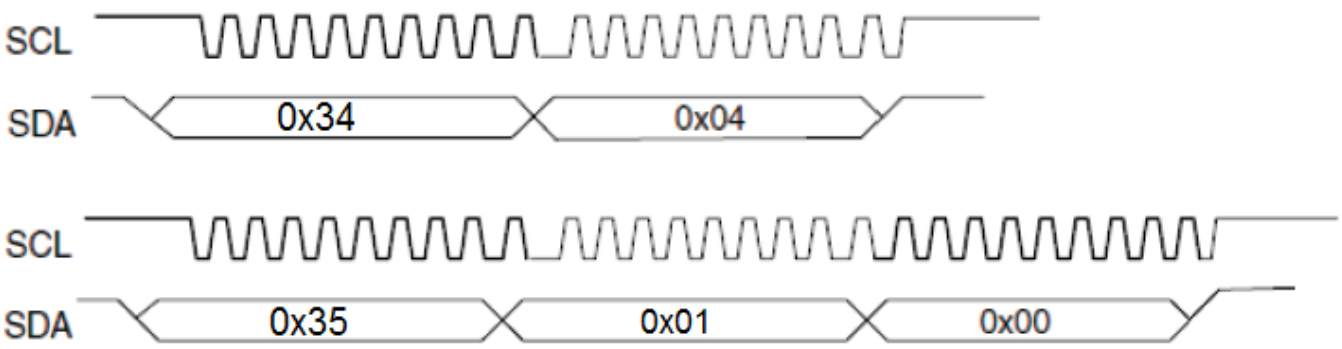

Figure 1-1. I²C Read Register Sequence

1.1.3 I²C Write Transaction Sequence

To issue a command to set a DLPC350 value, the host must perform the following steps:

1. Host sends a START condition (shown as S in Figure 1-2) followed by the DLPC350 address with the I²C read/write bit cleared (0x34 or 0x3A).
2. Host sends a subaddress byte that contains the command of the desired DLPC350 function with the DLPC350 read/write bit set.

NOTE: When in programming mode (see Section A.3 **DLPC350 Programming Commands**), the read/write bit must not be set for the write transactions.

3. Host sends the required bytes for the desired DLPC350 function.
4. Host issues a STOP condition (shown as P in Figure 1-2) to terminate the command write access.
5. (Optional) Read status byte with I²C read/write bit set (0x35 or 0x3B). If bit zero of the status byte is not set, the read transaction repeats until bit zero is set. If bit one is also set, an error occurred. Successful command requests only have bit zero set.

1.1.3.1 Example Write Transaction Sequence

An example of a host writing DLPC350's register 4h with the content 00h, shown in Figure 1-2, would follow this sequence:

S 34 84 00 P

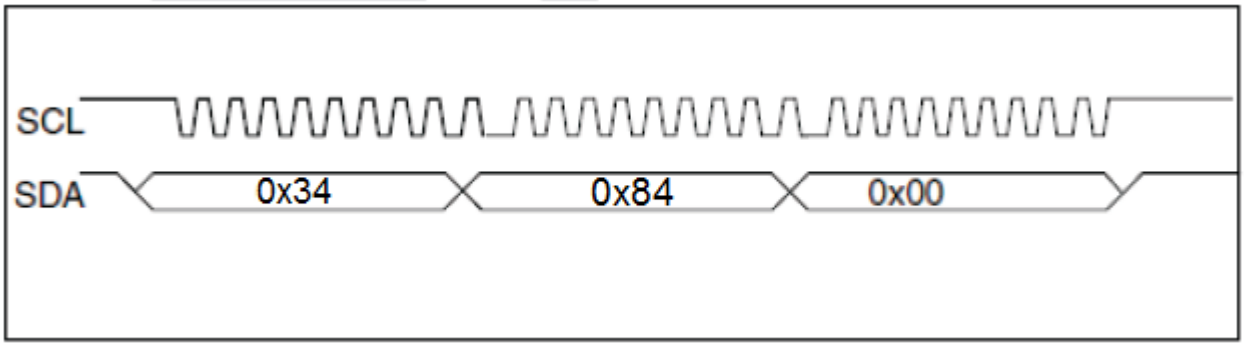

Figure 1-2. I²C Write Register Sequence

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1.2 USB Interface

The DLPC350 controller supports the USB 1.1 human interface device (HID) to exchange commands and data with a host processor. The USB commands are variable length data packets that are sent with the least significant byte first. The DLPC350 offers two different string descriptors for USB enumeration based on whether the I2C_ADDR_SEL pin is high or low. The two strings are 'L', 'C', 'R', '2' or alternatively 'L', 'C', 'R', '3'. The USB Vendor ID (VID) is 0x0451 and the Product ID (PID) is 0x6401.

1.2.1 USB Transaction Sequence

Figure 1-3 shows the structure of the USB 1.1 HID protocol.

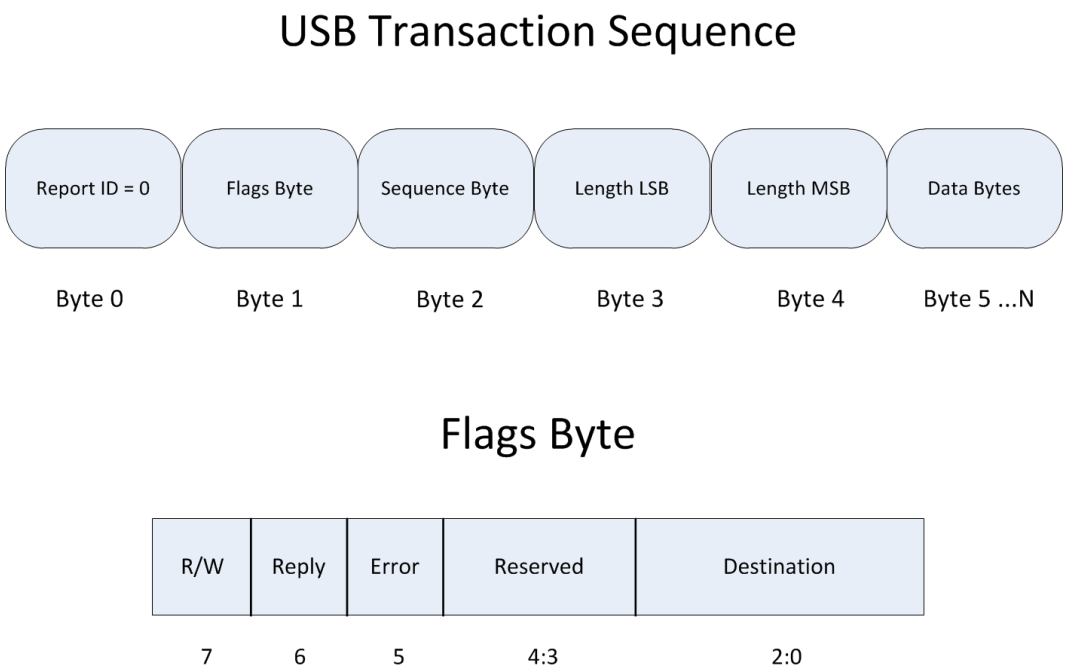

Figure 1-3. USB HID Protocol

1.2.2 USB Read Transaction Sequence

To issue a command to request a DLPC350 value, the host must perform the following steps:

1. Host sends the report ID byte, which is set to 0.
2. Host sends the Flags byte, where:
   - Bits 2:0 are set to 0x0 for regular DLPC350 operation, and is set to 0x7 for debugging assistance
   - Bit 6 is set to 0x1 which indiciates that the host requires a reply from the device
   - Bit 7 is set to 0x1 which indicates a read transaction
3. Host sends the sequence byte. When a single command is more than 64 bytes, the command is sent as multiple USB packets and the sequence byte numbers the packets so the device can assemble them in the right sequence. In other cases, this value is irrelevant and generally set to 0.
4. Host sends two bytes with the length of the data packet. This length denotes the number of data bytes in the packet and excludes the number of bytes in steps 1 through 4. It denotes the total number of bytes sent in steps 5 (command bytes) and 6 (data bytes).
5. Host sends two subcommand bytes: CMD2 and CMD3.
6. Host sends data appropriate to command.
7. After completion of this command, DLPC350 responds with a packet that includes:
   A. Byte with the command requested by the host (the matching sequence byte)

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B. Length of the data packet
C. Requested data

1.2.3 USB Write Transaction Sequence

To issue a command to set a DLPC350 value, the host must perform the following steps:

1. Host sends the report ID byte, which is set to 0.
2. Host sends the flags byte, where
   - Bits 2:0 are set to 0x0 for regular DLPC350 operation, and is set to 0x7 for debugging assistance
   - Bit 6 is set to 0x1 to indicate the host requires a reply from the device. This bit must be set for write transactions only if an acknowledgment or reply is required, which is not typical. For multi-packet transactions, bit 6 must not be set to 0x1 for intermediate packets
   - Bit 7 is set to 0x1 to indicate a read transaction
3. Host sends the sequence byte. When a single command is more than 64 bytes, the command is sent as multiple USB packets and the sequence byte numbers the packets so the device can assemble them in the right sequence. In other cases, this value is irrelevant and generally set to 0.
4. Host sends two bytes with the length of the data packet. This length denotes the number of data bytes in the packet and excludes the number of bytes in steps 1 through 4. It denotes the total number of bytes sent in steps 5 (command bytes) and 6 (data bytes).
5. Host sends two subcommand bytes: CMD2 and CMD3.
6. Host sends data appropriate to command.
7. After completion of this command, DLPC350 responds with a packet that includes a byte with the command requested by the host. This occurs only if bit 6 is set in the flags byte.

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DLPC350 Control Commands

The DLPC350 has two operational modes: normal mode and programming mode. Section A.3 shows the programming mode commands. Normal mode commands do not work while in program mode. This chapter lists the normal mode DLPC350 control commands.

The following sections list the supported control commands of the DLPC350. In the *Type* column, ‘ WR’ type is a writeable field through I^2C or USB write transactions. Data is read through I^2C or USB read transactions for ‘ WR’ type bits. Type *r* is read-only. Write transactions to read-only fields are ignored.

The *Reset* column in all of the following command tables is the default value after power up. These values may be overwritten after power up.

NOTE: **Reserved bits and registers.** When writing to valid command bit fields, all bits marked as unused or reserved must be set to 0, unless otherwise noted.

NOTE: **Momentary Image Corruption During Command Writes**. Certain commands may cause brief visual artifacts in the display image under some circumstances. Command data values may always be read without impacting displayed image. To avoid momentary image corruption due to a command, disable the LEDs prior to the command write, then reenable the LEDs after all commands are issued.

NOTE: **Writing or reading from undocumented registers is NOT recommended**.

2.1 DLPC350 Status Commands

The DLPC350 has the following set of status commands:

- Hardware Status
- System Status
- Main Status
- Retrieve Firmware Version
- Input Video Signal Detection Status

2.1.1 Hardware Status

(**I^2C**: 0x20)

(**USB**: CMD2: 0x1A, CMD3: 0x0A)

The Hardware Status command provides status information on the sequencer of the DLPC350, DMD controller, and initialization.

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Table 2-1. Hardware Status Register

BYTE	BITS	DESCRIPTION	RESET	TYPE
0	0	Internal Initialization	b1	R
		0 = Error		
		1 = Successful		
	1	Reserved	b0	R
	2	DMD Reset Controller Error	b0	R
		0 = No error has occurred		
		1 = Multiple overlapping bias or reset operations are accessing the same DMD block.		
	3	Forced Swap Error	b0	R
		0 = No error has occurred.		
		1 = Forced Swap Error occurred.		
	4	Reserved	b0	R
	5	Reserved	b0	R
	6	Sequencer Abort Status Flag	b0	R
		0 = No error has occurred		
		1 = Sequencer has detected an error condition that caused an abort		
	7	Sequencer Error	b0	R
		0 = No error has occurred.		
		1 = Sequencer detected an error.		

NOTE: Any error condition indicates a fault condition and must be corrected.

2.1.2 System Status

(**I²C**: 0x21)

(**USB**: CMD2: 0x1A, CMD3: 0x0B)

The System Status command provides DLPC350 status on internal memory tests.

Table 2-2. System Status Register

BYTE	BITS	DESCRIPTION	RESET	TYPE
0	0	Internal Memory Test	b1	R
		0 = Internal Memory Test failed		
		1 = Internal Memory Test passed		
	1:7	Reserved	b0	R

2.1.3 Main Status

(**I²C**: 0x22)

(**USB**: CMD2: 0x1A, CMD3: 0x0C)

The Main Status command shows the status of DMD park and DLPC350 sequencer, frame buffer, and gamma correction.

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Table 2-3. Main Status Register

BITS	BITS	DESCRIPTION	RESET	TYPE
0	0	DMD Park Status	b0	R
		0 = DMD micromirrors are not parked		
		1 = DMD micromirrors are parked		
	1	Sequencer Run Flag	b0	R
		0 = Sequencer is stopped		
		1 = Sequencer is running normally		
	2	Frame Buffer Swap Flag	b0	R
		0 = Frame buffer is not frozen		
		1 = Frame buffer is frozen		
	3	Gamma Correction Function Enable	b0	R
		0 = Gamma correction is disabled		
		1 = Gamma correction is enabled		
	4:7	Reserved	b0	R

2.1.4 Retrieve Firmware Version

(**I²C**: 0x11)

(**USB**: CMD2: 0x02, CMD3: 0x05)

This command (**supported in firmware version 2.0.0 and newer**) reads the version information of the DLPC350 firmware.

Table 2-4. Get Version Command

BYTE	BITS	DESCRIPTION	RESET	TYPE
3:0		Application software revision:	x0	R
	15:0	Application software patch number		
	23:16	Application software minor revision		
	31:24	Application software major revision		
7:4		API software revision:	x0	R
	15:0	API patch number		
	23:16	API minor revision		
	31:24	API major revision		
11:8		Software configuration revision:	x0	R
	15:0	Software configuration patch number		
	23:16	Software configuration minor revision		
	31:24	Software configuration major revision		
15:12		Sequencer configuration revision:	x0	R
	15:0	Sequencer configuration patch number		
	23:16	Sequencer configuration minor revision		
	31:24	Sequencer configuration major revision		

2.1.5 Input Video Signal Detection Status

(**I²C**: 0x01)

(**USB**: 0x04, CMD2: 0x07, CMD3: 0x1C)

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When this command (**supported in firmware version 2.0.0 and newer**) is executed, the DLPC350 controller returns the Input Video Signal timing information based the Video Port Selection made through I2C command 0x00 or USB commands 0x1A00. This command is applicable for RGB Parallel Interface and FPD-link interface. On receiving the command the controller monitors the signal for ~ 200 ms before reporting the signal status. This command is used as a debugging aid to detect if the controller reads the resolution correctly, especially in the Pattern Display Mode where the resolution must match the native resolution of 912 × 1140 pixels.

Table 2-5. Input Video Signal detection Status Read Command

BYTE	BITS	DESCRIPTION		RESET	TYPE
0	7:0	**Signal Detection Status**			
		0x00	**Stopped** – Controller is not processing the input video signal	x0	R
		0x01	**Processing** – Controller BUSY detecting the input video signal	x0	R
		0x02	**Detected** – Controller is successfully processed the input source	x0	R
		0x03	**Lock Failed** – Controller couldn't failed to process the video signal	x0	R
2:1	15:0	Horizontal resolution		x0	R
4:3	15:0	Vertical resolution		x0	R
5	7:0	Reserved 0x00		x0	R
6	7:0	**HSYNC Polarity**		x0	R
		0x00 – Negative			
		0x01 – Positive			
7	7:0	**VSYNC Polarity**		x0	R
		0x00 – Negative			
		0x01 – Positive			
11:8	31:0	Pixel clock in (100 × KHz)		x0	R
13:12	15:0	Horizontal frequency (100 × KHz)		x0	R
15:14	15:0	Vertical frequency (100 × Hz)		x0	R
17:16	15:0	Total pixels per line		x0	R
19:18	15:0	Total lines per frame		x0	R
21:20	15:0	Active pixels per line		x0	R
23:22	15:0	Active lines per frame		x0	R
25:24	15:0	First pixel (beginning of active pixel in the line)		x0	R
27:26	15:0	First Line (beginning of active line in the frame)		x0	R

2.2 DLPC350 Programming Commands

The programming commands download a new firmware image into flash memory. This is accomplished with I^2C or USB communication. When operating in normal mode, an enter program mode command can be issued, which exits normal mode and enters program mode. When in program mode, the user must issue the proper exit program mode command to return to normal mode. Normal mode commands do not work while in program mode. See Section A.3 for the list of program mode commands.

2.2.1 Enter Program Mode

(**I^2C**: 0x30)

(**USB**: CMD2: 0x30, CMD3: 0x01)

If the main application receives this command while in normal mode, the controller enters program mode. When called, the main application powers off the illumination system, parks the DMD, and jumps to the boot loader application. If the boot loader receives this command, then the command has no effect.

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Table 2-6. Enter Program Mode Command

BYTE	BITS	DESCRIPTION	RESET	TYPE
0	0	Program Mode	d0	W
		1 = Enter Program Mode – Jump to boot loader		
	7:1	Reserved		

2.3 Chipset Control Commands

The DLPC350 has the following set of control commands:

- Chipset configuration and control
- Interface configuration and control
- Input source control
- Image rotation and flip control
- Image processing control
- LED driver control
- Sleep mode control
- GPIO control

I^2C control commands are accepted in any order, except when special sequencing is required (for example, setting up the flash). Each control command is validated for subaddress and parameter errors as the command is received. Commands failing validation are ignored. On power up, it is required to wait for DLPC350 to complete initialization before sending the device any I^2C or USB transactions. The INIT_DONE pin signals when initialization is complete (see the DLPC350 data sheet, DLPS029).

2.3.1 Chipset Configuration and Control Commands

The Chipset and Configuration Control commands manage software reset, power down modes, buffer freeze, and image curtain display.

2.3.1.1 Software Reset

(**I^2C**: 0x13)

(**USB**: CMD2: 0x08, CMD3: 0x02)

This command issues a software reset to the DLPC350, regardless of the argument that is sent. This command provides a back-up recovery mechanism.

Table 2-7. Software Reset Command

BYTE	BITS	DESCRIPTION	RESET	TYPE
0	0	Software Reset. A set or reset of this bit performs a software reset:	d0	W
		0 or 1 – Perform a software reset		

2.3.1.2 DMD Park/Unpark

(**I^2C**: 0x14)

(**USB**: CMD2: 0x06, CMD3: 0x09)

This command is used to park or unpark the DMD, whenever system is idle user can send this command to park the DMD. By using this command, it will not alter the overall system configuration. For example, if the DLPC350 controller is configured in Pattern Mode, upon sending this command to park the DMD, user need not reconfigure the system after DMD unpark, this command not change the system configuration status.

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Table 2-8. DMD Park/Unpark Command

BYTE	BITS	DESCRIPTION	RESET	TYPE
0	0	0x00 – DMD un-park 0x01 – DMD park	d0	WR

2.3.1.3 Power Control

(**I²C**: 0x07)

(**USB**: CMD2: 0x02, CMD3: 0x00)

The power control places the DLPC350 in a low-power state and powers down the DMD interface. Standby mode must only be enabled after all data for the last frame is transferred to the DLPC350. Standby mode must be disabled prior to sending any new data.

Table 2-9. Interface Sleep Control Command

BYTE	BITS	DESCRIPTION	RESET	TYPE
0	0	Power control	d0	WR
		0 = Normal operation. The selected external source is displayed		
		1 = Standby mode. Places DLPC350 in low-power state and powers down the DMD interface		
	7:1	Reserved	d0	R

2.3.1.4 Buffer Controls

The Buffer Control commands allow buffer swaps, provides the current buffer pointer, and freezes the buffer.

2.3.1.4.1 Force Buffer Swap

(**I²C**: 0x71)

(**USB**: CMD2: 0x1A, CMD3: 0x26)

The Force Buffer Swap command switches between the two internal memory buffers by swapping the read and write pointers. After a buffer swap, the 24 bit-plane buffer that streams data to the DMD is now used for input, while the previous 24 bit-plane input buffer now streams data to the DMD. The buffer must be frozen before executing this command.

Table 2-10. Force Buffer Swap Command

BYTE	BITS	DESCRIPTION	RESET	TYPE
0	0	Buffer swap	d0	WR
		1 - Swap internal memory buffer pointers		
		0 - No change to the internal memory buffer pointers		
	7:1	Reserved	d0	R

2.3.1.4.2 Display Buffer Freeze

(**I²C**: 0x7C)

(**USB**: CMD2: 0x10, CMD3: 0x0A)

The Display Buffer Freeze command disables swapping the memory buffers. When reconfiguring the chipset through a series of commands that change the input source or operating mode, TI recommends the Display Buffer Swap Freeze command to prevent temporary artifacts from reaching the display. When the display buffer is frozen, the last image streamed to the DMD continues to display.

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Table 2-11. Display Buffer Freeze Command

BYTE	BITS	DESCRIPTION	RESET	TYPE
0	0	Display buffer swap freeze	d1	WR
		0 - Enable buffer swapping		
		1 - Disable buffer swapping (freeze display buffer)		

2.3.1.4.3 Buffer Write Disable

(**I²C**: 0x72)

(**USB**: CMD2: 0x1A, CMD3: 0x27)

The Buffer Write Disable command prevents the overwriting of the contents of the 48 bit-planes or two 24-bit frame buffers of the internal memory buffer.

Table 2-12. Buffer Write Disable Command

BYTE	BITS	DESCRIPTION	RESET	TYPE
0	0	Buffer write disable	d0	WR
		1 = Disables writes to all the internal memory buffer		
		0 = Normal operation		
	7:1	Reserved	d0	R

2.3.1.4.4 Current Read Buffer Pointer

(**I²C**: 0x73)

(**USB**: CMD2: 0x1A, CMD3: 0x28)

The Current Read Buffer Pointer command returns the pointer to the current internal memory buffer (this data is streamed to the DMD).

Table 2-13. Current Buffer Pointer Command

BYTE	BITS	DESCRIPTION	RESET	TYPE
0	0	Current read buffer pointer command	d0	WR
		1 = Buffer number 1 is streaming to DMD		
		0 = Buffer number 0 is streaming to DMD		
	7:1	Reserved	d0	R

2.3.1.5 Display Curtain Control

(**I²C**: 0x06)

(**USB**: CMD2: 0x11, CMD3: 0x00)

This register provides image curtain control. When enabled and the input source is set to external video with no video source connected, a solid color field is displayed on the entire DMD display. The Display Curtain Control provides an alternate method of masking temporary source corruption from reaching the display due to on-the-fly reconfiguration. The register is useful for optical test and debug support.

Table 2-14. Display Curtain Control Command

BYTE	BITS	DESCRIPTION	RESET	TYPE
1:0	9:0	Red color intensity in a scale from 0 to 1023	x0	WR
3:2	9:0	Green color intensity in a scale from 0 to 1023	x0	WR
5:4	9:0	Blue color intensity in a scale from 0 to 1023	x0	WR

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2.3.2 Interface Configuration and Control

The Interface Configuration and Control manages the operation of the parallel and FPD-link interfaces.

2.3.2.1 Input Data Channel Swap

(**I²C**: 0x04)

(**USB**: CMD2: 0x1A, CMD3: 0x37)

The Input Data Channel Swap commands configure the specified input data port and map the data subchannels. The DLPC350 interprets channel A as green, channel B as red, and channel C as blue.

Table 2-15. Input Data Channel Swap Command

BYTE	BITS	DESCRIPTION	RESET	TYPE
0	2:0	Swap Parallel Interface Data Subchannel:	x4	WR
		0 - ABC = ABC, No swapping of data subchannels		
		1 - ABC = CAB, Data subchannels are right shifted and circularly rotated		
		2 - ABC = BCA, Data subchannels are left shifted and circularly rotated		
		3 - ABC = ACB, Data subchannels B and C are swapped		
		4 - ABC = BAC, Data subchannels A and B are swapped		
		5 - ABC = CBA, Data subchannels A and C are swapped		
		6 - Reserved		
		7 - Reserved		
	6:3	Reserved	b0	R
	7	Specified Port	b0	WR
		0 - Parallel interface		
		1 - FPD-link interface		

2.3.3 FPD-Link Interface Configuration and Control

The following commands are unique to the FPD-link interface.

2.3.3.1 FPD-Link Mode and Field Select

(**I²C**: 0x05)

(**USB**: CMD2: 0x1A, CMD3: 0x04)

The FPD-Link Mode and Field Select command configures the FPD-link pixel map, polarity, and signal select.

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Table 2-16. FPD-Link Mode and Field Select Command

BYTE	BITS	DESCRIPTION	RESET	TYPE
0	2:0	Field signal select:[1]	x0	WR
		0 = Map FPD- link LVDS output from CONT1 onto field signal for FPD-link interface port (port 2)		
		1 = Map FPD- link LVDS output from CONT2 onto field signal for FPD-link interface port (port 2)		
		2 = Force 0 onto field signal for FPD-link interface port (port 2)		
		3 = Reserved		
	3	Swap polarity	x1	WR
	5:4	Reserved	x0	R
	7:6	FPD-link pixel mapping mode (see Table 2-17)[2]	x1	WR
		0 = Mode 1		
		1 = Mode 2		
		2 = Mode 3		
		3 = Mode 4		

(1) See Table 2-17 for CONT1 and CONT2 mapping.

(2) Pixel mapping mode defines how the FPD-Link LVDS output pixels are mapped into DLPC350 FPD-link interface port (port 2). Table 2-16 lists the mapping of the LVDS parallel data output buses RDA(6:0), RDB(6:0), RDC(6:0), RDD(6:0), and RDE(6:0) into the 30-bit LVDS input port (Port 2:FPD-link interface port of the DLPC350).

Table 2-17. FPD-Link Pixel Mapping Modes

PIXEL	MODE1	MODE2	MODE3	MODE4
Green[9]	RDB4	RDD3	RDE1	RDB4
Green[8]	RDB3	RDD2	RDE2	RDB3
Green[7]	RDB2	RDB4	RDD1	RDB2
Green[6]	RDB1	RDB3	RDD2	RDB1
Green[5]	RDB0	RDB2	RDB4	RDB0
Green[4]	RDA6	RDB1	RDB3	RDA6
Green[3]	RDD3	RDB0	RDB2	0
Green[2]	RDD2	RDA6	RDB1	0
Green[1]	RDE3	RDE3	RDB0	0
Green[0]	RDE2	RDE2	RDA6	0
Red[9]	RDA5	RDD1	RDE1	RDA5
Red[8]	RDA4	RDD0	RDE0	RDA4
Red[7]	RDA3	RDA5	RDD1	RDA3
Red[6]	RDA2	RDA4	RDD0	RDA2
Red[5]	RDA1	RDA3	RDA5	RDA1
Red[4]	RDA0	RDA2	RDA4	RDA0
Red[3]	RDD1	RDA1	RDA3	0
Red[2]	RDD0	RDA0	RDA2	0
Red[1]	RDE1	RDE1	RDA1	0
Red[0]	RDE0	RDE0	RDA0	0
Blue[9]	RDC3	RDD5	RDE5	RDC3
Blue[8]	RDC2	RDD4	RDE4	RDC2
Blue[7]	RDC1	RDC3	RDD5	RDC1
Blue[6]	RDC0	RDC2	RDD4	RDC0
Blue[5]	RDB6	RDC1	RDC3	RDB6
Blue[4]	RDB5	RDC0	RDC2	RDB5
Blue[3]	RDD5	RDB6	RDC1	0
Blue[2]	RDD4	RDB5	RDC0	0

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Table 2-17. FPD-Link Pixel Mapping Modes (continued)

PIXEL	MODE1	MODE2	MODE3	MODE4
Blue[1]	RDE5	RDE5	RDB6	0
Blue[0]	RDE4	RDE4	RDB5	0
DATA_EN	RDC6	RDC6	RDC6	RDC6
VSYNC	RDC5	RDC5	RDC5	RDC5
HSYNC	RDC4	RDC4	RDC4	RDC4
CONT1	RDD6	RDD6	RDD6	RDD6
CONT2	RDE6	RDE6	RDE6	RDE6

2.3.4 Input Source Control

The Input Source Selection determines the input source for the DLPC350 data display.

2.3.4.1 Port Clock Select (for Parallel Port)

(**I²C**: 0x03)

(**USB**: CMD2: 0x1A, CMD3: 0x03)

This command selects the port 1 clock for the parallel interface. For the FPD-Link, the port clock is automatically set to port 2.

Table 2-18. Input Source Selection Command

BYTE	BITS	DESCRIPTION	RESET	TYPE
0	2:0	Select port input clock	x0	WR
		0: Port 1, clock A		
		1: Port 1, clock B		
		2: Port 1, clock C		
	7:3	Reserved	x0	R

2.3.4.2 Input Source Selection

(**I²C**: 0x00)

(**USB**: CMD2: 0x1A, CMD3: 0x00)

The Input Source Selection command selects the input source that is displayed by the DLPC350: 30-bit parallel port, internal test pattern, flash memory, or FPD-link interface.

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Table 2-19. Input Source Selection Command

BYTE	BITS	DESCRIPTION	RESET	TYPE
0	2:0	Select the input source and interface mode:	x0	WR
		0 = Parallel interface with 8-bit, 16-bit, 20-bit, 24-bit, or 30-bit RGB or YCrCb data formats		
		1 = Internal test pattern; I^2C command 0x11 selects the test pattern type.		
		2 = Flash. Images are 24-bit single-frame, still images that are stored in flash and uploaded on command.		
		3 = FPD-link interface		
	5:3	Parallel Interface bit depth	x1	WR
		0 = 30 bits		
		1 = 24 bits		
		2 = 20 bits		
		3 = 16 bits		
		4 = 10 bits		
		5 = 8 bits		
	7:6	Reserved	x0	R

2.3.4.3 Input Pixel Data Format

(**I^2C**: 0x02)

(**USB**: CMD2: 0x1A, CMD3: 0x02)

The input pixel data format command defines the pixel data format input into the DLPC350.

Table 2-20. Input Pixel Data Format Command

BYTE	BITS	DESCRIPTION					RESET	TYPE
0	3:0	Select the pixel data format:	Supported Pixel Formats vs Source Type				d0	WR
			Parallel	Test Pattern	Flash Image	FPD-Link		
		0 - RGB 4:4:4 (30 bit)	Yes	Yes	Yes	Yes		
		1 - YCrCb 4:4:4 (30 bit)	Yes	No	No	No		
		2 - YCrCb 4:2:2	Yes	No	Yes	No		
	7:6	Reserved					x0	R

2.3.4.4 Internal Test Patterns Select

(**I^2C**: 0x0A)

(**USB**: CMD2: 0x12, CMD3: 0x03)

When the internal test pattern is the selected input, the internal test patterns select defines the test pattern displayed on the screen. These test patterns are internally generated and injected into the beginning of the DLPC350 image processing path. Therefore, all image processing is performed on the test images. All command registers must be set up as if the test images are input from an RGB 8:8:8 external source. The resolution of the test pattern must be configured with the Input Display Resolutions commands. Frame rate must be configured with the frame rate commands.

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Table 2-21. Internal Test Patterns Select Command

BYTE	BITS	DESCRIPTION	RESET	TYPE
0	3:0	Internal test pattern select:	x8	WR
		0x0 = Solid field		
		0x1 = Horizontal ramp		
		0x2 = Vertical ramp		
		0x3 = Horizontal lines		
		0x4 = Diagonal lines		
		0x5 = Vertical lines		
		0x6 = Grid		
		0x7 = Checkerboard		
		0x8 = RGB ramp		
		0x9 = Color bars		
		0xA = Step bars		
	7:4	Reserved		

2.3.4.5 Internal Test Patterns Color Control

(**I²C**: 0x1A)

(**USB**: CMD2: 0x12, CMD3: 0x04)

When the internal test pattern is the selected input, the internal test patterns color control defines the colors of the test pattern displayed on the screen. These test patterns are internally generated and injected into the beginning of the DLPC350 image processing path. Therefore, all image processing is performed on the test images. All command registers must be set up as if the test images are input from an RGB 8:8:8 external source. The foreground color setting affects all test patterns. The background color setting affects test patterns that have a foreground and background component, such as horizontal lines, diagonal lines, vertical lines, grid, and checkerboard.

Table 2-22. Internal Test Patterns Color Control Command

BYTE	BITS	DESCRIPTION	RESET	TYPE
1:0	9:0	Red Foreground Color intensity in a scale from 0 to 1023	x3FF	WR
		0x0 = No Red Foreground color intensity		
		—		
		0x3FF = Full Red Foreground color intensity		
3:2	9:0	Green Foreground Color intensity in a scale from 0 to 1023	x3FF	WR
		0x0 = No Green Foreground color intensity		
		—		
		0x3FF = Full Green Foreground color intensity		
5:4	9:0	Blue Foreground Color intensity in a scale from 0 to 1023	x3FF	WR
		0x0 = No Blue Foreground color intensity		
		—		
		0x3FF = Full Blue Foreground color intensity		
7:6	9:0	Red Background Color intensity in a scale from 0 to 1023	x0	WR
		0x0 = No Red Background color intensity		
		—		
		0x3FF = Full Red Background color intensity		
9:8	9:0	Green Background Color intensity in a scale from 0 to 1023	x0	WR
		0x0 = No Green Background color intensity		
		—		
		0x3FF = Full Green Background color intensity		

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Table 2-22. Internal Test Patterns Color Control Command (continued)

BYTE	BITS	DESCRIPTION	RESET	TYPE
11:10	9:0	Blue Background Color intensity in a scale from 0 to 1023	x0	WR
		0x0 = No Blue Background color intensity		
		—		
		0x3FF = Full Blue Background color intensity		

2.3.4.6 Load Image

(**I²C**: 0x7F)

(**USB**: CMD2: 0x1A, CMD3: 0x39)

This command loads an image from flash memory and then performs a buffer swap to display the loaded image on the DMD.

Table 2-23. Load Image Command

BYTE	BITS	DESCRIPTION	RESET	TYPE
0	7:0	Image Index. Loads the image at this index. Reading this back provides the index that was loaded most recently through this command.	x0	WR

2.3.4.7 Image Load Timing

(**I²C**: 0x61)

(**USB**: CMD2: 0x1A, CMD3: 0x3A)

When this command is executed, the system loads the image index shown in Section 2.3.4.6 and collects the amount of time that the image took to load. The busy status of the system is high until the images are loaded and the timing information is collected. This command cannot be executed while the system is already displaying patterns from flash.

Table 2-24. Image Load Timing Write Command

BYTE	BITS	DESCRIPTION	RESET	TYPE
0	7:0	Starting index of the image that requires timing information	x0	W
1	7:0	Number of images that require timing information	x0	W

The following data format is received when the load timing information is read back:

Table 2-25. Image Load Timing Read Command

BYTE	BITS	DESCRIPTION	RESET	TYPE
3:0	31:0	Image load time. Divide this value by 18667 to calculate the time in milliseconds.	x0	R

2.3.4.8 Retrieve Image Resolution Information

(**I²C**: 0x62)

(**USB**: CMD2: 0x1A, CMD3: 0x41)

When this command is executed, the system loads the image index shown in Section 2.3.4.6 and the horizontal and vertical resolution information of the image(s). The busy status of the system is high until the images resolution information is collected. This command cannot be executed while the system is already displaying patterns from flash.

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Table 2-26. Retrieve Image Resolution Information Write Command

BYTE	BITS	DESCRIPTION	RESET	TYPE
0	7:0	Starting index of the image that requires timing information	x0	W
1	7:0	Number of images that requires timing information	x0	W

The following data format is received when the load timing information is read back:

Table 2-27. Retrieve Image Resolution Information Read Command

BYTE	BITS	DESCRIPTION	RESET	TYPE
1:0	15:0	Horizontal resolution of first image	x0	R
3:2	15:0	Vertical resolution of first image	x0	R
5:4	15:0	Horizontal resolution of second image	x0	R
7:6	15:0	Vertical resolution of second image	x0	R
—	—	—	—	—
—	—	—	—	—
N-2:N-3	15:0	Horizontal resolution of nth image	x0	R
N:N-1	15:0	Vertical resolution of nth image	x0	R

2.3.4.9 RetrieveNumber of Images in the Flash

(**I²C**: 0x0C)

(**USB**: CMD2: 0x1A, CMD3: 0x42)

This command retrieves the information about the number of Images in the flash. During creation of pattern LUT this command is useful. Using this command decreases the chances of setting wrong index numbers in the image LUT. One dummy byte must be sent as part of the command

Table 2-28. [Write] Retrieve Number of Images in the Flash

BYTES	BITS	DESCRIPTION	RESET	TYPE
0	7:0	Reserved; set to 0x00	0x00	W

Table 2-29. [Response] Retrieve Number of Images in the Flash

BYTES	BITS	DESCRIPTION	RESET	TYPE
0	7:0	Number of images in the flash	N/A	R

2.3.5 Image Flip

The DLPC350 supports long- and short-axis image flips to support rear- and front-projection table- and ceiling-mounted projection.

NOTE: If showing image from Flash, load image (I2C: 0x7F, USB: 0x1A, 0x39). This must be called to update the image flip setting.

2.3.5.1 Long-Axis Image Flip

(**I²C**: 0x08)

(**USB**: CMD2: 0x10, CMD3: 0x08)

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The long-axis image flip defines whether the input image is flipped across the long axis of the DMD. If this parameter is changed while displaying a still image, the input still image must be resent. If the image is not resent, the output image may be slightly corrupted. Figure 2-1 shows an example of a long-axis image flip. In structured light mode, the image flip takes effect on the next bit-plane, image, or video frame load.

Table 2-30. Long-Axis Image Flip Command

BYTE	BITS	DESCRIPTION	RESET	TYPE
0	0	Flips image along the long side of the DMD:	d0	WR
		0 = Disable flip		
		1 = Enable flip		
	7:1	Reserved	d0	R

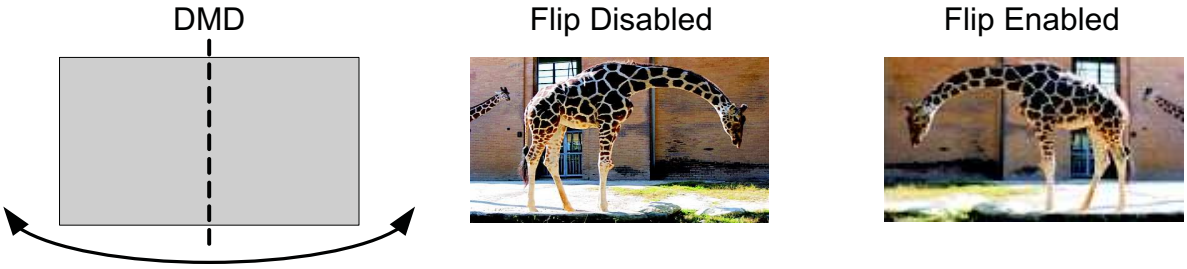

Figure 2-1. Image Long-Axis Flip Example

2.3.5.2 Short Axis Image Flip

(**I²C**: 0x09)

(**USB**: CMD2: 0x10, CMD3: 0x09)

The short-Axis image flip defines whether the input image is flipped across the short axis of the DMD. If this parameter is changed while displaying a still image, the input still image must be resent. If the image is not resent, the output image may be slightly corrupted. Figure 2-2 shows an example of a short-axis image flip. In structured light mode, the image flip takes effect on the next bit-plane, image, or video frame load.

Table 2-31. Short-Axis Image Flip Command

BYTE	BITS	DESCRIPTION	RESET	TYPE
0	0	Flips image along the short side of the DMD:	d0	WR
		0 - Disable flip		
		1 - Enable flip		
	7:1	Reserved	d0	R

Figure 2-2. Image Short-Axis Flip Example

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2.3.6 Image Processing Control

2.3.6.1 Color Space Conversion (CSC)

(**I²C**: 0x26)

(**USB**: CMD2: 0x1A, CMD3: 0x0D)

The CSC command specifies the color matrix used to translate the input data to RGB data or to color correct the RGB input data. The color space converter contains one color space matrix with nine elements. All nine command bytes must be sent as one contiguous block to ensure that all the coefficient values are updated simultaneously.

Table 2-32. CSC Command

BYTE	BITS	DESCRIPTION	RESET			TYPE
0	1:0	Attributes of input source:	d0			WR
		0 - RGB 4:4:4				
		1 - YCrCb 4:4:4				
		2 - YCrCb 4:2:2				
	7:2	Reserved	d0			R
			RGB 4:4:4	YCrCb 4:4:4	YCrCb 4:2:2	R
1	12:0	CSC coefficient 1	x0400	x04A8	x04A8	WR
2	12:0	CSC coefficient 2	x0000	xFDC7	xFCC0	WR
3	12:0	CSC coefficient 3	x0000	xFF26	xFE6F	WR
4	12:0	CSC coefficient 4	x0000	x04A8	x04A8	WR
5	12:0	CSC coefficient 5	x0400	x0715	x0662	WR
6	12:0	CSC coefficient 6	x0000	x0000	x0000	WR
7	12:0	CSC coefficient 7	x0000	x04A8	x04A8	WR
8	12:0	CSC coefficient 8	x0000	x0000	x0000	WR
9	12:0	CSC coefficient 9	x0400	x0875	x0812	WR

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = \begin{bmatrix} C1 & C2 & C3 \\ C4 & C5 & C6 \\ C7 & C8 & C9 \end{bmatrix} \begin{bmatrix} A \\ B \\ C \end{bmatrix}$$

Figure 2-3. CSC Matrix

All programmable CSC coefficient values represent numbers less than 4, but greater than or equal to –4. The CSC coefficient values are 13-bit signed 2's complement numbers with the binary point between bits 9 and 10 (s2.10 format).

Table 2-33. Color Space Conversion Coefficient Format

BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Sign	2^{1}	2^{0}	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}

2.3.7 LED Driver Control

LED driver operation is a function of the individual red, green, and blue LED-enable software-control parameters. The recommended order for initializing LED drivers is to:

1. Program the individual red, green, and blue LED driver currents.

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2. Program the LED PWM polarity.
3. Enable the individual LED enable outputs.
4. Turn on the DLP display sequence (see Section 2.4.1).

The LED-current software-control parameters define PWM values that drive corresponding LED current. The LED enables indicate which LED is activated.

CAUTION

Careful control of LED current is needed to prevent damage to LEDs. Follow all LED manufacturer recommendations and maintain LED current levels within recommended operating conditions. The setting of the LED current depends on many system and application parameters (including projector thermal design, LED specifications, selected display mode, and so forth). Therefore, the recommended and absolute-maximum settings vary greatly.

2.3.7.1 LED Enable Outputs

(**I²C**: 0x10)

(**USB**: CMD2: 0x1A, CMD3: 0x07)

The DLPC350 contains three sets of pins to control the LED enables:

- LEDR_EN for the red LED
- LEDG_EN for the green LED
- LEDB_EN for the blue LED

After reset, all LED enables are placed in the inactive state until the board initializes.

Table 2-34. LED Enable Outputs

BYTE	BITS	DESCRIPTION	RESET	TYPE
0	0	Red LED Enable	x0	WR
		0 - Red LED is disabled		
		1 - Red LED is enabled		
	1	Green LED Enable	x0	WR
		0 - Green LED is disabled		
		1 - Green LED is enabled		
	2	Blue LED Enable	x0	WR
		0 - Blue LED is disabled		
		1 - Blue LED is enabled		
	3	LED Enable Control	x1	WR
		0 - All LED enables are controlled by bits 2:0 and ignore sequencer control		
		1 - All LED enables are controlled by the sequencer and ignore the settings in bits 2:0		
	7:4	Reserved	x0	R

2.3.7.1.1 LED PWM Polarity

(**I²C**: 0x0B)

(**USB**: CMD2: 0x1A, CMD3: 0x05)

The LED PWM polarity command sets the polarity of all PWM signals. This command must be issued before powering up the LED drivers.

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Table 2-35. LED PWM Polarity Command

BYTE	BITS	DESCRIPTION	RESET	TYPE
0	1:0	Polarity of PWM signals	x0	WR
		0 - Normal polarity, PWM 0 value corresponds to no current while a PWM value of 255 corresponds to maximum current.		
		1 - Inverted polarity. PWM 0 value corresponds to maximum current while a PWM value of 255 corresponds to no current.		
	7:2	Reserved	x0	R

2.3.7.2 LED Driver Current Control

(**I²C**: 0x4B)

(**USB**: CMD2: 0x0B, CMD3: 0x01)

This parameter controls the pulse duration of the specific LED PWM modulation output pin. The resolution is eight bits and corresponds to a percentage of the LED current. The PWM value is set from 0 to 100% in 256 steps. If the LED PWM polarity is set to normal polarity, a setting of 0xFF gives the maximum PWM current. The LED current is a function of the specific LED driver design.

CAUTION

Care must be taken when using this command. Improper use of this command can lead to damage to the system. The setting of the LED current depends on many system and application parameters (including projector thermal design, LED specifications, selected display mode, and so forth). Therefore, recommended and absolute-maximum settings vary greatly.

Table 2-36. LED Driver Current Control Command

BYTE	BITS	DESCRIPTION	RESET	TYPE
0	7:0	Red LED PWM current control	x97	WR
		Valid range (assuming normal polarity of PWM signals) is:		
		0x00 (0% duty cycle → Red LED driver generates no current) to 0xFF (100% duty cycle → Red LED driver generates maximum current))		
		The current level corresponding to the selected PWM duty cycle is a function of the specific LED driver design and varies by design.		
1	7:0	Green LED PWM current control	x78	WR
		Valid range (assuming normal polarity of PWM signals) is:		
		0x00 (0% duty cycle → Green LED driver generates no current) to 0xFF (100% duty cycle → Green LED driver generates maximum current))		
		The current level corresponding to the selected PWM duty cycle is a function of the specific LED driver design and varies by design.		
2	7:0	Blue LED PWM current control	x7D	WR
		Valid range,(assuming normal polarity of PWM signals) is:		
		0x00 (0% duty cycle → Blue LED driver generates no current) to 0xFF (100% duty cycle → Blue LED driver generates maximum current))		
		The current level corresponding to the selected PWM duty cycle is a function of the specific LED driver design and varies by design.		

2.3.8 GPIO Control

The DLPC350 device contains 20 general-purpose input/output pins (GPIO). Some of these pins are configured for PWM output, PWM input, or clock output functionality. By default, all pins are configured as GPIO.

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2.3.8.1 GPIO Configuration

(**I²C**: 0x44)

(**USB**: CMD2: 0x1A, CMD3: 0x38)

The GPIO configuration command enables GPIO functionality on a specific set of DLPC350 device pins. The command sets the direction, output buffer type, and output state of the pins.

Table 2-37. GPIO Configuration Command

BYTE	BITS	DESCRIPTION	RESET	TYPE
0	7:0	GPIO selection. See Table 2-38 for description of available pins	N/A	WR
1	1:0	Reserved	x0	R
	2	Input value 0 = Low 1 = High	x0	R
	3	Output state 0 = Drive selected GPIO pin low, if the direction is set to output 1 = Drive selected GPIO pin high, if the direction is set to output and the pin is not set to open-drain buffer type	GPIO dependent	WR
	4	Output buffer type 0 = Standard buffer (drives high or low) 1 = Open-drain buffer (drives low only)	GPIO dependent	WR
	5	GPIO direction 0 = Input 1 = Output	GPIO dependent	WR
	6	Reserved	x0	R
	7	GPIO dsable 0 = Enable GPIO 1 = Disable GPIO (Enable alternative function. See Table 2-38.)	GPIO dependent	WR

Table 2-38. GPIO Selection

GPIO SELECTION	DLPC350 GPIO PIN	FUNCTION	ALTERNATE FUNCTION
0	GPIO_00	GPIO	PWM Output
1	Reserved		
2	GPIO_02	GPIO	PWM Output
4:3	Reserved		
5	GPIO_05	GPIO	PWM Input
6	GPIO_06	GPIO	PWM Input
10:7	Reserved		
11	GPIO_11	GPIO	Clock Out1
12	GPIO_12	GPIO	Clock Out2
13	GPIO_13	GPIO	
14	GPIO_14	GPIO	
15	GPIO_15	GPIO	
19:16	Reserved		
20	GPIO_20	GPIO	
21	GPIO_21	GPIO	
23:22	Reserved		
24	GPIO_24	GPIO	
25	GPIO_25	GPIO	
26	Reserved		

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Table 2-38. GPIO Selection (continued)

GPIO SELECTION	DLPC350 GPIO PIN	FUNCTION	ALTERNATE FUNCTION
27	GPIO_27	GPIO	
28	GPIO_28	GPIO	
29	GPIO_29	GPIO	
30	GPIO_30	I2C_ADDR_SEL	GPIO
32:31	Reserved		
33	GPIO_33	GPIO	
34	GPIO_34	GPIO	
35	GPIO_35	GPIO	
36	GPIO_36	GPIO	
56:37	Reserved		

2.3.8.2 GPIO Clock Configuration

(**I²C**: 0x48)

(**USB**: CMD2: 0x08, CMD3: 0x07)

The DLPC350 device supports two pins with clock output capabilities: GPIO_11 and GPIO_12. The GPIO clock configuration command enables the clock output functionality and sets the clock frequency.

Table 2-39. GPIO Clock Configuration Command

BYTE	BITS	DESCRIPTION	RESET	TYPE
0	1:0	Clock selection	N/A	WR
		1 = GPIO_11		
		2 = GPIO_12		
	7:2	Reserved	x0	R
1	0	Clock functionality disable	x0	WR
		0 = Enable clock functionality on selected pin		
		1 = Disable clock functionality on selected pin		
	7:1	Reserved	x0	R
2	7:0	Clock divider. Allowed values in the range of 2 to 127. Output frequency = 96 MHz / (clock divider)	x7F	WR
		0x0 = Reserved		
		0x1 = Reserved		
		0x2 = 2		
		—		
		0x7F = 127		
		0xFF:0x80 = Reserved		

2.3.9 Pulse Width Modulated (PWM) Control

The DLPC350 provides two general-purpose PWM channels that are used for a variety of control applications, such as fan speed. If the PWM functionality is not required, these signals can be programmed as GPIO pins. To enable the PWM signals:

1. Disable GPIO functionality using the GPIO Configuration command.
2. Program the PWM signal using the PWM Setup command.
3. Enable the PWM signal with the PWM Enable command.

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2.3.9.1 PWM Setup

(**I²C**: 0x41)

(**USB**: CMD2: 0x1A, CMD3: 0x11)

The PWM Setup command sets the clock period and duty cycle of the specified PWM channel. The PWM frequency and duty cycle is derived from an internal 18.67-MHz clock. To calculate the desired PWM period, divide the desired clock frequency by the internal 18.67Mhz clock. For example, a PWM frequency of 2 kHz requires a 18666667 / 2000 = 9333 or 0x2475. As a result, byte 1 is programmed to 0x24 and byte 3 is programmed to 0x75.

Table 2-40. PWM Setup Command

BYTE	BITS	DESCRIPTION	RESET	TYPE
0	4:0	Reserved	x0	R
	7:5	PWM channel select	x0	WR
		0 - PWM channel 0 (GPIO_0)		
		1 - Reserved		
		2 - PWM channel 2 (GPIO_2)		
		3-7 - Reserved		
4:1	31:0	Clock period in increments of 53.57 ns. Clock period = (value + 1) × 53.5 ns	Channel dependent	WR
5	6:0	Duty cycle = (value + 1)%. Value range is 1% to 99%	Channel dependent	WR
	7	Reserved	x0	R

2.3.10 PWM Enable

(**I²C**: 0x40)

(**USB**: CMD2: 0x1A, CMD3: 0x10)

After the PWM setup command configures the clock period and duty cycle, the PWM enable command activates the PWM signals.

Table 2-41. PWM Enable Command

BYTE	BITS	DESCRIPTION	RESET	TYPE
0	2:0	PWM channel select	N/A	WR
		0 - PWM channel 0 (GPIO_0)		
		1 - Reserved		
		2 - PWM channel 2 (GPIO_2)		
	6:3	Reserved	x0	R
	7	PWM Channel Enable	Channel 2 enabled Channel 0 disabled	WR
		0 -Disable selected PWM channel		
		1 - Enable selected PWM channel		

2.3.11 PWM Capture Configuration

(**I²C**: 0x43)

(**USB**: CMD2: 0x1A, CMD3: 0x12)

The PWM Capture Configuration command samples the specified PWM input signals and returns the PWM clock period in a 4-byte packet.

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Table 2-42. PWM Capture Configuration Command

BYTE	BITS	DESCRIPTION	RESET	TYPE
0	0	PWM capture port	N/A	WR
		0 - PWM input channel 0 (GPIO_5)		
		1 - PWM input channel 1 (GPIO_6)		
	7:1	Reserved	x0	R
4:1	24:0	PWM sample rate (285 Hz to 18666667 Hz)	Port dependent	WR
		Sample rate = Pulse frequency / duty cycle		

2.3.12 PWM Capture Read

(**I²C**: 0x4E)

(**USB**: CMD2: 0x1A, CMD3: 0x13)

The PWM Capture Read command indicates both the number of clock cycles and if the signal is low or high. The PWM Capture Read command sends the PWM input channel (x00 or x01) and reads back four bytes of data. The first two bytes indicate how many samples are taken during a low signal, and the third and fourth bytes indicate how many samples are taken during a high signal.

Table 2-43. PWM Capture Read Values

BYTE	BITS	DESCRIPTION	RESET	TYPE
0	0	PWM capture port	N/A	WR
		0 - PWM input channel 0 (GPIO_5)		
		1 - PWM input channel 1 (GPIO_6)		
	7:1	Reserved	x0	R
1:0	15:0	Low period	N/A	R
3:2	15:0	High period	N/A	R

2.3.13 I²C0 Master Port Control Command

(**I²C**: 0x7B)

(**USB**: CMD2: 0x1A, CMD3: 0x3B)

This command configures and controls any I²C slave device that is connected through I²C Port 0 of the DLPC350 controller. The command selects I²C clock bits, address bits, device address, and the number of bytes to write or read back up to 256.

I²C0 Master Write Command

Table 2-44. I²C0 Master Write Command [(1)]

BYTES	BITS	DESCRIPTION	RESET	TYPE
0	0	0 = 7-bit address 1 = 10-bit address	0	W
	7:1	—	—	—
4-1	31:0	I2C clock setting in Hz Valid range 18194Hz to 400000Hz	N/A	W
8-5	31:0	RESERVED	0x00	W
10-9	15:0	I2C device address	N/A	W
12-11	15:0	Bytes to be written. Valid Range 0 to 256	N/A	W
N-13	7:0	Data bytes to be written before read back, where N <= 256	N/A	W

(1) If a failure occurs while sending a message to the slave, the I²C0 Master Read/Write error status shows the reason for the error.

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I²C0 Master Read Command

This command reads the response from any slave device and is similar to the I²C0 Master Write command with the addition of the number of bytes to read back in response. The command accepts the number of bytes to write before reading the response which ranges from 0 – 256.

Table 2-45. I²C0 Master Read Command [(1)]

BYTES	BITS	DESCRIPTION	RESET	TYPE
0	0	0 = 7-bit address 1 = 10-bit address	0	W
	7:1	—	—	—
4-1	31:0	I²C clock setting in Hz Valid range: 18194Hz to 400000 Hz	N/A	W
8-5	31:0	Reserved	0x00	W
10-9	15:0	I²C device address	N/A	W
12-11	15:0	Bytes to write before reading from the slave device. Valid range: 0 to 256	N/A	W
14-13	15:0	Number of bytes to read back from the slave device	N/A	W
N-15	7:0	Data bytes to write before read back where N ≤ 256	N/A	W

(1) If a failure occurs while sending a message to the slave, the I²C0 Master Read/Write error status shows the reason for the error.

Table 2-46. I²C0 Master Read Response

BYTES	BITS	DESCRIPTION	RESET	TYPE
N-0	N/A	Number of requested bytes from the slave device where N is between 1 to 256	N/A	R

2.3.14 I²C0 Master Read/Write Error Response

(**I²C**: 0x3A)

(**USB**: CMD2: 0x1A, CMD3: 0x43)

This command returns the status of the I²C0 Master Read/Write command. This is helpful if there are any errors during the message transmission.

The response returns 1-byte data with the error flag set as Table 2-47 lists.

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Table 2-47. I2C0 Master Read/Write Error Response

BYTES	BITS	DESCRIPTION	RESET	TYPE
0	0	ACK response from the slave 0 = ACK response received 1 = No ACK received from the slave device	0x00	R
	1	Arbitration Lost 0 = No arbitration error 1 = I2C arbitration lost		
	2	Write Timeout Error 0 = No write timeout error 1 = write timeout error The DLPC350 waits one second to transmit before returning this error.		
	3	Read Timeout Error 0 = No read timeout error 1 = read timeout error The DLPC350 waits one second to transmit before returning this error.		
	4	Send Stop No ACK Received Error 0 = No send tmeout error occurred 1 = After write or read timeout error, I2C0 generates stop condition and verifies that ACK is returned for the stop condition. If not received, this flag is set.		
	5	I2C0 Core Internal Error 0 = No I2C0 core internal error occurred 1 = I2C0 core internal error occurred		
	7:6	Reserved		

2.4 Display Sequences

A DLP display sequence consists of several parameters which dictate the loading of the DMD and the control of PWM to the LEDs. The DLPC350 supports two main sequence modes:

- Video display mode
- Pattern display mode

The display mode selection command (Section 2.4.1) selects between video or pattern display mode.

In video mode, the DLPC350 supports up to 1280 × 800 pixel resolution at 120 Hz through 30-bit RGB or FPD-link interfaces. The DLPC350 processes the digital input image and converts the data into the appropriate format for the DLP4500 DMD. The DLPC350 processing functions include format conversion and video enhancement blocks (see Figure 2-4). Note that not all of these functions are available for user control.

In pattern display mode, the DLPC350 provides a high-speed, pixel accurate 912 × 1140 resolution up to 120 Hz that bypasses the video processing and image enhancement functions. This mode supports data input through the DLPC350 24-bit RGB or FPD-link interfaces and flash memory. This functionality is designed for techniques such as structured light, additive manufacturing, or digital exposure. The DLPC350 can display a set of patterns and signal a camera to capture when these patterns are displayed. Figure 2-4 shows the DLPC350 block diagram and the main functional blocks for video and pattern display mode. Table 2-48 lists the allowed pattern combinations of bit-depth, number of patterns, and maximum pattern speed.

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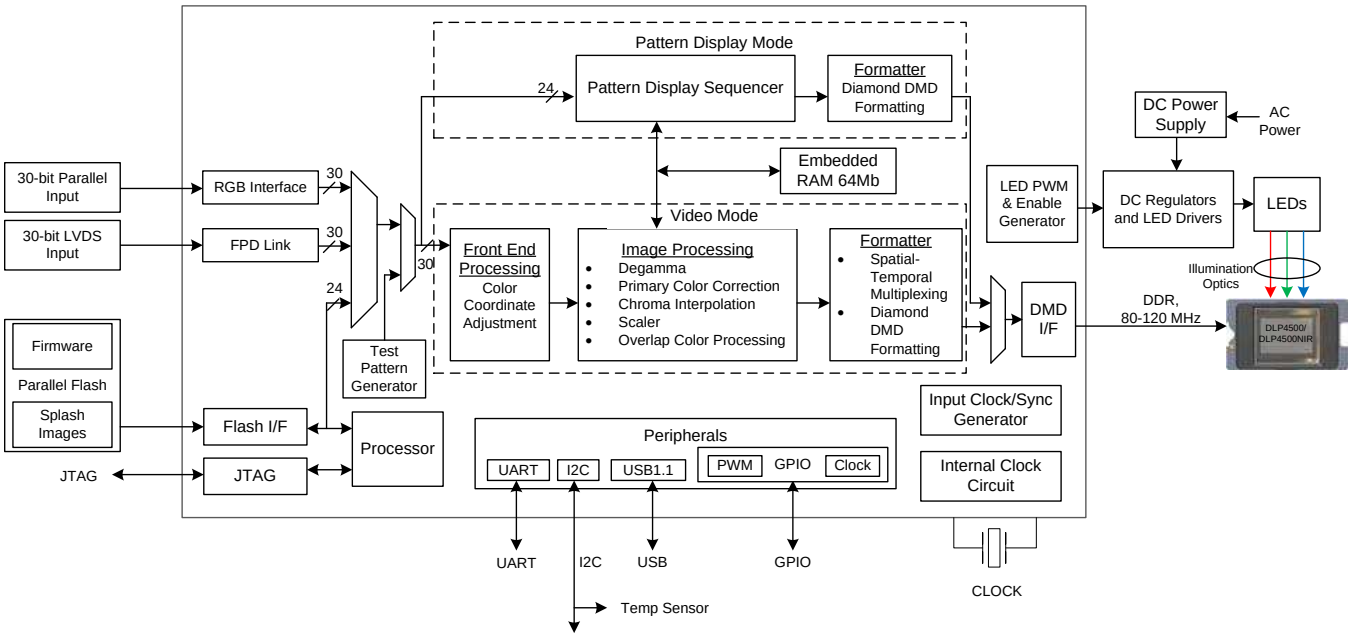

Figure 2-4. DLPC350 Functional Block Diagram

Table 2-48. Allowed Pattern Display Combinations

BIT-DEPTH	MAXIMUM EXTERNAL INPUT PATTERN RATE (Hz)	MAXIMUM PATTERN RATE FOR PRE-LOADED PATTERNS (Hz)	MAXIMUM NUMBER OF PATTERNS FOR PRE-LOADED PATTERNS
1	2880	4225	48
2	1428	1428	24
3	636	636	16
4	588	588	12
5	480	500	8
6	400	400	8
7	222	222	6
8	120	120	6

The video output modes operate on a per-frame basis where the DLPC350 allocates the input data in a frame. For example, a 24-bit RGB input image is allocated into a 60-Hz frame by dividing each color (red, green, and blue) into specific percentages of the frame (see Figure 2-5). Therefore, for a ratio of 40% red, 45% green, and 15% blue , the red, green, and blue colors have a 6.67-, 7.5-, and 2.54-ms time slot allocated, respectively. Because each color has an 8-bit depth, each color time slot is further divided into bit-planes, as shown in Figure 2-5. A bit-plane is the two-dimensional arrangement of one bit that is extracted from all the pixels in the full color 2D image.

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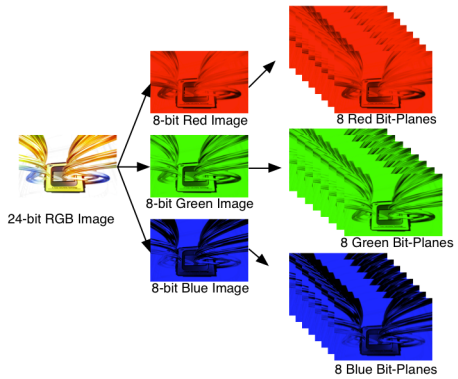

Figure 2-5. Bit-Planes of a 24-Bit RGB Image

The length of each bit-plane in the time slot is weighted by the corresponding power of two of the binary representation. This provides a binary pulse-width modulation of the image. In the 24-bit RGB streaming input, Figure 2-6 shows that each color time slot is divided into eight bit-planes. The sum of all bit that are weighed in the color time slot equal 255, with each bit-plane weighted by the binary representation.

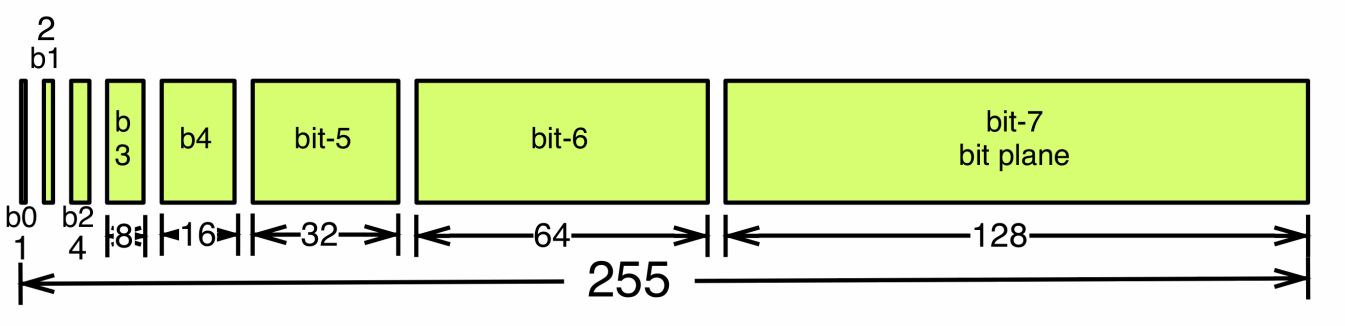

Figure 2-6. Bit Partition in a Frame for an 8-Bit Monochrome Image

As a result, a single video frame is composed of a series of bit-planes. Because the DMD mirrors c are on or off, an image is created by turning on and shining light on the mirrors that correspond to the bit set in a bit-plane . With the binary pulse-width modulation, the intensity level of the color is reproduced by controlling the amount of time the mirror is on and illuminated. For a 24-bit RGB frame image input to the DLPC350, the DLPC350 creates 24 bit-planes, stores the planes on the internal memory buffer, and sends the planes to the DLP4500 DMD on the next frame, one bit-plane at a time. Depending on the bit weight of the bit-plane, the DLPC350 controls the time this bit-plane is exposed to light. The time a bit plane is illuminated is directly proportional to the intensity of the bit-plane. The DLPC350 intertwines and interleaves bit planes, time slots, and color frames to improve image quality. Note this functionality is performed automatically in video mode and is not adjustable by the user.

For other applications where this image enhancement is not desired, the video processing algorithms are bypassed and replaced with a specific set of bit-planes. The bit-depth of the pattern is allocated into the corresponding binary weighted time slots. Furthermore, output trigger signals synchronize with these time slots to indicate when the image is displayed. For structured light applications, this mechanism displays a set of patterns and signals a camera to capture these patterns that are overlaid on an object.

As shown in Figure 2-7, the DLPC350 stores two 24-bit frames in the internal memory buffer. This 48 bit-plane display buffer allows the DLPC350 to send one 24-bit buffer to the DMD array while the second buffer is filled from flash or streamed in through the 24-bit RGB interface. In streaming mode, the DMD array displays the previous 24-bit frame while the current frame fills the second 24-bit frame of the display buffer. After a 24-bit frame is displayed, the buffer rotates and accesses the next 24-bit frame to the DMD. As a result, the displayed image is a 24-bit frame behind the data that is streamed through the 24-bit RGB parallel interface.

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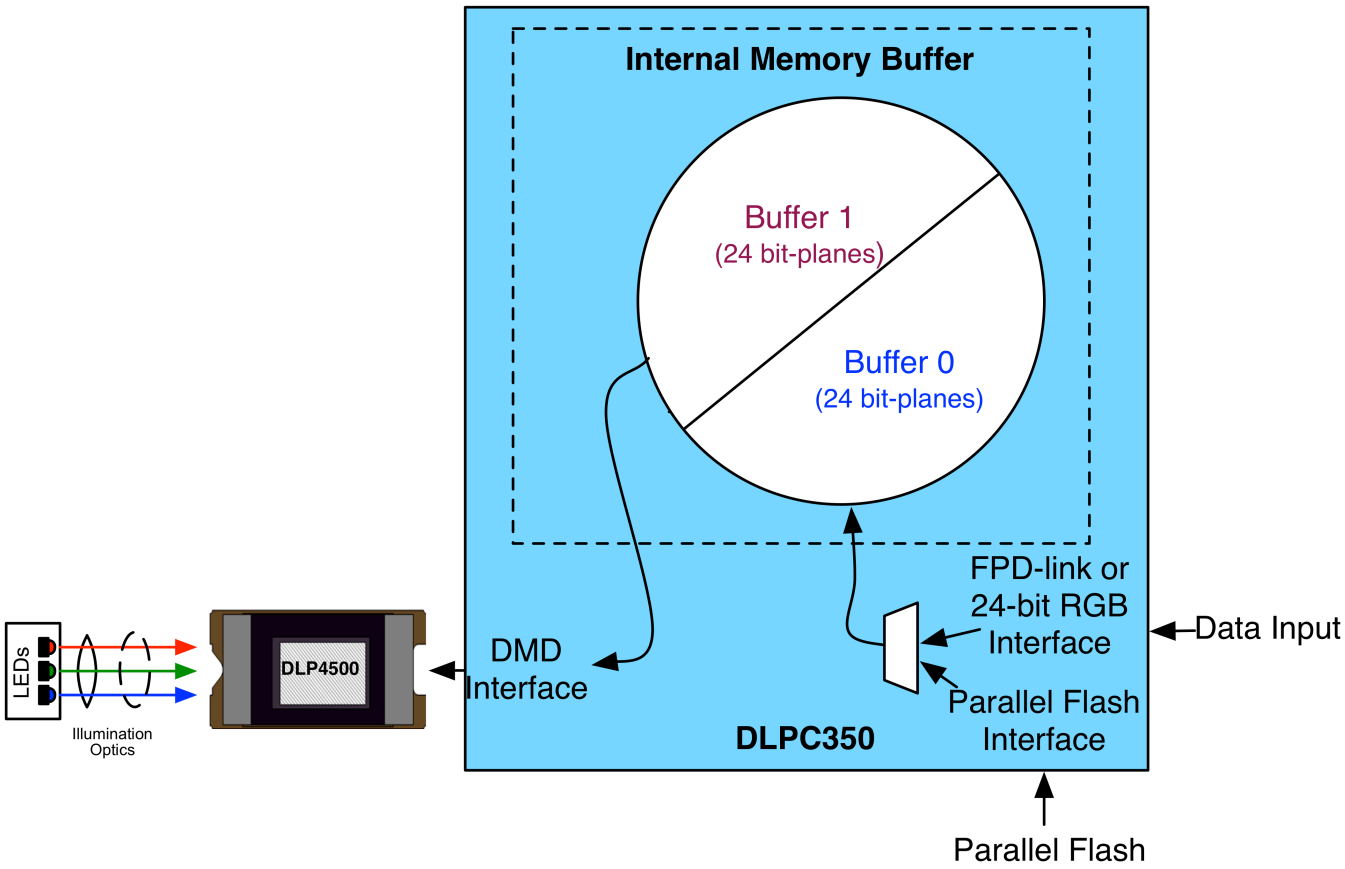

Figure 2-7. DLP4500 Frame Buffer

Note that the displayed image is frame delayed in relation to the data streamed through the 24-bit RGB parallel bus, as shown in Figure 2-8.

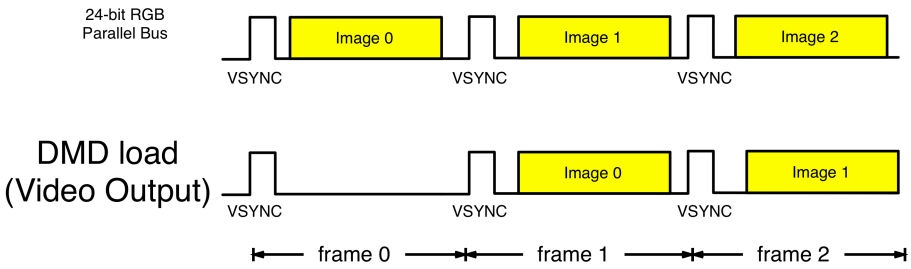

Figure 2-8. Frame Delay Between RGB Input and Video Output

2.4.1 Display Mode Selection Command

(**I²C**: 0x69)

(**USB**: CMD2: 0x1A, CMD3: 0x1B)

The Display Mode Selection Command enables the internal image processing functions of the DLPC350 for video mode or bypasses the functions for pattern display mode. This command selects between video or pattern display mode of operation.

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Table 2-49. Display Mode Selection Command

BYTE	BITS	DESCRIPTION	RESET	TYPE
0	0	Display Mode Selection	d0	WR
		0 = Video display mode. Assumes streaming video image from the 30-bit RGB or FPD-link interface with a pixel resolution of up to 1280 × 800 up to 120 Hz.		
		1 = Pattern display mode. Assumes a 1-bit through 8-bit image with a pixel resolution of 912 × 1140 and bypasses all the image processing functions of DLPC350.		

2.4.2 Video Mode Commands

In video mode, the DLPC350 supports up to a 1280 × 800 pixel resolution at 120 Hz through the 30-bit RGB or FPD-link interfaces. The following commands are only supported in external video mode:

- Gamma Correction
- Input Display Resolution

2.4.2.1 Gamma Correction

(**I²C**: 0x31)

(**USB**: CMD2: 0x1A, CMD3: 0x0E)

Because the DMD is inherently linear in response, the Gamma Correction command specifies the removal of the gamma curve that is applied to the video data at the source. Two degamma tables are provided: TI Video (Enhanced) and TI Video (Max Brightness).

Table 2-50. Gamma Correction Command

BYTE	BITS	DESCRIPTION	RESET	TYPE
0	0	Degamma correction table pointer: 0 = TI Video (Enhanced)	d0	WR
	6:1	Reserved	d0	R
	7	Gamma correction enable: 0 = Disable, no gamma correction	d1	WR

NOTE: In pattern sequence mode, a linear 1:1 degamma table is applied. This register only applies for video mode.

2.4.2.2 Input Display Resolution

(**I²C**: 0x7E)

(**USB**: CMD2: 0x10, CMD3: 0x00)

The Input Display Resolution command defines the active input resolution and active output (displayed) resolution. The maximum supported input and output resolutions for the DLP4500 0.45 WXGA DMD is 1280 pixels (columns) by 800 lines (rows). This command provides the option to define a subset of active input frame data using pixel (column) and line (row) counts relative to the source-data enable signal (DATEN). This feature crops the source image as the first step in the processing chain.

Table 2-51. Input Display Resolution Command

BYTE	BITS	DESCRIPTION	RESET	TYPE
1:0	15:0	Input image, first active pixel (column) of cropped area	d0	WR
3:2	15:0	Input image, first active line (row) of cropped area	d0	WR
5:4	15:0	Input image vertical resolution, pixels (columns) per line (row) of cropped area	d0	WR

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Table 2-51. Input Display Resolution Command (continued)

BYTE	BITS	DESCRIPTION	RESET	TYPE
7:6	15:0	Input image horizontal resolution, lines (rows) per frame of cropped area	d0	WR
9:8	15:0	Output image, first active pixel (column) of displayed image	d0	WR
11:10	15:0	Output image, first active line (row) of displayed image	d0	WR
13:12	15:0	Output image horizontal resolution, pixels (columns) per line (row)	d1280	WR
15:14	15:0	Output image vertical resolution, lines (rows) per frame	d800	WR

2.4.3 Pattern Display Mode Commands

In pattern display mode, the DLPC350 supports 1-, 2-, 3-, 4-, 5-, 6-, 7-, and 8-bit images with a 912 × 1140 pixel resolution streamed through the 24-bit RGB or FPD-link interface or stored in the flash memory locations. The following commands are only supported in pattern display mode:

- Validate Data
- Trigger Controls
- LED Enable Delay Controls
- Pattern Display Controls
- Exposure Controls
- Buffer Controls

NOTE: If the pattern display is already active, the display must be stopped using the I^2C command 0x65 before making a change.

NOTE: Any changes in the setting must be validated using the validate data command.

(I^2C: 0x7D)

(USB: CMD2: 0x1A, CMD3: 0x1A).

When a streaming source is used in pattern display mode, use the following procedure to apply any parameter changes.

1. Ensure the source is still active
2. Issue a Stop command
3. Wait at least two frame periods
4. Read the status register to check that pattern mode is stopped. If it is not, then poll the status register, delaying one frame time per read until the register indicates pattern mode has stopped.
5. Apply the new setting(s)
6. Ensure the source is active
7. Send the Validate command
8. Start the sequence

The commands mentioned in the steps can be found in the following subsections.

2.4.3.1 Validate Data Command Response

(**I^2C**: 0x7D)

(**USB**: CMD2: 0x1A, CMD3: 0x1A)

The Validate Data command checks the programmed pattern display modes and indicates any invalid settings. To execute the command, write a dummy byte followed by a one byte read. The byte read contains the status byte. This command must be executed after all pattern display configurations are completed.

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Table 2-52. Validate Data Command Response

BYTE	BITS	DESCRIPTION	RESET	TYPE
0	0	Validity of exposure or frame period settings	d0	R
		1 = Selected exposure or frame period settings are invalid		
		0 = Selected exposure or frame period settings are valid		
	1	Validity of pattern numbers in lookup table (LUT)	d0	R
		1 = Selected pattern numbers in LUT are invalid		
		0 = Selected pattern numbers in LUT are valid		
	2	Status of Trigger Out1	d0	R
		1 = Warning, continuous Trigger Out1 request or overlapping black sectors		
		0 = Trigger Out1 settings are valid		
	3	Status of post sector settings	d0	R
		1 = Warning, post vector is not inserted prior to external triggered vector		
		0 = Post vector settings are valid		
	4	Status of frame period and exposure difference	d0	R
		1 = Warning, frame period or exposure difference is less than 230 µsec		
		0 = Frame period or exposure difference is valid		
	6:5	Reserved		
	7	1 = DLPC350 is busy validating. Once the bit is clear, interpret the rest of the bits		
		0 = DLPC350 is valid. The rest of the bits can be interpreted.		

NOTE: Poll or read the response byte. Only interpret the data when bit 7 goes from 1 to 0.

2.4.3.2 Trigger Controls

To synchronize a camera with the displayed patterns, the DLPC350 supports three trigger modes:

- Trigger Mode 0 (applicable when pattern data from RGB parallel port OR FPD port):
  - VSYNC is the trigger input.
  - TRIG_OUT1 frames the exposure time of the pattern.
  - TRIG_OUT2 indicates the start of the pattern sequence or internal buffer boundary of a 24-bit plane.
- Trigger Mode 1 (applicable for pattern data from flash):
  - TRIG_IN1 advances to next pattern, while TRIG_IN2 starts and pauses the pattern sequence.
  - TRIG_OUT1 frames the exposure time of the pattern.
  - TRIG_OUT2 indicates the start of the pattern sequence or internal buffer boundary of a 24-bit plane.
- Trigger Mode 2 (applicable for pattern data from flash):
  - TRIG_IN1 toggles between two consecutive patterns
  - TRIG_IN2 advances to the next pair of patterns
  - TRIG_OUT1 frames the exposure time of the pattern.
  - TRIG_OUT2 indicates the start of the pattern sequence or internal buffer boundary of a 24-bit plane.

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Figure 2-9 shows an example of Trigger Mode 0, where the VSYNC starts the pattern sequence display. Frame time indicates the time between VSYNC triggers, and display time indicates the length of pattern sequence. This display time must be less than the frame time. The pattern sequence consists of a series of three consecutive patterns. The first pattern sequence consists of P1, P2, and P3. Since P3 is an RGB pattern, P3 is shown with the time sequential representation of P3.1, P3.2, and P3.3. The second pattern sequence consists of three patterns: P4, P5, and P6. The third sequence consists of P7, P8, and P9. TRIG_OUT_1 frames each pattern exposed, while TRIG_OUT_2 indicates the start of each of the three pattern sequences. See Section 4.2 for detailed steps on how to generate this pattern sequence.

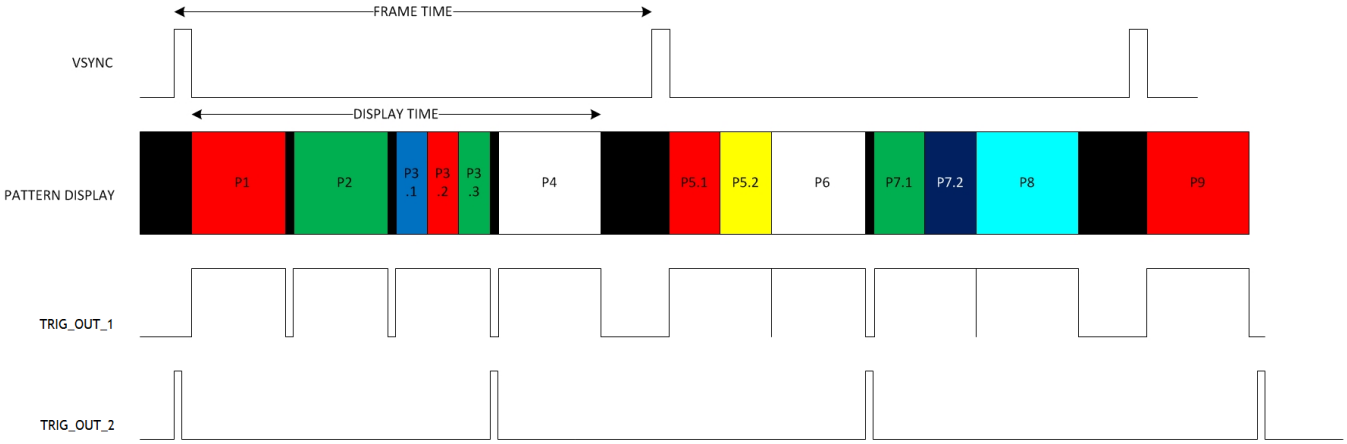

Figure 2-9. Trigger Mode 0 Timing Diagram Example

Figure 2-10 shows an example of Trigger Mode 1. A set of three-pattern sequences are displayed. TRIG_OUT_1 frames each pattern exposed, while TRIG_OUT_2 indicates the start of each three-pattern sequence. TRIG_IN_2 serves as a start and pause signal. By raising TRIG_IN_2, the pattern sequence starts. By lowering TRIG_IN_2, the pattern sequence pauses. If the pattern sequence is previously started, raising TRIG_IN_2 continues the pattern sequence until this signal is lowered. If TRIG_IN_2 is lowered while a pattern is displayed (see P4 in Figure 2-10), when this pattern sequence is continued, this pattern is displayed again since the full exposure is not complete.

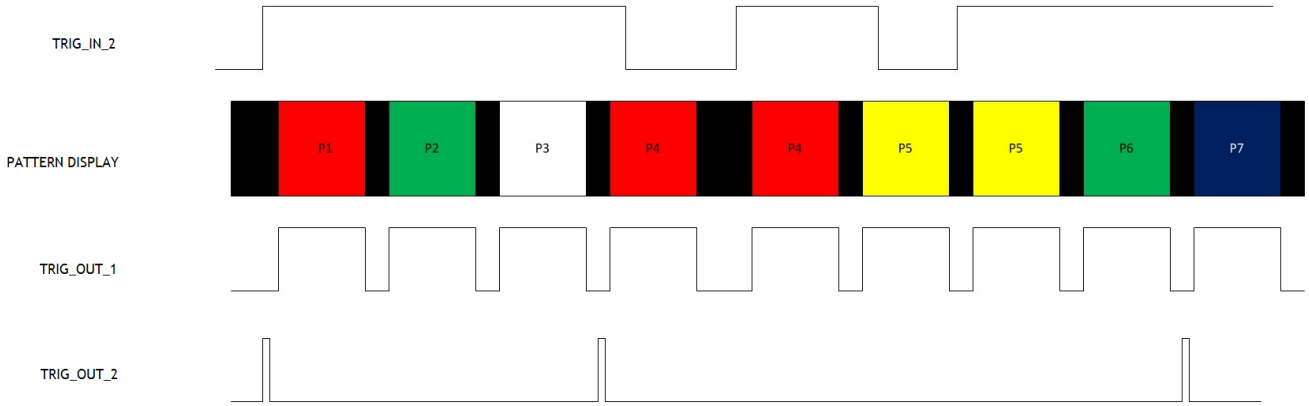

Figure 2-10. Trigger Mode 1 Timing Diagram Example

An example of trigger mode 2 is shown in Figure 2-11, where TRIG_IN_1 alternates between two patterns and TRIG_IN_2 advances to the next pair of patterns. shows the allowed pattern combinations in relation to the bit depth of the pattern.

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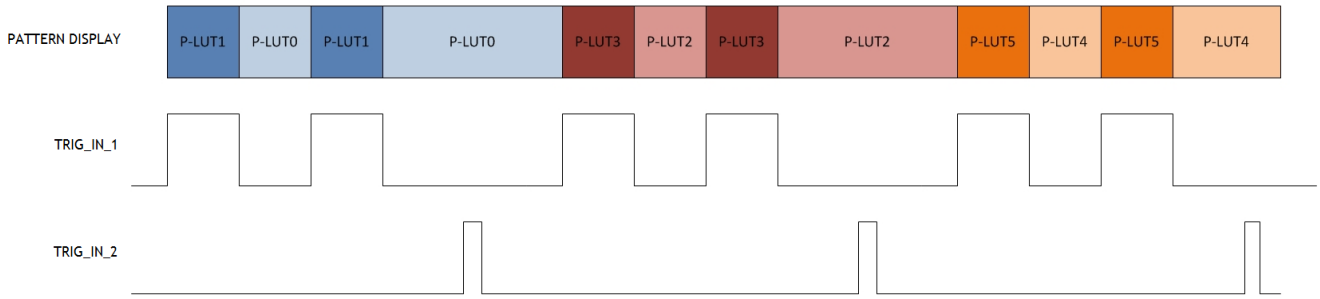

Figure 2-11. Trigger Mode 2 Timing Diagram Example

WARNING

When using an external hardware triggering mode, it is critical that unused trigger, VSYNC and pixel clock lines be properly isolated, even if not in use by the mode selected. Any noise or signal presence on these lines can cause undesired behavior.

2.4.3.2.1 Pattern Trigger Mode Selection

(**I²C**: 0x70)

(**USB**: CMD2: 0x1A, CMD3: 0x23)

The Pattern Trigger Mode Selection command selects between one of the five pattern trigger modes. Before executing this command, stop the current pattern sequence. After executing this command, send the validation command (I^2C: 0x7D or USB: 0x1A1A) once before starting the pattern sequence.

Table 2-53. Pattern Trigger Mode Selection Command

BYTE	BITS	DESCRIPTION	RESET	TYPE
0	2:0	Pattern trigger mode selection	d1	WR
		0 = Pattern Trigger Mode 0: VSYNC triggers the pattern display sequence For proper operation, the pattern exposure must equal the total pattern period in this mode		
		1 = Pattern Trigger Mode 1: Internally or externally (through TRIG_IN_1 and TRIG_IN_2) generated trigger		
		2 = Pattern Trigger Mode 2: TRIG_IN_1 alternates between two patterns and TRIG_IN_2 advances to the next pair of patterns		
		3 = Pattern Trigger Mode 3: Internally or externally generated trigger for variable exposure display sequence. This trigger mode follows the same timing diagram as in Figure 2-10.		
		4 = Pattern Trigger Mode 4: VSYNC triggered for variable exposure display sequence. This trigger mode follows the same timing diagram as in Figure 2-9. For proper operation, the pattern exposure must equal the total pattern period in this mode		
	7:3	Reserved	d0	R

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2.4.3.2.2 Trigger Out1 Control

(**I²C**: 0x6A)

(**USB**: CMD2: 0x1A, CMD3: 0x1D)

The Trigger Out1 Control command sets the polarity, rising edge delay, and falling edge delay of the TRIG_OUT_1 signal of the DLPC350. The delays are compared to when the pattern is displayed on the DMD. Before executing this command, stop the current pattern sequence. After executing this command, send the Validation command (I^2C: 0x7D or USB: 0x1A1A) once before starting the pattern sequence.

Table 2-54. Trigger Out1 Control Command

BYTE	BITS	DESCRIPTION	RESET	TYPE
0	0	Reserved	d0	R
	1	TRIG_OUT_1 polarity	d0	WR
		1 = Invert TRIG_OUT_1 polarity to an active low signal		
		0 = Normal TRIG_OUT_1 polarity, active high signal		
	7:2	Reserved	d0	R
1	7:0	TRIG_OUT_1 rising edge delay control ranging from –20.05 µs to 2.787 µs. Each bit adds 107.2 ns.	xBB	WR
		0x00 = –20.05 µs		
		0x01 = –19.9428 µs		
		0x02 = –19.835 µs		
		—		
		0xBB = 0 µs (default)		
		—		
		0xD4 = 2.68 µs		
		0xD5 = 2.787 µs		
2	7:0	TRIG_OUT_1 falling edge delay control with range -20.05 µs to +2.787 µs. Each bit adds 107.2 ns	xBB	WR
		0x00 = –20.05 µs		
		0x01 = –19.9428 µs		
		0x02 = –19.835 µs		
		—		
		0xBB = 0 µs (default)		
		—		
		0xD4 = 2.68 µs		
		0xD5 = 2.787 µs		

2.4.3.2.3 Trigger Out2 Control

(**I²C**: 0x6B)

(**USB**: CMD2: 0x1A, CMD3: 0x1E)

The Trigger Out2 Control command sets the polarity and rising edge delay of the TRIG_OUT_2 signal of the DLPC350. The delay is compared to when the pattern is displayed on the DMD. Before executing this command, stop the current pattern sequence. After executing this command, send the Validation command (I^2C: 0x7D or USB: 0x1A1A) once before starting the pattern sequence.

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Table 2-55. Trigger Out2 Control Command

BYTE	BITS	DESCRIPTION	RESET	TYPE
0	0	Reserved	d0	R
	1	TRIG_OUT_2 polarity	d0	WR
		1 = Invert TRIG_OUT_2 polarity to an active low signal		
		0 = Normal TRIG_OUT_2 polarity, active high signal		
	7:2	Reserved	d0	R
1	7:0	TRIG_OUT_2 rising edge delay control ranging from –20.05 µs to 7.29 µs. Each bit adds 107.2 ns.	xBB	WR
		0x00 = –20.05 µs		
		0x01 = –19.9428 µs		
		0x02 = –19.835 µs		
		—		
		0xBB = 0 µs (default)		
		—		
		0xFE = 7.1828 µs		
		0xFF = 7.29 µs		

2.4.3.2.4 Trigger In1 Control

(**I²C**: 0x79)

(**USB**: CMD2: 0x1A, CMD3: 0x35)

The Trigger In1 Control command sets the rising edge delay TRIG_IN_1 signal of the DLPC350 compared to when the pattern is displayed on the DMD. The polarity of TRIG_IN_1 is set in the lookup table of the pattern sequence. Before executing this command, stop the current pattern sequence. After executing this command, send the Validation command (I^2C: 0x7D or USB: 0x1A1A) once before starting the pattern sequence.

Table 2-56. Trigger In1 Control Command

BYTE	BITS	DESCRIPTION	RESET	TYPE
3:0	18:0	TRIG_IN_1 rising edge delay. Each bit adds a107.136 ns delay.	d0	WR

2.4.3.2.5 Trigger In2 Control

(**I²C**: 0x7A)

(**USB**: CMD2: 0x1A, CMD3: 0x36)

The Trigger In2 Control command sets the polarity of the TRIG_IN_2 signal of the DLPC350 in Trigger Mode 2. For Trigger Mode 0 or 1, TRIG_IN_2 acts as a start or stop signal. If the sequence is not previously started by a software command, the rising edge on TRIG_IN_2 signal input starts or resumes the pattern sequence. If the pattern sequence is active, the falling edge on TRIG_IN_2 signal input stops the pattern sequence. Before executing this command, stop the current pattern sequence. After executing this command, send the Validation command (I^2C: 0x7D or USB: 0x1A1A) once before starting the pattern sequence.

Table 2-57. Trigger In2 Control Command

BYTE	BITS	DESCRIPTION	RESET	TYPE
0	0	Advance pattern polarity for Trigger Mode 2	d0	WR
		0 = Advance pattern to the next pair on rising edge of TRIG_IN_2 signal		
		1 = Advance pattern to the next pair on falling edge of TRIG_IN_2 signal		
	7:1	Reserved	d0	R

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2.4.3.3 LED Enable Delay Controls

The LED Enable Delay Controls commands set the rising and falling edge offsets of the LED enable signals compared to when the pattern is displayed on the DMD. This command is only for pattern display mode. Invideo mode, these delays must be set to 0x0.

2.4.3.3.1 Red LED Enable Control

(**I²C**: 0x6C)

(**USB**: CMD2: 0x1A, CMD3: 0x1F)

The Red LED Enable Delay Control command sets the rising and falling edge delay of the red LED enable signal.

Table 2-58. Red LED Enable Control Command

BYTE	BITS	DESCRIPTION	RESET	TYPE
0	7:0	Red LED enable rising edge delay control ranging from –20.05 µs to 7.29 µs. Each bit adds 107.2 ns.	xBB	WR
		0x00 = –20.05 µs		
		0x01 = –19.9428 µs		
		0x02 = –19.835 µs		
		—		
		0xBB = 0.00 µs (default)		
		—		
		0xFE = 7.1828 µs		
		0xFF = 7.29 µs		
1	7:0	Red LED enable falling edge delay control ranging from –20.05 µs to 7.29 µs. Each bit adds 107.2 ns.	xBB	WR
		0x00 = –20.05 µs		
		0x01 = –19.9428 µs		
		0x02 = –19.835 µs		
		—		
		0xBB = 0 µs (default)		
		—		
		0xFE = 7.1828 µs		
		0xFF = 7.29 µs		

2.4.3.3.2 Green LED Enable Control

(**I²C**: 0x6D)

(**USB**: CMD2: 0x1A, CMD3: 0x20)

The Green LED Enable Delay Control command sets the rising and falling edge delay of the green LED enable signal.

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Table 2-59. Green LED Enable Control Command

BYTE	BITS	DESCRIPTION	RESET	TYPE
0	7:0	Green LED enable rising edge delay control ranging from –20.05 µs to 7.29 µs. Each bit adds 107.2 ns.	xBB	WR
		0x00 = –20.05 µs		
		0x01 = –19.9428 µs		
		0x02 = –19.835 µs		
		—		
		0xBB = 0 µs (default)		
		—		
		0xFE = 7.1828 µs		
		0xFF = 7.29 µs		
1	7:0	Green LED enable falling edge delay control ranging from –20.05 µs to 7.29 µs. Each bit adds 107.2 ns.	xBB	WR
		0x00 = –20.05 µs		
		0x01 = –19.9428 µs		
		0x02 = –19.835 µs		
		—		
		0xBB = 0 µs (default)		
		—		
		0xFE = 7.1828 µs		
		0xFF = 7.29 µs		

2.4.3.3.3 Blue LED Enable Control

(**I²C**: 0x6E)

(**USB**: CMD2: 0x1A, CMD3: 0x21)

The Blue LED Enable Delay Control command sets the rising and falling edge delay of the blue LED enable signal.

Table 2-60. Blue LED Enable Control Command

BYTE	BITS	DESCRIPTION	RESET	TYPE
0	7:0	Blue LED enable rising edge delay control ranging from –20.05 µs to 7.29 µs. Each bit adds 107.2 ns.	xBB	WR
		0x00 = –20.05 µs		
		0x01 = –19.9428 µs		
		0x02 = –19.835 µs		
		—		
		0xBB = 0 µs (default)		
		—		
		0xFE = 7.1828 µs		
		0xFF = 7.29 µs		

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Table 2-60. Blue LED Enable Control Command (continued)

BYTE	BITS	DESCRIPTION	RESET	TYPE
1	7:0	Blue LED enable falling edge delay control ranging from –20.05 µs to 7.29 µs. Each bit adds 107.2 ns.	xBB	WR
		0x00 = –20.05 µs		
		0x01 = –19.9428 µs		
		0x02 = –19.835 µs		
		—		
		0xBB = 0 µs (default)		
		—		
		0xFE = 7.1828 µs		
		0xFF = 7.29 µs		

2.4.3.4 Pattern Display Controls

2.4.3.4.1 Pattern Display Data Input Source

(**I²C**: 0x6F)

(**USB**: CMD2: 0x1A, CMD3: 0x22)

The Pattern Display Data Input Source command selects the source of the data for pattern display: streaming through the 24-bit RGB/FPD-link interface or stored data in the flash image memory area from external flash. Before executing this command, stop the current pattern sequence. After executing this command, send the Validation command (I^2C: 0x7D or USB: 0x1A1A) once before starting the pattern sequence.

Table 2-61. Pattern Display Data Input Source Command

BYTE	BITS	DESCRIPTION	RESET	TYPE
0	1:0	Pattern display data input source	x3	WR
		0b00 = Pattern display data streams through the 24-bit RGB/FPD-link interface		
		0b01 = Reserved		
		0b10 = Reserved		
		0b11 = Pattern display data is fetched from flash memory		
	7:2	Reserved	d0	R

2.4.3.4.2 Pattern Display Start/Stop Pattern Sequence

(**I²C**: 0x65)

(**USB**: CMD2: 0x1A, CMD3: 0x24)

The Pattern Display Start/Stop Pattern sequence command starts or stops the programmed pattern sequence.

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Table 2-62. Pattern Display Start/Stop Pattern Sequence Command

BYTE	BITS	DESCRIPTION	RESET	TYPE
0	1:0	Pattern Display Start/Stop Pattern Sequence	d0	WR
		0b00 = Stop Pattern Display Sequence. The next Start command restarts the pattern sequence from the beginning.		
		0b01 = Pause pattern display sequence. The next Start command starts the pattern sequence by displaying the current pattern in the sequence again.		
		0b10 = Start pattern display sequence		
	7:2	Reserved	d0	R

NOTE: When stopped, before "Start," at a minimum Pattern Display LUT (0x75 I^2C) and pattern display lookup table must be sent again, followed by Validate. If the pattern exposure and frame period are not equal, the pattern exposure time must be less than the frame period by 230 µs.

NOTE: This is an example of how to calculate frame period and pattern exposure time for a 60-Hz refresh rate, 24-bit video signal. Frame Period: 10^6 µs / 60 (refresh rate) = 16666 µs (Frame Period). Pattern Exposure Time: 16666 µs (Frame Period) / 24 (image bit depth) = 694 µs (Pattern Exposure Time). .

2.4.3.4.3 Pattern Exposure Time and Frame Period

(**I^2C**: 0x66)

(**USB**: CMD2: 0x1A, CMD3: 0x29)

The Pattern exposure time and frame period dictates the length of time a pattern is exposed and the frame period. The pattern exposure time must be equivalent to the frame period or the pattern exposure time must be less than the frame period by 230 µs. Before executing this command, stop the current pattern sequence. After executing this command, send the Validation command (I^2C: 0x7D or USB: 0x1A1A) once before starting the pattern sequence.

Table 2-63. Pattern Display Exposure and Frame Period Command

BYTE	BITS	DESCRIPTION	RESET	TYPE
3:0	31:0	Pattern exposure time (µs)	x4010	WR
7:4	31:0	Frame period (µs)	x411A	WR

NOTE: In external video input pattern sequence modes, the pattern exposure time must equal the frame period.

2.4.3.4.4 Pattern Display Invert Data

(**I^2C**: 0x74)

(**USB**: CMD2: 0x1A, CMD3: 0x30)

The Pattern Display Invert Data command dictates how the DLPC350 interprets a value of 0 or 1 to control mirror position for displayed patterns. Before executing this command, stop the current pattern sequence. After executing this command, send the Validation command (I^2C: 0x7D or USB: 0x1A1A) once before starting the pattern sequence.

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Table 2-64. Pattern Display Invert Data Command

BYTE	BITS	DESCRIPTION	RESET	TYPE
0	0	Pattern display invert data	d0	WR
		0 = Normal operation. A data value of 1 flips the mirror to output light, while a data value of 0 flips the mirror to block light		
		1 = Inverted operation. A data value of 0 flips the mirror to output light, while a data value of 1 flips the mirror to block light		
	7:1	Reserved	d0	R

2.4.3.4.5 Pattern Display LUT Control

(**I²C**: 0x75)

(**USB**: CMD2: 0x1A, CMD3: 0x31)

The Pattern Display LUT Control Command controls the execution of patterns stored in the lookup table. Before executing this command, stop the current pattern sequence. After executing this command, send the Validation command (I^2C: 0x7D or USB: 0x1A1A) once before starting the pattern sequence.

Table 2-65. Pattern Display LUT Control Command

BYTE	BITS	DESCRIPTION	RESET	TYPE
0	6:0	Number of LUT entries = value + 1 (ranging from 1 to 128)	x15	WR
		0 = One entry		
		1 = Two entries		
		—		
		127 = 128 entries		
	7	Reserved	x0	WR
1	0	Repeat pattern sequence	x1	WR
		0 = Execute the pattern sequence once		
		1 = Always repeat the pattern sequence once a sequence is completed		
	7:1	Reserved	x0	R
2	7:0	Number of patterns to display = value + 1 (ranging from 1 to 256). If in repeat mode (byte 1, bit 0), then this value dictates how often TRIG_OUT_2 is generated.	x15	WR
3	5:0	Number of Image Index LUT Entries = value + 1 (ranging from 1 to 64). Field is irrelevant for pattern display data input source that is set to a value other than 0x3.	x0	WR
	7:6	Reserved	x0	R

2.4.3.4.6 Pattern Display Look-Up Table

The DLPC350 supports a Pattern Display Look-Up Table (LUT) that defines the pattern sequence and the configuration parameters for each pattern in the sequence. To create this LUT, the programmer must first set up the display mode, trigger mode, exposure, frame rate, and so forth before writing data to the LUT. After properly configured, the Pattern Display LUT Access Control command writes the LUT.

2.4.3.4.7 Pattern Display LUT Offset Pointer

(**I²C**: 0x76)

(**USB**: CMD2: 0x1A, CMD3: 0x32)

The Pattern Display LUT offset pointer defines the location of the LUT entries in the memory of the DLPC350.

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Table 2-66. Pattern Display LUT Offset Pointer Command

BYTE	BITS	DESCRIPTION	RESET	TYPE
0	7:0	Defines offset for LUT entries (data mailbox)	x0	W

2.4.3.4.8 Pattern Display LUT Access Control

(**I²C**: 0x77)

(**USB**: CMD2: 0x1A, CMD3: 0x33)

The LUT on the DLPC350 contains a mailbox to send data to different registers. This command selects which register receives the data. To select the flash image indexes or define the patterns used in the pattern sequence for the pattern display mode:

1. Open the mailbox for the appropriate function by writing the appropriate bit.
2. Write the desired data to the mailbox using the Pattern Display LUT Data command (I^2C: 0x78 or USB 0x1A34)
3. Use this command to close the mailbox.

. . Before executing this command, stop the current pattern sequence. After executing this command, send the Validation command (I^2C: 0x7D or USB: 0x1A1A) once before starting the pattern sequence.

Table 2-67. Pattern Display LUT Access Control Command

BYTE	BITS	DESCRIPTION	RESET	TYPE
0	7:0	Write the appropriate value to the mailbox	x0	W
		0 = Disable (close) the mailboxes		
		1 = Open the mailbox for image index configuration		
		2 = Open the mailbox for pattern definition		
		3 = Open the mailbox for variable exposure pattern definition		
		4 to 127 = Reserved		

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2.4.3.4.9 Pattern Display LUT Data

(**I²C**: 0x78)

(**USB**: CMD2: 0x1A, CMD3: 0x34)

The following parameters: display mode, trigger mode, exposure, and frame rate must be set up before sending any mailbox data. If the Pattern Display Data Input Source is set to streaming, the image indexes are not required to be set. Regardless of the input source, the pattern definition must be set.

If the mailbox is opened to define the flash image indexes, list the index numbers in the mailbox. For example, if image indexes 0 through 3 are desired, write 0x0 0x1 0x2 0x3 to the mailbox. Similarly, if the desired image index sequence is 0, 1, 2, 1, then write 0x0 0x1 0x2 0x1 to the mailbox.

Table 2-68. Pattern Display LUT Data: Image Index Command

BYTE	BITS	DESCRIPTION	RESET	TYPE
0	7:0	Image index (0 based index)	x0	W

If the mailbox is opened to define the individual patterns, write three bytes of data per pattern to the mailbox.

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Table 2-69. Pattern Display LUT Data:Pattern Definition Command

BYTE	BITS	DESCRIPTION	RESET	TYPE
0	1:0	Select the trigger type for the pattern	LUT Entries [1] x042120 x002124 x002128 x00212C x002130 x002134 x002138 x00213C x002100 x002104 x002108 x00210C x002110 x002114 x002118 x00211C x002140 x002144 x002148 x00214C x002150 x002154	W
		b00 = Internal		
		b01 = External positive		
		b10 = External negative		
		b11 = No input trigger (continue from previous; pattern still has full exposure time)		
	7:2	Pattern number (0 based index). For pattern number 0x3F, there is no pattern display. The maximum number supported is 24 for 1 bit-depth patterns. Setting the pattern number to 25 with a bit-depth of 1 inserts a white-fill pattern. Inverting this pattern inserts a black-fill pattern. These patterns have the same exposure time as defined in the Pattern Display Exposure and Frame Period command. shows which bit planes are illuminated by each pattern number.		W
1	3:0	Select desired bit-depth		W
		b0000 = Reserved		
		b0001 = 1 bit		
		b0010 = 2 bit		
		...		
		b1000 = 8 bit		
		0x9-0xF = Reserved		
	7:4	Choose the LEDs that are on: b0 = Red, b1 = Green, b2 = Blue		W
		b000 = No LED (pass through)		
		b001 = Red		
		b010 = Green		
		b011 = Yellow (green + red)		
		b100 = Blue		
		b101 = Magenta (blue + red)		
		b110 = Cyan (blue + green)		
		b111 = White (blue + green + red)		
2	0	0 = Do not invert pattern		W
		1 = Invert pattern		
	1	0 = Do not insert any post pattern		W
		1 = Insert black-fill pattern after current pattern. This setting requires 230 µs of time before the start of the next pattern.		
	2	0 = Do not perform a buffer swap		W
		1 = Perform a buffer swap		
	3	0 = Trigger Out 1 has a rising edge at the start of a pattern and a falling edge at the end of the pattern		W
		1 = Trigger Out 1 continues to be high. There is no falling edge between the end of the previous pattern and the start of the current pattern. Exposure time is shared between all patterns defined under a common trigger out). This setting cannot be combined with the black-fill pattern (byte 2, bit 1).		
	7:4	Reserved		R

(1) The default LUT entries are listed. Each hex value describes an individual pattern (bytes 2:0).

Table 2-70 lists the mapping between the DLPC350 24-bit RGB interface and the expected image contents of the display sequence. For example, when displaying an 8-bit pattern, three patterns are inputted through the 24-bit RGB interface. One pattern is streamed through the green data pins, a second pattern is streamed through the red data pins, and a third pattern is streamed through the blue data pins. When displaying a 1-bit pattern, 24 patterns are inputted through the 24-bit RGB interface, with each pattern streamed through a bit of this interface.

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Table 2-70. Pattern Number Mapping

PATTERN NUMBER	1-BIT	2-BIT	3-BIT	4-BIT	5-BIT	6-BIT	7-BIT	8-BIT
0	G0	G1 G0	G2 G1 G0	G3 G2 G1 G0	G5 G4 G3 G2 G1	G5 G4 G3 G2 G1 G0	G7 G6 G5 G4 G3 G2 G1	G7 G6 G5 G4 G3 G2 G1 G0
1	G1	G3 G2	G5 G4 G3	G7 G6 G5 G4	R3 R2 R1 R0 G7	R3 R2 R1 R0 G7 G6	R7 R6 R5 R4 R3 R2 R1	R7 R6 R5 R4 R3 R2 R1 R0
2	G2	G5 G4	R0 G7 G6	R3 R2 R1 R0	B1 B0 R7 R6 R5	B1 B0 R7 R6 R5 R4	B7 B6 B5 B4 B3 B2 B1	B7 B6 B5 B4 B3 B2 B1 B0
3	G3	G7 G6	R3 R2 R1	R7 R6 R5 R4	B7 B6 B5 B4 B3	B7 B6 B5 B4 B3 B2		
4	G4	R1 R0	R6 R5 R4	B3 B2 B1 B0				
5	G5	R3 R2	B1 B0 R7	B7 B6 B5 B4				
6	G6	R5 R4	B4 B3 B2					
7	G7	R7 R6	B7 B6 B5					
8	R0	B1 B0						
9	R1	B3 B2						
10	R2	B5 B4						
11	R3	B7 B6						
12	R4							
13	R5							
14	R6							
15	R7							
16	B0							
17	B1							
18	B2							
19	B3							
20	B4							
21	B5							
22	B6							
23	B7							
24	Black							

2.4.3.4.10 Pattern Display Variable Exposure LUT Offset Pointer

(**I²C**: 0x5C)

(**USB**: CMD2: 0x1A, CMD3: 0x3F)

The Pattern Display Variable Exposure LUT Offset Pointer defines the location of the variable exposure LUT entries in the memory of the DLPC350.

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Table 2-71. Pattern Display Variable Exposure LUT Offset Pointer Command

BYTE	BITS	DESCRIPTION	RESET	TYPE
1:0	10:0	Defines the offset of the LUT entries within the data mailbox. (ranging from 0 to 1823) 0 = First entry 1 = Second entry : 1823 = Last entry	x0	W
	15:11	Reserved	x0	W

2.4.3.4.11 Pattern Display Variable Exposure LUT Control

(**I²C**: 0x5B)

(**USB**: CMD2: 0x1A, CMD3: 0x40)

The Pattern Display Variable Exposure LUT Control Command controls the execution of patterns stored in the lookup table. Before executing this command, stop the current pattern sequence. After executing this command, send the Validation command (I^2C: 0x7D or USB: 0x1A1A) once before starting the pattern sequence.

Table 2-72. Pattern Display Variable Exposure LUT Control Command

BYTE	BITS	DESCRIPTION	RESET	TYPE
1:0	10:0	Number of LUT entries. Value + 1 (ranging from 1 to 1824)	x0	WR
		0 = One entry		
		1 = Two entries		
		—		
		1823 = 1824 entries		
	15:11	Reserved	x0	R
3:2	10:0	Number of patterns to display. Value + 1 (ranging from 1 to 1824). If in repeat mode (byte 5, bit 0), then this value dictates how often TRIG_OUT_2 is generated.	x0	WR
	15:11	Reserved	x0	R
4	7:0	Number of Image Index LUT Entries. Value + 1 (ranging from 1 to 256). Field is irrelevant for Pattern Display Data Input Source set to value other than 0x3.	x0	WR
5	5:0	Repeat pattern sequence 0 = Execute the pattern sequence once 1 = Always repeat the pattern sequence once a sequence is completed	x0	WR
	7:6	Reserved	x0	R

2.4.3.4.12 Pattern Display Variable Exposure LUT Data

(**I²C**: 0x5D)

(**USB**: CMD2: 0x1A, CMD3: 0x3E)

The following parameters: display pattern mode, display data input source, variable exposure trigger mode, variable exposure access control, variable exposure LUT control, and variable exposure offset pointer control must be set-up before sending any mailbox data. For each LUT entry that is sent, the variable exposure offset pointer must be incremented. See Figure 2-12 for an example of sending a variable exposure pattern sequence. If the Pattern Display Data Input Source is set to streaming, the image indexes are not required to be set. Regardless of the input source, the pattern definition must be set.

If the mailbox is opened to define the flash image indexes, list the index numbers in the mailbox. For example, if image indexes 0 through 3 are desired, write 0x0 0x1 0x2 0x3 to the mailbox. Similarly, if the desired image index sequence is 0, 1, 2, 1, then write 0x0 0x1 0x2 0x1 to the mailbox.

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Table 2-73. Pattern Display Variable Exposure LUT Data Command

BYTE	BITS	DESCRIPTION	RESET	TYPE
0	1:0	Select the trigger type for the pattern	x0	WR
		b00 = Internal		
		b01 = External positive		
		b10 = External negative		
		b11 = No input trigger (continue from previous; pattern still has full exposure time)		
	7:2	Pattern number (0 based index). For pattern number 0x3F, there is no pattern display. The maximum number supported is 24 for 1 bit-depth patterns. Setting the pattern number to 25 with a bit-depth of 1 inserts a white-fill pattern. Inverting this pattern inserts a black-fill pattern. shows which bit planes are illuminated by each pattern number.		WR
1	3:0	Select desired bit-depth		WR
		b0000 = Reserved		
		b0001 = 1 bit		
		b0010 = 2 bit		
		—		
		b1000 = 8 bit		
		0x9-0xF = Reserved		
	7:4	Choose the LEDs that are on: b0 = Red, b1 = Green, b2 = Blue		WR
		b000 = No LED (pass through)		
		b001 = Red		
		b010 = Green		
		b011 = Yellow (green + red)		
		b100 = Blue		
		b101 = Magenta (blue + red)		
		b110 = Cyan (blue + green)		
		b111 = White (blue + green + red)		
2	0	0 = Do not invert pattern		WR
		1 = Invert pattern		
	1	0 = Do not insert any post pattern		WR
		1 = Insert black-fill pattern after current pattern. This setting requires 230 µs of time before the start of the next pattern.		
	2	0 = Do not perform a buffer swap		WR
		1 = Perform a buffer swap		
	3	0 = Trigger Out 1 has a rising edge at the start of a pattern and a falling edge at the end of the pattern		WR
		1 = Trigger Out 1 continues to be high. There is no falling edge between the end of the previous pattern and the start of the current pattern. Exposure time is retained for each pattern. This setting cannot be combined with the black-fill pattern (byte 2, bit 1).		
	7:4	Reserved		R
3	7:0	Reserved		R
7:4	31:0	Exposure period of the pattern (µs)		WR
11:8	31:0	Frame period of the pattern (µs)		WR

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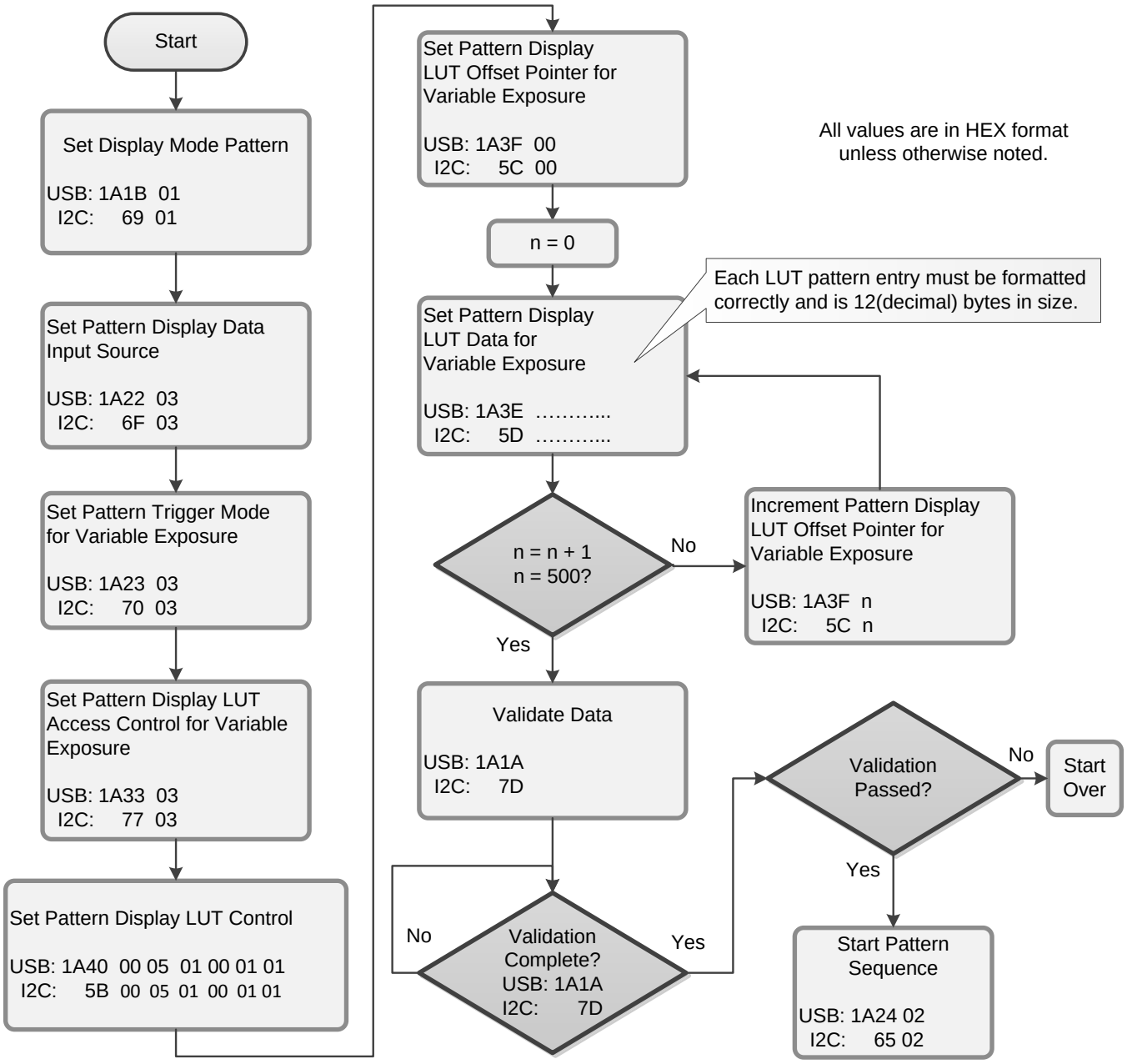

Figure 2-12. Flowchart Example for Programming 1280 Variable Exposures

2.4.3.4.13 Read Firmware Tag Info

(**I²C**: 0x5E)

(**USB**: CMD2: 0x1A, CMD3: 0xFF)

This command retrieves firmware tag (up to 32 bytes) information stored in the flash. This is useful in identifying multiple DLPC350 firmware builds having different patterns and configuration settings.

Table 2-74. Read Firmware Tag Info Command

BYTE	BITS	DESCRIPTION	RESET	TYPE
31-0	N/A	Firmware tag ASCII bytes	N/A	R

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Note: The firmware tag information is stored using DLP LightCrafter 4500 evaluation module (EVM) GUI v3.0 and later under Firmware Build option. See http://www.ti.com/tool/dlplcr4500evm.

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Power-Up, Power-Down and Initialization Considerations

This chapter describes the initial power-up and power-down considerations, and other initialization considerations.

3.1 Power Up

The DLPC350 is initialized and ready to process commands 0.1 seconds after the signal $\overline{\text{RESET}}$ is driven high. Detailed power-up timing is provided in the DLPC350 data sheet, DLPS029.

3.2 Power Down

No commands are required at power down of the DLPC350. The DC power supplies must be turned off, and PWRGOOD must be set low, according to the timing in the DLPC350 data sheet, DLPS029.

3.3 Power-Up Auto-Initialization

Upon release of system reset, the DLPC350 executes an auto-initialization routine that is automatically uploaded from flash. This initialization process consists of setting specific register configurations, uploading specific configuration tables (such as sequence), displaying a defined splash screen. The goal of the auto-initialization process is to allow the DLPC350 to fully configure itself for default operation with no external I^2C control.

An *auto-initialization* status flag (INIT_DONE), is held high to indicate that auto-initialization is in progress. It is set low when auto-initialization is complete. Subsequently, INIT_DONE is configured as an output interrupt signal that outputs an active high pulse when an error condition exists. Additionally, after INIT_DONE is set low, the EXT_PWR_ON signal is set high to indicate to the host processor or power supply that the DLPC350 is powered on.

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Pattern Display Mode Examples

4.1 Pattern Display Mode Example

The following table lists how to set up pattern sequences.

Table 4-1. Pattern Display Mode Example

STEP	I2C[1]	USB[1]		DATA [1]	DESCRIPTION
		CMD2	CMD3		
1	69	1A	1B	01	Set display to pattern mode.
2	6F	1A	22	03 Flash Memory	Set pattern display from flash memory
				00 External Video	Set pattern display from external video
3	75	1A	31	Byte 0	Number of LUT entries
				Byte 1	Setting 0x00 means the pattern sequence is executed once; setting 0x01 means the pattern sequence is repeated.
				Byte 2	Determines the number of patterns in the pattern sequence (how many patterns between Trigger Out2 pulses)
				Byte 3	If pattern display mode (step 2) is set to flash memory this indicates the number of flash images used as patterns
4	70	1A	23	00	Mode 0
				01	Mode 1
				02	Mode 2
5	66	1A	29	8 bytes	Set the exposure (four bytes) and fame rate (four bytes)
6	Set up the image indexes if using images from flash memory				
	77	1A	33	01	Open mailbox
	76	1A	32		Set mailbox offset
	78	1A	34		Set image indexes. Selecting one or two image indexes pre-fills the buffer
	77	1A	33	00	Close mailbox

(1) All bytes are in HEX notation.

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Table 4-1. Pattern Display Mode Example (continued)

STEP	I2C[1]	USB[1]		DATA [1]	DESCRIPTION
7	Set up the LUT				
	77	1A	33	01	Open mailbox
	76	1A	32		Set mailbox offset
	78	1A	34	1. Byte 0, b1:0, choose trigger: internal (0x00), external positive (0x01), external negative (0x02), continue from previous (0x03) 2. Byte 0, b7:2, choose pattern number (what bit planes will be illuminated). Max is 24 for 1 bit-depth 3. Byte 1, b3:0, choose bit weight (1 to 8) 4. Byte 1, b6:4, choose which LEDs are on (blue, green, red) 5. Byte 2: (a) b0: Invert pattern if 1 (b) b1: Insert black pattern after current pattern if 1 (must be 0 if continuous trigger) (c) b2: Perform buffer swap if 1 (d) b3: Trigger out1 stays high (if this stays high for n patterns, then exposure time is shared between n patterns)	Repeat these steps (fill pattern data) for each pattern in the sequence
	77	1A	33	00	Close mailbox
8	7D	1A	1A	00	Write Validate command.
9	7D	1A	1A	Read one byte	Read validation status and check response flags. See Table 2-52 for response flags. If validation passed, proceed to step 10. Otherwise, check all steps above are correctly defined and start over.
10	65	1A	24	02	Validation passed. Start pattern sequence with command 0x1A24
11	65	1A	24	00	Send this command to stop the pattern sequence.

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4.2 Trigger Mode 0 Example

The following table lists how to set up Trigger Mode 0.

Table 4-2. Trigger Mode 0 Example

Step	I2C[1]	USB[1]		Data[1]	Description
		CMD2	CMD3		
1	69	1A	1B	01	Set display to pattern mode.
2	6F	1A	22	00	Set pattern display from External Video
3	75	1A	31	0C 01 03 00	Byte 0: Number of LUT entries
					Byte 1: Repeat the pattern sequence
					Byte 2: Determines the number of patterns in the pattern sequence (how many patterns between trigger out2 pulses)
					Byte 3: If pattern display mode (step 2) is set to flash memory this indicates the number of flash images used as patterns
4	70	1A	23	00	Mode 0: Pattern Trigger mode = VSYNC
5	66	1A	29	8 bytes	Set the exposure and frame rate (4 bytes for each) so that the time between vsync triggers will allow three patterns to be shown For example, for a 60-Hz vsync, the maximum exposure time is 16667 ÷ 3.
6	Set up the image indexes if using images from flash memory				
	77	1A	33	02	Open mailbox for LUT
	76	1A	32		Set mailbox offset
	78	1A	34	1. Byte 0, b1:0, choose trigger. The first pattern in the sequence must have an external positive trigger. The next patterns in the sequence must be set to the continuous trigger. 2. Byte 0, b7:2, choose pattern number (what bit planes will be illuminated). Max is 24 for 1 bit-depth 3. Byte 1, b3:0, choose bit weight (1 to 8) 4. Byte 1, b6:4, choose which LEDs are on (blue, green, red) 5. Byte 2 (a) b0: invert pattern if 1 (b) b1: insert black pattern after current pattern if 1 (must be 0 if continuous trigger) (c) b2: perform buffer swap if 1 (this must be done at every external positive trigger in streaming mode) (d) b3: trigger out1 stays high (if this stays high for n patterns, then exposure time is shared between n patterns) 6. Repeat these steps (fill pattern data) for each pattern in the sequence. The LUT for this example is: 0x62101 0x21107 0x0410B 0x8110B 0xA210B 0x27117 0x41119 0x8311B 0x27123 0x02127 0x84127 0x2612F 0x61131	
	77	1A	33	00	Close mailbox
7	7D	1A	1A	00	Write Validate command.

(1) All bytes are in HEX notation.

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Table 4-2. Trigger Mode 0 Example (continued)

Step	I2C[(1)]	USB[(1)]		Data[(1)]	Description
8	7D	1A	1A	Read one byte	Read Validation status and check response flags. See Table 2-52 for response flags. If validation passed, proceed to step 10, otherwise check all steps above are correctly defined and start over.
9	65	1A	24	02	Validation Passed. Start pattern sequence with command 0x1A24
10	65	1A	24	00	Send this command to stop the pattern sequence.

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4.3 Variable Exposure Pattern Sequence Example

The following table lists how to program three variable exposures using three images from flash.

Table 4-3. Variable Exposure Pattern Mode Example

STEP	I2C[1]	USB[1]		DATA[1]	DESCRIPTION
		CMD2	CMD3		
1	69	1A	1B	01	Set display to pattern mode.
2	6F	1A	22	03	Set pattern display from flash memory.
3	70	1A	23	03	Set trigger mode for internally triggered for variable exposure.
4	77	1A	33	03	Set pattern access for variable exposure.
5	5B	1A	40	02 00 02 00 02 01	Set the pattern definition for the variable exposures. 3 exposure patterns, 3 patterns to display, 3 images from flash, always repeat.
6	5C	1A	3F	00 00	Set offset pointer: Initialize to 0.
7	5D	1A	3E	00 28 06 00 E8 80 00 00 40 0D 03 00	Pattern Data: Internal trigger, Image index 0, Green LED, 8 bit-depth, Insert black, buffer swap, exposure = 33 ms, period = 200 ms.
B	5C	1A	3F	01 00	Offset pointer: Increment by 1.
9	5D	1A	3E	04 18 06 00 A8 61 00 00 38 32 04 00	Pattern Data: Internal trigger, Image index 1, Red LED, 8 bit-depth, Insert black, Buffer swap, Exposure = 25ms, Period = 275ms.
10	5C	1A	3F	02 00	Offset Pointer: Increment by 1.
11	5D	1A	3E	08 48 06 00 C8 AF 00 00 E0 93 04 00	Pattern Data: Internal trigger, Image index 2, Blue LED, 8 bit-depth, Insert black, Buffer swap, Exposure = 45ms, Period = 300ms.
12	77	1A	33	00	Close the mailbox access.
13	5C	1A	3F	00 00	Set offset pointer: Initialize to 0.
14	77	1A	33	01	Set splash mailbox access.
15	76	1A	32	00	Set offset pointer: Initialize to 0.
16	78	1A	34	00 01 02	Splash index data.[2]
17	77	1A	33	00	Close the mailbox access.
18	7D	1A	1A	00	Write Validate command.
19	7D	1A	1A	Read one byte	Read Validation status and check response flags. See Table 2-52 for response flags.
20	7D	1A	1A	Read one byte	Read Validation status and check response flags. See Table 2-52 for response flags. If validation passed, proceed to step 21. Otherwise, check all steps above are correctly defined and start over.
21	65	1A	24	02	Validation Passed. Start pattern sequence.
22	65	1A	24	00	Send this command to stop the pattern sequence.

(1) All bytes are in HEX notation.
(2) There must be at least three pattern images in flash memory.

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4.4 Variable Exposure Video Streaming Pattern Sequence Example

The following table shows how to program three variable exposures using images from video input.

Table 4-4. Variable Exposure Video Streaming Pattern Mode Example

Step	I2C[1]	USB[1]		Data[1]	Description
		CMD2	CMD3		
1	69	1A	1B	01	Set display to pattern mode.
2	6F	1A	22	00	Set pattern display from video input source.
3	70	1A	23	04	Set trigger mode for VSYNC triggered for variable exposure.
4	77	1A	33	03	Set pattern access for variable exposure.
5	5B	1A	40	02 00 02 00 00 01	Set the pattern definition for the variable exposures. 3 exposure patterns, 3 patterns to display, always repeat.
6	5C	1A	3F	00 00	Set offset pointer: Initialize to 0.
7	5D	1A	3E	01 28 06 00 34 21 00 00 34 21 00 00	Pattern Data: External positive trigger, Image index 0, Green LED, 8 bit-depth, Insert black, Buffer swap, Exposure =8.5ms, Period = 8.5ms.
8	5C	1A	3F	01 00	Offset Pointer: Increment by 1.
9	5D	1A	3E	07 17 06 00 94 11 00 00 94 11 00 00	Pattern Data: Continue from previous trigger, Image index 1, Red LED, 7 bit-depth, Insert black, Buffer swap, Exposure = 4.5ms, Period = 4.5ms.
10	5C	1A	3F	02 00	Offset Pointer: Increment by 1.
11	5D	1A	3E	07 46 06 00 C4 09 00 00 C4 09 00 00	Pattern Data: Continue from previous trigger, Image index 2, Blue LED, 6 bit-depth, Insert black, Buffer swap, Exposure = 2.5ms, Period = 2.5ms.
12	77	1A	33	00	Close the mailbox access.
13	7D	1A	1A	00	Write Validate command. [2]
14	7D	1A	1A	Read one byte	Read Validation status and check response flags. See Table 2-52 for response flags.
15	7D	1A	1A	Read one byte	Read Validation status and check response flags. See Table 2-52 for response flags. If validation passed, proceed to step 16, otherwise check all steps above are correctly defined and start over.
16	65	1A	24	02	Validation Passed. Start pattern sequence.
17	65	1A	24	00	Send this command to stop the pattern sequence.

(1) All bytes are in HEX notation.
(2) A video source must be connect before performing this step.

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Register Quick Reference

This appendix provides a quick reference summary of all available registers.

A.1 I²C Register Quick Reference

Table A-1. Register Quick Reference

I²C Address	Description	Type	Reset Value	Default Action
0x00	Input Source Select	WR	0x8	24-bit parallel interface
0x02	Pixel Format	WR	0x0	RGB 4:4:4
0x03	Port Clock Select	WR	0x0	Port clock A
0x04	Channel Swap	WR	0x4	ABC = BAC
0x05	FPD Mode	WR	0x20	Pixel Mapping Mode 2 with FPD-Link output mapped from CONT1 onto Field Signal for FPD-Link interface port
0x06	Curtain Color Control	WR	0x0 0x0 0x0 0x0 0x0 0x0	Curtain is black
0x07	Power Control	WR	0x0	Normal operation
0x08	Long Axis Flip	WR	0x0	Flip disabled
0x09	Short Axis Flip	WR	0x0	Flip disabled
0x0A	Test Pattern Select	WR	0x8	RGB ramp
0x0B	LED PWM Polarity	WR	0x0	Normal polarity
0x10	LED Enable	WR	0x8	LEDs controlled by Sequencer
0x11	Get Version	R	0x00010100	Version 1.1.0
0x13	Reset	W	0x0	N/A
0x14	DMD Park/Un-park	WR	0x0	N/A
0x1A	Test Pattern Color	WR	0x3FF 0x3FF 0x3FF 0x0 0x0 0x0	White foreground, black background
0x20	Hardware Status	R	0x1	No errors
0x21	System Status	R	0x1	No errors
0x22	Main Status	R	0x0	No errors
0x26	CSC Data	WR	0x400 0x0 0x0 0x0 0x400 0x0 0x0 0x0 0x400	RGB 4:4:4 Color-Space Coefficients
0x31	Gamma Control	WR	0x8	Gamma Correction Enabled
0x40	PWM Enable	WR	Channel dependent	Channel dependent
0x41	PWM Setup	WR	Channel dependent	Channel dependent
0x43	PWM Capture	WR	Channel dependent	Channel dependent
0x44	GPIO Configuration	WR	Channel dependent	Channel dependent
0x48	Clock Configuration	WR	Channel dependent	Channel dependent

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Table A-1. Register Quick Reference (continued)

I²C Address	Description	Type	Reset Value	Default Action
0x4B	LED Current	WR	0x97 0x78 0x7D	LED PWMs
0x4E	PWM Capture Read	R	Channel Dependent	Channel dependent
0x61	Image Load Timing	WR	0x0	N/A
0x65	Pattern Start/Stop	WR	0x0	Pattern stopped
0x66	Pattern Exposure/Frame Rate Period	WR	0x4010 0x411A	100-ms Exposure with 100-ms frame rate
0x69	Display Mode	WR	0x0	Video Mode (Opposed to Pattern Display Mode)
0x6A	Trigger Out 1 Control	WR	0x0 0xBB 0xBB	Normal Polarity with no rising or falling delay
0x6B	Trigger Out 2 Control	WR	0x0 0xBB	Normal Polarity with no rising delay
0x6C	Red Enable Delay	WR	0xBB 0xBB	No rising or falling delay
0x6D	Green Enable Delay	WR	0xBB 0xBB	No rising or falling delay
0x6E	Blue Enable Delay	WR	0xBB 0xBB	No rising or falling delay
0x6F	Pattern Display Mode	WR	0x3	Display Patterns from flash
0x70	Pattern Trigger Mode	WR	0x1	Control Pattern Sequence with internal or external trigger
0x71	Buffer Swap	WR	0x0	No Buffer Swap Performed
0x72	Buffer Write Disable	WR	0x0	Buffer Write Enabled
0x73	Current Read Buffer	WR	0x0	Current Buffer Streaming to DMD is Buffer number 0
0x74	Invert Data	WR	0x0	Normal operation
0x75	Pattern Configuration	WR	0x17 0x1 0x17 0x0	24 LUT Entries to be Repeated in a Pattern Sequence of Length 24, From 1 Flash Image
0x76	Mailbox Address	W	0x0	No Offset to LUT Location
0x77	Mailbox Control	W	0x0	Malbox closed
0x78	Mailbox Data	W	See Command Description	See Command Description
0x79	Trigger In 1 Control	WR	0x0	No delay
0x7A	Trigger In 2 Control	WR	0x0	Advance Pattern Pair on Rising Edge (for Trigger Mode 2)
0x7C	Buffer Freeze	WR	0x1	Disable Buffer Swapping
0x7D	Validate	R	0x0	Pattern Display Mode Settings are valid
0x7E	Manual Input Display Resolution	WR	0x0 0x0 0x0 0x0 0x0 0x0 0x500 0x320	Output Display Resolution is 1280 × 800
0x7F	Image Load	WR	0xFF	Last Image Index
Supported Commands in Firmware Version 2.0.0 or Greater				
0x5B	Pattern Display Variable Exposure LUT Control	WR	0x0 0x0 0x0 0x0 0x0 0x0	N/A
0x5C	Pattern Display Variable Exposure LUT Offset Pointer	WR	0x0 0x0	N/A
0x5D	Pattern Display Variable Exposure LUT Data	W	All 0x0	N/A
0x01	Input Video Signal Detection Status	R	0x0 0x0	N/A
0x62	Retrieve Image Resolution Information	WR	All 0x0	N/A
Supported Commands in Firmware Version 3.0.0 or Greater				
0x0C	Get number of images in the flash	R	N/A	Reads number of 24-bit images stored in the flash

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Table A-1. Register Quick Reference (continued)

I²C Address	Description	Type	Reset Value	Default Action
0x5E	Read Firmware Tag Info	R	N/A	Reads 32 bytes
0x3A	I2C0 Master Read/Write Error Response	R	0x00	Error, if any, for the requested action on the I2C0 port
0x7B	I2C0 Master Port Control Command	WR	0x00	DLPC350 as I2C Master on I2C0 Port; send and receive any commands to any slave connected on I2C0

A.2 Command Guide

This section shows which commands can be used in which modes. I²C control commands are accepted in any order, except when special sequencing is required (for example, setting up the flash).

Table A-2. Command Matrix

Command Name	I2C	USB	Number of Bytes	External Video Mode	Flash Image Mode	Test Pattern Mode	Pattern Streaming Mode	Patterns from Flash Mode
Input Source Select	0x00	0x1A00	1	x	x	x	x	x
Pixel Format	0x02	0x1A02	1	x			x	
Port Clock Select	0x03	0x1A03	1	x			x	
Channel Swap	0x04	0x1A37	1	x			x	
FPD Mode	0x05	0x1A04	1	x			x	
Curtain Color Control	0x06	0x1100	6	x			x	
Power Control	0x07	0x0200	1	x	x	x	x	x
Long Axis Flip	0x08	0x1008	1	x	x	x	x	x
Short Axis Flip	0x09	0x1009	1	x	x	x	x	x
Test Pattern Select	0x0A	0x1203	1	x	x	x		
LED PWM Polarity	0x0B	0x1A05	1	x	x	x	x	x
LED Enable	0x10	0x1A07	1	x	x	x	x	x
Get Version	0x11	0x0205	16	x	x	x	x	x
Reset	0x13	0x0802	1	x	x	x	x	x
Test Pattern Color	0x1A	0x1204	12			x		
Hardware Status	0x20	0x1A0A	1	x	x	x	x	x
System Status	0x21	0x1A0B	1	x	x	x	x	x
Main Status	0x22	0x1A0C	1	x	x	x	x	x
CSC Data	0x26	0x1A0D	18	x			x	
Gamma Control	0x31	0x1A0E	1	x	x	x		
PWM Enable	0x40	0x1A10	1	x	x	x	x	x
PWM Setup	0x41	0x1A11	6	x	x	x	x	x
PWM Capture	0x43	0x1A12	5	x	x	x	x	x
GPIO Configuration	0x44	0x1A38	2	x	x	x	x	x
Clock Configuration	0x48	0x0807	2	x	x	x	x	x
LED Current	0x4B	0x0B01	3	x	x	x	x	x
PWM Capture Read	0x4E	0x1A13	5	x	x	x	x	x

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Table A-2. Command Matrix (continued)

Command Name	I2C	USB	Number of Bytes	External Video Mode	Flash Image Mode	Test Pattern Mode	Pattern Streaming Mode	Patterns from Flash Mode
Image Load Timing	0x61	0x1A3A	4	x		x	x	x
Pattern Start/Stop	0x65	0x1A24	1				x	x
Pattern Exposure/Frame Rate Period	0x66	0x1A29	8				x	x
Display Mode	0x69	0x1A1B	1	x	x	x	x	x
Trigger Out 1 Control	0x6A	0x1A1D	3				x	x
Trigger Out 2 Control	0x6B	0x1A1E	2				x	x
Red Enable Delay	0x6C	0x1A1F	2				x	x
Green Enable Delay	0x6D	0x1A20	2				x	x
Blue Enable Delay	0x6E	0x1A21	2				x	x
Pattern Display Mode	0x6F	0x1A22	1				x	x
Pattern Trigger Mode	0x70	0x1A23	1				x	x
Buffer Swap	0x71	0x1A26	1	x	x	x	x	x
Buffer Write Disable	0x72	0x1A27	1	x	x	x	x	x
Current Read Buffer	0x73	0x1A28	1	x	x	x	x	x
Invert Data	0x74	0x1A30	1				x	x
Pattern Configuration	0x75	0x1A31	4				x	x
Mailbox Address	0x76	0x1A32	1				x	x
Mailbox Control	0x77	0x1A33	1				x	x
Mailbox Data	0x78	0x1A34	4				x	x
Trigger In 1 Control	0x79	0x1A35	4				x	x
Trigger In 2 Control	0x7A	0x1A36	1				x	x
Buffer Freeze	0x7C	0x100A	1	x	x	x	x	x
Validate	0x7D	0x1A1A	1				x	x
Manual Input Display Resolution	0x7E	0x1000	16	x				
Image Load	0x7F	0x1A39	1	x	x	x		x
Supported Commands in Firmware Version 2.0.0 or Greater								
Pattern Display Variable Exposure LUT Data	0x5D	0x1A3E	12				x	x
Pattern Display Variable Exposure LUT Offset Pointer	0x5C	0x1A3F	2				x	x
Pattern Display Variable Exposure LUT Control	0x5B	0x1A40	6				x	x
Input Video Signal Detection Status	0x01	0x071C	28	x			x	

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Table A-2. Command Matrix (continued)

Command Name	I2C	USB	Number of Bytes	External Video Mode	Flash Image Mode	Test Pattern Mode	Pattern Streaming Mode	Patterns from Flash Mode
Retrieve Image Resolution Information	0x62	0x1A41	2 and (4 * number of images)	x	x		x	x
Supported Commands in Firmware Version 3.0.0 or Greater								
Get number of images in the flash	0x0C	0x1A42	1	x	x	x	x	x
Read Firmware Tag Info	0x5E	0x1AFF	32	x	x	x	x	x
I2C0 Master Read/Write Error Response	0x3A	0x1A43	1	x	x	x	x	x
I2C0 Master Port Control Command	0x7B	0x1A3B	variable	x	x	x	x	x

A.3 DLPC350 Programming Commands

The Programming commands manage downloading a new firmware image into flash memory. This can be done with I^{2}C or USB communication. The commands in the DLPC350 Programming Commands section are only valid in program mode except for Enter Program Mode (**I^{2}C**: 0x30), which exits normal mode and enters program mode. The user must issue the proper Exit Program Mode (**I^{2}C**: 0x30) command to return to normal mode. While in program mode, commands outside of this section will not work.

NOTE: When issuing a write in programming mode (see Section 1.1.3 **I2C Write Transaction Sequence**), the read/write bit must not be set for the write transactions.

A.3.1 Read Control

(**I^{2}C**: 0x15)

(**USB**: CMD2: 0x00, CMD3: 0x15)

This command reads the Flash Manufacturer and Device IDs and Checksum.

Table A-3. Query Flash IDs Command

BYTE	BITS	DESCRIPTION	RESET	TYPE
0	3:0	ID 0x00 = Returns Checksum[(1)(2)] 0x0C = Requests Flash Manufacturer ID[(3)] 0x0D = Requests Flash Device ID[(4)]	d0	r
	7:4	Reserved		

(1) To read the Checksum, the Calculate Checksum command (I2C: 0x26) must be issued first.
(2) The Return Checksum command can be sent at any time to read the general status information through status BYTE0 and BYTE1 of the boot loader application.
(3) To query the Manufacturer Device ID, write register 0x15 with the value 0x0C. Then read the required number of data bytes back from register 0x15 (as defined in Table A-4)
(4) To query the Flash Device ID, write register 0x15 with the value 0x0D. Then read the required number of data bytes back from register 0x15 (as defined in Table A-4)

NOTE: **Do not** perform the general status query when sending the Download Data (i.e., in middle of programming).

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Table A-4. Response to Query Flash IDs Command

BYTE	BITS	DESCRIPTION
0	2:0	Reserved
	3	Busy Bit 0 = no flash operation in progress 1 = Flash operation in progress
	6:4	Reserved
	7	Programming Mode Bit 0 = Does not allow flash programming operations 1 = Allows flash programming operations
1	7:0	Boot loader application version
2	7:0	Reserved 0x08
3	7:0	Reserved 0x48
4	7:0	Reserved 0x00
5	7:0	Reserved 0x00
Bytes 6 - 9 return Checksum, Flash Manufacturer ID, Flash Device ID - as requested by command 0x15 bits 3:0 Table A-3		
6	7:0	LSB
7	7:0	LSB+1
8	7:0	LSB+2
9	7:0	LSB+3

A.3.2 Exit Program Mode

(**I²C**: 0x30)

(**USB**: CMD2: 0x00, CMD3: 0x30)

This command tells the boot loader application to exit program mode. When called, the boot loader resets the processor and make a boot decision based on the HOLD_IN_BOOT pin. If the pin is set, it will remain in the boot loader. Otherwise, if there is a valid image in the flash area, it will jump to the main application. In normal mode, if the main application receives the exit command, the command has no effect.

Table A-5. Exit Program Mode Command

BYTE	BITS	DESCRIPTION	RESET	TYPE
0	0	1 = Exit Program Mode – Reset controller and run application	d0	w
	7:1	Reserved		

A.3.3 Start Address

(**I²C**: 0x29)

(**USB**: CMD2: 0x00, CMD3: 0x29)

The Start Address command specifies the start address for the next flash download. It is the responsibility of the user to ensure that the Start Address is on a sector boundary in the current flash device. This command must be followed by a Flash Data Size command and a Flash Erase command to completely describe the programming operation.

The start address is also used in specifying the start of a checksum operation

Table A-6. Start Address Command

BYTE	BITS	DESCRIPTION	RESET	TYPE
3:0	32:0	Flash address. Byte 0 is LSB, byte 3 is MSB.	x0	w

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A.3.4 Erase Sector

(**I²C**: 0x28)

(**USB**: CMD2: 0x00, CMD3: 0x28)

This is a system write command to erase a sector of flash memory. This command must not be executed until valid data has been written to the Flash Start Address. Users are responsible for ensuring that a valid address has been written. The Busy bit will be set in the Boot Loader status byte while the sector erase is in progress.

NOTE: TI cautions against erasing the boot sector of the device as this contains key initialization parameters and the flash programming functionality. Only the sector that contains the start address will be erased, not all sectors from the start address to the end of the device. Users must either pre-erase all sectors to be programmed, or erase and program each sector individually.

Table A-7. Sector Erase Command

BYTE	BITS	DESCRIPTION	RESET	TYPE
0	7:0	0x00 - Dummy byte for erase sector command.	x0	w

A.3.5 Download Data Size

(**I²C**: 0x2C)

(**USB**: CMD2: 0x00, CMD3: 0x2C)

System write command to specify the size of the following flash download. The data size is sent to tell the Boot Loader how many bytes to expect to program into the flash device during the current operation. It is also used for specifying the checksum range when requesting that operation.

Table A-8. Download Data Size Command

BYTE	BITS	DESCRIPTION	RESET	TYPE
3:0	32:0	Flash address. Byte 0 is LSB, byte 3 is MSB.	x0	w

A.3.6 Download Data

(**I²C**: 0x25)

(**USB**: CMD2: 0x00, CMD3: 0x25)

This command contains the flash data to be programmed. The maximum data size which can be sent in each command is 512 bytes, which corresponds to a data length of 514. The number of bytes downloaded by consecutive download data commands must match the predefined Flash Data Size for the operation to be successful.

Table A-9. Download Data Command

BYTE	BITS	DESCRIPTION	RESET	TYPE
0	7:0	Length LSB	x0	w
1	7:0	Length MSB		
513:2	4095:0	Up to 512 Data Bytes		

A.3.7 Calculate Checksum

(**I²C**: 0x26)

(**USB**: CMD2: 0x00, CMD3: 0x26)

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This command calculates the checksum. Executing this command causes the Boot Loader to read the data in the flash memory and calculate a 4-byte 8-bit checksum. The Busy bit will be set in the Boot Loader status byte while the checksum computation is in progress. After completion, the 4-byte checksum can be read back through the Read Control command. The data range to be summed is specified by writing appropriate data with the Flash Start Address and Flash Data Size commands.

Table A-10. Calculate Checksum Command

BYTE	BITS	DESCRIPTION	RESET	TYPE
0	0	1 = Calculate Checksum	d0	w
	7:1	Reserved		

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Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from F Revision (October 2016) to G Revision	Page
• Added information about USB VID and PID in Section 1.2	9
• Added Section 2.3.1.2	15
• Fixed binary/hex mislabel in Section 2.4.3.4.1	47
• Fixed binary/hex mislabel in Section 2.4.3.4.2	47
• Changed first byte of example command to correspond to the correct number of patterns in Table 4-2	61
• Fixed example in Section 4.4	64
• Added DMD Park/Un-park to Table A-1	65

Changes from E Revision (February 2015) to F Revision	Page
• Changed "0.45 WXGA chipset" to DLP4500 and DLP4500NIR chipsets"	5
• Removed reference to 0.45 WXGA chipset manual DLPU009	5
• Added reference to DLP4500NIR DMD	5
• Addded reference to DLP4500NIR datasheet DLPS032	5
• Added reference to DLPR350 "DLPC350 Configuration and Support Firmware"	5
• Changed reference to "DLP LightCrafter 4500 Develepment Platform Forum"	5
• Changed Section Section 1.1.1.2	6
• Changed Section Section 1.1.1.3	7
• Added Note referencing DLPC350 Programming Commands	8
• Changed USB enumeration description	9
• Added "Input Video Signal Detection Status"	11
• Updated normal mode programming commands section	14
• Changed Value to Enter Program Mode to 1	15
• Removed "After executing this command, poll the system status using I2C commands: 0x20, 0x21, and 0x22 or the respective USB commands: 0x1A0A, 0x1A0B, and 0x1A0C" because it is no longer necessary.	16
• Changed Table 2-16	19
• Removed "After executing this command, poll the system status using I2C commands: 0x20, 0x21, and 0x22 or the respective USB commands: 0x1A0A, 0x1A0B, and 0x1A0C" because it is no longer necessary.	20
• Removed "After executing this command, poll the system status using I2C commands: 0x20, 0x21, and 0x22 or the respective USB commands: 0x1A0A, 0x1A0B, and 0x1A0C" because it is no longer necessary.	23
• Removed "After executing this command, poll the system status using I2C commands: 0x20, 0x21, and 0x22 or the respective USB commands: 0x1A0A, 0x1A0B, and 0x1A0C" because it is no longer necessary.	23
• Removed "After executing this command, poll the system status using I2C commands: 0x20, 0x21, and 0x22 or the respective USB commands: 0x1A0A, 0x1A0B, and 0x1A0C" because it is no longer necessary.	23
• Added Get Number of Images in the Flash command 0x0C	24
• Added entry for GPIO Selection 30	30
• Added I2C0 Master Port Control command 0x7B	32
• Changed "upto" to "up to"	32
• Changed "b/w to" to "between"	33
• Added I2C0 Master Read/Write Error Response command 0x3A	33
• Changed "Video mode" to "Video display mode"	34
• Changed description of "format conversion and video enhancement blocks"	34
• Changed label on DMD to "DLP4500/DLP4500NIR"	35
• Added "(Hz)" unit	35
• Changed sentence "To improve image quality"	36
• Removed "After executing this command, poll the system status using I2C commands: 0x20, 0x21, and 0x22 or the respective USB commands: 0x1A0A, 0x1A0B, and 0x1A0C" because it is no longer necessary.	37
• Updated Gamma Correction details	38
• Removed "After executing this command, poll the system status using I2C commands: 0x20, 0x21, and 0x22 or the	

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respective USB commands: 0x1A0A, 0x1A0B, and 0x1A0C" because it is no longer necessary. 38
- Changed bits for Gamma Correction command 0x31 38
- Removed "After executing this command, poll the system status using I2C commands: 0x20, 0x21, and 0x22 or the respective USB commands: 0x1A0A, 0x1A0B, and 0x1A0C" because it is no longer necessary. 38
- Added description for updating a parameter in streaming Pattern Display mode 39
- Added warning for external trigger modes 42
- Changed from "three" to "five" Pattern Trigger Modes 42
- Removed "After executing this command, poll the system status using I2C commands: 0x20, 0x21, and 0x22 or the respective USB commands: 0x1A0A, 0x1A0B, and 0x1A0C" because it is no longer necessary. 47
- Changed note attached to Pattern Display Start/Stop Pattern Sequence Command 48
- Added units (μs) 55
- Added units (μs) 55
- Added Read Firmware Tag Info command 0x5E 56
- Updated format of Pattern Display Mode Example 59
- Changed "Display Mode Example" to "Pattern Display Mode Example" 59
- Removed "trig in2" 60
- Updated format of Trigger Mode 0 Example 61
- Changed "Target Mode 0" to "Trigger Mode 0" 61
- Changed "Target Mode 0" to "Trigger Mode 0" 61
- Removed "0x1A29" 61
- Removed previous step 7 and moved up lower steps 61
- Removed "trig in2 or" 62
- Added "Supported Commands in Firmware Version 3.0.0 or Greater" 66
- Added "Supported Commands in Firmware Version 3.0.0 or Greater" 69
- Programming mode commands moved to appendix 69
- Added Note about issuing a write in programming mode 69
- Added Table notes to Query Flash IDs Commond 69
- Added Note to 0x0D 69
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- Added Response to Query Flash IDs Command 0x15 70
- Changed value for Exit Program Mode to 1; removed line 70
- Added table "Sector Erase Command" 71
- Added table for Calculate Checksum command 0x26 72

Changes from D Revision (July 2014) to E Revision **Page**

- Changed Clock Period bytes from 3:1 to 4:1 and Duty Cycle from byte 4 to 5. 31

Changes from C Revision (April 2014) to D Revision **Page**

- Corrected upper frequency limit of I2C communication 6
- Corrected I2C read register and graphic to show only one byte 7
- Updated I2C Write Sequence and figure with 1 byte sub-address 8
- Added a note on accessing undocumented registers 11
- Added note to correct errors from Hardware Status Register 12
- Added reset for byte 3:0 for Get Version Command 13
- Added 24-bit frame buffers to example for Buffer Write Disable command 17
- Corrected formatting of FPD-Link Mode and Field Select Command table 19
- Added Parallel Port to Port Clock Select heading 20
- Adjusted Input Pixel Data Format Command formatting 21
- Added a Note about changing an image flip settings 24
- Provided an upper limit for frequency of pattern display sequences 34

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- Added note for changing Pattern Display 39
- Added note for using Validate Data Command after Pattern Display changes 39
- Corrected table title: Validate Data Command Response 40
- Added bit 7 info for validate data command table 40
- Added note about reading response byte of Validate Data Command 40
- Added clarification of when Trigger modes apply for Mode 0, 1, and 2 40
- Added new trigger modes for variable exposure in 2.4.3.2.1. 42
- Added two clarifications about delay control range to Trigger Out1 and Trigger Out2 tables 43
- Added clarifications about delay control range to Red, Green, and Blue LED Enable Control tables 45
- Added a note about stopping and starting Pattern Display Sequence 48
- Moved example of Frame Period into a Note. 48
- Added new mailbox for variable exposure in 2.4.3.4.8. 50
- Added emphasis to Pattern Display LUT Data information 51
- Added new variable exposure command in 2.4.3.4.10. 53
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- Added new variable exposure command in 2.4.3.4.12. 54
- Added flowchart example for programming a variable exposure pattern sequence. 56
- Added Read Firmware Tag Info command in 2.4.3.4.12. 56
- Added variable exposure pattern sequence example in 4.3. 63
- Added variable exposure video streaming pattern sequence example in 4.4. 64
- Added new commands to Appendix A for firmware version 2.0.0. 65
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Changes from B Revision (August 2013) to C Revision **Page**

- Updated sub-address of write example sequence 8
- Updated I2C Write Sequence figure with correct sub-address 8
- Corrected bit position for GPIO Clock Configuration command to bit 0 and 1 30
- Fixed typo in PWM Control command 30
- Added a step to disable GPIO pins before enabling PWM functionality 30
- Display Mode Selection bit was reversed between Video mode and Pattern Display mode 38
- Included a calculation of Pattern Exposure time and Frame Period 48
- Added clarification for Programming Commands section differentiating between program mode and normal mode of DLPC350 operation 69
- Changed Return Checksum command to correct Read Control command 72

Changes from A Revision (July 2013) to B Revision **Page**

- Changed Current Control Unit From 1/2 256 Steps to 256 Steps 28
- Changed Trigger Signals to follow TRIG_X_X Format 40
- Changed Description of Pattern Exposure and Frame Period 48
- Changed Description of Number of Patterns in LUT Control Command 49
- Changed Black-Fill Time from 225 µs to 230 µs 52

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- Added Input Value Bits for GPIO Configuration 29
- Added GPIO Channel Byte for PWM Capture 32
- Changed Max TRIG_OUT_1 Delays 43
- Changed Pattern Exposure and Frame Period Values 48

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- Changed Default Number of Patterns in LUT 49
- Changed Default Pattern LUT 52
- Deleted Temperature Commands from Register Quick Reference 65
- Deleted Temperature Commands from Command Matrix 67

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