DLPA2005 Power Management and LED/Lamp Driver IC

1 Features

- High Efficiency RGB LED/Lamp Driver With Buck-Boost DC-to-DC Converter, DMD Supplies, DPP Core Supply, 1.8-V Load Switch, and Measurement System in a Small Chip-Scale Package
- Three Low-Impedance (30 mΩ Typical at 27°C) MOSFET Switches for Channel Selection
- Independent, 10-Bit Current Control per Channel
- 2.4-A Max LED Current for DLPA2005 Embedded Applications
- DMD Regulators
  - Requires Only a Single Inductor
  - VOFS: 10 V
  - VBIAS: 18 V
  - VRST: –14 V
  - Passive Discharge to GND When Disabled
- DPP 1.1-V Core Supply
  - Synchronous Step-Down Converter With Integrated Switching FETs
  - Supports up to 600-mA Output Current
- VLED Buck Boost Converter
  - Power Save Mode at Light Load Current
- Low-Impedance Load Switch
  - V_{IN} Range from 1.8 to 3.6 V
  - Supports up to 200 mA of Current
  - Passive Discharge to GND When Disabled
- DMD Reset Signal Generation and Power Supply Sequencing
- 33-MHz Serial Peripheral Interface (SPI)
- Multiplexer for Measuring Analog Signals
  - Battery Voltage
  - LED Voltage, LED Current
  - Light Sensor (for White Point Correction)
  - Internal Reference Voltage
  - External (Thermistor) Temperature Sensor
- Monitoring and Protection Circuits
  - Hot Die Warning and Thermal
  - Low-Battery Warning
  - Programmable Battery Undervoltage Lockout (UVLO)
  - Load Switch UVLO
  - Overcurrent and Undervoltage Protection
- DLPA2005 QFN Package
  - 48-Pin 0.4-mm Pitch
  - Die Size: 6.0 mm × 6.0 mm ± 0.15 mm

2 Applications

DLP® Pico™ Projector

DLP® Mobile Sensing

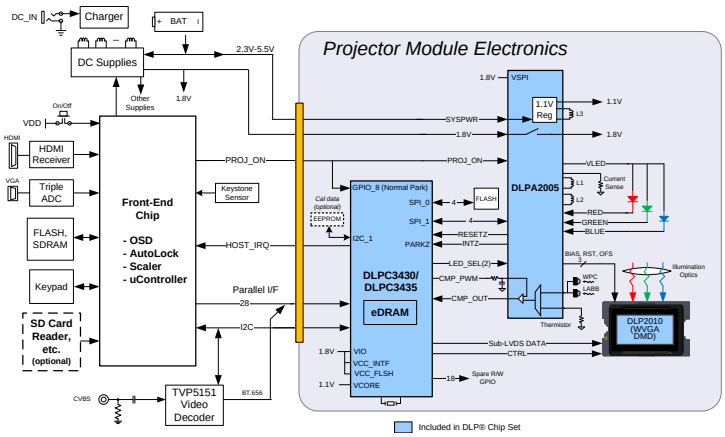
3 Description

DLPA2005 is a dedicated PMIC/RGB LED/Lamp driver for the DLP2010, DLP2010NIR and DLP3010 Digital Micromirror Devices (DMD) when used with a DLPC3430, DLPC3433, DLPC3435, DLCP3438, or DLPC150 digital controller. For reliable operation of these chipsets it is mandatory to use a DLPA2000 or DLPA2005.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DLPA2005	VQFN (48)	6.00 mm × 6.00 mm ± 0.150 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

Changes from Revision A (September 2014) to Revision B	Page
• Updated title	1
• Updated *Features*, *Applications*, and *Description*	1
• Added mobile sensing application	1
• Updated *Detailed Description*	12
• Added new Typical Mobile Sensing application in *Application Information*	38

Changes from Original (August 2014) to Revision A	Page
• Changed device status from Product preview to Production Data and released full version of the document.	1

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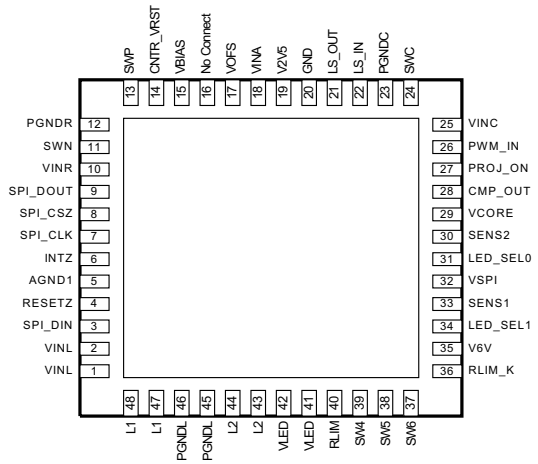
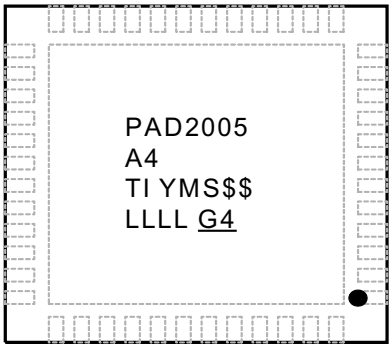
5 Pin Configuration and Functions

DLPA2005 VQFN Package
(BOTTOM VIEW)



Package Marking DLPA2005
(TOP VIEW)



TI = TI LETTERS
YM = YEAR / MONTH DATE CODE
LLLL = ASSY LOT CODE
S = ASSEMBLY SITE CODE PER QSS 005-120
$$ = WAFER FAB CODE (1 or 2 CHARACTERS)
● =pin 1 Marking

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NUMBER		
VINL	1	I	Power supply input for VLED BUCK-BOOST power stage. Connect to system power.
	2		
SPI_DIN	3	I	SPI data input
RESETZ	4	O	Reset output to the DLP system (active low). Pin is held low to reset DLP system.
AGND1	5	GND	Analog ground. Connect to ground plane.
INTZ	6	O	Interrupt output signal (open drain). Connect to pullup resistor or short to ground.
SPI_CLK	7	I	Clock input for SPI interface
SPI_CSZ	8	I	SPI chip select (active low)
SPI_DOUT	9	O	SPI data output
VINR	10	I	Power supply input for DMD switch mode power supply (SMPS). Connect to system power.
SWN	11	I	Connection for the DMD SMPS-inductor (high-side switch).
PGNDR	12	GND	Power ground for DMD SMPS. Connect to ground plane.
SWP	13	O	Connection for the DMD SMPS-inductor (low-side switch).
CNTR_VRST	14	O	Connection to VRST for fast discharge function
VBIAS	15	O	VBIAS output rail. Connect to ceramic capacitor.
No Connect	16	I	Previously reference pin for the VRST regulator. On A4 design this reference is internal to DLPA2005 chip.
VOFS	17	O	VOFS output rail. Connect to ceramic capacitor.
VINA	18	POWER	Power supply input for sensitive analog circuitry
V2V5	19	O	Internal supply filter pin for digital logic; typical 2.5 V
GND	20	GND	Ground connection to be connected to ground plane.
LS_OUT	21	O	Load switch
LS_IN	22	I	Load switch
PGNDC	23	GND	Power ground for VCORE BUCK
SWC	24	I/0	Connection for 1.1-V BUCK inductor
VINC	25	I	Power supply input for VCORE BUCK power stage. Connect to system power.
PWM_IN	26	I	Reference voltage input for analog comparator.
PROJ_ON	27	I	Input signal to enable or disable the IC and DLP projector.

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Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NUMBER		
CMP_OUT	28	O	Analog-comparator output.
VCORE	29	I	VCORE BUCK converter feedback pin.
SENS2	30	I	Input signal from temperature sensor.
LED_SEL0	31	I	Digital input to the RGB Strobe Decoder
VSPI	32	I	Power supply input for SPI interface. Connect to system I/O voltage.
SENS1	33	I	Input signal from light sensor.
LED_SEL1	34	I	Digital input to the RGB Strobe Decoder
V6V	35	O	Internal supply filter pin for gate driver circuitry. Typical 6.25 V
RLIM_K	36	I	Kelvin sense connection to top side of LED current sense resistor. For best accuracy, route this trace directly to the top of the current sense resistor and separate it from the normal trace from the current sense resistor to the RLIM pins.
SW6	37	O	Low-side MOSFET switch for LED cathode. Connect to RGB LED assembly.
SW5	38	O	Low-side MOSFET switch for LED cathode. Connect to RGB LED assembly.
SW4	39	O	Low-side MOSFET switch for LED cathode. Connect to RGB LED assembly.
RLIM	40	O	Connection to LED ‘current sense’ resistor. Bottom side of sense resistor is connected to GND.
VLED	41 / 42	O	VLED BUCK-BOOST converter output pin.
L2	43 / 44	I	Connection for VLED BUCK-BOOST inductor.
PGNDL	45 / 46	GND	Power ground for VLED BUCK-BOOST. Connect to ground plane.
L1	47 / 48	O	Connection for VLED BUCK-BOOST inductor.

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6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature (unless otherwise noted)[1]

		MIN	MAX	UNIT
	Input voltage at VINL, VINA, VINR, VINC	–0.3	7	V
	Ground pins to system ground	–0.3	0.3	V
	Voltage at SWN	–18	7	V
	Voltage at SWP, VBIAS	–0.3	20	V
	Voltage at VOFS	–0.3	12	V
	Voltage at V6V, VLED, L1, L2, SWC, SW4, SW5, SW6, INTZ, PROJ_ON	–0.3	7	V
	Voltage at all pins, unless noted otherwise	–0.3	3.6	V
	Source current RESETZ, CMP_OUT		1	mA
	Source current SPI_DOUT		5.5	mA
	Sink current RESETZ, CMP_OUT		1	mA
	Sink current SPI_DOUT, INTZ		5.5	mA
	Peak output current	Internally limited		
	Continuous total power dissipation	Internally limited by thermal shutdown		
T_J	Operating junction temperature	–30	150	°C
T^{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* . Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted).

		MIN	NOM	MAX	UNIT
Input voltage at VINL, VINA, VINR, VINC,	Full functional and parametric performance	2.7	3.6	6	V
	Extended operating range, limited parametric performance	2.3	3.6	6	
Voltage at VSPI		1.65	1.8	3.6	V
Operational ambient temperature		–10		85	°C
Operational junction temperature		–10		120	°C

6.4 Thermal Information

THERMAL METRIC[1]		DLPA2005 RSL (48 PINS)	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance[2]	27.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) Estimated when mounted on high K JEDEC board per JESD 51-7 with thickness of 1.6 mm, 4 layers, size of 76.2 mm × 114.3 mm, and 2-oz. copper for top and bottom plane. Actual thermal impedance will depend on PCB used in the application.

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6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted) (see [1][2][3])

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLIES						
INPUT VOLTAGE						
V_{IN}	Input voltage range	VINA, VINR, VINL, VINC	2.7	3.6	6	V
	Extended input voltage range[1]		2.3	3.6	6	
V_{LOW_BAT}	Low-battery warning threshold	V_{INA} falling		3		V
	Hysteresis	V_{INA} rising		100		mV
$V_{hys(UVLO)}$	Undervoltage lockout threshold	V_{INA} falling (through 5-bit trim function)	2.3		4.5	V
	Hysteresis	V_{INA} rising		100		mV
$V_{STARTUP}$	Startup voltage	VBIAS, VOFS, VRST; loaded with 2 mA	2.5			V
INPUT CURRENT						
I_Q	ACTIVE mode	Motor current excluded		15		mA
I_{STD}	STANDBY mode			900		µA
I_{IDLE}	IDLE mode			10		µA
INTERNAL SUPPLIES						
V_{V6V}	Internal supply, analog			6.25		V
C_{LDO_V6V}	Filter capacitor for V6V LDO			100		nF
V_{V2V5}	Internal supply, logic			2.5		V
C_{LDO_V2V5}	Filter capacitor for V2V5 LDO			2.2		µF
DMD REGULATOR						
$R_{DS(ON)}$	MOSFET ON-resistance	Switch E (from VINR to SWN)		1000		mΩ
		Switch F (from SWP to PGNDR)		320		
V_{FW}	Forward voltage drop	Switch G[2] (from SWP to VBIAS[2]) V_{INR} = 5 V, V_{SWP} = 2 V, I_F = 100 mA		1.3		V
		Switch H (from SWP to VOFS) V_{INR} = 5 V, V_{SWP} = 2 V, I_F = 100 mA		1.3		
t_{DIS}	Rail discharge time	V_{IN} = 2.9 V; C_{OUT} = 110 nF			40	µs
t_{PG}	Power-good timeout	Not tested in production		6		ms
I_{LIMIT}	Switch current limit			312		mA
L	Inductor value			10		µH
VOFS REGULATOR						
V_{OFS}	Output voltage			10		V
	DC output voltage accuracy	I_{OUT} = 2 mA	–2%		2%	
	DC load regulation	V_{IN} = 3.6 V, I_{OUT} = 0 to 2 mA		–19		V/A
	DC line regulation	VINA, VINL, VINR, VINC 2.7 to 6 V, I_{OUT} = 2 mA		35		mV/V
V_{RIPPLE}	Output ripple	V_{IN} = 3.6 V, I_{OUT} = 2 mA, C_{OUT} = 440 nF[4]		375		mVpp
I_{OUT}	Output current		0		3	mA
PG	Power-good threshold (fraction of nominal output voltage)	V_{OFS} rising		86%		
		V_{OFS} falling		66%		
R_{DIS}	Output discharge resistor	Active when rail is disabled		100		Ω
C_{OUT}	Output capacitor	Recommended value (output capacitors for VOFS / VBIAS must be equal)	110	220		nF
		$t_{DISCHARGE}$ < 40 µs at 2.9 V	100		110	nF

(1) Fully functional but limited parametric performance
(2) Including rectifying diode
(3) Typicals are at 25 C.
(4) To reduce ripple the C_{OUT} can be increased. V_{RIPPLE} is inversely proportional to C_{OUT}.

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Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted) (see [1][2][3])

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VBIAS REGULATOR						
V_{BIAS}	Output voltage			18		V
	DC output voltage accuracy	I_{OUT} = 2 mA	–2%		2%	
	DC Load regulation	V_{IN} = 3.6 V, I_{OUT} = 0 to 2 mA		–14		V/A
	DC Line regulation	VINA, VINL, VINR, VINC 2.7 to 6 V, I_{OUT} = 2 mA		18		mV/V
V_{RIPPLE}	Output ripple	V_{IN} = 3.6 V, I_{OUT} = 2 mA, C_{OUT} = 440 nF (see [4])		375		mVpp
I_{OUT}	Output current		0		4	mA
PG	Power-good threshold (fraction of nominal output voltage)	V_{BIAS} rising		86%		
		V_{BIAS} falling		66%		
R_{DIS}	Output discharge resistor	Active when rail is disabled		100		Ω
C_{OUT}	Output capacitor	Recommended value (output capacitors for VOFS / VBIAS must be equal)	110	220		nF
		$t_{DISCHARGE}$ < 40 µs at 2.9 V	100		110	
VRST REGULATOR						
V_{RST}	Output voltage			–14		V
	DC output voltage accuracy	I_{OUT} = 2 mA	–3%		3%	
	DC load regulation	V_{IN} = 3.6 V, I_{OUT} = 0 to 2 mA		13		V/A
	DC line regulation	VINA, VINL, VINR, VINC 2.7 to 6 V, I_{OUT} = 2 mA		–21		mV/V
V_{RIPPLE}	Output ripple	V_{IN} = 3.6 V, I_{OUT} = 2 mA, C_{OUT} = 440 nF (see [4])		375		mVpp
V_{REF_VRST}	Reference voltage			500		mV
I_{OUT}	Output current		0		4	mA
PG	Power-good threshold (fraction of nominal output voltage)	V_{RST} rising		90%		
		V_{RST} falling		90%		
R_{DIS}	Output discharge resistor	Active when rail is disabled		±150		Ω
C_{OUT}	Output capacitor		110	220		nF
		$t_{DISCHARGE}$ < 70 µs at VBAT ≥ 2.7 V	100		110	
LED DRIVER						
VLED BUCK-BOOST						
V_{LED}	Output voltage range		1.2		5.4	V
	Default output voltage	SW4, SW5, SW6 in OPEN position		3.5		
V_{OVP}	Output overvoltage protection	Clamps buck-boost output	5.5		7	V
V_{LED_OVP}	Fault detection threshold	Triggers VLED_OVP interrupt		5.4		V
I_{SW}	Switch current limit		3.5	4.0	4.5	A
$R_{DS(ON)}$	MOSFET ON-resistance	Switch A (from VINL to L1)		50		mΩ
		Switch B (from L1 to PGNDL)		50		
		Switch C (from L2 to PGNDL)		50		
		Switch D (from L2 to VLED)		50		
f_{SW}	Switching frequency			2.25		MHz
C_{OUT}	Output capacitance			2 × 22		µF
RGB STROBE CONTROLLER SWITCHES						
$R_{DS(ON)}$	Drain-source ON-resistance	SW4, SW5, SW6		30	75	mΩ
I_{LEAK}	OFF-state leakage current	VDS = 5 V			1	µA

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Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted) (see [1][2][3])

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LED CURRENT CONTROL						
V_f	LED forward voltage				4.55	V
I_{LED}	LED Currents	V_{IN} ≥4.50 V, V_{LED} ≤4.8 V; (closed loop operation) Covers USB power and 5 V AC adapter Current at max. code 0x3CBh for SWx_IDAC[9:0] R_{LIM} =39mΩ, 0.1%, T_A ≤45°C (see register settings)	2200	2400	2600	mA
		V_{IN} ≥ 2.7 V, V_{LED} ≤4.8 V, (closed loop operation) Covers single cell Li-ion battery with high current loading Current at max. code 0x20Eh for SWx_IDAC[9:0] R_{LIM} = 39 mΩ, 0.1%, TA=25 C (see register settings)		1300		
	DC current accuracy, SW4, 5, 6	R_{LIM} = 39 mΩ		±100		mA
	Transient LED current limit range	ILIM[3:0] = 0000 at RLIM = 39 mΩ		333		mA
		ILIM[3:0] = 1111 at RLIM = 39 mΩ		3846		
t_{rise}	Current rise time	I_{LED} from 5% to 95%, I_{LED} = 300 mA, Transient current limit disabled Not tested in production			50	µs
1.1-V REGULATOR						
VCORE (BUCK)						
V_{IN}	Input voltage		2.3		6	V
V_{OUT}	Nominal fixed output voltage			1.1		V
	DC output voltage accuracy	0 mA ≤ I_{OUT} ≤ 600 mA at V_{IN} > 2.5 V V_{OUT} = 1.1 V	–1.5%		1.5%	
d	Maximum duty cycle				100%	
$R_{DS(ON)}$	Low-side MOSFET on-resistance	V_{IN} = 3.6 V, T_J = 27ºC		185	380	mΩ
	High-side MOSFET on-resistance			240	480	mΩ
I_{OUT}	Output current	V_{IN} > 2.3 V		300	600	mA
I_{LIMIT}	Switch current limit			1		A
t_{SS}	Soft-start time	Time to ramp from 10% to 90% of V_{OUT}, V_{IN} = 3.6 V		250		µs
C_{OUT}	Output capacitance			10		µF
L	Nominal Inductance			2.2		µH
LOAD SWITCH						
V_{IN}	Input voltage range	LS_IN	1.8		3.6	V
$R_{DS(ON)}$	P-channel MOSFET on-resistance	V_{IN} = 1.8 V, over full temperature range		340	385	mΩ
C_{OUT}	Output capacitor	Ceramic	4.7	10	12	µF
	ESR of output capacitor	Ceramic	5	20	500	mΩ
MEASUREMENT SYSTEM (AFE)						
G	Amplifier gain (PGA)	AFE_GAIN[1:0] = 01		1.0		V/V
		AFE_GAIN[1:0] = 10		9.5		
		AFE_GAIN[1:0] = 11		18		

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Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted) (see [1][2][3])

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OFS}	Input referred offset voltage	PGA, AFE_CAL_DIS = 1 Not tested in production	–1		1	mV
		Comparator Not tested in production	–1.5		1.5	
t_{settle}	Settling time	To 1% of final value (not tested in production)			15	µs
		To 0.1% of final value (not tested in production)			52	
f_{sample}	Sampling rate	Not tested in production			19	kHz
LOGIC LEVELS AND TIMING CHARACTERISTICS						
V_{OL}	Output low-level	I_O = 0.5-mA sink current (RESETZ, CMP_OUT)	0		0.3	V
		I_O = 5-mA sink current (SPI_DOUT, INTZ)	0		0.3 × V_{SPI}	
V_{OH}	Output high-level	I_O = 0.5-mA source current (RESETZ, CMP_OUT)	1.3		2.5	V
		I_O = 5-mA source current (SPI_DOUT)	0.7 × V_{SPI}		V_{SPI}	
V_{IL}	Input low-level	PROJ_ON, LED_SEL0, LED_SEL1	0		0.4	V
		SPI_CSZ, SPI_CLK, SPI_DIN	0		0.3 × V_{SPI}	
V_{IH}	Input high-level	PROJ_ON, LED_SEL0, LED_SEL1	1.2			V
		SPI_CSZ, SPI_CLK, SPI_DIN	0.7 × V_{SPI}		V_{SPI}	
I_{BIAS}	Input bias current	V_{IO} = 3.3 V, any input pin			0.5	µA
$t_{DEGLITCH}$	Deglitch time	PROJ_ON, (not tested in production)		1		ms
		LED_SEL0, LED_SEL1 pins (not tested in production)		300		ns
INTERNAL OSCILLATOR						
f_{OSC}	Oscillator frequency			9		MHz
	Frequency accuracy	T_A = –30 to 85°C	–10%		10%	
THERMAL SHUTDOWN						
T_{WARN}	Thermal warning (HOT threshold)			120		°C
	Hysteresis			10		
T_{SHTDWN}	Thermal shutdown (TSD threshold)			150		°C
	Hysteresis			15		

6.6 Data Transmission Timing Requirements

VBAT = 3.6 ± 5%, T_A = 25 ºC, C_L = 10 pF (unless otherwise noted)

		MIN	TYP	MAX	UNIT
f_{CLK}	Serial clock frequency	0		36	MHz
t_{CLKL}	Pulse width low, SPI_CLK, 50% level	10			ns
t_{CLKH}	Pulse width high, SPI_CLK, 50% level	10			ns
t_t	Transition time, 20% to 80% level, all signals	0.2		4	ns
t_{CSCR}	SPI_CSZ falling to SPI_CLK rising, 50% level	8			ns
t_{CFCS}	SPI_CLK falling to SPI_CSZ rising, 50% level			1	ns
t_{CDS}	SPI_DIN data setup time, 50% level	7			ns
t_{CDH}	SPI_DIN data hold time, 50% level	6			ns
t_{iS}	SPI_DOUT data setup time(1), 50% level	10			ns
t_{iH}	SPI_DOUT data hold time(1), 50% level	0			ns
t_{CFDO}	SPI_CLK falling to SPI_DOUT data valid, 50% level			13	ns
t_{CSZ}	SPI_CSZ rising to SPI_DOUT HiZ			6	ns

(1) The DLPC3430/DLPC3435 processors send and receive data on the falling edge of the clock.

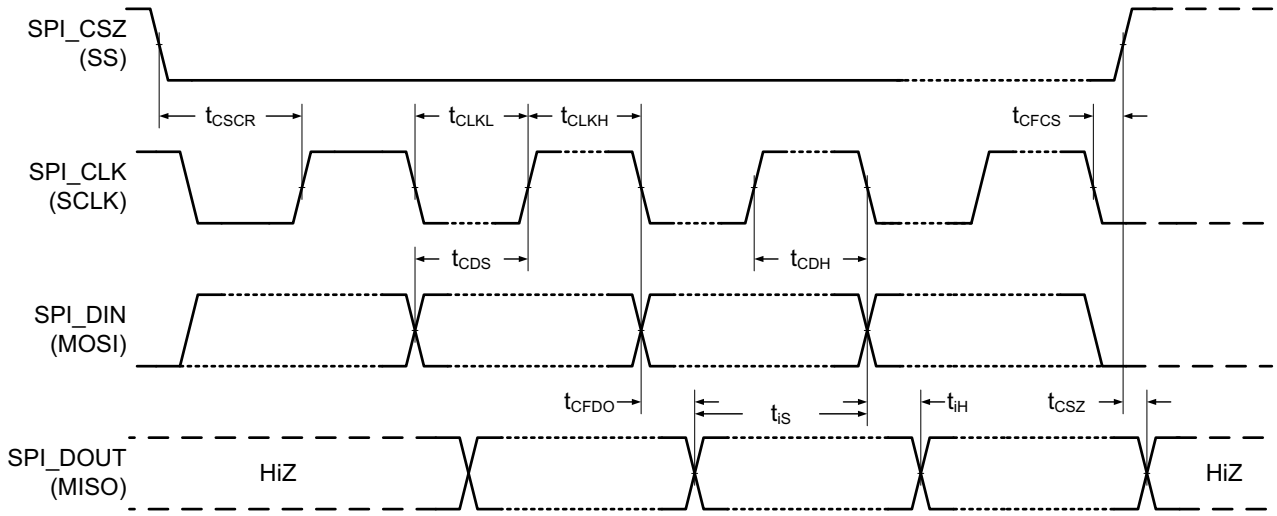

Figure 1. SPI Timing Diagram

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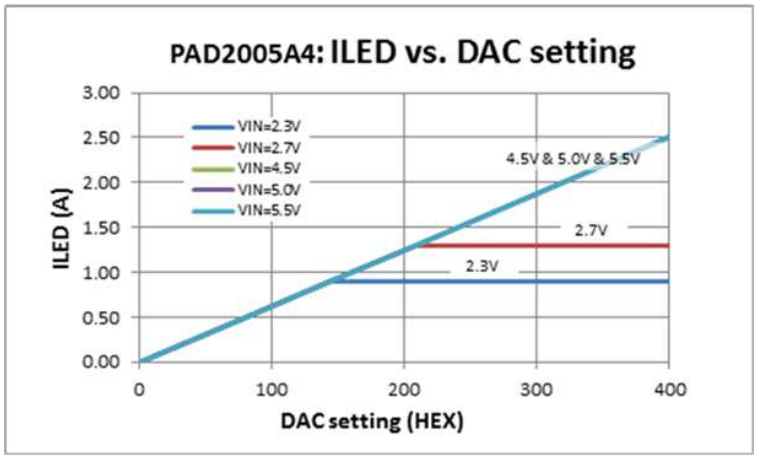
6.7 Typical Characteristics

The maximum output current of the buck-boost is a function of input voltage (VIN), and output voltage (VLED). The relationship between VIN, VLED, and MAX ILED is shown in Figure 2. Please note that VLED is the output of the buck-boost regulator, which includes the voltage drop across the sense resistor RLIM (39 mOhms typical), internal strobe control switch (75 mΩ max), and the forward voltage of the LED. For example, to drive 2.4 A of current through a LED with Vƒ = 4.8 V using the DLPA2005, the minimum input voltage needs to be 4.5 V.



2.3 V < VLED < 4.8 V

Figure 2. Maximum LED Output Current as a Function of Input Voltage (VIN) and Buck-Boost Output Voltage (VLED)

NOTE

Measured on a typical unit. VLED is the output of the buck-boost regulator and includes the voltage drop across the sense resistor, internal strobe control switch, and the forward voltage of the LED.

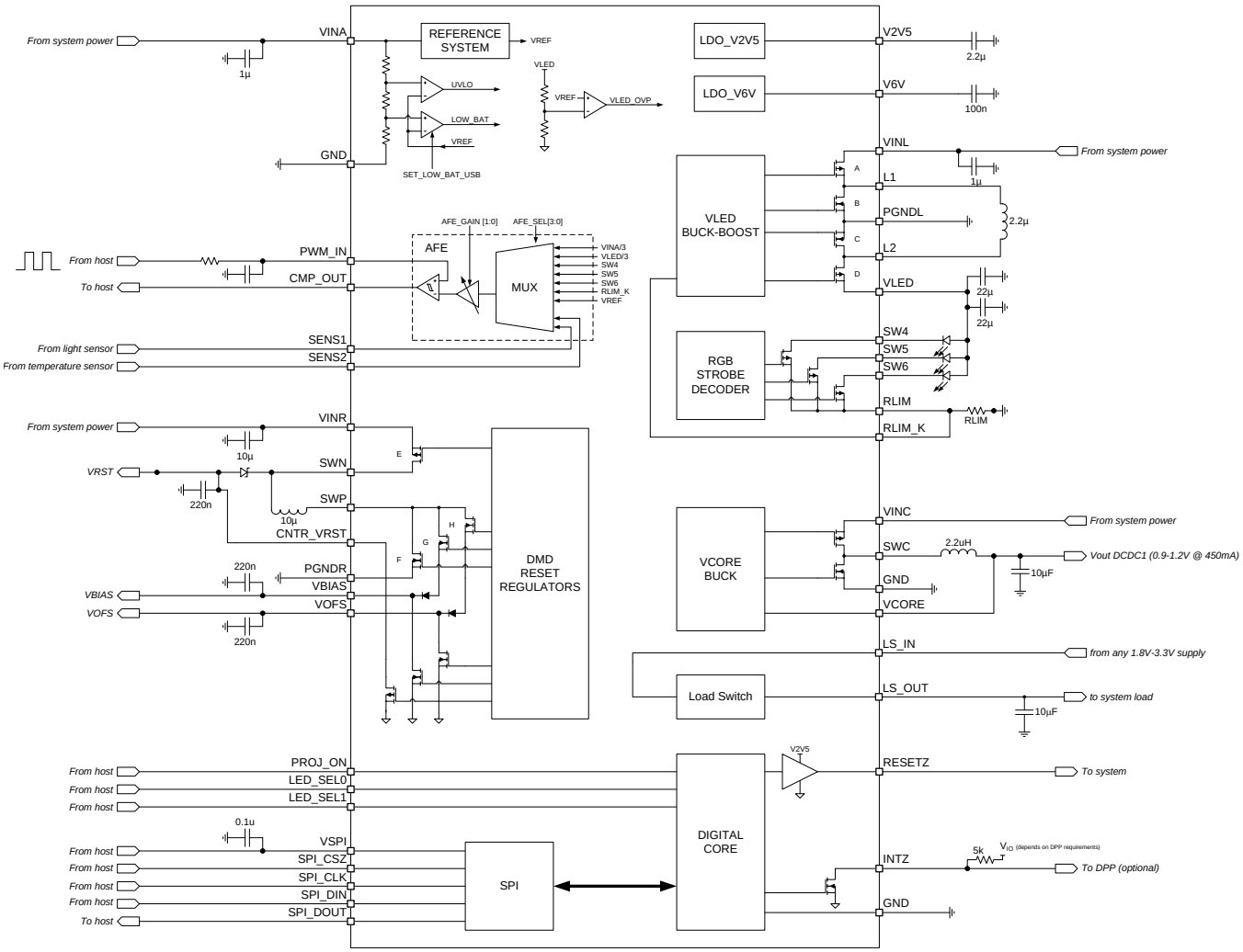
---

7 Detailed Description

7.1 Overview

The DLPA2005 is a power management and LED driver IC optimized for DLP video and data display systems. DLPA2005 is part of the chipset comprising of either DLP2010 (.2WVGA) DMD and DLPC3430/DLPC3435 controller, the DLP2010NIR (.2WVGA-NIR) DMD and DLPC150 controller, or the DLP3010 (.3 720p) DMD and DLPC3433/DLPC3438 controller. The DLPA2005 contains a complete LED driver including high efficiency power convertors. The DLPA2005 can supply up to 2.4 A per LED. Integrated high-current switches are included for sequentially selecting R, G, and B LEDs. The DLPA2005 also contains three regulated DC supplies for the DMD reset circuitry: VBIAS, VRST and VOFS, as well as a regulated DC supply of 1.1 V and a load switch for the 1.8 V to support the controllers. The DLPA2005 has a SPI used for setting the configuration. Using SPI, currents can be set independently for each LED with 10-bit resolution. Other features included are the generation of the system reset, power sequencing, input signals for sequentially selecting the active LED, IC self-protections, and an analog MUX for routing analog information to an external ADC.

7.2 Functional Block Diagram



A. Pin names refer to DLPA2005 pinout

B. Pins connected to 'system power' can be locally decoupled with the capacity as indicated in the block diagram. At least adequate decoupling capacity (50 µF or more) should be connected at the location the supply is entering the board.

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7.3 Feature Description

7.3.1 DMD Regulators

DLPA2005 contains three switch-mode power supplies that power the DMD. These rails are VOFS, VBIAS, and VRST. After pulling the PROJ_ON pin high, the DMD is first initialized followed by a power-up of the VOFS line after a small delay of less than 10 ms followed by VBIAS and VRST with an additional delay of 145 ms. The LED driver and STROBE DECODER circuit can only be enabled after all three rails are enabled. There are two power-down sequences, the normal power-down timing initiated after pulling the PROJ_ON pin low, and a fast power-down mode where if any one of the rails encounters a fault such as an output short, all three rails are discharged simultaneously. The detailed power-up and power-down diagrams are shown in Figure 3 and Figure 4.

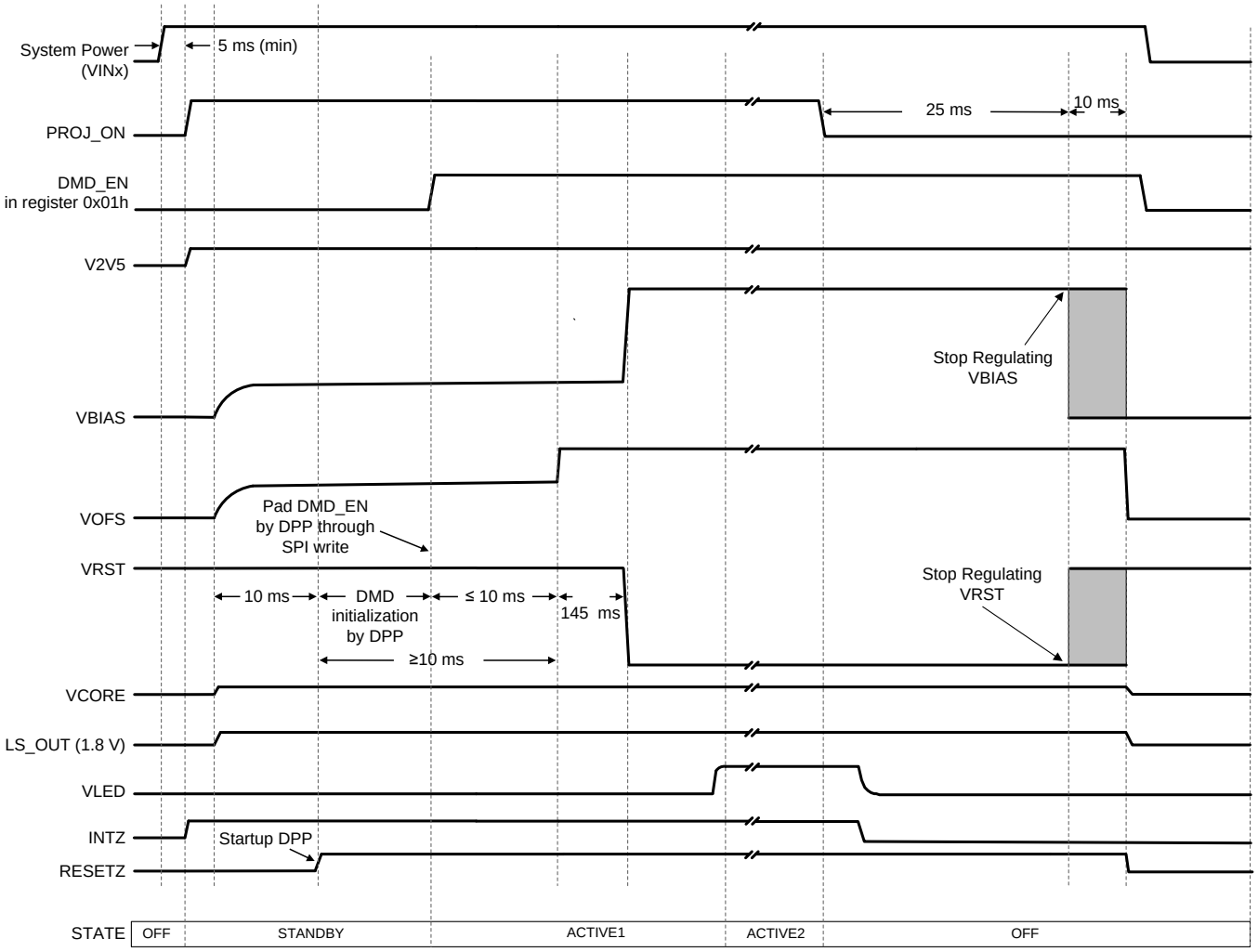
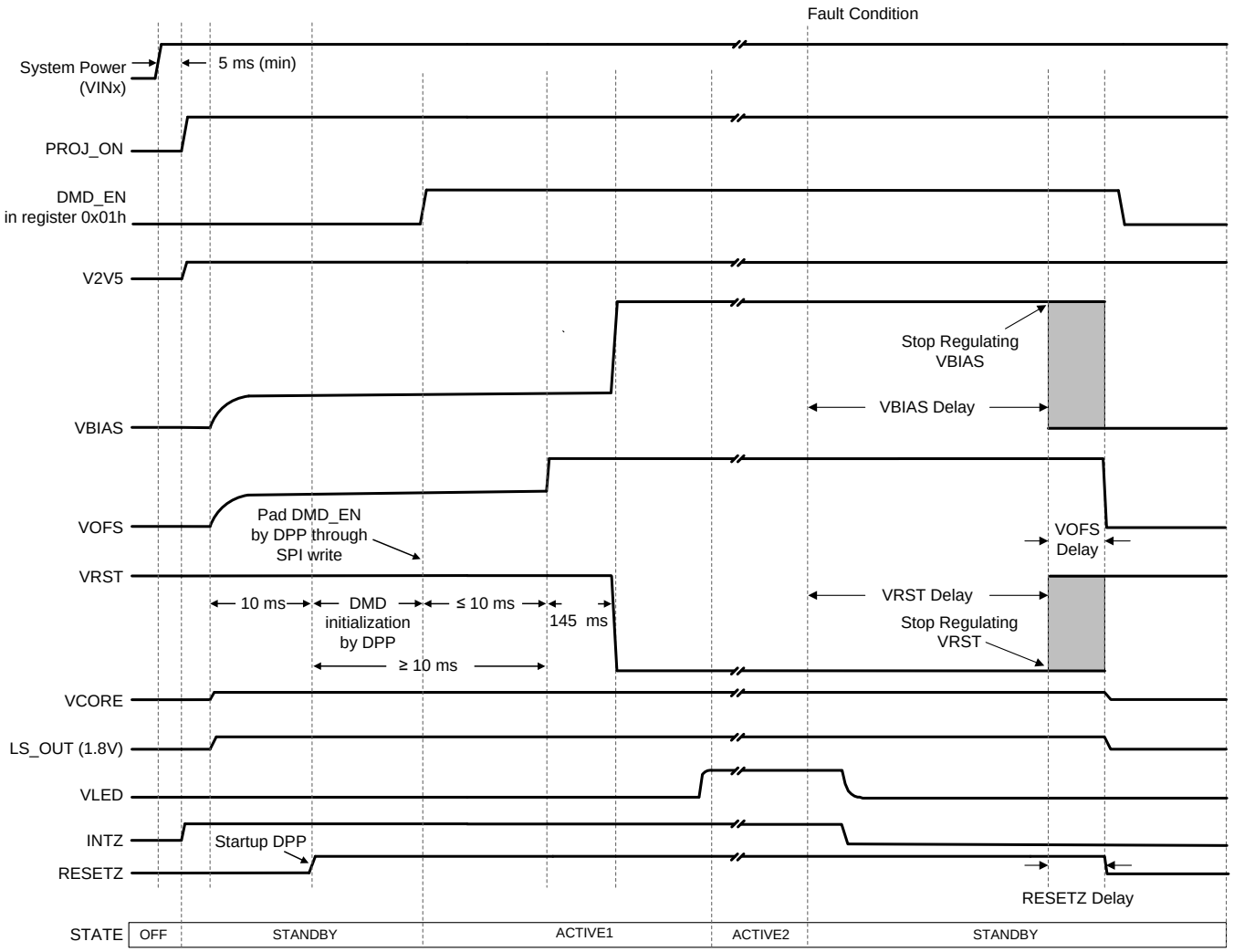


Figure 3. Power Sequence Normal Shutdown Mode

NOTE

All values are typical (unless otherwise noted).

Feature Description (continued)



(1) If the FAULT condition happens and its associated interrupt is masked in the Interrupt Mask Register (0Dh), the INTZ does not go low, but all other timing shown in the diagram is unaffected.

Figure 4. Power Sequence Fault Shutdown Mode

NOTE

All values are typical (unless otherwise noted).

7.3.2 RGB Strobe Decoder

DLPA2005 contains RGB color-sequential circuitry that is composed of three NMOS switches, the LED driver, the strobe decoder, and the LED current control. The NMOS switches are connected to the terminals of the external LED package and turn the currents through the LEDs on and off. Package connections are shown in Figure 5 and Figure 9 and corresponding switch map in Table 1.

The LED_SEL[1:0] signals typically receive a rotating code switching from RED to GREEN to BLUE and then back to RED. When the LED_SEL[1:0] input signals select a specific color, the NMOSFETs are controlled based on the color selected, and a 10-bit current control DAC for this color is selected that provides a control current to the RGB LEDs feedback control network.

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Feature Description (continued)

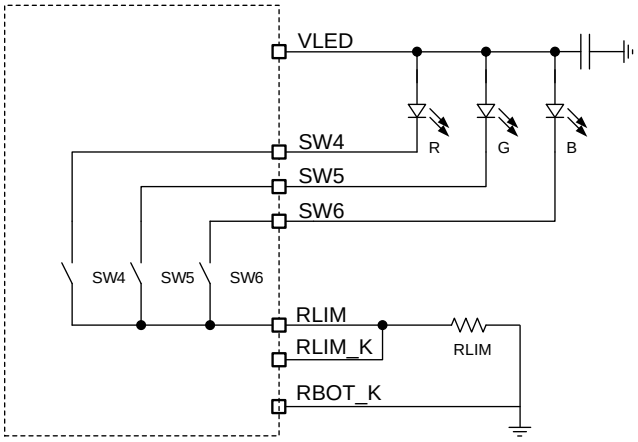

Figure 5. Switch Connection for a Common-Anode LED Assembly

Table 1. Switch Positions for Common Anode RGB LEDs (MAP = 0)

Common Anode				
LED_SEL[1:0]	**SW6**	**SW5**	**SW4**	**IDAC Input**
0x00h	Open	Open	Open	N/A
0x01h	Open	Open	Closed	SW4_IDAC[9:0]
0x02h	Open	Closed	Open	SW5_IDAC[9:0]
0x03h	Closed	Open	Open	SW6_IDAC[9:0]

The switching of the three NMOS switches is controlled such that switches are returned to the open position first before the closed connections are made (break before make). The dead time between opening and closing switches is controlled through the BBM register. Switches that already are in the closed position (and are to remain in the closed state according to the SWCNTRL register) are not opened during the BBM delay time.

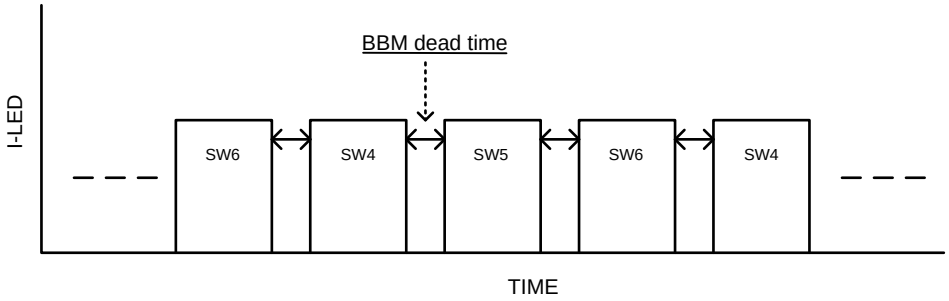

Figure 6. BBM Timing (See Register 0Bh in Table 20)

7.3.3 LED Current Control

DLPA2005 provides time-sequential circuitry to drive three LEDs with independent current control. A system based on a common anode LED configuration is shown in Figure 9 and consists of a buck-boost converter, which provides the voltage to drive the LEDs, three switches connected to the cathodes of the LEDs, an RLIM resistor used to sense the LED current, and a current DAC to control the LED current. The voltage measured at the pin V(RLIM_K) is used by the regulator loop.

The STROBE DECODER controls the switch positions as described in the previous section (*RGB Strobe Decoder*). With all switches in the open position, the buck-boost output assumes an output voltage of 3.5 V.

For a common-anode RGB LED configuration, the buck-boost output voltage (VLED) assumes a value such that the voltage drop across the sense resistor equals

(SW4_IDAC[9:0]Ivalue + ILED) × RLIM (1)

when SW4 is closed. The exact value of VLED depends on the current setting and the voltage drop across the LED but is limited to 5.4 V. When the STROBE decoder switches from SW4 to SW5, the buck-boost assumes a new output voltage such that the sense voltage equals:

(SW5_IDAC[9:0]Ivalue + ILED) × RLIM (2)

and finally when SW6 is selected.

(SW6_IDAC[9:0]Ivalue + ILED) × RLIM (3)

7.3.4 Maximum Led Currents and Efficiency Considerations

The DLPA2005 comprises a buck-boost power converter to supply the appropriate VLED to the LEDs. The maximum obtainable LED current for a given LED forward voltage are limited by three items:

- The inherent maximum LED current of the PAD2005, i.e. for DAC setting 03FFh.
- The maximum input current of about 4 A.
- The converter efficiency.
- Junction and ambient temperature

In the Figure 2 graph the LED current versus DAC setting is given for several supply voltages (VIN). The load was configured for each supply case such that at the maximum attainable current VOUT max=4.8 V.

For the higher supply voltages VIN>4.5 V the DAC current increases linearly up to the max setting of 3FFh. At that setting the ILED is about 2.5 A. For VIN=2.3 V and VIN=2.7 V the LED current is typically limited to 0.9 A and 1.3 A, respectively. Main reason of this limitation is the maximum input current in combination with the limited converter efficiency. This can be understood by looking at the equation describing the power conversion:

$$V_{OUT} \cdot I_{OUT} = \eta_{eff} \cdot V_{IN} \cdot I_{IN}$$

This equation states that the output power of the converter is equal to the input power times the converter efficiency. As indicated above, the input current IIN of the power converter is maximized to about 4A. The n_{eff} is the efficiency of the power converter, as described further down this section. For the lower input voltage the power converter runs as a boost converter.

(VOUT=4.8 V). Assuming 100% efficiency, VIN=2.3 V, VOUT=4.8 V and IINmax=4 A, the maximum attainable ILED is:

$$I_{LED} = \frac{\eta_{eff} \cdot V_{IN} \cdot I_{IN}}{V_{OUT}} = \frac{1 \cdot 2.3V \cdot 4A}{4.8V} = 1.9A$$

For the power converter approaching the maximum input current, the efficiency can roll down significantly. As a result the maximum LED current for VIN=2.3 V and VOUT=4.8 V is about 0.9 A.

The efficiency of the power converter depends on the input supply voltage and the output loading, i.e. output voltage and output current. In the below graph efficiency curves as a function of the LED current are given for several input supply voltages. Again for each of these supply cases the load was controlled such that at maximum output current the output voltage was about 4.8 V.

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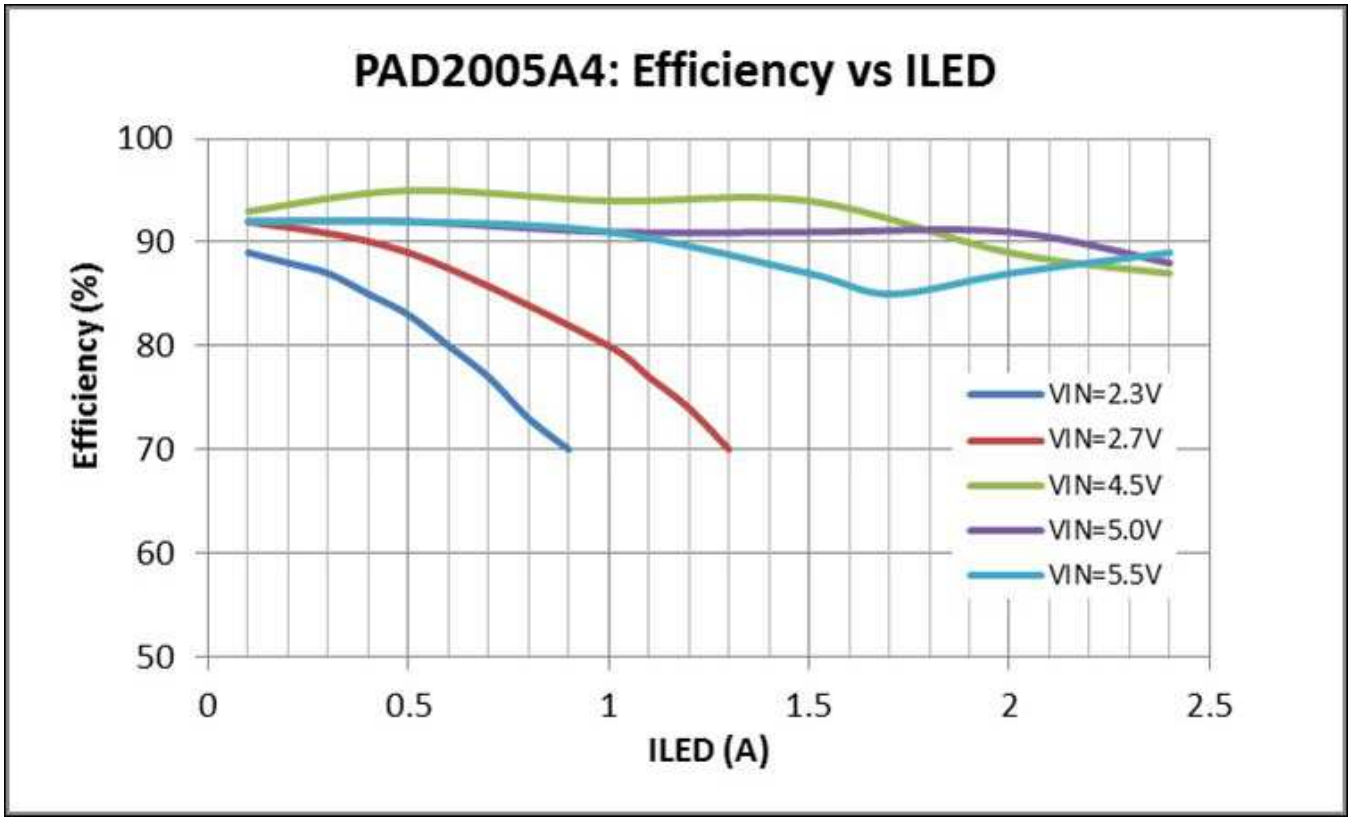

Figure 7. Measured Typical Power converter efficiency as a function of ILED for several supply voltages (VOUTmax=4.8V for each supply)

Note that in the measurement the output of the buck-boost regulator includes the voltage drop across the sense resistor RLIM, the voltage drop across the internal strobe control switch, and the forward voltage of the LED.

For higher input voltages the power converter runs at an efficiency of 85% or better. For the lower supply voltages because of the boost action, the efficiency quickly rolls down. Refer to section Thermal Considerations for information related to these efficiencies.

7.3.5 Calculating Inductor Peak Current

To properly configure the DLPA2005 device, a 2.2-µH inductor must be connected between pin L1 and pin L2. The peak current for the inductor in steady state operation can be calculated.

Equation 4 shows how to calculate the peak current I_1 in step down mode operation, and Equation 5 shows how to calculate the peak current I_2 in boost mode operation. V_{IN1} is the maximum input voltage, V_{IN2} is the minimum input voltage, f is the switching frequency (2.25 MHz), and L the inductor value (2.2 µH).

$$I_1 = \frac{I_{OUT}}{0.8} + \frac{V_{OUT}\left(V_{IN1} - V_{OUT}\right)}{2 \times V_{IN1} \times f \times L} \tag{4}$$

$$I_2 = \frac{V_{OUT} \times I_{OUT}}{0.8 \times V_{IN2}} + \frac{V_{IN2}\left(V_{OUT} - V_{IN2}\right)}{2 \times V_{OUT} \times f \times L} \tag{5}$$

The critical current value for selecting the right inductor is the higher value of I_1 and I_2. Also consider that load transients and error conditions may cause higher inductor currents. This needs to be accounted for when selecting an appropriate inductor. Internally the switching current is limited to a maximum of 4 A.

7.3.6 LED Current Accuracy

The LED drive current is controlled by a current DAC (Digital to Analog Converter) and can be set independently for switch SW4, SW5 and SW6. For the DLPA2005, the DAC is trimmed at a current of 2528 mA at code: 0x3FFh, and the step size is 2.47 mA. First order gain-error of the DAC can be neglected, but an offset current error must be taken into account. This offset error differs depending on the used RLIM, and is ±100 mA for the DLPA2005 using a current sense resistor of 39 mΩ.

The max current of the DLPA2005 (SWx_IDAC[9:0] = 0x3FFh) is regulated to 2528 mA. At the lowest setting (SWx_IDAC[9:0] = 0x029h) the current is regulated to 101 mA (DLPA2005). For this current setting (0x028h), the absolute current error results into a large relative error, however this is not a typical operating point.

For best accuracy of the LED current, take the below two considerations into account:

- The LED current setting does not only depend on the accuracy of the RLIM resistor but also strongly depends on the added resistance of pcb traces in the ground route of RLIM and the soldering quality. Due to the low value of the current sense resistor RLIM, any extra introduced resistance of e.g. several milliohms will result in a noticeable different LED current.
- Voltage sensing across RLIM is internally referred to the analog ground, i.e. pin 5 AGND1 and pin 20 GND. To prevent any voltage drop between the ground connection of RLIM and the AGND of the PAD2005, make a star connection of the RLIM ground near pin 5. Take care to make it a low ohmic route that can handle the high LED current. Subsequently, make the ground connection for pin 5 to the system ground low ohmic as well.

Taking the above measures relative to RLIM, the ILED current should align with the calculated value according to:

- Decimal_Code# = (set_current - min_current)/ step_current.
- If needed translate the Decimal_Code# to HEX code before entering in the control software.

7.3.7 Transient Current Limiting

Typically the forward voltages of the green and blue diodes are close to each other (about 3 to 4 V). However, the forward voltage of the red diode is significantly lower (1.8 to 2.5 V). This can lead to a current spike in the red diode when the strobe controller switches from green or blue to red because VLED is initially at a higher voltage than required to drive the RED diode. DLPA2005 provides transient current limiting for each switch to limit the current in the LEDs during the transition. The transient current limit value is controlled through the ILIM[3:0] bits in the IREG register. The same register also contains three bits to select which switch employs the transient current limiting feature. In a typical application, the transient current limit will only apply to the RED diode, and the ILIM[3:0] value will typically be set approximately 10% higher than the DC regulation current. The effect that the transient current limit has on the LED current is shown in Figure 8.

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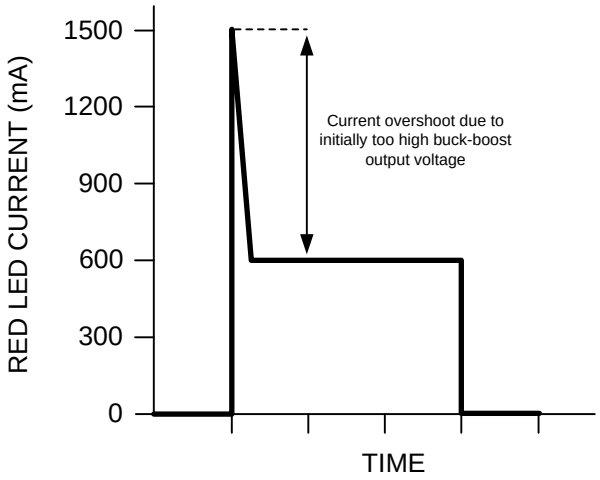
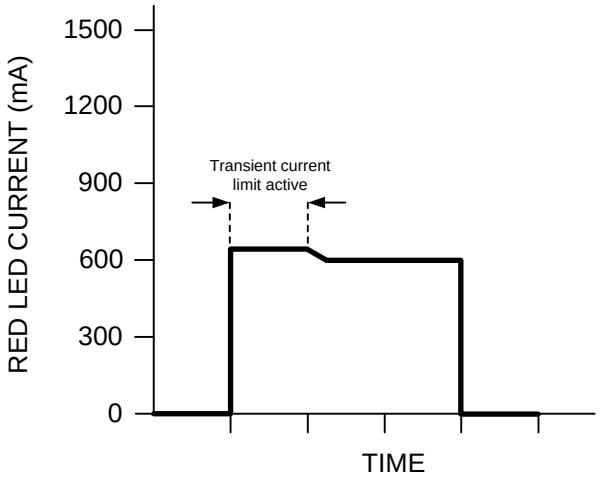


Red LED current without transient current limit. The current overshoots because the buck-boost voltage starts at the (higher) level of the green or blue LED.



LED current with transient current limit.

Figure 8. RED LED Current With and Without Transient Current Limit

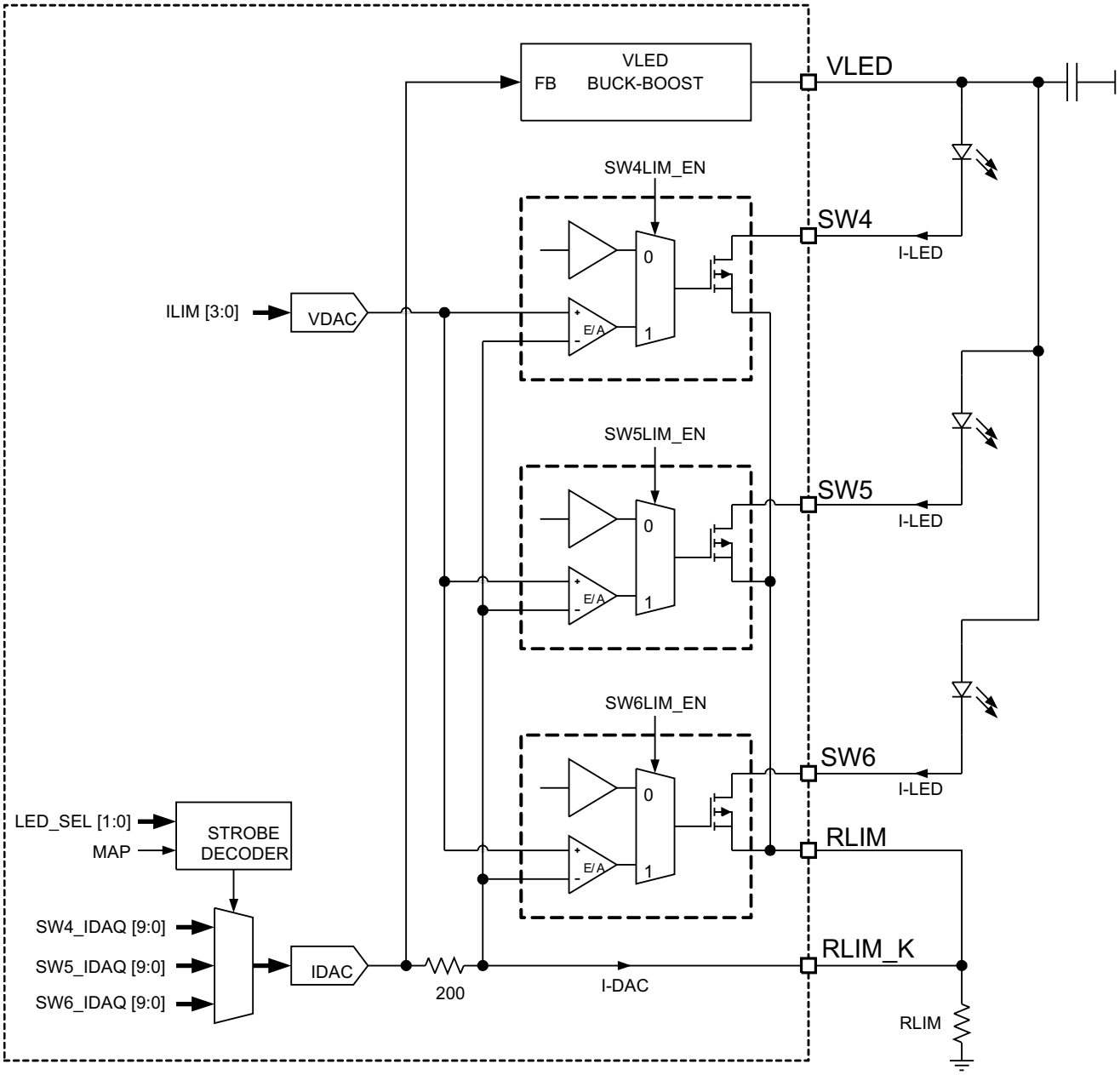


Figure 9. LED Driver Block Diagram

7.3.8 1.1-V Regulator (Buck Converter)

The buck converter creates a voltage of 1.1 V, and due to its switching nature, an output ripple with a frequency of approximately 2.25 MHz occurs on its output. This ripple is strongly dependent on the decoupling capacitor at the output in combination with the inductor. The magnitude of the ripple can be calculated with Equation 6.

$$\Delta V_{CORE} = V_{CORE} \times \frac{1 - \frac{V_{CORE}}{V_{INC}}}{L \times f} \times \left(\frac{1}{8 \times C_{OUT} \times f} + ESR \right) \tag{6}$$

The best way to minimize this ripple is to select a capacitor with a very-low ESR.

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7.3.9 Measurement System

The measurement system is composed of a 10:1 analog multiplexer (MUX), a programmable-gain amplifier, and a comparator. It works together with the DPP processor to provide:

- White-point correction (WPC) by independently adjusting the RGB LED currents after measuring the brightness of each color with an external light sensor
- A measurement of the:
  - Battery voltage
  - LED forward voltage
  - Exact LED current
  - Temperature as derived by measuring the voltage across an external thermistor

Figure 10 shows a block diagram of the measurement system.

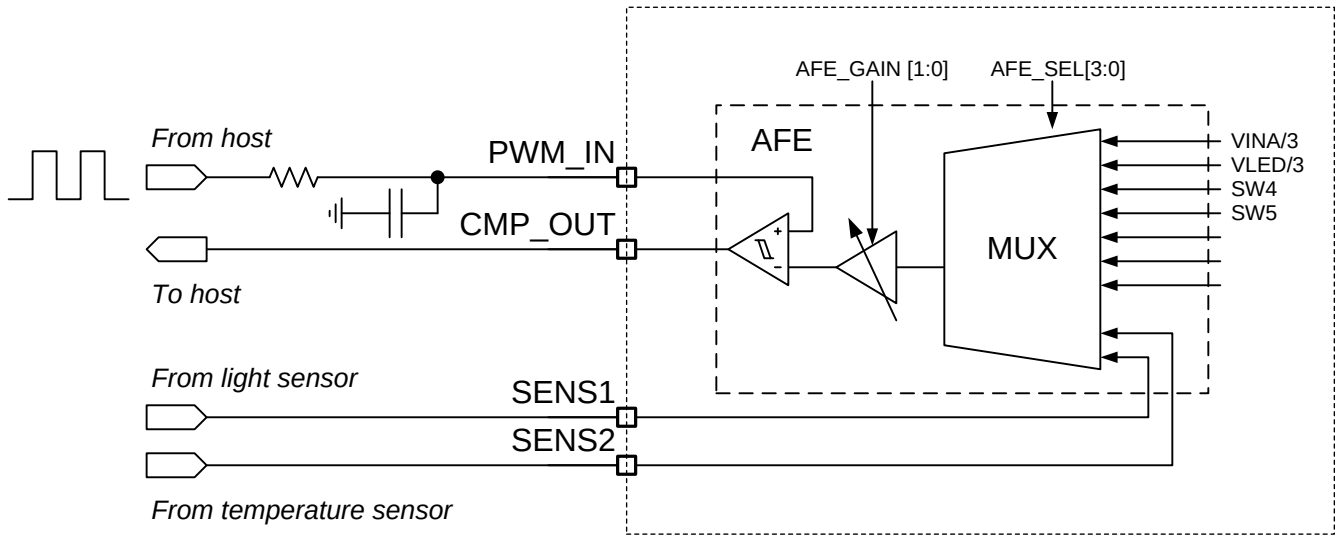

Figure 10. Block Diagram of the Measurement System

Table 2. Recommended Configuration of the AFE for Different Input Selections

AFE_SEL[3:0]	SELECTED INPUT	RECOMMENDED GAIN SETTING AFE-GAIN[1:0]	RECOMMENDED SETTING OF AFE_CAL_DIS BIT
0x00h	SENS2	0x01h (1x)	Setting has no effect on measurement
0x01h	VLED	0x01h (1x)	Setting has no effect on measurement
0x02h	VINA	0x01h (1x)	Setting has no effect on measurement
0x03h	SENS1	0x01h (1x)	Setting has no effect on measurement
0x04h	RLIM_K	0x03h (18x)	Set to 1 if sense voltage is >100 mV. Otherwise set to 0 (default)
0x05h	SW4	0x02h (9.5x)	Set to 1 if sense voltage is >200 mV. Otherwise set to 0 (default)
0x06h	SW5	0x02h (9.5x)	Set to 1 if sense voltage is >200 mV. Otherwise set to 0 (default)
0x07h	SW6	0x02h (9.5x)	Set to 1 if sense voltage is >200 mV. Otherwise set to 0 (default)
0x08h	No connect	N/A	N/A
0x09h	VREF	0x01h (1x)	Setting has no effect on measurement

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7.3.10 Protection Circuits

DLPA2005 has several protection circuits to protect the IC and system from damage due to excessive power consumption, die temperature, or over-voltages. These circuits are described in the following sections.

7.3.10.1 Thermal Warning (HOT) and Thermal Shutdown (TSD)

DLPA2005 continuously monitors the junction temperature and issues a HOT interrupt if temperature exceeds the HOT threshold. If the temperature continues to increase above the thermal shutdown threshold, all rails are disabled and the TSD bit in the INT register is set. After the temperature drops below its threshold, the system recovers and waits for the DPP to resend the DMD_EN bit.

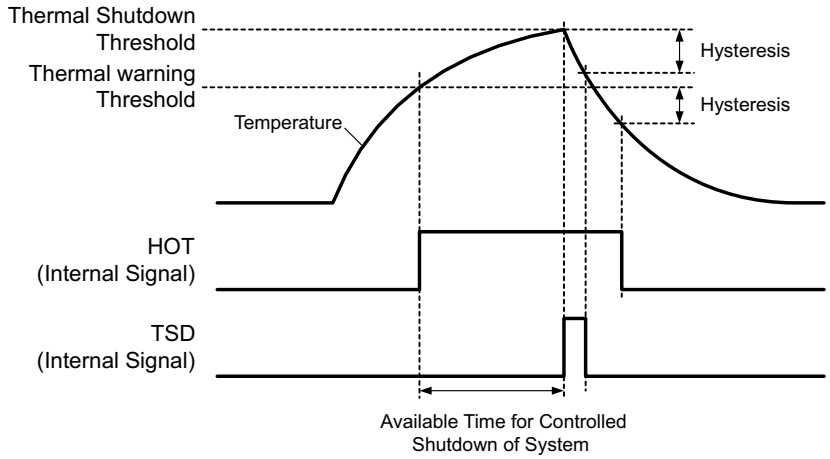

Figure 11. Definition of the Thermal Shutdown and Hot-Die Temperature Warning

7.3.10.2 Low Battery Warning (BAT_LOW) and Undervoltage Lockout (UVLO)

If the battery voltage drops below the BAT_LOW threshold (typically 3 V) the BAT_LOW interrupt is issued, but normal operation continues. After the battery drops below the undervoltage threshold which has a default hardcoded value of 2.3 V (this UVLO voltage can be changed through register 09 h from 2.3 to 4.5 V), the UVLO interrupt is issued, all rails are powered down in sequence, the DMD_EN bit is reset, and the part enters STANDBY mode. The power rails cannot be re-enabled before the input voltage recovers to >2.4 V. To re-enable the rails, the PROJ_ON pin must be toggled. The undervoltage threshold is programmable from 2.3 to 4.5 V in 31 steps.

The UVLO shutdown process will protect the DMD by allowing time for the mirrors to park, then doing a fast discharge of VOFS, VRST, and VBIAS. This protection occurs even in the case of sudden battery removal from the projector, as long as the bulk capacitance on the battery voltage (VINx) keeps this voltage above 2.3 V for as long as needed for VOFS, VRST, and VBIAS to discharge to the required safe levels as shown in the DMD data sheet. VOFS, VRST, and VBIAS discharge times depend on the load capacitance on each regulator. When for instance every supply is decoupled using a capacitor of 0.5 µF, VINx should stay above 2.3 V for at least 100 µs after the battery is suddenly removed. During this time, the mirrors can be placed in a safe position and VOFS, VRST, and VBIAS can be discharged.

NOTE

Capacitive loads should be such that LS_OUT stays above 1.65 V until VOFS, VRST, and VBIAS have discharged to their required safe levels.

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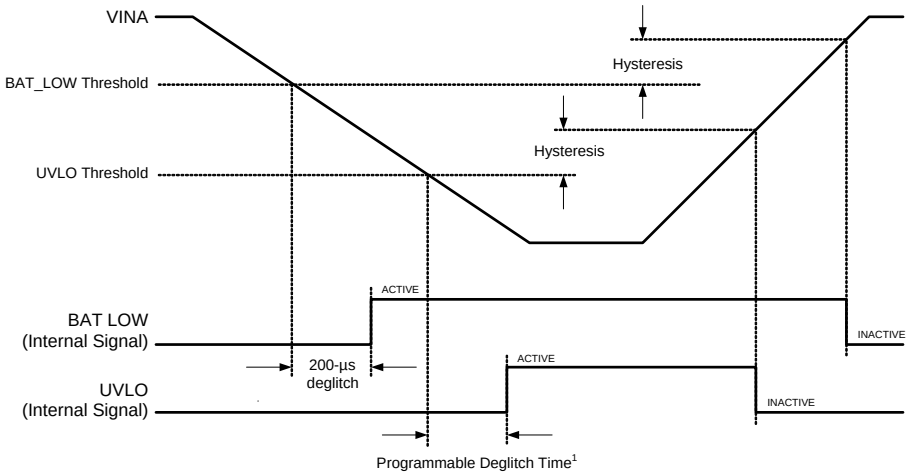

(1) This time is programmable from 0 to 100 µs

Figure 12. UVLO is Asserted When the Input Supply Drops Below the UVLO Threshold

7.3.10.3 DMD Regulator Fault (DMD_FLT)

The DMD regulator is continuously monitored to check if the output rails are in regulation and if the inductor current increases as expected during a switching cycle. If either one of the output rails drops out of regulation (for example, due to a shorted output) or the inductor current does not increase as expected during a switching cycle (due to a disconnected inductor), the DMD_FLT interrupt bit is set in the INT register, the DMD_EN bit is reset, and the DMD regulator is shut down. Resetting the DMD_EN bit also causes the LED driver to power down. To restart the system, the PROJ_ON pin must be toggled. In case the interrupt is masked, it is sufficient to set the DMD_EN bit to restart the system.

7.3.10.4 V6V Power-Good (V6V_PGF) Fault

The LED driver regulation loop requires the V6V rail for proper operation. The rail is continuously monitored and should the output drop below the power-good threshold, the V6V_PGF bit is set. The VLED buck-boost is then disabled and attempts to restart automatically.

7.3.10.5 VLED Overvoltage (VLED_OVP) Fault

If the buck-boost output voltage rises above 5.4 V, the VLED_OVP interrupt is set but the buck-boost regulator is not turned off. A typical condition to cause this fault is an open LED.

7.3.10.6 VLED Power Save Mode

In normal PWM operation, the efficiency of the VLED buck-boost converter dramatically reduces for LED currents below 100 mA. In this case, the power save mode allows high converting efficiency at low output currents by skipping pulses in the switcher's gate driver control.

7.3.10.7 V1V8 PG Failure

If for any reason the voltage on the LS_OUT drops below approximately 1.3 V, then VOFS, VBIAS, and VRST immediately go into fast shut down. Holding off power down to do mirror parking is not included since 1.3 V is too low to wait for this. Reactivating can only be done by toggling the PROJ_ON off and on again.

7.3.10.8 Interrupt Pin (INTZ)

Use the interrupt pin to signal events and fault conditions to the host processor. Whenever a fault or event occurs in the IC, the corresponding interrupt bit is set in the INT register, and the open-drain output is pulled low. The INTZ pin is released (returns to HiZ state) and fault bits are cleared when the INT register is read by the host.

However, if a failure persists, the corresponding INT bit remains set and the INTZ pin is pulled low again after a maximum of 32 µs.

Interrupt events include fault conditions such as power-good faults, over-voltage, over-temperature shutdown, and UVLO. For all interrupt conditions see the interrupt register on Table 22.

The MASK register is used to mask events from generating interrupts, that is, from pulling the INTZ pin low. The MASK settings affect the INTZ pin only and have no impact on protection and monitor circuits themselves. When an interrupt is masked, the event causing the interrupt still sets the corresponding bit in the INT register. However, it does not pull the INTZ pin low.

7.3.10.9 SPI

DLPA2005 provides a 4-wire SPI port that supports high-speed serial data transfers up to 33.3 MHz. Support includes register and data buffer write and read operations. The SPI_CSZ input serves as the active low chip select for the SPI port. The SPI_CSZ input must be forced low in order to write or read registers and data buffers. When SPI_CSZ is forced high, the data at the SPI_DIN input is ignored, and the SPI_DOUT output is forced to a high-impedance state. The SPI_DIN input serves as the serial data input for the port; the SPI_DOUT output serves as the serial data output. The SPI_CLK input serves as the serial data clock for both the input and output data. Data is latched at the SPI_DIN input on the rising edge of SPI_CLK, while data is clocked out of the SPI_DOUT output on the falling edge of SPI_CLK. Figure 13 illustrates the SPI port protocol. Byte 0 is referred to as the command byte, where the most significant bit is the write/not read bit. For the W/nR bit, a 1 indicates a write operation, while a 0 indicates a read operation. The remaining seven bits of the command byte are the register address targeted by the write or read operation. The SPI port supports write and read operations for multiple sequential register addresses through the implementation of an auto-increment mode. As shown in Figure 13, the auto-increment mode is invoked by simply holding the SPI_CSZ input low for multiple data bytes. The register address is automatically incremented after each data byte transferred, starting with the address specified by the command byte. After reaching address 0x7Fh the address pointer jumps back to 0x00h.

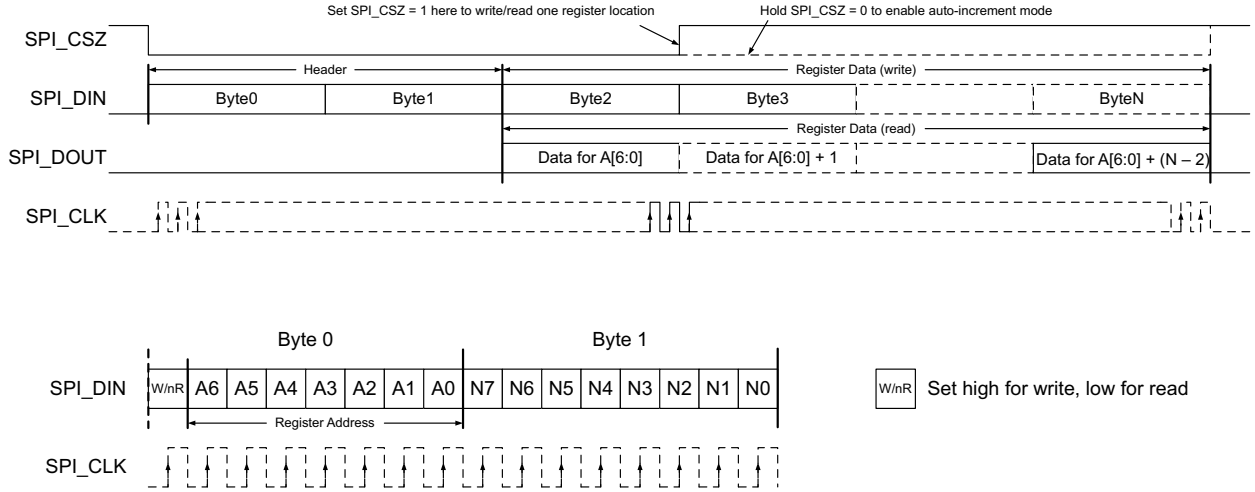

Figure 13. SPI Protocol

7.3.11 Password Protected Registers

Register addresses 0x11h through 0x27h can be read-accessed the same way as any other register, but are protected against accidental write operations through the PASSWORD register (address 0x10h). To write to a protected register, follow these steps:

1. Write data 0xBAh to register address 0x10h.
2. Write data 0xBEh to register address 0x10h.

Both writes must be consecutive, that is, there must be no other read or write operation in between sending the two bytes. After the password has been successfully written, registers 0x11h through 0x27h are unlocked and can be write accessed using the regular SPI protocol. They remain unlocked until any byte other than 0xBAh is written to the PASSWORD register or the part is power cycled.

To check if the registers are unlocked, read back the PASSWORD register. If the data returned is 0x00h, the registers are locked. If the PASSWORD register returns 0x01h, the registers are unlocked.

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7.4 Device Functional Modes

MODES OF OPERATION

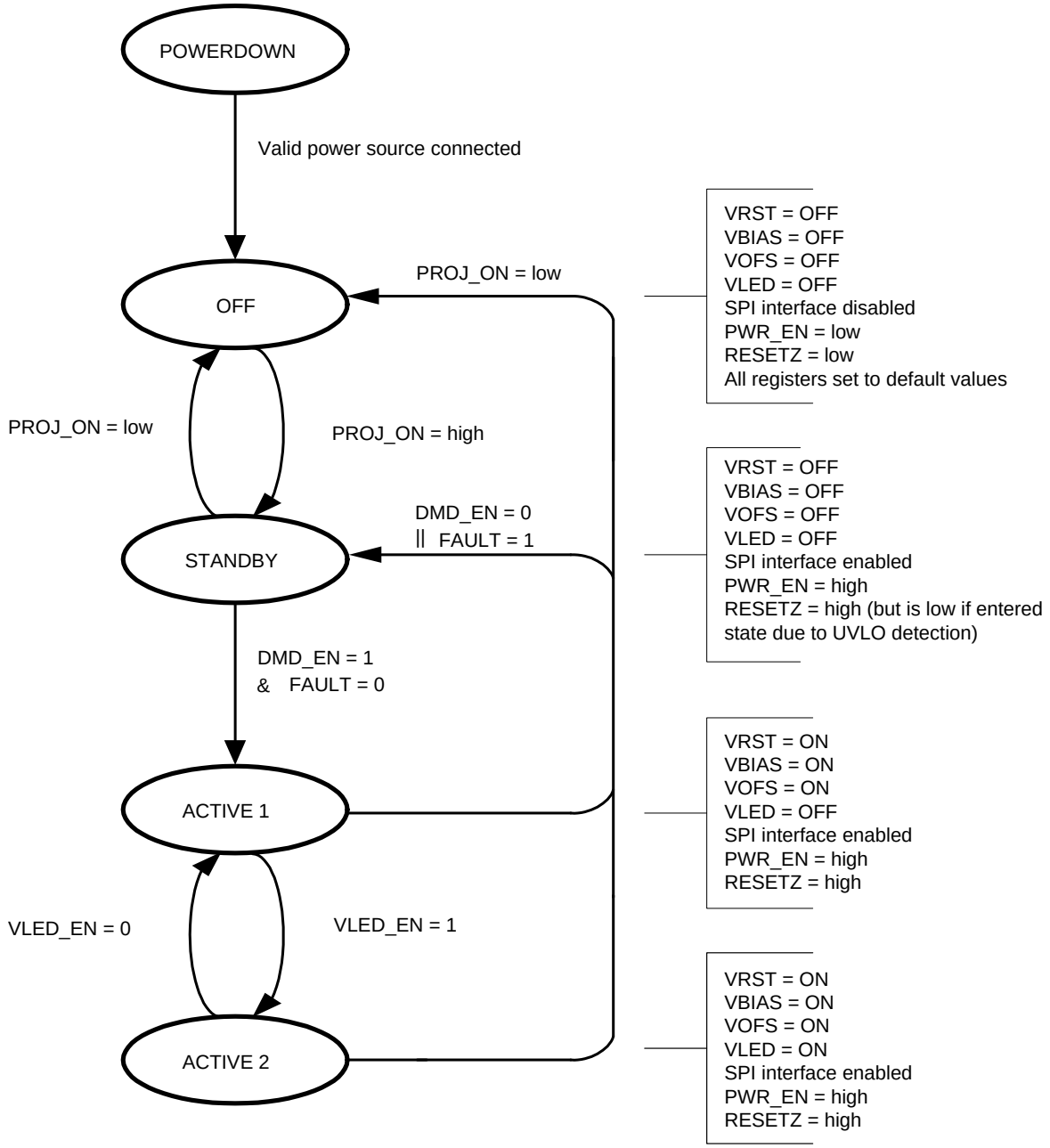
OFF This is the lowest-power mode of operation. All power functions are turned off, registers are reset to their default values and the IC does not respond to SPI commands. RESETZ pin is pulled low. The IC will enter OFF mode whenever the PROJ_ON pin is low.

STANDBY The DMD regulators and LED power (VLED) are turned off, but the IC does respond to the SPI interface. The device enters STANDBY mode whenever PROJ_ON is set high or DMD_EN7 bit is set to 0 using the SPI interface after PROJ_ON is already high. The device also enters STANDBY mode when a fault condition is detected8. (see the section about Protection Circuits on pages 28 & 30)

ACTIVE1 The DMD supplies are enabled but LED power (VLED) is disabled. PROJ_ON pin must be high, DMD_EN bit must be set to 1, and VLED_EN9 bit is set to 0.

ACTIVE2 DMD supplies and LED power are enabled. PROJ_ON pin must be high and DMD_EN and VLED_EN bits must both be set to 1.

Device Functional Modes (continued)



A. || = OR , & = AND

B. FAULT = Undervoltage on any supply (except LS_OUT), thermal shutdown, or UVLO detection

C. UVLO detection, per the diagram, causes the DLPA2005 to go into the standby state. This is not the lowest power state. If lower power is desired, PROJ_ON should be set low.

D. DMD_EN register bit can be reset or set by SPI writes. DMD_EN defaults to 0 when PROJ_ON goes from low to high and then the DPP ASIC software automatically sets it to 1. Also, FAULT = 1 causes the DMD_EN register bit to be reset.

E. PWR_EN is a signal internal to the DLPA2005. This signal turns on the VCORE regulator and the load switch that drives pin LS_OUT

Figure 14. State Diagram

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Table 3. Device State as a Function of Control-Pin Status

PROJ_ON PIN	STATE
LOW	OFF
HIGH	STANDBY ACTIVE1 ACTIVE2 (Device state depends on DMD_EN and VLED_EN bits and whether there are any fault conditions.)

Table 4. Modes of Operation

MODE	DESCRIPTION
OFF	This is the lowest-power mode of operation. All power functions are turned off, registers are reset to their default values, and the IC does not respond to SPI commands. RESETZ pin is pulled low. The IC will enter OFF mode whenever the PROJ_ON pin is low.
STANDBY	The DMD regulators and LED power (VLED) are turned off, but the IC does respond to the SPI. The device enters STANDBY mode whenever PROJ_ON is set high or DMD_EN(1) bit is set to 0 using the SPI interface after PROJ_ON is already high. The device also enters STANDBY mode when a fault condition is detected(2). (See *Protection Circuits* .)
ACTIVE1	The DMD supplies are enabled but LED power (VLED) is disabled. PROJ_ON pin must be high, DMD_EN bit must be set to 1, and VLED_EN(3) bit is set to 0.
ACTIVE2	DMD supplies and LED power are enabled. PROJ_ON pin must be high and DMD_EN and VLED_EN bits must both be set to 1.

(1) Settings can be done through Reg01h [9] and Reg2E [119]
(2) Power-good faults, over-voltage, overtemperature shutdown, and undervoltage lockout
(3) Settings can be done through Reg47h [60], bit is named VLED_EN_SET

7.5 Register Maps

Table 5. Register Description

REGISTER	ADDRESS (Hex)	NAME	TABLE	DESCRIPTION	DEFAULT
USER CONFIGURATION DEFINITIONS					
R	0x00	CHIP ID	Table 6	Chip Revision Register; DLPA2005	C4
R/W	0x01	CHIPENABLE	Table 7	Enable Register	0F
R/W	0x02	IREG	Table 8	Transient-current limit settings	30
R/W	0x03	SW4MSB	Table 9	Regulation current MSB, SW4	0
R/W	0x04	SW4LSB	Table 10, Table 11	Regulation current LSB, SW4	0
R/W	0x05	SW5MSB	Table 12	Regulation current MSB, SW5	0
R/W	0x06	SW5LSB	Table 13, Table 14	Regulation current LSB, SW5	0
R/W	0x07	SW6MSB	Table 15	Regulation current MSB, SW6	0
R/W	0x08	SW6LSB	Table 16, Table 17	Regulation current LSB, SW6	0
R/W	0x09	SWCNTRL	Table 18	Switch ON/OFF control (direct mode)	0
R/W	0x0A	AFE	Table 19	AFE (MUX) control	0
R/W	0x0B	BBM	Table 20, Table 21	Break Before Make timing	0
R	0x0C	INT	Table 22, Table 23	Interrupt register	0
R/W	0x0D	INT MASK	Table 24, Table 25	Interrupt Mask register	DFh
R/W	0x0E	TIMING	Table 26, Table 27	Timing register VOFS, VBIAS, VRST, and RESETZ	7
USER PROTECTED DEFINITION					
R/W	0x10	PASSWORD	Table 28	Password register	0
R/W	0x11	SYSTEM	Table 29	System Configuration register	0
USER EEPROM SCRATCH PAD DEFINITION					
R/W	0x20	BYTE0	Table 31	User EEPROM, Byte0	0

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Register Maps (continued)

Table 5. Register Description (continued)

REGISTER	ADDRESS (Hex)	NAME	TABLE	DESCRIPTION	DEFAULT
R/W	0x21	BYTE1	Table 32	User EEPROM, Byte1	0
R/W	0x22	BYTE2	Table 33	User EEPROM, Byte2	0
R/W	0x23	BYTE3	Table 34	User EEPROM, Byte3	0
R/W	0x24	BYTE4	Table 35	User EEPROM, Byte4	0
R/W	0x25	BYTE5	Table 36	User EEPROM, Byte5	0
R/W	0x26	BYTE6	Table 37	User EEPROM, Byte6	0
R/W	0x27	BYTE7	Table 38	User EEPROM, Byte7	0

Table 6. Chip Revision Register

REGISTER = 00h									
DATA BIT	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
FIELD NAME	CHIP ID [7:0]								
READ/WRITE	R	R	R	R	R	R	R	R	
RESET VALUE DLPA2005	1	1	0	0	0	1	0	0	C4
FIELD NAME	**BIT**	**BIT DEFINITION**							
CHIP ID	[7:0]	7:4		CHIPID<3:0>					
		3:0		REVID<3:0>					

Table 7. Enable Register

REGISTER = 01h									
DATA BIT	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
FIELD NAME	CHIPENABLE [15:8]								
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
RESET VALUE	0	0	0	0	1	1	1	1	0F
FIELD NAME	**BIT**	**BIT DEFINITION**							
CHIPENABLE	[15:8]	15:12		USER_GPO<3:0>					
		11		VLED_POWER_SAVE_MODE_DIS Power save mode is used to improve efficiency at light load.					
		10		FAST_SHUTDOWN_EN Applicable only during a fault condition. Shutdown timing is defined by register 0Eh. (see Figure 5)					
		9		DMD_EN					
		8		VLED_EN					

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Table 8. Transient-Current Limit Settings

REGISTER = 02h									
DATA BIT	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
Field Name	IREG [23:16]								
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset Value	0	0	1	1	0	0	0	0	30

FIELD NAME	**BIT**	**BIT DEFINITION**		
Not used	[23:16]	23	TBD	
IREG [3:0]		22:19	IREG_ILIM<3:0>	Rlim = 39 mΩ
			0000	333 mA
			0001	385 mA
			0010	442 mA
			0011	494 mA
			0100	564 mA
			0101	705 mA
			0110	846 mA
			0111	1128 mA
			1000	1410 mA
			1001	1692 mA
			1010	1974 mA
			1011	2256 mA
			1100	2538 mA
			1101	2974 mA
			1110	3410 mA
			1111	3846 mA
SW6LIM_EN		18	SW6LIM_EN	
			Transient current-limit enable for SW6 0 – Transient current-limit is disabled 1 – Transient current-limit is enabled	
SW5LIM_EN		17	SW5LIM_EN	
			Transient current-limit enable for SW5 0 – Transient current-limit is disabled 1 – Transient current-limit is enabled	
SW4LIM_EN		16	SW4LIM_EN	
			Transient current-limit enable for SW4 0 – Transient current-limit is disabled 1 – Transient current-limit is enabled	

Table 9. Regulation Current MSB, SW4[(1)]

REGISTER = 03h									
DATA BIT	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
FIELD NAME	SW4MSB [31:24]								
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
RESET VALUE	0	0	0	0	0	0	0	0	00

FIELD NAME	**Bit**	**BIT DEFINITION**	
SW4MSB	[31:24]	31:26	TBD
		25:24	SW4_IDAC<9:8>

(1) The DLPA2005 can use up to code 0x3ffh for SW4_IDAC[9:0].

Table 10. Regulation Current LSB, SW4

REGISTER = 04h									
DATA BIT	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
FIELD NAME	SW4LSB [39:32]								
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
RESET VALUE	0	0	0	0	0	0	0	0	00
FIELD NAME	**Bit**	**BIT DEFINITION**							
SW4LSB	[39:32]	39:32		SW4_IDAC<7:0>					

Table 11. Regulation Current LSB, SW4 Bit Definitions

DLPA2005 (1) (2)							
SW4_IDAC[9:0]	**LED CURRENT**	**SW4_IDAC[9:0]**	**LED CURRENT**	**SW4_IDAC[9:0]**	**LED CURRENT**	**SW4_IDAC[9:0]**	**LED CURRENT**
0x000h	0 mA	0x100h	633 mA	0x200h	1265 mA	0x300h	1898 mA
0x029h	101 mA	0x101h	635 mA	0x201h	1268 mA	0x301h	1900 mA
0x02Ah	104 mA	0x102h	638 mA	0x202h	1270 mA	0x302h	1903 mA
...	...	...	...	...	...	...	...
0x0FEh	628 mA	0x1FEh	1260 mA	0x2FEh	1893 mA	0x3FEh	2526 mA
0x0FFh	630 mA	0x1FFh	1263 mA	0x2FFh	1895 mA	0x3FFh	2528 mA

(1) Values shown are for a typical DLPA2005 unit at T = 25°C. Typical step size is 2.47 mA for R_{LIM} = 39 mΩ
(2) The DLPA2005 can use up to code 0x3FFh for SW4_IDAC[9:0].

Table 12. Regulation Current MSB, SW5 (1)

REGISTER = 05h									
DATA BIT	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
FIELD NAME	SW5MSB [47:40]								
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
RESET VALUE	0	0	0	0	0	0	0	0	00
FIELD NAME	**Bit**	**BIT DEFINITION**							
SW5MSB	[47:40]	47:42		TBD					
		41:40		SW5_IDAC<9:8>					

(1) The DLPA2005 can use up to code 0x3FFh for SW5_IDAC[9:0].

Table 13. Regulation Current LSB, SW5

REGISTER = 06h									
DATA BIT	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
FIELD NAME	SW5LSB [55:48]								
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
RESET VALUE	0	0	0	0	0	0	0	0	00
FIELD NAME	**BIT**	**BIT DEFINITION**							
SW5LSB	[55:48]	55:48		SW5_IDAC<7:0>					

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Table 14. Regulation Current LSB, SW5 Bit Definitions

DLPA2005 (1) (2)							
SW5_IDAC[9:0]	**LED CURRENT**	**SW5_IDAC[9:0]**	**LED CURRENT**	**SW5_IDAC[9:0]**	**LED CURRENT**	**SW5_IDAC[9:0]**	**LED CURRENT**
0x000h	0 mA	0x100h	633 mA	0x200h	1265 mA	0x300h	1898 mA
0x029Ch	101 mA	0x101h	635 mA	0x201h	1268 mA	0x301h	1900 mA
0x02Ah	104 mA	0x102h	638 mA	0x202h	1270 mA	0x302h	1903 mA
...	...	...	...	...	...	...	...
0x0FEh	628 mA	0x1FEh	1260 mA	0x2FEh	1893 mA	0x3FEh	2526 mA
0x0FFh	630 mA	0x1FFh	1263 mA	0x2FFh	1895 mA	0x3FFh	2528 mA

(1) Values shown are for a typical DLPA2005 unit at T = 25°C. Typical step size is 2.47 mA for $_{RLIM}$ = 39 mΩ
(2) The DLPA2005 can use up to code 0x3FFh for SW5_IDAC[9:0].

Table 15. Regulation Current MSB, SW6 (1)

REGISTER = 07h									
DATA BIT	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
FIELD NAME	SW6MSB [63:56]								
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
RESET VALUE	0	0	0	0	0	0	0	0	00
FIELD NAME	**BIT**	**BIT DEFINITION**							
SW6MSB	[63:56]	63:58		TBD					
		57:56		SW6_IDAC<9:8>					

(1) The DLPA2005 can use up to code 0x3FFh for SW6_IDAC[9:0].

Table 16. Regulation Current LSB, SW6

REGISTER = 08h									
DATA BIT	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
FIELD NAME	SW6LSB [71:64]								
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
RESET VALUE	0	0	0	0	0	0	0	0	00
FIELD NAME	**BIT**	**BIT DEFINITION**							
SW6LSB	[71:64]	71:64		SW6_IDAC<7:0>					

Table 17. Regulation Current LSB, SW6 Bit Definitions

DLPA2005 (1) (2)							
SW6_IDAC[9:0]	**LED CURRENT**	**SW6_IDAC[9:0]**	**LED CURRENT**	**SW6_IDAC[9:0]**	**LED CURRENT**	**SW6_IDAC[9:0]**	**LED CURRENT**
0x000h	0 mA	0x100h	633 mA	0x200h	1265 mA	0x300h	1898 mA
0x029h	101 mA	0x101h	635 mA	0x201h	1268 mA	0x301h	1900 mA
0x02Ah	104 mA	0x102h	638 mA	0x202h	1270 mA	0x302h	1903 mA
...	...	...	...	...	...	...	...
0x0FEh	628 mA	0x1 FEh	1260 mA	0x2FEh	1893 mA	0x3FEh	2526 mA
0x0FFh	630 mA	0x1 FFh	1263 mA	0x2FFh	1895 mA	0x3FFh	2528 mA

(1) Values shown are for a typical DLPA2005 unit at T = 25°C. Typical step size is 2.47 mA for R_{LIM} = 39 mΩ
(2) The DLPA2005 can use up to code 0x3FFh for SW6_IDAC[9:0].

Table 18. Switch On/Off Control (Direct Mode)

REGISTER = 09h									
DATA BIT	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
FIELD NAME	SWCNTRL [79:72]								
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
RESET VALUE	0	0	0	0	0	0	0	0	00

FIELD NAME	**BIT**	**BIT DEFINITION**	
SWCNTRL	[79:72]	79	SW6 (controls switch 6 if direct mode (see reg 11h) is enabled)
		78	SW5 (controls switch 5 if direct mode (see reg 11h) is enabled)
		77	SW4 (controls switch 4 if direct mode (see reg 11h) is enabled)
		76:72	UVLO_TRIM<4:0>
		00000 00001 ..... 11110 11111	2.3 V (minimum value – default value) 2.37 V Step approximately 70 mV 4.43 V 4.5 V (maximum value)

Table 19. AFE (MUX) Control

REGISTER = 0Ah									
DATA BIT	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
FIELD NAME	AFE [87:80]								
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
RESET VALUE	0	0	0	0	0	0	0	0	00

FIELD NAME	**BIT**	**BIT DEFINITION**	
AFE	[87:80]	87	AFE_EN
		86	AFE_CAL_DIS
		85:84	AFE_GAIN<1:0>
		83:80	AFE_SEL<3:0>

Table 20. Break Before Make (BBM) Timing

REGISTER = 0Bh									
DATA BIT	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
FIELD NAME	BBM [95:88]								
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
RESET VALUE	0	0	0	0	0	0	0	0	00

Table 21. Break Before Make (BBM) Timing Bit Definitions (1)

FIELD NAME	**BIT**	**BIT DEFINITION**				
BBM	[95:88]	95:88	BBM_DELAY<7:0>			
			0x00 – 0 ns	0x40 – 7326 ns	0x80 – 14430 ns	0xC0 – 21534 ns
			0x01 – 333 ns	0x41 – 7437 ns	0x81 – 14541 ns	0xC1 – 21645 ns
			0x02 – 444 ns	0x42 – 7548 ns	0x82 – 14652 ns	0xC2 – 21756 ns
			...	...	...	...
			0x3E – 7104 ns	0x7E – 14208 ns	0xBE – 21312 ns	0xFE – 28416 ns
			0x3F – 7215 ns	0x7F – 14319 ns	0xBF – 21423 ns	0xFF – 28527 ns

(1) It takes 333 to 444 ns to turn off the switches from the time a change occurs on LED_SEL[1:0].

Table 22. Interrupt Register

REGISTER = 0Ch									
DATA BIT	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
FIELD NAME	INT [103:96]								
READ/WRITE	R	R	R	R	R	R	R	R	
RESET VALUE	0	0	0	0	0	0	0	0	00

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Table 23. Interrupt Register Bit Definitions

FIELD NAME	BIT	BIT DEFINITION	
INT	[103:96]	103	VLED_OVP VLED buck_boost overvoltage fault interrupt (normal operation resumes) 0 – No fault 1 – Buck_boost output is above OVP threshold
		102	IREG_PG_FAULT V6V power-good fault interrupt (normal operation resumes) 0 – No fault 1 – V6V is not in regulation
		101	PROJ_ON_INT Proj_On interrupt (part enters OFF mode) 0 – Pin is pulled high, normal mode 1 – Pin is pulled low, alerts the DPP that the DMD regulator is about to shut down.
		100	DMD_FAULT DMD regulator fault (part enters STANDBY mode and DMD_EN bit is cleared) 0 – No fault 1 – The inductor current is not increasing at the correct rate, likely to be caused by an open inductor. Or, one of the regulator outputs has dropped below the power-good threshold, likely to be caused by a short
		99	UVLO UVLO interrupt (sensed at VINA pin), DMD bit is cleared. 0 – Battery voltage is above the UVLO threshold 1 – Battery voltage has dropped below the UVLO threshold
		98	BAT_LOW_WARN Low battery warning interrupt (sensed at VINA pin, normal operation resumes) 0 – Battery voltage is above the low-battery threshold 1 – Battery voltage has dropped below the low-battery threshold
		97	TS_WARN Thermal warning interrupt (normal operation resumes) 0 – Die temperature is in normal operating range 1 – Die temperature is above the HOT threshold Or, part has not cooled down enough to recover from HOT.
		96	TS_WARN Thermal Warning Interrupt (normal operation resumes) 0 – Die temperature is in normal operating range 1 – Die temperature is above the HOT threshold Or, part has not cooled down enough to recover from HOT.

Table 24. Interrupt Mask Register

REGISTER = 0Dh									
DATA BIT	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
FIELD NAME	INT MASK [111:104]								
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
RESET VALUE	1	1	0	1	1	1	1	1	DF

Table 25. Interrupt Mask Register Bit Definitions

FIELD NAME	BIT	BIT DEFINITION	
INT MASK	[111:104]	111	VLED BUCK_BOOST Overvoltage fault interrupt mask 0 – Interrupt is not masked 1 – Interrupt is masked
		110	IREG_PG_FAULT_MASK 0 – Interrupt is not masked 1 – Interrupt is masked
		109	PROJ_ON interrupt mask 0 – Interrupt is not masked 1 – Interrupt is masked
		108	DMD_REGULATOR fault mask 0 – Interrupt is not masked 1 – Interrupt is masked
		107	UVLO_MASK 0 – Interrupt is not masked 1 – Interrupt is masked
		106	Low Battery Warning Mask (sensed at VINA pin) 0 – Interrupt is not masked 1 – Interrupt is masked
		105	Thermal Shutdown Interrupt Mask 0 – Interrupt is not masked 1 – Interrupt is masked
		104	Thermal Warning Interrupt Mask 0 – Interrupt is not masked 1 – Interrupt is masked

Table 26. Timing Register VOFS, VBIAS, VRST, and RESETZ

REGISTER = 0Eh									
DATA BIT	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
FIELD NAME	TIMING [119:112]								
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
RESET VALUE	0	0	0	0	0	1	1	1	07

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Table 27. Timing Register VOFS, VBIAS, VRST, and RESETZ Bit Definitions

FIELD NAME	BIT	BIT DEFINITION		
TIMING	[119:112]	119:116	VOFS/RESETZ_DELAY<3:0> (for values see min and max delay)	
		115:112	VBIAS/VRST_DELAY<3:0> (for values see min and max delay)	
			Min Delay (µs)	Max Delay (µs)
		0000	4.0	4.4
		0001	8.0	8.9
		0010	16.0	17.8
		0011	32.0	35.5
		0100	64.0	71.1
		0101	128.0	142.2
		0110	256.0	284.4
		0111	512.0	569.0
		1000	6.2	7.1
		1001	12.4	14.2
		1010	24.9	28.4
		1011	49.8	56.9
		1100	99.5	113.8
		1101	199.1	227.6
		1110	398.3	455.2
		1111	1024.2	1138.0

Table 28. Password Register

REGISTER = 10h									
DATA BIT	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
FIELD NAME	PASSWORD [135:128]								
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
RESET VALUE	0	0	0	0	0	0	0	0	00
FIELD NAME	**BIT**	**BIT DEFINITION**							
PASSWORD	[135:128]	135:128	USER PASSWORD (0xBAh + 0xBEh) Disable (0x00h) Once set, register 11h can be written.						

Table 29. System Configuration Register

REGISTER = 11h									
DATA BIT	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
FIELD NAME	SYSTEM [143:136]								
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
RESET VALUE	0	0	0	0	0	0	0	0	00

Table 30. System Configuration Register Bit Definitions

FIELD NAME	BIT	BIT DEFINITION	
SYSTEM	[143:136]	143:139	TBD
		138	EEPROM_PROGRAM Program scratch pad values to EEPROM
		137	DIRECT_MODE Allows direct control of switches through SW CONTROL REGISTER
		136	TBD

Table 31. User EEPROM, BYTE0

REGISTER = 20h									
DATA BIT	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
FIELD NAME	BYTE0 [7:0]								
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
RESET VALUE	0	0	0	0	0	0	0	0	00
FIELD NAME	**BIT**	**BIT DEFINITION**							
BYTE0	[7:0]	7:0		USER BYTE 0					

Table 32. User EEPROM, BYTE1

REGISTER = 21h									
DATA BIT	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
FIELD NAME	BYTE1 [15:8]								
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
RESET VALUE	0	0	0	0	0	0	0	0	00
FIELD NAME	**BIT**	**BIT DEFINITION**							
BYTE1	[15:8]	15:8		USER BYTE 1					

Table 33. User EEPROM, BYTE2

REGISTER = 22h									
DATA BIT	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
FIELD NAME	BYTE2 [23:16]								
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
RESET VALUE	0	0	0	0	0	0	0	0	00
FIELD NAME	**BIT**	**BIT DEFINITION**							
BYTE2	[23:16]	23:16		USER BYTE 2					

Table 34. User EEPROM, BYTE3

REGISTER = 23h									
DATA BIT	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
FIELD NAME	BYTE3 [31:24]								
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
RESET VALUE	0	0	0	0	0	0	0	0	00
FIELD NAME	**BIT**	**BIT DEFINITION**							
BYTE3	[31:24]	31:24		USER BYTE 3					

Table 35. User EEPROM, BYTE4

REGISTER = 24h									
DATA BIT	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
FIELD NAME	BYTE4 [39:32]								
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
RESET VALUE	0	0	0	0	0	0	0	0	00
FIELD NAME	**BIT**	**BIT DEFINITION**							
BYTE4	[39:32]	39:32		USER BYTE 4					

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Table 36. User EEPROM, BYTE5

REGISTER = 25h									
DATA BIT	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
FIELD NAME	BYTE5 [47:40]								
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
RESET VALUE	0	0	0	0	0	0	0	0	00
FIELD NAME	**BIT**	**BIT DEFINITION**							
BYTE5	[47:40]	47:40		USER BYTE 5					

Table 37. User EEPROM, BYTE6

REGISTER = 26h									
DATA BIT	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
FIELD NAME	BYTE6 [55:48]								
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
RESET VALUE	0	0	0	0	0	0	0	0	00
FIELD NAME	**BIT**	**BIT DEFINITION**							
BYTE6	[55:48]	55:48		USER BYTE 6					

Table 38. User EEPROM, BYTE7

REGISTER = 27h									
DATA BIT	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
FIELD NAME	BYTE7 [63:56]								
READ/WRITE	R	R	R	R	R	R	R	R	
RESET VALUE	0	0	0	0	0	0	0	0	00
FIELD NAME	**BIT**	**BIT DEFINITION**							
BYTE7	[63:56]	63:56		USER BYTE 7					

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

A DLPC343x controller can be used with a DLP2010 (.2 WVGA) DMD or DLP3010 (.3 720p) DMD to provide a compact, reliable, high-efficiency display solution for many different video display applications. The DMDs are spatial light modulators which reflect incoming light from an illumination source to one of two directions with the primary direction being into collection optics within a projection lens. The projection lens sends the light to the destination needed for the application. Each application is derived primarily from the optical architecture of the system and the format of the pixel data being input into the DLPC343x.

In display applications using the DLP2010 DMD or DLP3010 DMD, the DLPA2005 provides all needed analog functions including the analog power supplies and the RGB LED driver to provide a robust and efficient display solution. Display applications of interest include pico-projectors embedded in display devices like smart phones, tablets, cameras, and camcorders. Other applications include wearable (near-eye) displays, battery-powered mobile accessory, interactive display, low latency gaming displays, and digital signage.

Alternately, a DLPC150 controller can be used with a DLP2010 or DLP2010NIR DMD. Applications of interest when using the DLPC150 controller include machine vision systems, spectrometers, skin analysis, medical systems, material identification, chemical sensing, infrared projection, and compressive sensing. In a spectroscopy application the DLPC150 controller and DLP2010NIR DMD are often combined with a single element detector to replace expensive InGaAs array-based detector designs. In this application the DMD acts as a wavelength selector reflecting specific wavelengths of light into the single point detector.

8.2 Typical Projector Application

A common application when using DLPA2005 with DLP2010 DMD and DLPC3430/DLPC3435 controller is for creating an accessory projector for a smart phone, tablet or any other portable smart device. The DLPC3430/DLPC3435 in an accessory projector typically receives images from a smart device over either HDMI as shown below (WI-FI can also be used to transmit data). DLPA2005 provides power supply sequencing and controls the RGB LED currents as required by the application.

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Typical Projector Application (continued)

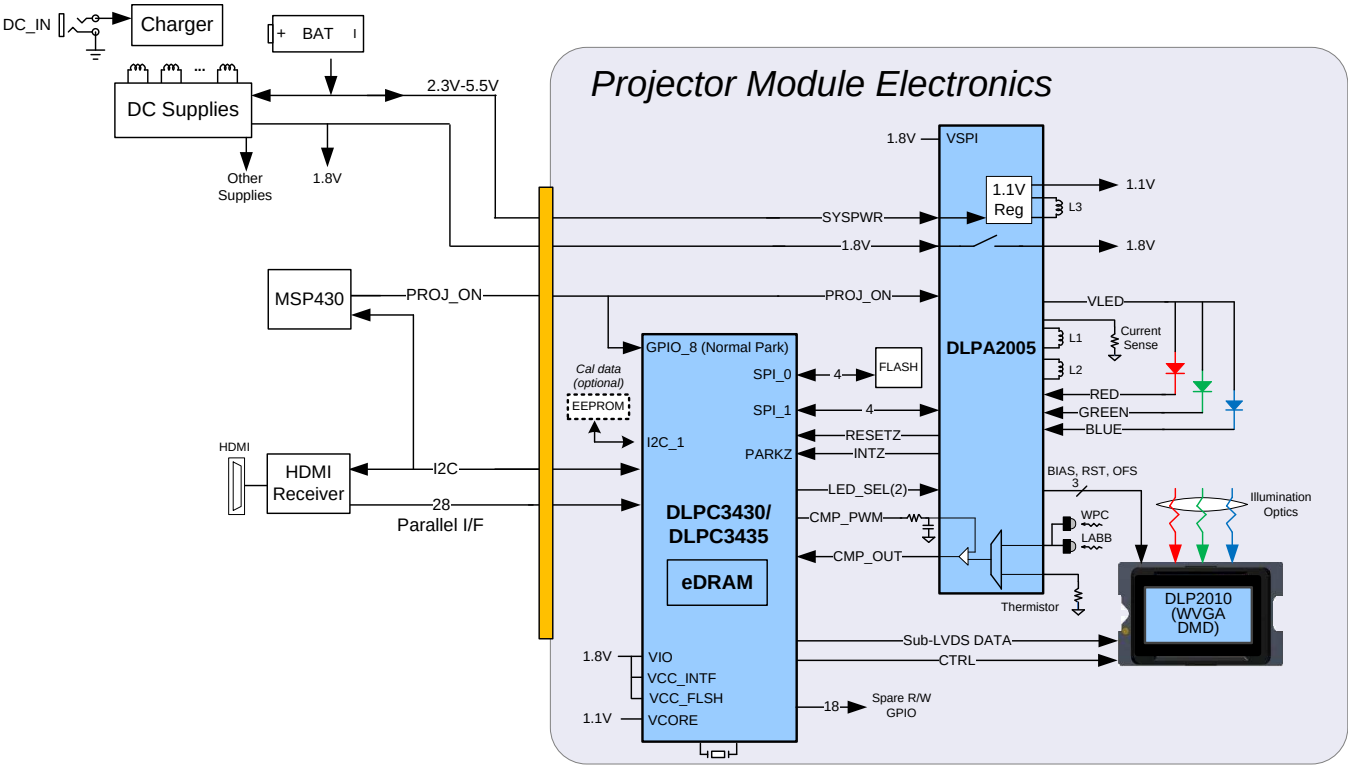

Figure 15. Typical Setup Using DLPA2005

8.2.1 Design Requirements

A pico-projector is created by using a DLP chip set comprised of DLP2010 (.2 WVGA) DMD, DLPC3430 or DLPC3435 controller and DLPA2005 PMIC/LED driver. The DLPC3430 or DLPC3435 does the digital image processing, the DLPA2005 provides the needed analog functions for the projector, and DMD is the display device for producing the projected image. In addition to the three DLP chips in the chip set, other chips may be needed. At a minimum a flash part is needed to store the software and firmware to control the DLPC3430 or DLPC3435. The illumination light that is applied to the DMD is typically from red, green, and blue LEDs. These are often contained in three separate packages, but sometimes more than one color of LED die may be in the same package to reduce the overall size of the pico-projector. For connecting the DLPC3430 or DLPC3435 to the front end for receiving images parallel interface is used. While using parallel interface, I^2C should be connected to the front end for sending commands to the DLPC3430 or DLPC3435. The only power supplies needed external to the projector are the battery (SYSPWR) and a regulated 1.8 V supply. The entire pico-projector can be turned on and off by using a single signal called PROJ_ON. When PROJ_ON is high, the projector turns on and begins displaying images. When PROJ_ON is set low, the projector turns off and draws just microamps of current on SYSPWR. When PROJ_ON is set low, the 1.8 V supply can continue to be left at 1.8 V and used by other non-projector sections of the product. If PROJ_ON is low, the DLPA2005 will not draw current on the 1.8 V supply.

8.2.2 Detailed Design Procedure

For connecting together the DLP2010, DLPC3430 or DLPC3435 and DLPA2005, see the reference design schematic. When a circuit board layout is created from this schematic a very small circuit board is possible. An example small board layout is included in the reference design data base. Layout guidelines should be followed to achieve a reliable projector. The optical engine that has the LED packages and the DMD mounted to it is typically supplied by an optical OEM who specializes in designing optics for DLP projectors.

Typical Projector Application (continued)

8.2.3 Application Curves

As the LED currents that are driven time-sequentially through the red, green, and blue LEDs are increased, the brightness of the projector increases. This increase is somewhat non-linear, and the curve for typical white screen lumens changes with LED currents. It's assumed that the same current amplitude is applied to the red, green, and blue LEDs.

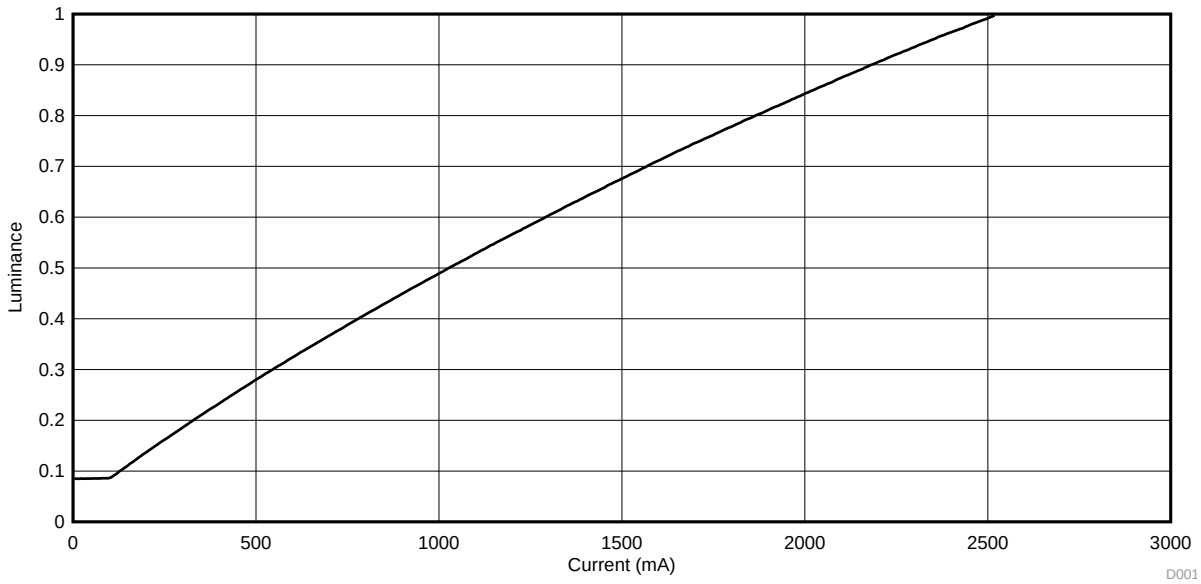

Figure 16. Luminance vs Current

8.3 Typical Mobile Sensing Application

A typical embedded system application using the DLPC150 controller and the DLPC2010NIR is shown in Figure 17. In this configuration, the DLPC150 controller supports a 24-bit parallel RGB input, typical of LCD interfaces, from an external source or processor. The DLPC150 controller processes the digital input image and converts the data into the format needed by the DLP2010NIR. The DLP2010NIR steers light by setting specific micromirrors to the "on" position, directing light to the detector, while unwanted micromirrors are set to "off" position, directing light away from the detector. The microprocessor sends binary images to the DLP2010NIR to steer specific wavelengths of light into the detector. The microprocessor uses an analog-to-digital converter to sample the signal received by the detector into a digital value. By sequentially selecting different wavelengths of light and capturing the values at the detector, the microprocessor can then plot a spectral response to the light.

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Typical Mobile Sensing Application (continued)

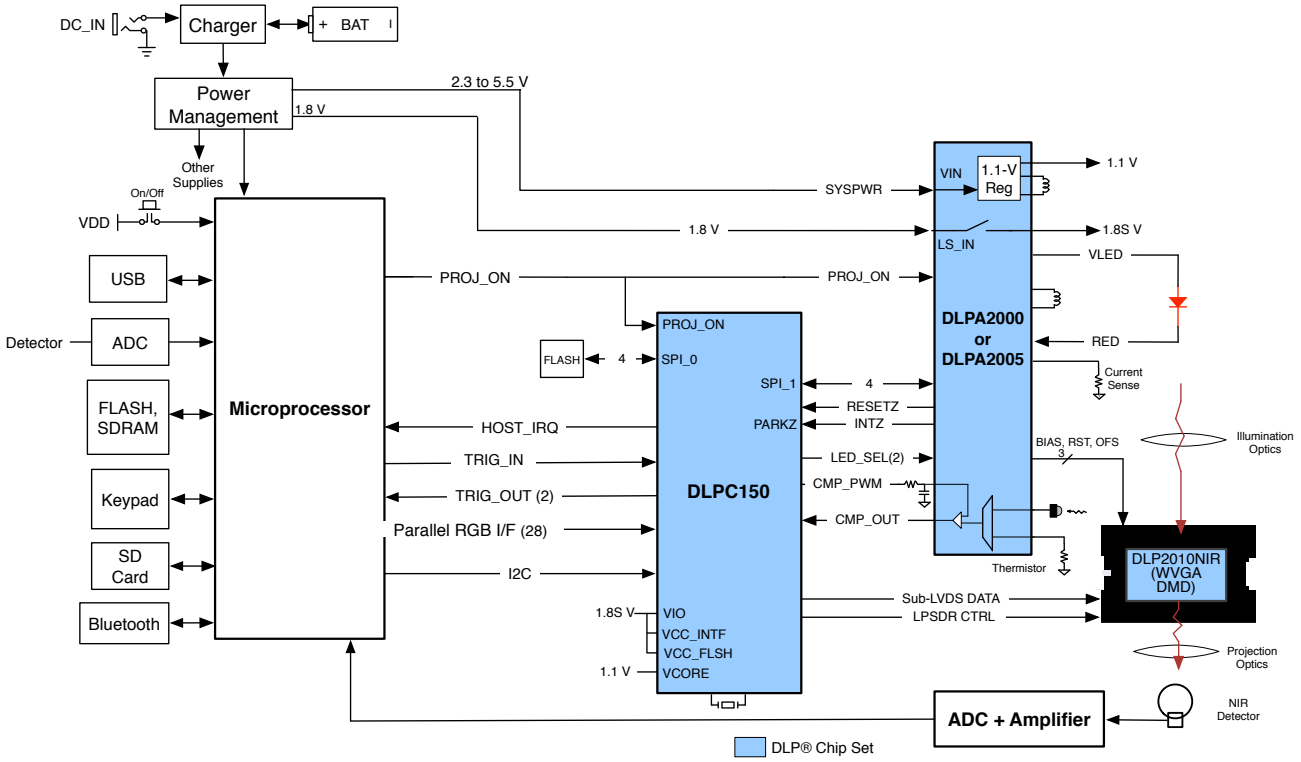

Figure 17. Typical Application Diagram

8.3.1 Design Requirements

All applications using the DLP 0.2-inch WVGA chipset require the:

- DLPC150 controller, and
- DLPA2005 PMIC, and
- DLP2010 or DLP2010NIR DMD

components for operation. The system also requires an external parallel flash memory device loaded with the DLPC150 configuration and support firmware. DLPC150 does the digital image processing and formats the data for the DMD. DLPA2005 PMIC provides the needed analog functions for the DLPC150 and DLP2010 or DLP2010NIR. The chipset has several system interfaces and requires some support circuitry. The following interfaces and support circuitry are required:

- DLPC150 system interfaces:
  - Control interface
  - Trigger interface
  - Input data interface
  - Illumination interface
- DLPC150 support circuitry and interfaces:
  - Reference clock
  - PLL
  - Program memory flash interface
- DMD interfaces:
  - DLPC150 to DMD digital data
  - DLPC150 to DMD control interface
  - DLPC150 to DMD micromirror reset control interface

Typical Mobile Sensing Application (continued)

8.3.2 Detailed Design Procedure

8.3.2.1 Dlpc150 System Interfaces

The 0.2-inch WVGA chipset supports a16-bit or 24-bit parallel RGB interface for image data transfers from another device. There are two primary output interfaces: illumination driver control interface and sync outputs.

8.3.2.1.1 Control Interface

The 0.2-inch WVGA chipset supports I2C commands through the control interface. The control interface allows another master processor to send commands to the DLPC150 controller to query system status or perform realtime operations such as LED driver current settings.

8.3.3 Application Curve

In a reflective spectroscopy application, a broadband light source illuminates a sample and the reflected light spectrum is dispersed onto the DLP2010NIR. A microprocessor in conjunction with the DLPC150 controls individual DLP2010NIR micromirrors to reflect specific wavelengths of light to a single point detector. The microprocessor uses an analog-to-digital converter to sample the signal received by the detector into a digital value. By sequentially selecting different wavelengths of light and capturing the values at the detector, the microprocessor can then plot a spectral response to the light. This systems allows the measurement of the collected light and derive the wavelengths absorbed by the sample. This process leads to the absorption spectrum shown in Figure 18.

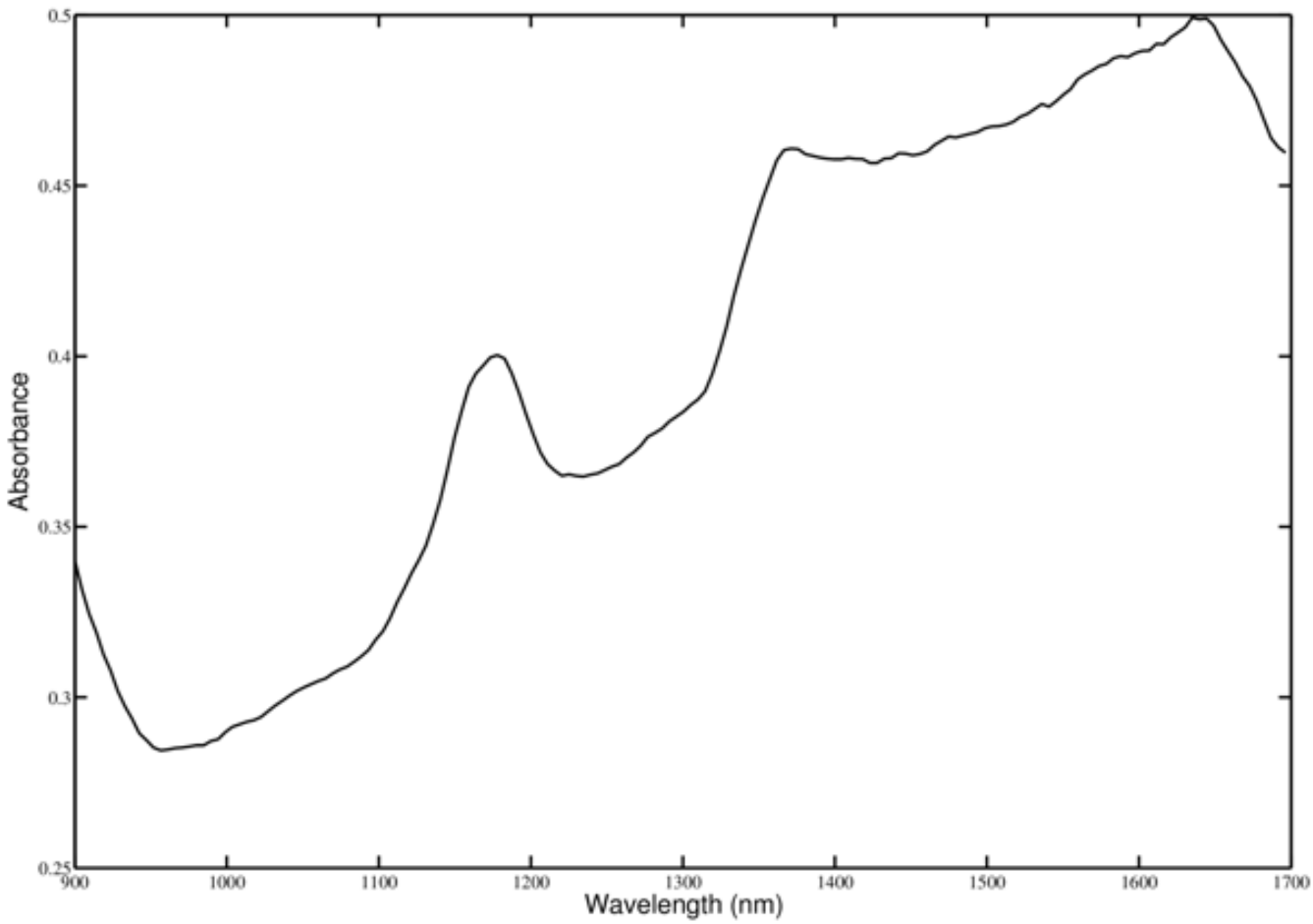

Figure 18. Sample Dlpc150 Based Spectrometer Output

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9 Power Supply Recommendations

The DLPA2005 is designed to operate from a 2.3 to 6 V input voltage supply or battery. To avoid insufficient supply current due to line drop, ringing due to trace inductance at the VIN terminal, or supply peak current limitations, additional bulk capacitance may be required. In the case ringing that is caused by the interaction with the ceramic input capacitors, an electrolytic or tantalum type capacitor may be needed for damping.

The amount of bulk capacitance required should be evaluated such that the input voltage can remain in spec long enough for a proper fast shutdown to occur for the vofs, vrst, and vbias supplies. The shutdown begins when the input voltage drops below the programmable UVLO threshold such as when the external power supply or battery supply is suddenly removed from the system.

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10 Layout

10.1 Layout Guidelines

As for all chips with switching power supplies, the layout is an important step in the design, especially in the case of high peak currents and high switching frequencies. If the layout is not carefully done, the regulators could show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current paths and for the power ground tracks. Input capacitors, output capacitors, and inductors should be placed as close as possible to the IC.

Figure 19 shows an example layout that has critical parts placed as close as possible to the pins they are connected to. Here are recommendations for the following components:

R1	is RLIM and is connected via a wide trace (low resistance) to the system ground. The analog ground at pin 5 should be star connected to the point where RLIM is connected to the system ground. Aim on a wide and low-ohmic trace as well, although this one is less critical (tens of mA).
L1	is the big inductor for the VLED that is connected via two wide traces to the pins
C4	are the decoupling capacitors for the VLED and they are as close as possible placed to the part and directly connected to ground.
L3/C20	are components used for the VCORE BUCK. L3 is placed close to the pin and connected with a wide trace to the part. C20 is placed directly beside the inductor and connected to the PGND pin
L2	This inductor is part of the DMD reset regulators and is also placed as close as possible to the DLPA2005 using wide PCB traces.

10.2 Layout Example

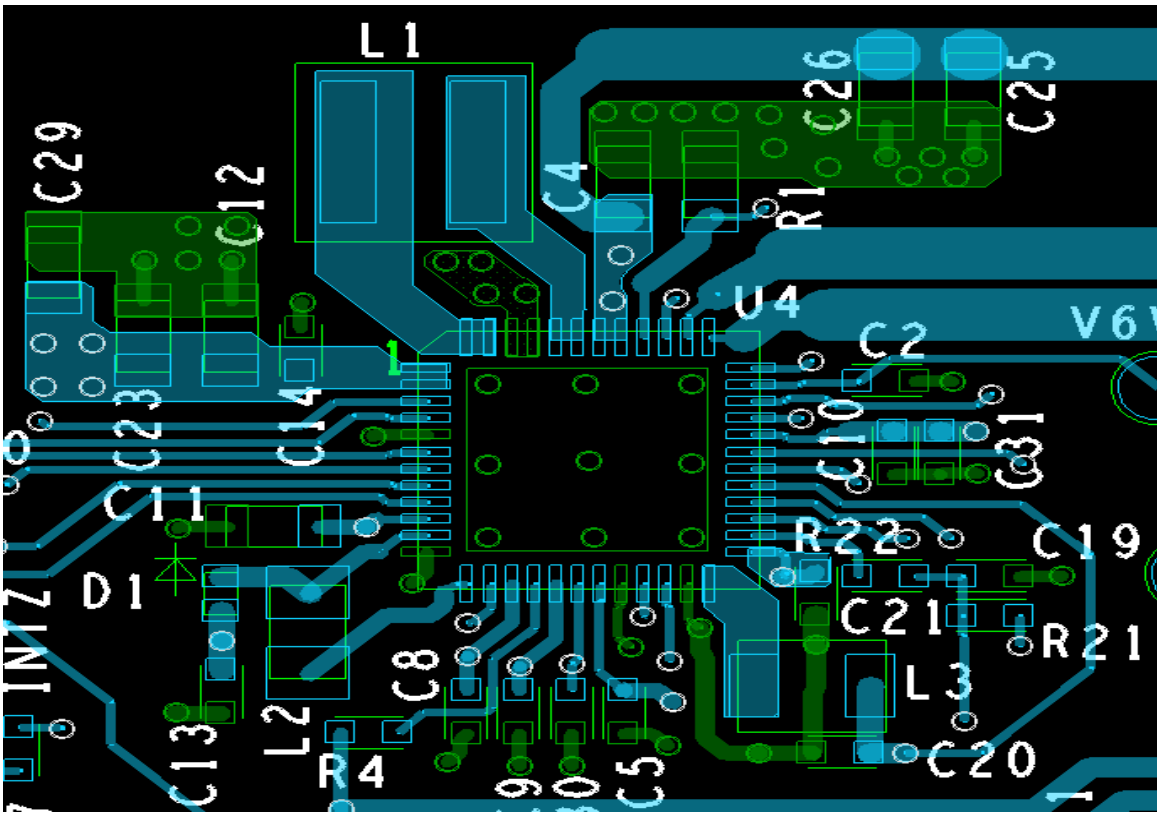

Figure 19. Example Layout of DLPA2005

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10.3 Thermal Considerations

An important consequence of the efficiency numbers shown in Figure 7 is that it enables to perform DLPA2005 thermal calculations. Since the efficiency is not 100%, power is dissipated in the DLPA2005 chip. Due to that dissipation die temperature will rise. For reliability reasons it is good to aim for as low as possible die temperatures. Using a heat sink and airflow are efficient means to keep die temperature reasonably low. In cases that airflow and / or a heat sink are / is not feasible, the system designer should specifically pay attention to the thermal design. The die temperature for regular operation should remain below 120°C.

In the following an example is given of such a thermal calculation. The calculation starts with summarizing all blocks in the DLPA2005 that dissipate. Clearly, the buck-boost converter supplying the LED power is the main source of dissipation. For illustrating purposes here we assume this buck-boost converter to be the only block that dissipates significantly. For the example assume: VOUT=4.8 V (for all three LEDs), IOUT=2.4 A and VIN=5 V. From Figure 7 it can be derived that the related efficiency equals about n_{eff}=88%.

The power dissipated by the DLPA2005 is then given by:

$$P_{DISS} = P_{IN} - P_{OUT} = P_{OUT}\left(\frac{100\%}{\eta_{eff}} - 1\right) = 4.8V \cdot 2.4A \cdot \left(\frac{100\%}{88\%} - 1\right) = 1.6W$$

The rise of die temperature due to this power dissipation can be calculated using the thermal resistance from junction to ambient, M JA=27.9°C/W. This calculation yields:

$$T_{JUNCTION} = T_{AMBIENT} + P_{DISS} \cdot \theta_{JA} = 25°C + 1.6W \cdot 27.9°C/W = 69.6°C$$

It is also possible to calculate the maximum allowable ambient temperature to prevent surpassing the maximum die temperature. Assume again the dissipation of PDISS=1.6W. The maximum ambient temperature that is allowed is then given by:

$$T_{AMBIENT-\max} = T_{JUNCTION-\max} - P_{DISS} \cdot \theta_{JA} = 120°C - 1.6W \cdot 27.9°C/W = 75.4°C$$

It is again stressed here that for proper calculations the total power dissipation of the PAD2005 should be taken into account. On top of that, if components that are close to the PAD2005 also dissipate a significant amount of power, the (local) ambient temperature can be higher than the ambient temperature of the system.

If calculations show that the die temperature will surpass the maximum specified value, two basic options exist:

- Adding a heat sink with or without airflow. This will reduce 0_{JA} yielding lower die temperature.
- Lowering the dissipation in the PAD2005 implying lowering the maximum allowable LED current.

11 Device and Documentation Support

11.1 Device Support

11.1.1 Device Nomenclature

Package Marking DLPA2005
(TOP VIEW)

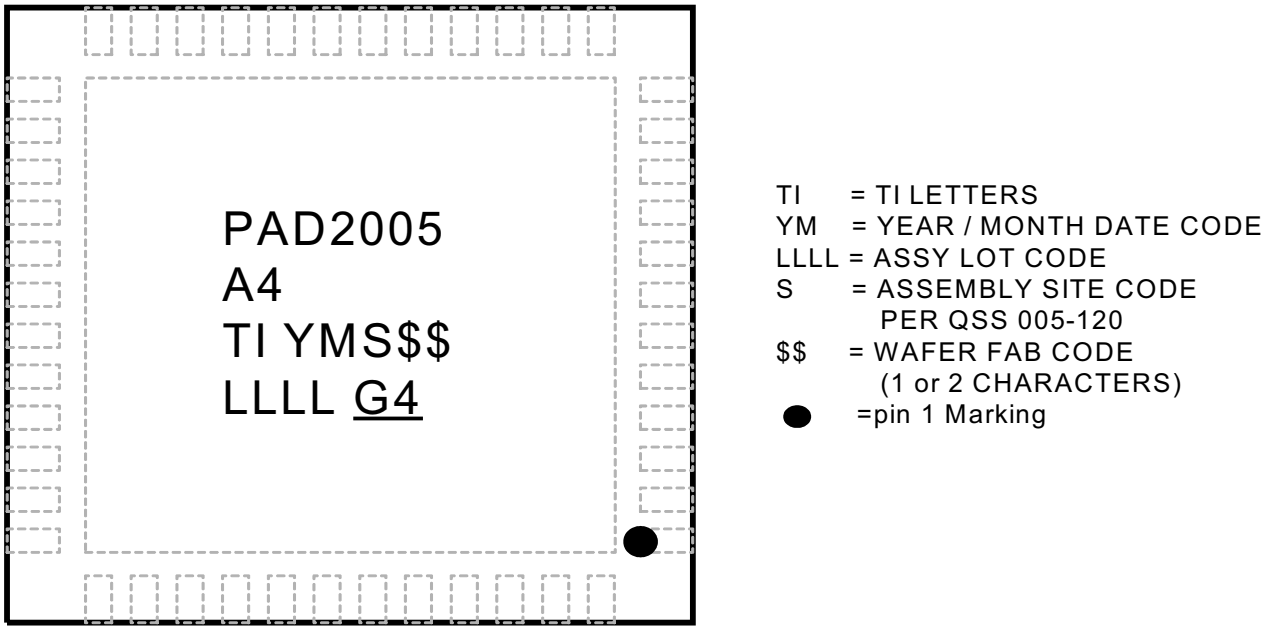

Figure 20. Package Marking DLPA2005 (Top View)

11.2 Trademarks

Pico is a trademark of Texas Instruments.
DLP is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Cover Tape The cover tape does not cover the index hole and does not shift to outside from carrier tape.

ESD Countermeasure Plastic material used in both carrier tape and cover tape are static dissipative.

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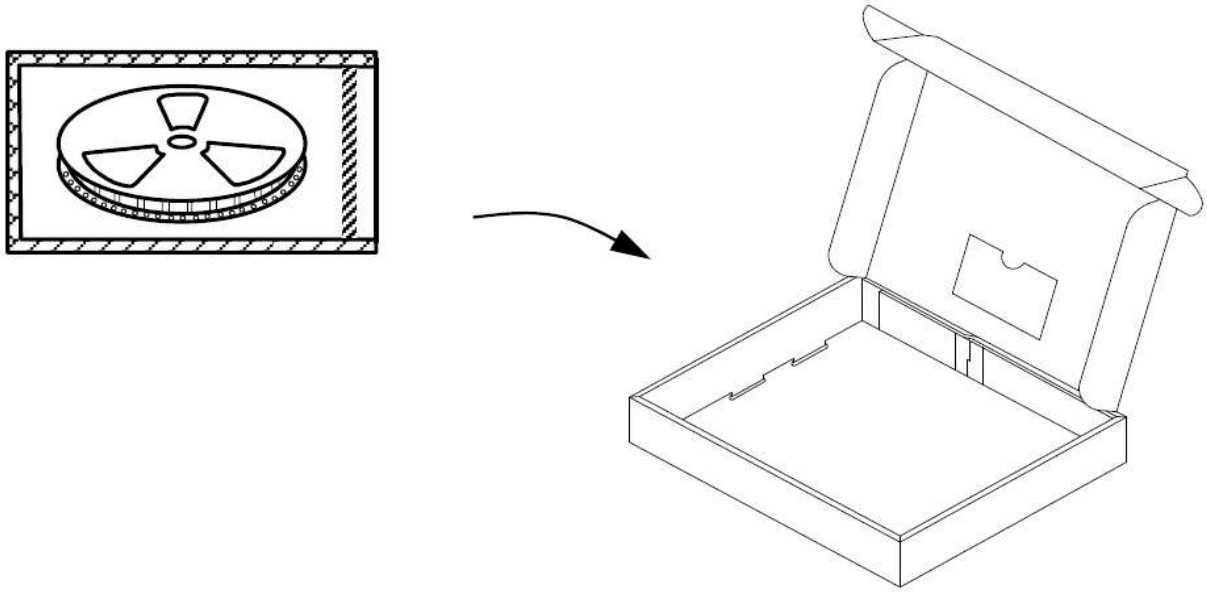
Insertion of Device The device is located such as symbolization in upper side and lead pins in lower side.

Packing Method The reel is packed into Moisture Barrier bag and fastened by heat-sealing after fixed the end of leader tape by tape. The QFN device packing includes desiccant, humidity indicator.

Reel Box Each Moisture Barrier bag is packed into reel box.

Tape Structure The carrier tape is made of plastic and the structure is shown in above schematic. The device is put on embossed area of carrier tape, and covered by cover tape made of plastic.



Reel box (carton)

Reel Box Material Corrugated Fiberboard

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DLPA2005ERSLR	ACTIVE	VQFN	RSL	48	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR		PAD2005 A4	Samples
DLPA2005ERSLT	ACTIVE	VQFN	RSL	48	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR		PAD2005 A4	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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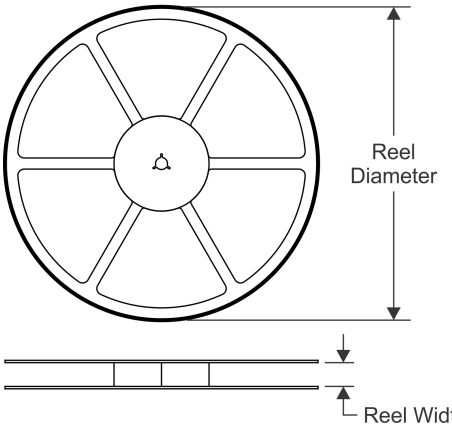
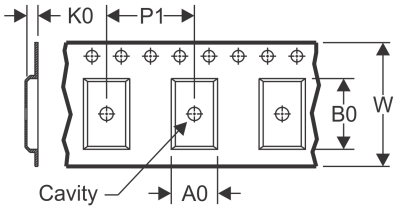
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

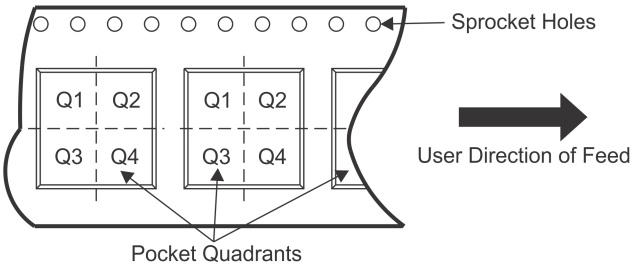


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

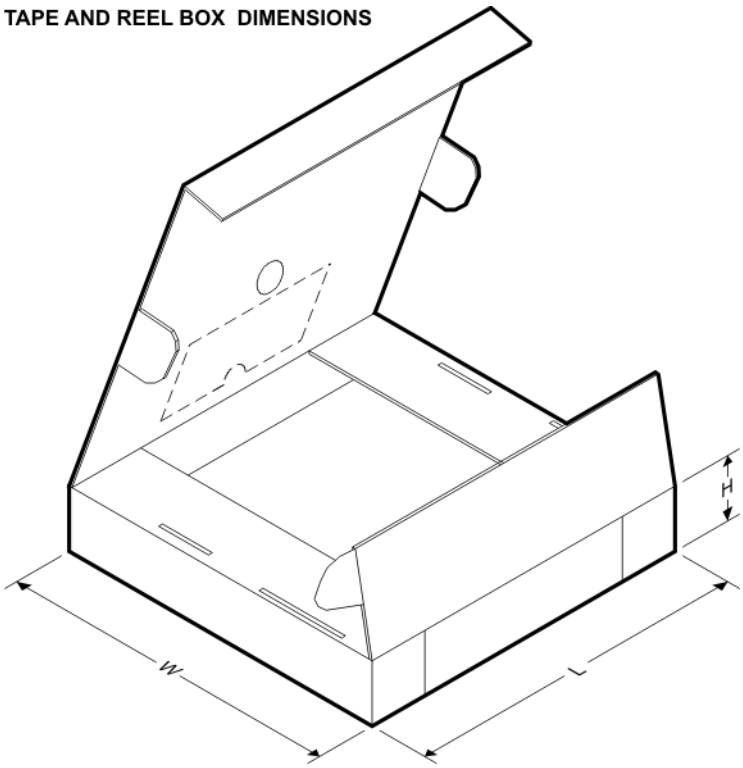
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DLPA2005ERSLR	VQFN	RSL	48	3000	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
DLPA2005ERSLT	VQFN	RSL	48	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2

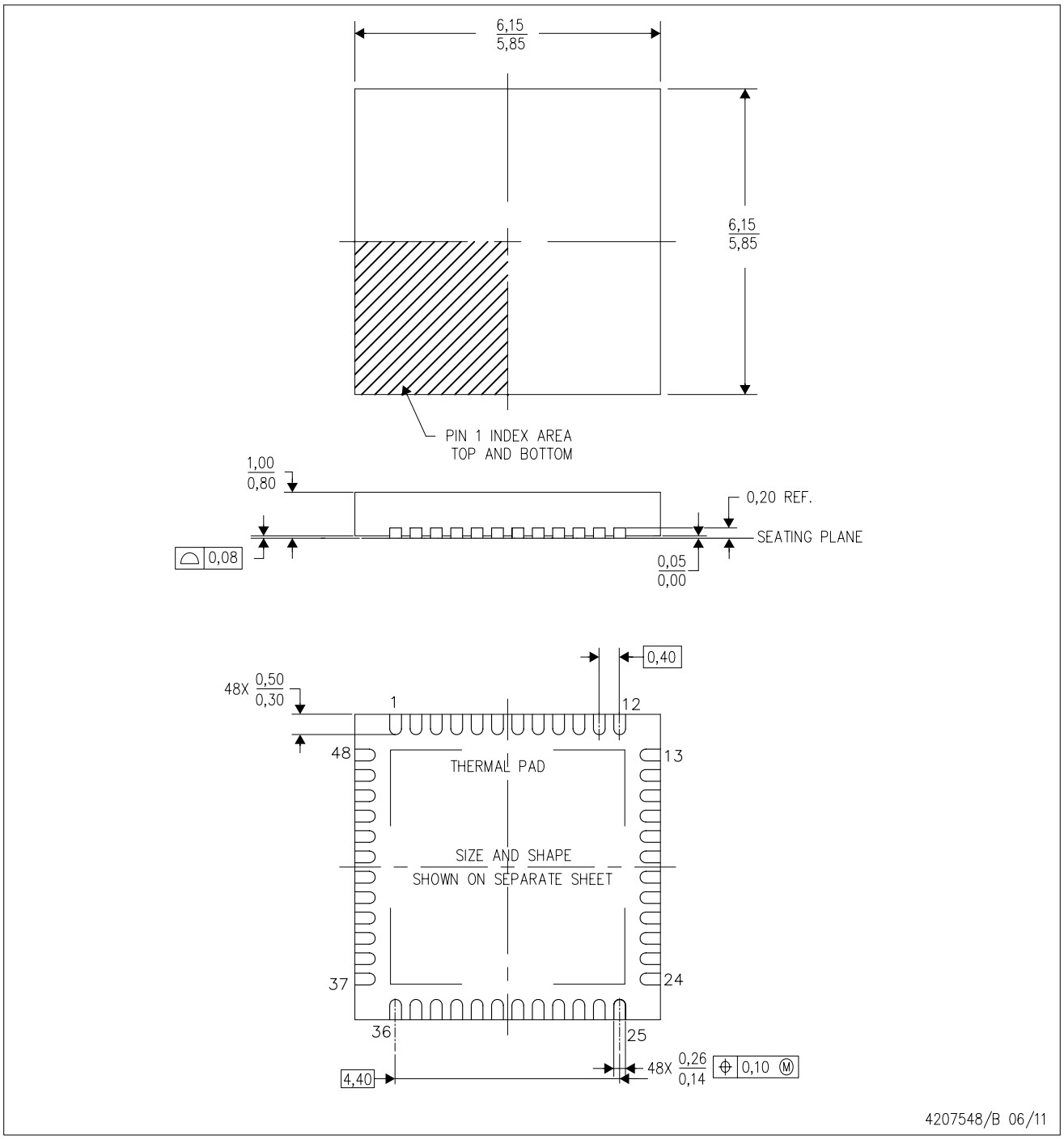
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DLPA2005ERSLR	VQFN	RSL	48	3000	367.0	367.0	38.0
DLPA2005ERSLT	VQFN	RSL	48	250	210.0	185.0	35.0

RSL (S-PVQFN-N48) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No-leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

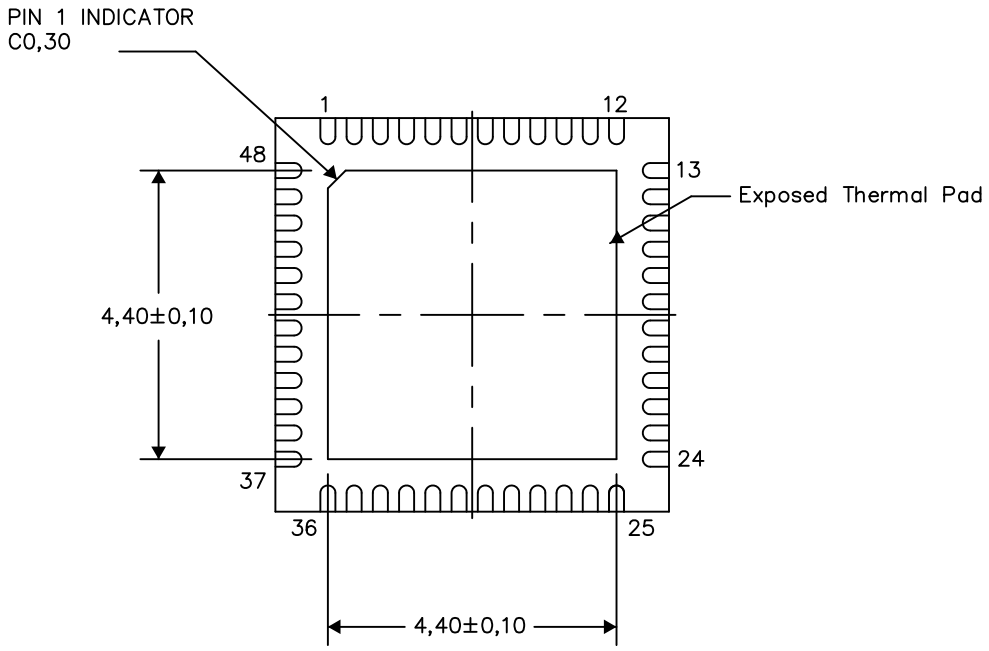
RSL (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



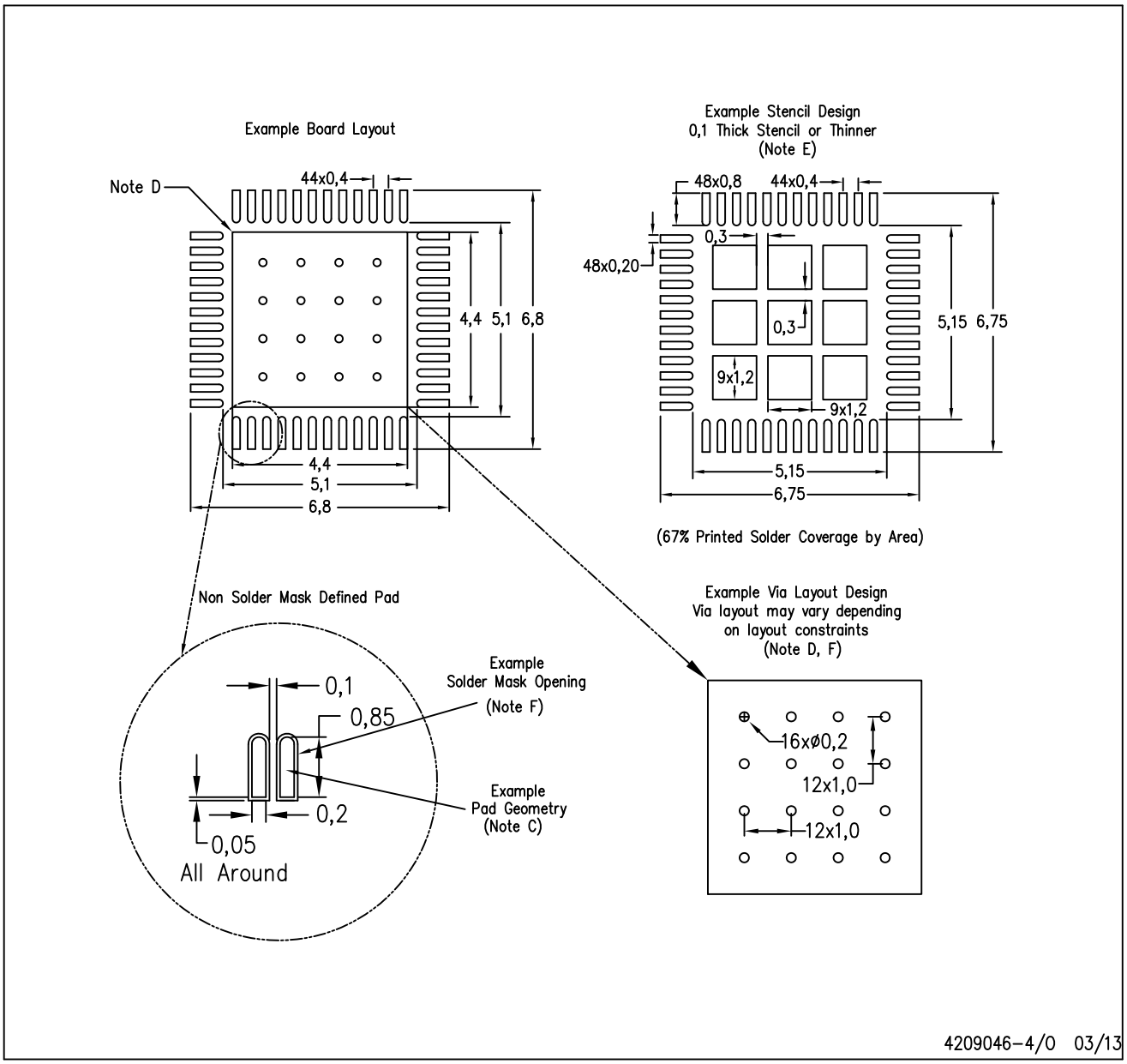
Bottom View

Exposed Thermal Pad Dimensions

4207841–2/P 03/13

NOTE: All linear dimensions are in millimeters

RSL (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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