DLP470TP .47 4K UHD DMD

1 Features

- 0.47-Inch diagonal micromirror array
  - 4K UHD (3840 × 2160) Display Resolution
  - 5.4-µm micromirror pitch
  - ±17° micromirror tilt (relative to flat surface)
  - Bottom illumination
- 2xLVDS input data bus
- Supports 4K UHD at 60 Hz and full HD at 240 Hz
- LED operation supported by two dedicated DLPC6421 display controllers, and DLPA3005 power management device (PMIC) and LED driver

2 Applications

- Mobile smart TV
- Mobile projector
- Digital signage
- Commercial gaming
- Smart home displays
- Mobile home cinema

3 Description

The DLP470TP digital micromirror device (DMD) is a digitally controlled micro-electromechanical system (MEMS) spatial light modulator (SLM) that enables bright 4K UHD display systems. The DLP® 0.47” 4K UHD chipset is composed of the DMD, two DLPC6421 display controllers, and DLPA3005 PMIC and LED driver. The compact physical size of the chipset provides a complete system solution that enables small form factor 4K UHD displays.

The DLP470TP ecosystem includes established resources to help the user accelerate the design cycle, which include production ready optical modules, optical module manufacturers, and design houses.

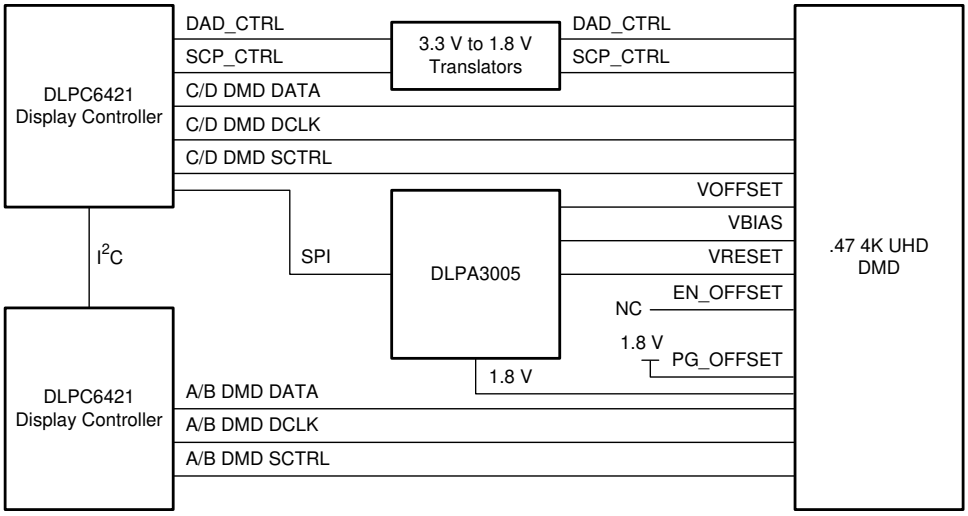
Visit the Getting Started with TI DLP Pico™ display technology page to learn more about how to start designing with the DMD.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DLP470TP	FQN (250)	25.65 mm × 16.9 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Application (LED Configuration)



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

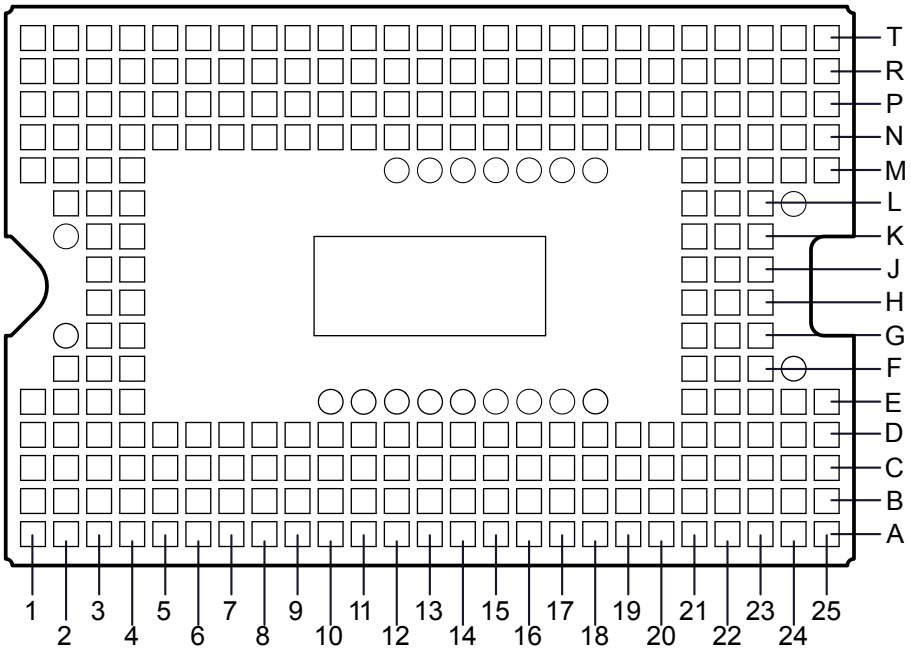
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
September 2019	*	Initial release

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5 Pin Configuration and Functions

FQN Package
250-Pin CLGA
Bottom View



CAUTION

To ensure reliable, long-term operation of the .47” 4K UHD S316 DMD, it is critical to properly manage the layout and operation of the signals identified in the table below.

For specific details and guidelines, refer to the *PCB Design Requirements for TI DLP Pico TRP Digital Micromirror Devices* application report before designing the board.

Pin Functions[1]

PIN		I/O[2]	SIGNAL	DATA RATE	INTERNAL TERMINATION	DESCRIPTION	TRACE LENGTH (mm)
NAME	NO.						
D_AN(0)	B5	I	LVDS	DDR	Differential	Data negative	8.98747
D_AN(1)	B1						8.97919
D_AN(2)	B3						9.21384
D_AN(3)	F2						9.39087
D_AN(4)	D2						9.54145
D_AN(5)	D3						9.27074
D_AN(6)	C7						9.02002
D_AN(7)	B9						9.36086
D_AN(8)	C9						9.0579
D_AN(9)	D7						9.38275
D_AN(10)	B10						9.06869
D_AN(11)	B13						9.04589
D_AN(12)	C11						9.46624
D_AN(13)	D10						9.09742
D_AN(14)	C12						9.09742
D_AN(15)	D12						9.42403
D_AP(0)	B4	I	LVDS	DDR	Differential	Data positive	9.08754
D_AP(1)	C1						9.07961
D_AP(2)	B2						9.31429
D_AP(3)	F3						9.50425
D_AP(4)	E2						9.65859
D_AP(5)	D4						9.3646
D_AP(6)	C6						9.12022
D_AP(7)	B8						9.46125
D_AP(8)	C8						9.15806
D_AP(9)	D6						9.48372
D_AP(10)	B11						9.1687
D_AP(11)	B12						9.14277
D_AP(12)	C10						9.5666
D_AP(13)	D9						9.19838
D_AP(14)	C13						9.40291
D_AP(15)	D13						9.52321

(1) The .47” 4K UHD 2xLVDS series 316 DMD is a component of one or more DLP chipsets. Use the .47” 4K UHD 2xLVDS series 316 DMD in conjunction with other components of the applicable DLP chipset to make sure there is reliable operation. These include components that contain or implement TI DMD control technology. TI DMD control technology consists of the TI technology and devices used for operating or controlling a DLP DMD.
(2) I = Input, O = Output, P = Power, G = Ground, NC = No connect.

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Pin Functions[1] (continued)

PIN		I/O[2]	SIGNAL	DATA RATE	INTERNAL TERMINATION	DESCRIPTION	TRACE LENGTH (mm)
NAME	NO.						
D_BN(0)	R5	I	LVDS	DDR	Differential	Data negative	9.10693
D_BN(1)	R1						8.96073
D_BN(2)	P3						9.10705
D_BN(3)	T2						9.06795
D_BN(4)	N3						9.48088
D_BN(5)	N1						9.85003
D_BN(6)	P7						9.06246
D_BN(7)	R7						9.64953
D_BN(8)	P9						9.37131
D_BN(9)	N7						9.40519
D_BN(10)	R10						9.06869
D_BN(11)	R13						9.0549
D_BN(12)	P11						9.45471
D_BN(13)	N10						9.09742
D_BN(14)	P12						9.37251
D_BN(15)	N12						9.43745
D_BP(0)	R4	I	LVDS	DDR	Differential	Data positive	9.21371
D_BP(1)	P1						9.06786
D_BP(2)	R3						9.20554
D_BP(3)	R2						9.17689
D_BP(4)	M3						9.59954
D_BP(5)	N2						9.94411
D_BP(6)	P6						9.16937
D_BP(7)	R6						9.75042
D_BP(8)	P8						9.47818
D_BP(9)	N6						9.51286
D_BP(10)	R11						9.16197
D_BP(11)	R12						9.15849
D_BP(12)	P10						9.55989
D_BP(13)	N9						9.20509
D_BP(14)	P13						9.46661
D_BP(15)	N13						9.52992

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Pin Functions[1] (continued)

PIN		I/O[2]	SIGNAL	DATA RATE	INTERNAL TERMINATION	DESCRIPTION	TRACE LENGTH (mm)
NAME	NO.						
D_CN(0)	C15	I	LVDS	DDR	Differential	Data negative	9.41325
D_CN(1)	C16						9.03449
D_CN(2)	D15						9.52465
D_CN(3)	C18						9.02915
D_CN(4)	B17						9.04775
D_CN(5)	D18						9.02956
D_CN(6)	B18						9.36461
D_CN(7)	D21						9.02729
D_CN(8)	C20						9.11449
D_CN(9)	B20						9.00902
D_CN(10)	C22						9.05166
D_CN(11)	C24						8.99211
D_CN(12)	B22						9.0163
D_CN(13)	A25						9.15166
D_CN(14)	D25						9.17016
D_CN(15)	A23						9.03448
D_CP(0)	C14	I	LVDS	DDR	Differential	Data positive	9.50523
D_CP(1)	C17						9.1478
D_CP(2)	D16						9.64383
D_CP(3)	C19						9.12978
D_CP(4)	B16						9.13427
D_CP(5)	D19						9.13402
D_CP(6)	B19						9.46507
D_CP(7)	D22						9.12774
D_CP(8)	C21						9.2337
D_CP(9)	B21						9.12611
D_CP(10)	C23						9.15286
D_CP(11)	D24						9.09244
D_CP(12)	B23						9.14094
D_CP(13)	B25						9.25197
D_CP(14)	E25						9.2705
D_CP(15)	A24						9.14097

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Pin Functions[1] (continued)

PIN		I/O[2]	SIGNAL	DATA RATE	INTERNAL TERMINATION	DESCRIPTION	TRACE LENGTH (mm)
NAME	NO.						
D_DN(0)	P15	I	LVDS	DDR	Differential	Data negative	9.39144
D_DN(1)	P16						9.03449
D_DN(2)	N15						9.4803
D_DN(3)	P18						8.96795
D_DN(4)	R17						9.04775
D_DN(5)	N18						9.02956
D_DN(6)	R18						9.36461
D_DN(7)	N21						9.02729
D_DN(8)	P20						9.11449
D_DN(9)	R20						9.00902
D_DN(10)	P22						9.03774
D_DN(11)	P24						8.99211
D_DN(12)	R22						8.9767
D_DN(13)	T25						9.13373
D_DN(14)	N25						9.15485
D_DN(15)	T23						9.03448
D_DP(0)	P14	I	LVDS	DDR	Differential	Data positive	9.49852
D_DP(1)	P17						9.1316
D_DP(2)	N16						9.60619
D_DP(3)	P19						9.06186
D_DP(4)	R16						9.14735
D_DP(5)	N19						9.12731
D_DP(6)	R19						9.45836
D_DP(7)	N22						9.12103
D_DP(8)	P21						9.22699
D_DP(9)	R21						9.1194
D_DP(10)	P23						9.13666
D_DP(11)	N24						9.08573
D_DP(12)	R23						9.07467
D_DP(13)	R25						9.22784
D_DP(14)	M25						9.26064
D_DP(15)	T24						9.14037
SCTRL_AN	E4	I	LVDS	DDR	Differential	Serial control negative	9.44429
SCTRL_AP	F4	I	LVDS	DDR	Differential	Serial control positive	9.5515
SCTRL_BN	N4	I	LVDS	DDR	Differential	Serial control negative	9.80493
SCTRL_BP	M4	I	LVDS	DDR	Differential	Serial control positive	9.89456
SCTRL_CN	E23	I	LVDS	DDR	Differential	Serial control negative	9.19249
SCTRL_CP	F23	I	LVDS	DDR	Differential	Serial control positive	9.29266
SCTRL_DN	M23	I	LVDS	DDR	Differential	Serial control negative	9.19321
SCTRL_DP	L23	I	LVDS	DDR	Differential	Serial control positive	9.28668
DCLK_AN	C5	I	LVDS		Differential	Clock negative	9.4868
DCLK_AP	C4	I	LVDS		Differential	Clock positive	9.58794
DCLK_BN	P5	I	LVDS		Differential	Clock negative	9.67816
DCLK_BP	P4	I	LVDS		Differential	Clock positive	9.78601
DCLK_CN	E21	I	LVDS		Differential	Clock negative	9.54268
DCLK_CP	E22	I	LVDS		Differential	Clock positive	9.6428

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Pin Functions[1] (continued)

PIN		I/O[2]	SIGNAL	DATA RATE	INTERNAL TERMINATION	DESCRIPTION	TRACE LENGTH (mm)
NAME	NO.						
DCLK_DN	M21	I	LVDS		Differential	Clock negative	9.54268
DCLK_DP	M22	I	LVDS		Differential	Clock positive	9.63609
SCPCLK	B6	I	LVCMOS		Pull down	Serial communications port clock. Active only when SCPENZ is logic low.	
SCPDI	A7	I	LVCMOS	SDR	Pull down	Serial communications port data input. Synchronous to SCPCLK rising edge.	
SCPENZ	A8	I	LVCMOS		Pull down	Serial communications port enable active low.	
SCPDO	B7	O	LVCMOS	SDR		Serial communications port output.	
RESET_ADDR(0)	T8	I	LVCMOS		Pull down	Reset driver address select	
RESET_ADDR(1)	R9						
RESET_ADDR(2)	T7						
RESET_ADDR(3)	R8						
RESET_MODE(0)	T5	I	LVCMOS		Pull down	Reset driver mode select	
RESET_SEL(0)	T4	I	LVCMOS		Pull down	Reset driver level select	
RESET_SEL(1)	L2	I	LVCMOS		Pull down	Reset driver level select	
RESET_STROBE	L4	I	LVCMOS		Pull down	Rising edge latches in RESET_ADDR, RESET_MODE, & RESET_SEL	
PWRDNZ	A4	I	LVCMOS		Pull down	Active low device reset	
RESET_OEZ	T14	I	LVCMOS		Pull up	Active low output enable for internal reset driver circuits	
RESET_IRQZ	R14	O	LVCMOS			Active low output interrupt to DLP display controller	
EN_OFFSET	C3	O	LVCMOS			Active high enable for external V_{OFFSET} regulator	
PG_OFFSET	A2	I	LVCMOS		Pull up	Active low fault from external V_{OFFSET} regulator	
TEMP_N	A16	I	Analog			Temperature sensor diode cathode	
TEMP_P	B14	I	Analog			Temperature sensor diode anode	
NO CONNECT	E10, E11, E12, E13, E14, E15, E16, E17, M12, M13, M14, M15, K2, G2, L24, F24, M16, M17, M18, E18	NC				Do not connect on DLP system board.	
SCP_TEST_MUX	A5	I	LVCMOS		Pull down	Connect to ground on DLP system board	
V_{BIAS}[3]	A19, A20, T19, T20	P	Analog			Supply voltage for positive bias level of micromirror reset signal.	
V_{RESET}[3]	A10, A11, T10, T11	P	Analog			Supply voltage for negative reset level of micromirror reset signal	
V_{OFFSET}[3]	A1, C25, P25, T1, T13	P	Analog			Supply voltage for HVCMOS logic. Supply voltage for positive offset level of micromirror reset signal. Supply voltage for stepped high voltage at micromirror address electrodes.	

(3) V_{BIAS}, V_{CC}, V_{OFFSET}, and V_{RESET} power supplies must be connected for proper DMD operation.

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Pin Functions[1] (continued)

PIN		I/O[2]	SIGNAL	DATA RATE	INTERNAL TERMINATION	DESCRIPTION	TRACE LENGTH (mm)
NAME	NO.						
V_{CC}[3]	A13, A14, D1, E1, F21, F22, G3, G4, G21, G22, G23, H3, H4, H21, H22, H23, J3, J4, J21, J22, J23, K3, K4, K21, K22, K23, L21, L22, M1, M2	P	Analog			Supply voltage for LVCMOS core. Supply voltage for positive offset level of micromirror reset signal during Power down. Supply voltage for normal high level at micromirror address electrodes.	
V_{SS}[4]	A3, A6, A9, A12, A15, A17, A18,A21, A22, B15, B24, C2, D5, D8, D11, D14, D17, D20, D23, E3, E24, L3, M24, N5, N8, N11, N14, N17, N20, N23, P2, R15, R24, T3, T6, T9, T12, T15, T16, T17, T18, T21, T22	G				Device ground. Common return for all power.	

(4) V_{SS} must be connected for proper DMD operation.

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6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
SUPPLY VOLTAGES				
V_{CC}	Supply voltage for LVCMOS core logic(2)	–0.5	2.3	V
V_{OFFSET}	Supply voltage for HVCMOS and micromirror electrode(2)(3)	–0.5	11	V
V_{BIAS}	Supply voltage for micromirror electrode(2)	–0.5	19	V
V_{RESET}	Supply voltage for micromirror electrode(2)	–15	–0.3	V
$\lvert V_{BIAS} - V_{OFFSET} \rvert$	Supply voltage difference (absolute value)(4)		11	V
$\lvert V_{BIAS} - V_{RESET} \rvert$	Supply voltage difference (absolute value)(5)		34	V
INPUT VOLTAGES				
	Input voltage for all other LVCMOS input pins(2)	–0.5	V_{CC} + 0.5	V
$\lvert V_{ID} \rvert$	Input differential voltage (absolute value)(6)		500	mV
I_{ID}	Input differential current(7)		6.3	mA
CLOCKS				
f_{CLOCK}	Clock frequency for LVDS interface, DCLK_A		400	MHz
f_{CLOCK}	Clock frequency for LVDS interface, DCLK_B		400	MHz
f_{CLOCK}	Clock frequency for LVDS interface, DCLK_C		400	MHz
f_{CLOCK}	Clock frequency for LVDS interface, DCLK_D		400	MHz
ENVIRONMENTAL				
T_{ARRAY} and T_{WINDOW}	Temperature, operating(8)	–20	90	°C
	Temperature, non–operating(8)	–40	90	°C
$\lvert T_{DELTA} \rvert$	Absolute temperature delta between any point on the window edge and the ceramic test point TP1(9)		30	°C
T_{DP}	Dew point temperature, operating and non–operating (noncondensing)		81	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device is not implied at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure above or below the *Recommended Operating Conditions* for extended periods of time may affect device reliability.
(2) All voltages are referenced to the common ground V_{SS}. V_{BIAS}, V_{CC}, V_{OFFSET}, and V_{RESET} power supplies are all required for proper DMD operation. V_{SS} must also be connected.
(3) V_{OFFSET} supply transients must be within specified voltages.
(4) Exceeding the recommended allowable voltage difference between V_{BIAS} and V_{OFFSET} may result in excessive current draw.
(5) Exceeding the recommended allowable voltage difference between V_{BIAS} and V_{RESET} may result in excessive current draw.
(6) This maximum LVDS input voltage rating applies when each input of a differential pair is at the same voltage potential.
(7) LVDS differential inputs must not exceed the specified limit or damage may result to the internal termination resistors.
(8) The highest temperature of the active array (as calculated using *Micromirror Array Temperature Calculation*) or of any point along the window edge as defined in Figure 10. The locations of thermal test points TP2, TP3, TP4 and TP5 in Figure 10 are intended to measure the highest window edge temperature. If a particular application causes another point on the window edge to be at a higher temperature, use that point.
(9) Temperature delta is the highest difference between the ceramic test point 1 (TP1) and anywhere on the window edge as shown in Figure 10. The window test points TP2, TP3, TP4, and TP5 shown in Figure 10 are intended to result in the worst case delta. If a particular application causes another point on the window edge to result in a larger delta temperature, use that point.

6.2 Storage Conditions

Applicable for the DMD as a component or non-operating in a system

		MIN	MAX	UNIT
T_{DMD}	DMD storage temperature	–40	85	°C
T_{DP-AVG}	Average dew point temperature, non-condensing (1)		24	°C
T_{DP-ELR}	Elevated dew point temperature range, non-condensing (2)	28	36	°C
CT_{ELR}	Cumulative time in elevated dew point temperature range		6	months

(1) The average over time (including storage and operating) that the device is not in the elevated dew point temperature range.
(2) Limit exposure to dew point temperatures in the elevated range during storage and operation to less than a total cumulative time of CT_{ELR}.

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6.3 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.4 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted). The functional performance of the device specified in this data sheet is achieved when operating the device within the limits defined by this table. No level of performance is implied when operating the device above or below these limits.

		MIN	NOM	MAX	UNIT
VOLTAGE SUPPLY					
V_{CC}	LVCMOS logic supply voltage (1)	1.65	1.8	1.95	V
V_{OFFSET}	Mirror electrode and HVCMOS voltage (1)(2)	9.5	10	10.5	V
V_{BIAS}	Mirror electrode voltage (1)	17.5	18	18.5	V
V_{RESET}	Mirror electrode voltage (1)	–14.5	–14	–13.5	V
$\lvert V_{BIAS} - V_{OFFSET} \rvert$	Supply voltage difference (absolute value) (3)			10.5	V
$\lvert V_{BIAS} - V_{RESET} \rvert$	Supply voltage difference (absolute value) (4)			33	V
LVCMOS INTERFACE					
$V_{IH(DC)}$	DC input high voltage (5)	0.7 × V_{CC}		V_{CC} + 0.3	V
$V_{IL(DC)}$	DC input low voltage (5)	–0.3		0.3 × V_{CC}	V
$V_{IH(AC)}$	AC input high voltage (5)	0.8 × V_{CC}		V_{CC} + 0.3	V
$V_{IL(AC)}$	AC input low voltage (5)	–0.3		0.2 × V_{CC}	V
t_{PWRDNZ}	PWRDNZ pulse duration (6)	10			ns
SCP INTERFACE					
f_{SCPCLK}	SCP clock frequency (7)			500	kHz
t_{SCP_PD}	Propagation delay, clock to Q, from rising–edge of SCPCLK to valid SCPDO (8)	0		900	ns
$t_{SCP_NEG_ENZ}$	Time between falling-edge of SCPENZ and the first rising-edge of SCPCLK	1			µs
$t_{SCP_POS_ENZ}$	Time between falling-edge of SCPCLK and the rising-edge of SCPENZ	1			µs
t_{SCP_DS}	SCPDI clock setup time (before SCPCLK falling edge) (8)	800			ns
t_{SCP_DH}	SCPDI hold time (after SCPCLK falling edge) (8)	900			ns
$t_{SCP_PW_ENZ}$	SCPENZ inactive pulse duration (high level)	2			µs

(1) All voltages are referenced to common ground V_{SS}. V_{BIAS}, V_{CC}, V_{OFFSET}, and V_{RESET} power supplies are all required for proper DMD operation. V_{SS} must also be connected.
(2) V_{OFFSET} supply transients must fall within specified max voltages.
(3) To prevent excess current, the supply voltage difference $\lvert V_{BIAS} - V_{OFFSET} \rvert$ must be less than specified limit. See *Power Supply Recommendations*, Figure 15, and Table 8.
(4) To prevent excess current, the supply voltage difference $\lvert V_{BIAS} - V_{RESET} \rvert$ must be less than specified limit. See *Power Supply Recommendations*, Figure 15, and Table 8.
(5) Low-speed interface is LPSDR and adheres to the Electrical Characteristics and AC/DC Operating Conditions table in JEDEC Standard No. 209B, "Low-Power Double Data Rate (LPDDR)" JESD209B. Tester conditions for V_{IH} and V_{IL}.
  (a) Frequency = 60 MHz, maximum rise time = 2.5 ns @ (20% - 80%)
  (b) Frequency = 60 MHz, maximum fall time = 2.5 ns @ (80% - 20%)
(6) PWRDNZ input pin resets the SCP and disables the LVDS receivers. PWRDNZ input pin overrides SCPENZ input pin and tristates the SCPDO output pin.
(7) The SCP clock is a gated clock. Duty cycle must be 50% ± 10%. SCP parameter is related to the frequency of DCLK.
(8) See Figure 2.

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Recommended Operating Conditions (continued)

Over operating free-air temperature range (unless otherwise noted). The functional performance of the device specified in this data sheet is achieved when operating the device within the limits defined by this table. No level of performance is implied when operating the device above or below these limits.

		MIN	NOM	MAX	UNIT
LVDS INTERFACE					
f_{CLOCK}	Clock frequency for LVDS interface (all channels), DCLK (9)			400	MHz
$\|V_{ID}\|$	Input differential voltage (absolute value) (10)	150	300	440	mV
V_{CM}	Common mode voltage (10)	1100	1200	1300	mV
V_{LVDS}	LVDS voltage (10)	880		1520	mV
t_{LVDS_RSTZ}	Time required for LVDS receivers to recover from PWRDNZ			2000	ns
Z_{IN}	Internal differential termination resistance	80	100	120	Ω
Z_{LINE}	Line differential impedance (PWB/trace)	90	100	110	Ω
ENVIRONMENTAL					
T_{ARRAY}	Array temperature, long–term operational (11)(12)(13)(14)	0		40 to 70 (13)	°C
	Array temperature, short–term operational, 25 hr max (12)(15)	–20		–10	°C
	Array temperature, short–term operational, 500 hr max (12)(15)	–10		0	°C
	Array temperature, short–term operational, 500 hr max (12)(15)	70		75	°C
T_{WINDOW}	Window temperature – operational (16)(17)			85	°C
$\|T_{DELTA}\|$	Absolute temperature delta between any point on the window edge and the ceramic test point TP1 (18)			14	°C
$T_{DP\ -AVG}$	Average dew point temperature (non–condensing) (19)			24	°C
T_{DP-ELR}	Elevated dew point temperature range (non-condensing) (20)	28		36	°C
CT_{ELR}	Cumulative time in elevated dew point temperature range			6	months
ILL_{UV}	Illumination wavelengths < 400 nm (11)			2.00	mW/cm^2
ILL_{VIS}	Illumination wavelengths between 400 nm and 700 nm		Thermally limited		mW/cm^2
ILL_{IR}	Illumination wavelengths > 700 nm			10	mW/cm^2
ILL_{θ}	Illumination marginal ray angle (17)			55	degrees

(9) See LVDS timing requirements in *Timing Requirements* and Figure 6.
(10) See Figure 5 LVDS waveform requirements.
(11) Simultaneous exposure of the DMD to the maximum *Recommended Operating Conditions* for temperature and UV illumination reduces device lifetime.
(12) The array temperature cannot be measured directly and must be computed analytically from the temperature measured at test point 1 (TP1) shown in Figure 10 and the package thermal resistance using the *Micromirror Array Temperature Calculation*.
(13) Per Figure 1, the maximum operational array temperature derates based on the micromirror landed duty cycle that the DMD experiences in the end application. See *Micromirror Landed-On/Landed-Off Duty Cycle* for a definition of micromirror landed duty cycle.
(14) Long-term is defined as the useful life of the device.
(15) Short-term is the total cumulative time over the useful life of the device.
(16) The locations of thermal test points TP2, TP3, TP4, and TP5 shown in Figure 10 are intended to measure the highest window edge temperature. For most applications, the locations shown are representative of the highest window edge temperature. If a particular application causes additional points on the window edge to be at a higher temperature, add test points to those locations.
(17) Ensure that the maximum marginal ray angle of the incoming illumination light at any point in the micromirror array (including pond of micromirrors (POM)), does not exceed 55 degrees from the normal to the device array plane. The device window aperture has not necessarily been designed to allow incoming light at higher maximum angles to pass to the micromirrors, and the device performance has not been tested nor qualified at angles exceeding this. Illumination light exceeding this angle outside the micromirror array (including POM) contributes to thermal limitations described in this document, and may negatively affect lifetime.
(18) Temperature delta is the highest difference between the ceramic test point 1 (TP1) and anywhere on the window edge as shown in Figure 10. The window test points TP2, TP3, TP4, and TP5 shown in Figure 10 are intended to result in the worst case delta temperature. If a particular application causes another point on the window edge to result in a larger delta in temperature, use that point.
(19) The average over time (including storage and operating) that the device is not in the 'elevated dew point temperature range'.
(20) Limit exposure to dew point temperatures in the elevated range during storage and operation to less than a total cumulative time of CT_{ELR}.

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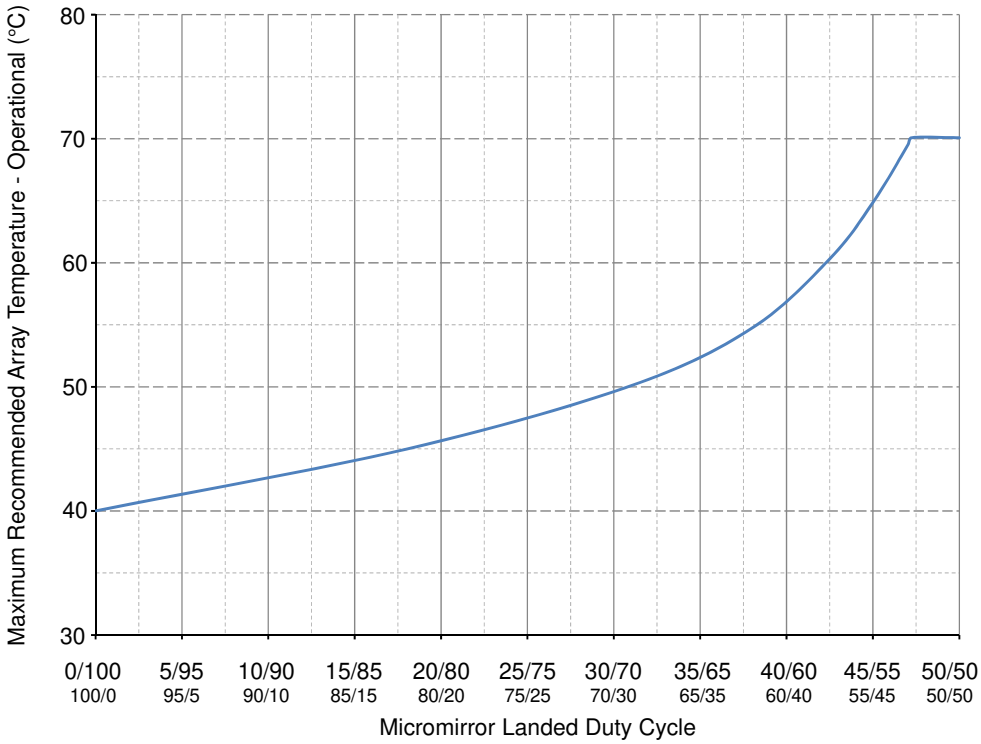


Figure 1. Maximum Recommended Array Temperature - Derating Curve

6.5 Thermal Information

THERMAL METRIC	DLP470TP FQN Package 250 PINS	UNIT
Thermal resistance, active area to test point 1 (TP1)(1)	1.2	°C/W

(1) The DMD is designed to conduct absorbed and dissipated heat to the back of the package. The cooling system must be capable of maintaining the package within the temperature range specified in the *Recommended Operating Conditions*. The total heat load on the DMD is largely driven by the incident light absorbed by the active area; although other contributions include light energy absorbed by the window aperture and electrical power dissipation of the array. design optical systems to minimize the light energy falling outside the window clear aperture because any additional thermal load in this area can significantly degrade the reliability of the device.

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6.6 Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High level output voltage	V_{CC} = 1.8 V, I_{OH} = –2 mA	0.8 × V_{CC}			V
V_{OL}	Low level output voltage	V_{CC} = 1.95 V, I_{OL} = 2 mA			0.2 × V_{CC}	V
I_{OZ}	High impedance output current	V_{CC} = 1.95 V	–40		25	µA
I_{IL}	Low level input current	V_{CC} = 1.95 V, V_I = 0	–1			µA
I_{IH}	High level input current (1)(2)	V_{CC} = 1.95 V, V_I = V_{CC}			110	µA
I_{CC}	Supply current V_{CC}	V_{CC} = 1.95 V			1290	mA
I_{OFFSET}	Supply current V_{OFFSET} (2)	V_{OFFSET} = 10.5 V			13.2	mA
I_{BIAS}	Supply current V_{BIAS} (2) (3)	V_{BIAS} = 18.5 V			3.6	mA
I_{RESET}	Supply current V_{RESET} (3)	V_{RESET} = –14.5 V			–9	mA
P_{CC}	Supply power dissipation V_{CC}	V_{CC} = 1.95 V			2515.5	mW
P_{OFFSET}	Supply power dissipation V_{OFFSET} (2)	V_{OFFSET} = 10.5 V			138.6	mW
P_{BIAS}	Supply power dissipation V_{BIAS} (2)(3)	V_{BIAS} = 18.5 V			66.6	mW
P_{RESET}	Supply power dissipation V_{RESET} (3)	V_{RESET} = –14.5 V			130.5	mW
P_{TOTAL}	Supply power dissipation V_{TOTAL}				2851.2	mW

(1) Applies to LVCMOS pins only. Excludes LVDS pins and MBRST (15:0) pins.
(2) To prevent excess current, the supply voltage difference $|V_{BIAS} – V_{OFFSET}|$ must be less than the specified limits listed in the *Recommended Operating Conditions* table.
(3) To prevent excess current, the supply voltage difference $|V_{BIAS} – V_{RESET}|$ must be less than the specified limit in *Recommended Operating Conditions*.

6.7 Capacitance at Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{I_lvds}	LVDS input capacitance 2× LVDS	f = 1 MHz			20	pF
$C_{I_nonlvds}$	Non-LVDS input capacitance 2× LVDS	f = 1 MHz			20	pF
C_{I_tdiode}	Temperature diode input capacitance 2× LVDS	f = 1 MHz			30	pF
C_O	Output capacitance	f = 1 MHz			20	pF

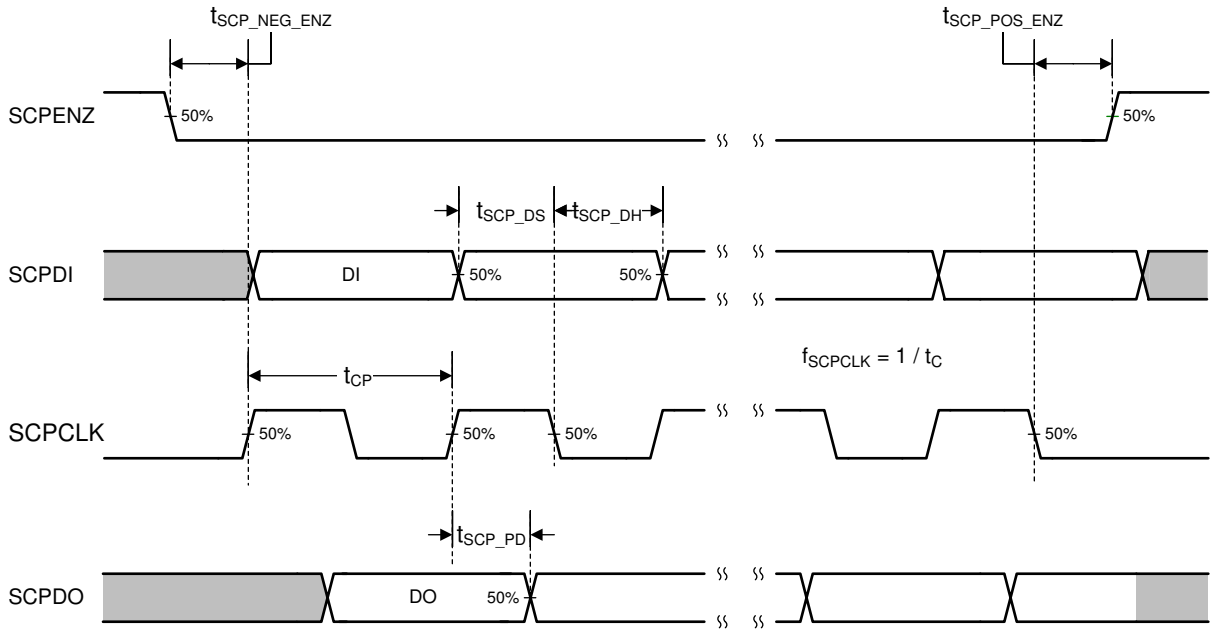
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6.8 Timing Requirements

			MIN	NOM	MAX	UNIT
SCP(1)						
t_r	Rise slew rate	20% to 80% reference points	1		3	V/ns
t_f	Fall slew rate	80% to 20% reference points	1		3	V/ns
LVDS(2)						
t_r	Rise slew rate	20% to 80% reference points	0.7	1		V/ns
t_f	Fall slew rate	80% to 20% reference points	0.7	1		V/ns
t_C	Clock cycle	DCLK_A, LVDS pair	2.5			ns
		DCLK_B, LVDS pair	2.5			ns
		DCLK_C, LVDS pair	2.5			ns
		DCLK_D, LVDS pair	2.5			ns
t_W	Pulse duration	DCLK_A LVDS pair	1.19	1.25		ns
		DCLK_B LVDS pair	1.19	1.25		ns
		DCLK_C LVDS pair	1.19	1.25		ns
		DCLK_D LVDS pair	1.19	1.25		ns
t_{Su}	Setup time	D_A(15:0) before DCLK_A, LVDS pair	0.275			ns
		D_B(15:0) before DCLK_B, LVDS pair	0.275			ns
		D_C(15:0) before DCLK_C, LVDS pair	0.275			ns
		D_D(15:0) before DCLK_D, LVDS pair	0.275			ns
		SCTRL_A before DCLK_A, LVDS pair	0.275			ns
		SCTRL_B before DCLK_B, LVDS pair	0.275			ns
		SCTRL_C before DCLK_C, LVDS pair	0.275			ns
		SCTRL_D before DCLK_D, LVDS pair	0.275			ns
t_h	Hold time	D_A(15:0) after DCLK_A, LVDS pair	0.195			ns
		D_B(15:0) after DCLK_B, LVDS pair	0.195			ns
		D_C(15:0) after DCLK_C, LVDS pair	0.195			ns
		D_D(15:0) after DCLK_D, LVDS pair	0.195			ns
		SCTRL_A after DCLK_A, LVDS pair	0.195			ns
		SCTRL_B after DCLK_B, LVDS pair	0.195			ns
		SCTRL_C after DCLK_C, LVDS pair	0.195			ns
		SCTRL_D after DCLK_D, LVDS pair	0.195			ns
LVDS(2)						
t_{SKEW}	Skew time	Channel B relative to channel A(3)(4), LVDS pair	–1.25		1.25	ns
t_{SKEW}	Skew time	Channel D relative to channel C(5)(6), LVDS pair	–1.25		1.25	ns

(1) See Figure 3 for rise time and fall time for SCP.
(2) See Figure 5 for timing requirements for LVDS.
(3) Channel A (Bus A) includes the following LVDS pairs: DCLK_AN and DCLK_AP, SCTRL_AN and SCTRL_AP, D_AN(15:0), and D_AP(15:0).
(4) Channel B (Bus B) includes the following LVDS pairs: DCLK_BN and DCLK_BP, SCTRL_BN and SCTRL_BP, D_BN(15:0), and D_BP(15:0).
(5) Channel C (Bus C) includes the following LVDS pairs: DCLK_CN and DCLK_CP, SCTRL_CN and SCTRL_CP, D_CN(15:0), and D_CP(15:0).
(6) Channel D (Bus D) includes the following LVDS pairs: DCLK_DN and DCLK_DP, SCTRL_DN and SCTRL_DP, D_DN(15:0), and D_DP(15:0).

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SCPCLK falling–edge captures SCPDI

SCPCLK rising–edge launches SCPDO

See *Recommended Operating Conditions* for f_{SCPCLK}, t_{SCP_DS}, t_{SCP_DH}, and t_{SCP_PD} specifications.

Figure 2. SCP Timing Requirements

See *Timing Requirements* for t_r and t_f specifications and conditions shown in Figure 3.) For output timing analysis, make sure to consider the effect that tester pin electronics and its transmission line can cause. Use IBIS or other simulation tools to correlate the timing reference load to a system environment. (See Figure 4.)

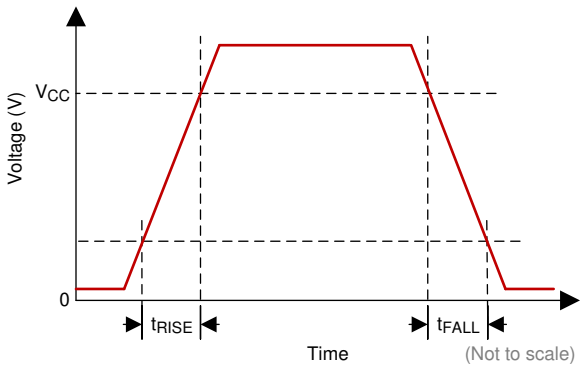


Figure 3. SCP Requirements for Rise and Fall

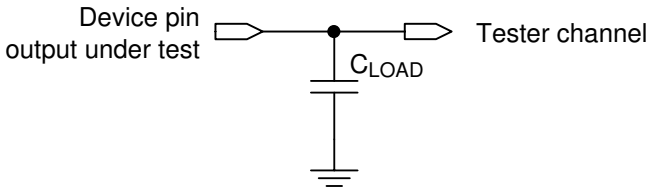
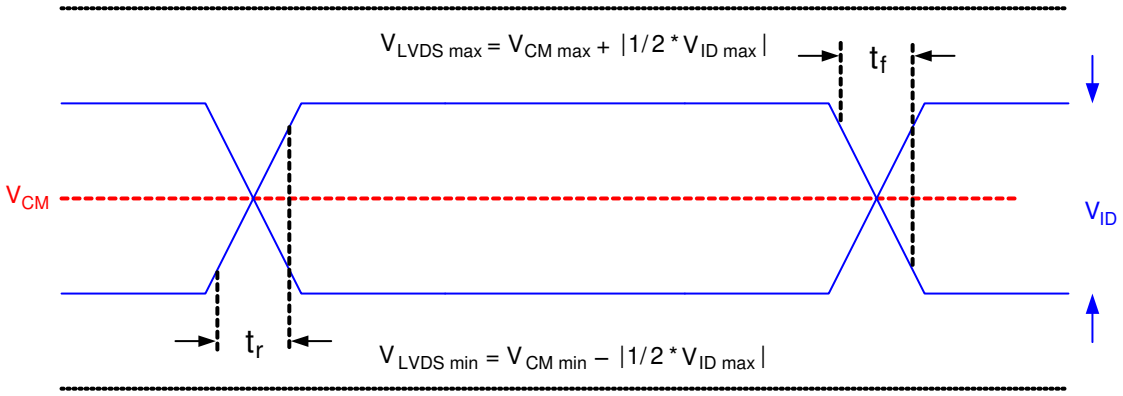


Figure 4. Test Load Circuit for Output Propagation Measurement

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Not to Scale



See *Recommended Operating Conditions* for V_{CM}, V_{ID}, and V_{LVDS} specifications and conditions.

Figure 5. LVDS Waveform Requirements

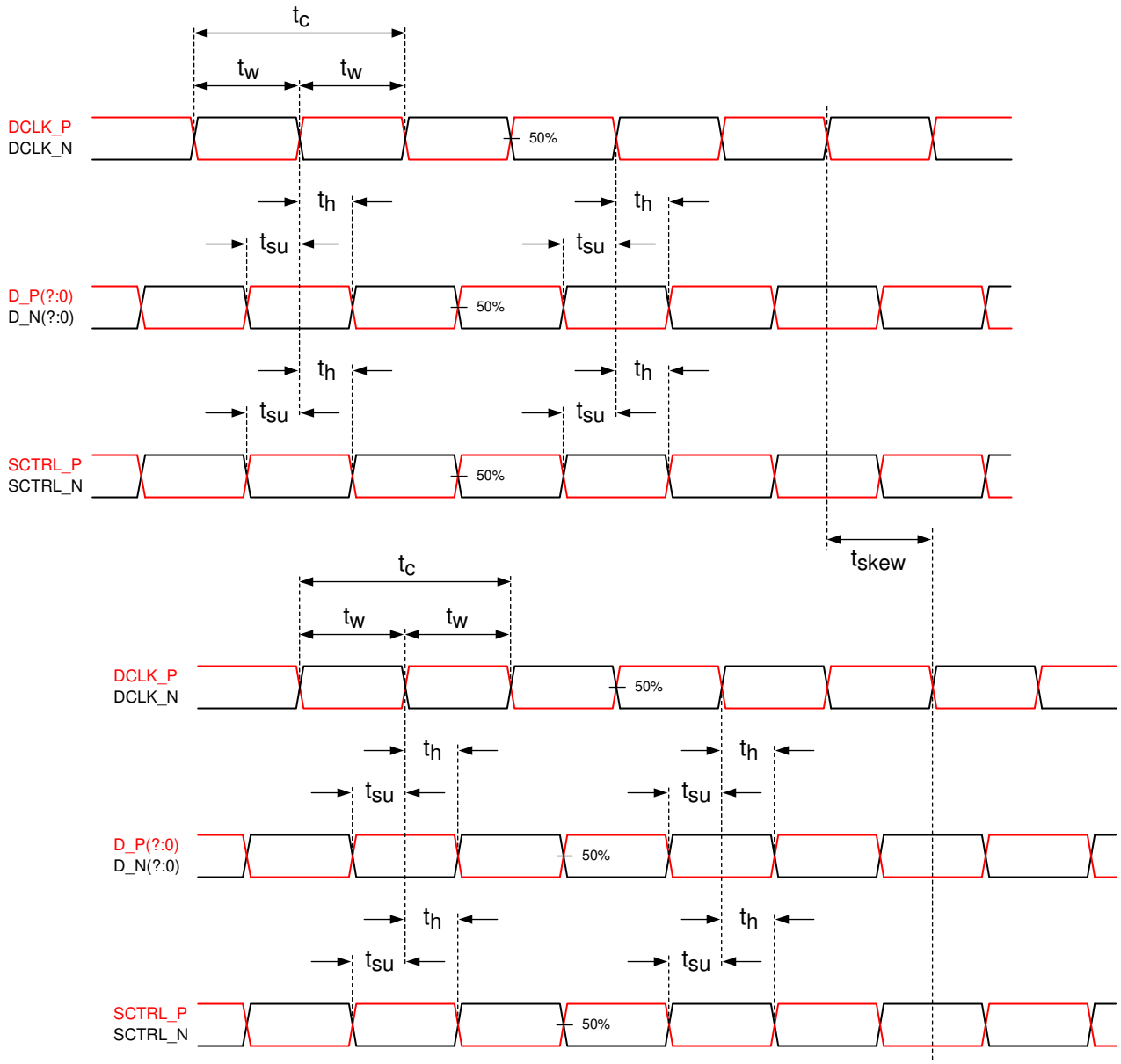


Figure 6. Timing Requirements

See *Timing Requirements* for timing requirements and LVDS pairs per channel (bus) defining D_P(?:0) and D_N(?:0).

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6.9 System Mounting Interface Loads

Table 1. System Mounting Interface Loads

PARAMETER	MIN	NOM	MAX	UNIT
Thermal interface area(1)			100	N
Electrical interface area(1)			245	N

(1) Uniformly distributed within area shown in Figure 7.

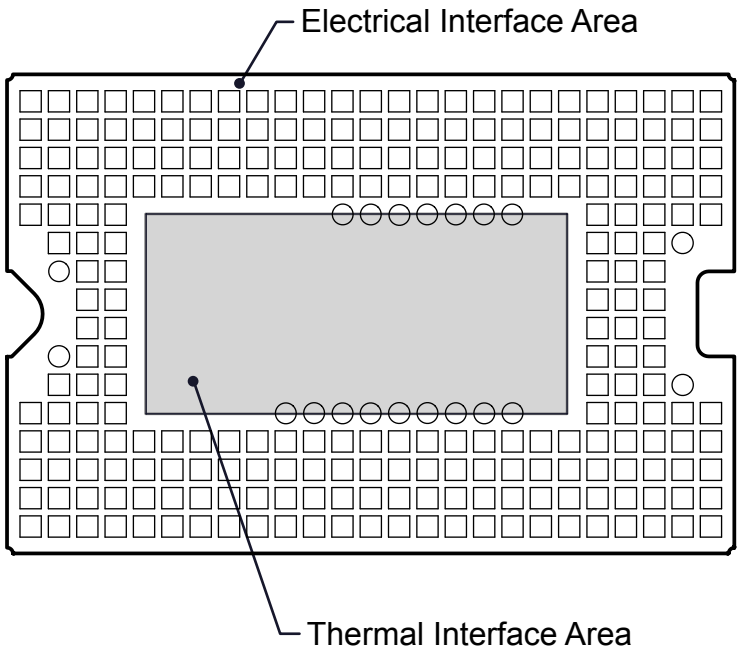


Figure 7. System Mounting Interface Loads

6.10 Micromirror Array Physical Characteristics

Table 2. Micromirror Array Physical Characteristics

PARAMETER DESCRIPTION		VALUE	UNIT
Number of active columns (1)(2)	M	1920	micromirrors
Number of active rows (1)(2)	N	1080	micromirrors
Micromirror (pixel) pitch (1)	P	5.4	µm
Micromirror active array width (1)	Micromirror pitch × number of active columns	10.368	mm
Micromirror active array height (1)	Micromirror pitch × number of active rows	5.832	mm
Micromirror active border (3)	Pond of micromirrors (POM)	20	micromirrors/side

(1) See Figure 8.
(2) The fast switching speed of the DMD micromirrors combined with advanced DLP image processing algorithms enables each micromirror to display four distinct pixels on the screen during every frame, resulting in a full 3840 × 2160 pixel image being displayed.
(3) The structure and qualities of the border around the active array includes a band of partially functional micromirrors referred to as the *Pond Of Micromirrors* (POM). These micromirrors are structurally and/or electrically prevented from tilting toward the bright or ON state but still require an electrical bias to tilt toward the OFF state.

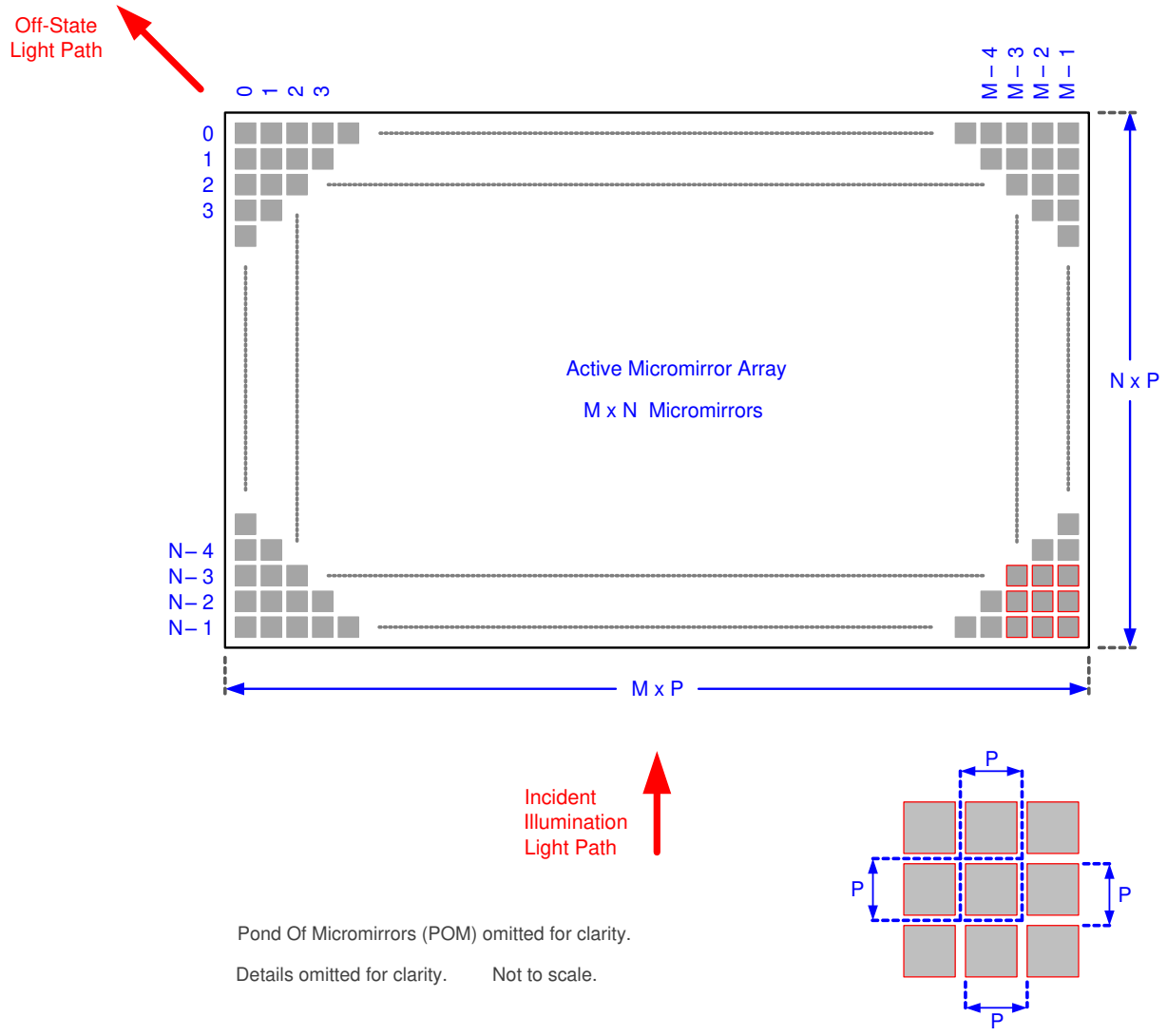


Figure 8. Micromirror Array Physical Characteristics

Refer to section *Micromirror Array Physical Characteristics* table for M, N, and P specifications.

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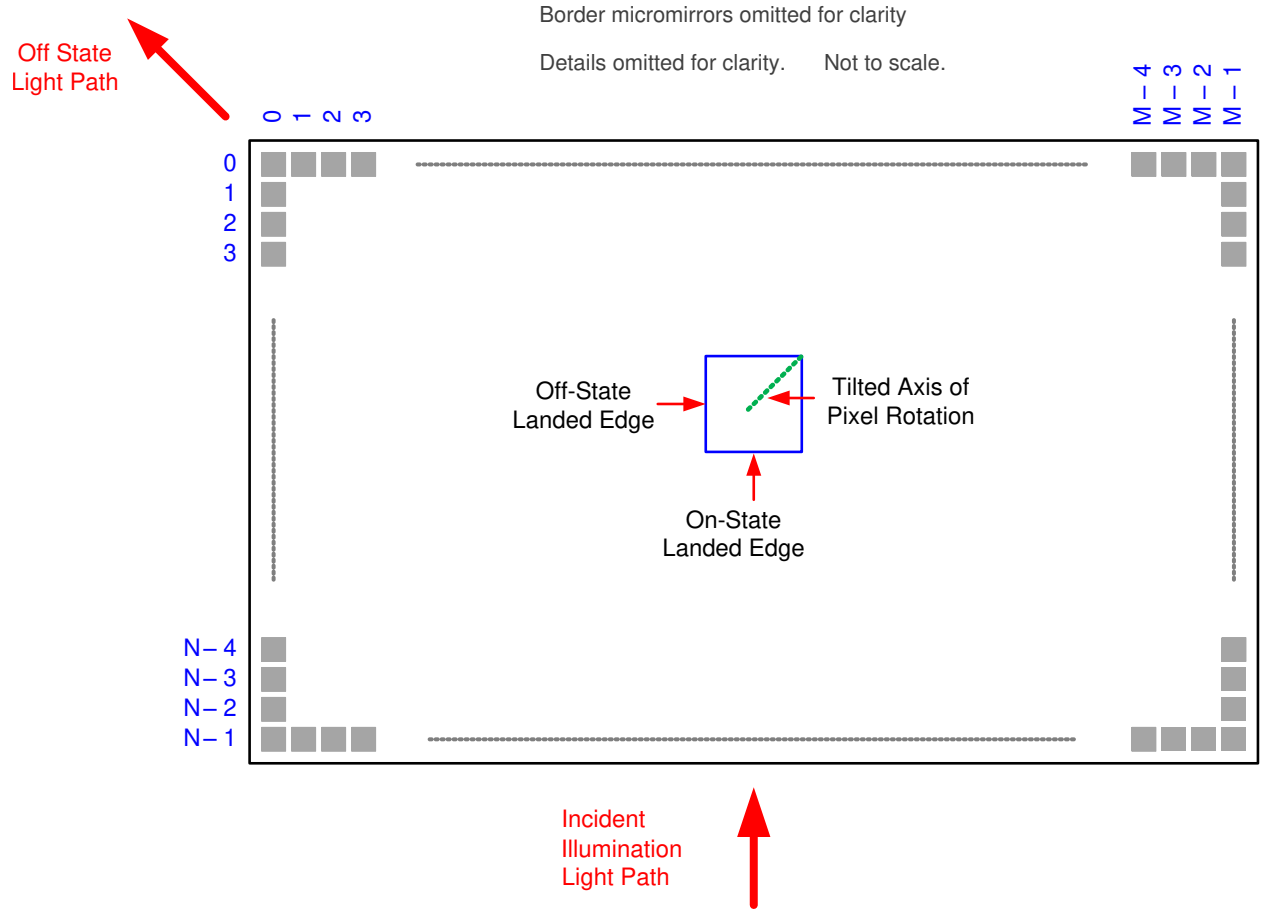
6.11 Micromirror Array Optical Characteristics

Table 3. Micromirror Array Optical Characteristics

PARAMETER		MIN	NOM	MAX	UNIT
Micromirror tilt angle	DMD landed state(1)		17		degrees
Micromirror tilt angle tolerance(2)(3)(4)(5)		–1.4		1.4	degrees
Micromirror tilt direction(6)(7)	Landed ON state		270		degrees
	Landed OFF state		180		
Micromirror crossover time(8)	Typical performance		1	3	µs
Micromirror switching time(9)	Typical performance	6			
Number of out-of-specification micromirrors(10)	Adjacent micromirrors			0	micromirrors
	Non-adjacent micromirrors			10	

(1) Measured relative to the plane formed by the overall micromirror array.
(2) Additional variation exists between the micromirror array and the package datums.
(3) Represents the landed tilt angle variation relative to the nominal landed tilt angle.
(4) Represents the variation that can occur between any two individual micromirrors, located on the same device or located on different devices.
(5) For some applications, it is critical to account for the micromirror tilt angle variation in the overall system optical design. With some system optical designs, the micromirror tilt angle variation within a device may result in perceivable non-uniformities in the light field reflected from the micromirror array. With some system optical designs, the micromirror tilt angle variation between devices may result in colorimetry variations, system efficiency variations or system contrast variations.
(6) When the micromirror array is landed (not parked), the tilt direction of each individual micromirror is dictated by the binary contents of the CMOS memory cell associated with each individual micromirror. A binary value of 1 results in a micromirror landing in the ON state direction. A binary value of 0 results in a micromirror landing in the OFF state direction.
(7) Micromirror tilt direction is measured as in a typical polar coordinate system: Measuring counter-clockwise from a 0° reference which is aligned with the +X Cartesian axis.
(8) The time required for a micromirror to nominally transition from one landed state to the opposite landed state.
(9) The minimum time between successive transitions of a micromirror.
(10) An out-of-specification micromirror is defined as a micromirror that is unable to transition between the two landed states within the specified micromirror switching time.

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(1) Pond of micromirrors (POM) omitted for clarity.

(2) Refer to *Micromirror Array Physical Characteristics* table for M, N, and P specifications.

Figure 9. Micromirror Landed Orientation and Tilt

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6.12 Window Characteristics

Table 4. DMD Window Characteristics

DESCRIPTION(1)		MIN	NOM	MAX
Window material			Corning Eagle XG	
Window refractive index	At wavelength 546.1 nm		1.5119	
Window aperture(2)				See (2)
Illumination overfill(3)				See (3)
Window transmittance, single-pass through both surfaces and glass	Minimum within the wavelength range 420 nm to 680 nm. Applies to all angles 0° to 30° AOI. (4)	97%		
Window transmittance, single-pass through both surfaces and glass	Average over the wavelength range 420 nm to 680 nm. Applies to all angles 30° to 45° AOI. (4)	97%		

(1) See *Optical Interface and System Image Quality Considerations* for more information.
(2) See the package mechanical characteristics for details regarding the size and location of the window aperture.
(3) The active area of the DLP470TP device is surrounded by an aperture on the inside of the DMD window surface that masks structures of the DMD device assembly from normal view. The aperture is sized to anticipate several optical conditions. Overfill light illuminating the area outside the active array can scatter and create adverse effects to the performance of an end application using the DMD. Design illumination optical systems to limit light flux incident outside the active array to less than 10% of the average flux level in the active area. Depending on the particular optical architecture and assembly tolerances, the amount of overfill light on the outside of the active array may cause system performance degradation.
(4) Angle of incidence (AOI) is the angle between an incident ray and the normal to a reflecting or refracting surface.

6.13 Chipset Component Usage Specification

Reliable function and operation of the DLP470TP DMD requires that it be used in conjunction with the other components of the applicable DLP chipset, including those components that contain or implement TI DMD control technology. TI DMD control technology is the TI technology and devices for operating or controlling a DLP DMD.

NOTE

TI assumes no responsibility for image quality artifacts or DMD failures caused by optical system operating conditions exceeding limits described previously.

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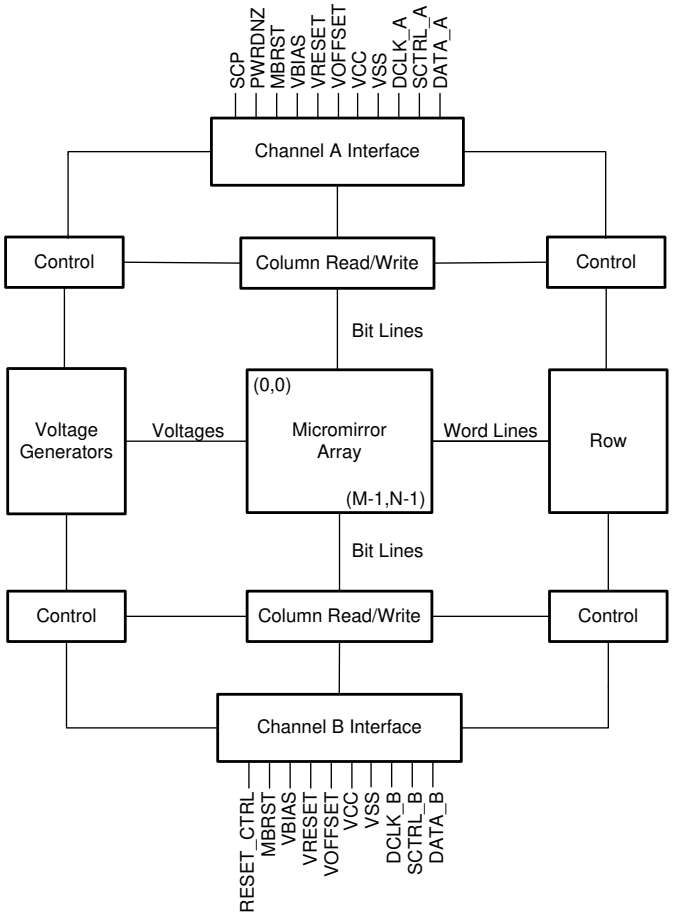
7 Detailed Description

7.1 Overview

The DMD is a 0.47-inch diagonal spatial light modulator which consists of an array of highly reflective aluminum micromirrors. The DMD is an electrical input, optical output micro-optical-electrical-mechanical system (MOEMS). The fast switching speed of the DMD micromirrors combined with advanced DLP image processing algorithms enables each micromirror to display four distinct pixels on the screen during every frame, resulting in a full 3840 × 2160 pixel image being displayed. The electrical interface is low-voltage differential signaling (LVDS). The DMD consists of a two-dimensional array of 1-bit CMOS memory cells. The array is organized in a grid of M memory cell columns by N memory cell rows. Refer to the *Functional Block Diagram*. The positive or negative deflection angle of the micromirrors can be individually controlled by changing the address voltage of underlying CMOS addressing circuitry and micromirror reset signals.

The DLP 0.47" 4K UHD chipset is comprised of the DLP470TP DMD, two DLPC6421 display controllers, and DLPA3005 PMIC and LED driver. To ensure reliable operation, the DLP470TP DMD must always be used with the DLP display controller and the PMIC specified in the chipset.

7.2 Functional Block Diagram



Channels C and D are not shown. For pin details on channels A, B, C, and D, refer to *Pin Configuration and Functions* section and LVDS interface section of *Timing Requirements*.

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7.3 Feature Description

7.3.1 Power Interface

The DMD requires 4 DC voltages: 1.8 V, V_{OFFSET}, V_{RESET}, and V_{BIAS}. In a typical LED-based system, 1.8 V is provided by a TPS54320 and the V_{OFFSET}, V_{RESET}, and V_{BIAS} are managed by the DLPA3005 PMIC and LED driver.

7.3.2 Timing

The data sheet provides timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be taken into account. Figure 4 shows an equivalent test load circuit for the output under test. Timing reference loads are not intended to be precise representations of any particular system environment or depiction of the actual load presented by a production test. Use IBIS or some other simulation tools to correlate the timing reference load to a system environment. The load capacitance value stated is only for characterization and measurement of AC timing signals. This load capacitance value does not indicate the maximum load the device is capable of driving.

7.4 Device Functional Modes

DMD functional modes are controlled by the DLPC6421 display controller. See the DLPC6421 display controller data sheet or contact a TI applications engineer.

7.5 Optical Interface and System Image Quality Considerations

TI assumes no responsibility for end-equipment optical performance. Achieving the desired end-equipment optical performance involves making trade-offs between numerous component and system design parameters. Optimizing system optical performance and image quality strongly relate to optical system design parameter trades. Although it is not possible to anticipate every conceivable application, projector image quality and optical performance is contingent on compliance to the optical system operating conditions described in the following sections.

7.5.1 Numerical Aperture and Stray Light Control

TI recommends that the light cone angle defined by the numerical aperture of the illumination optics is the same as the light cone angle defined by the numerical aperture of the projection optics. This angle must not exceed the nominal device micromirror tilt angle unless appropriate apertures are added in the illumination and/or projection pupils to block out flat-state and stray light from the projection lens. The micromirror tilt angle defines DMD capability to separate the "ON" optical path from any other light path, including undesirable flat-state specular reflections from the DMD window, DMD border structures, or other system surfaces near the DMD such as prism or lens surfaces. If the numerical aperture exceeds the micromirror tilt angle, or if the projection numerical aperture angle is more than two degrees larger than the illumination numerical aperture angle (and vice versa), contrast degradation and objectionable artifacts in the display border and/or active area could occur.

7.5.2 Pupil Match

TI's optical and image quality specifications assume that the exit pupil of the illumination optics is nominally centered within 2° of the entrance pupil of the projection optics. Misalignment of pupils can create objectionable artifacts in the display border and/or active area, which may require additional system apertures to control, especially if the numerical aperture of the system exceeds the pixel tilt angle.

7.5.3 Illumination Overfill

The active area of the device is surrounded by an aperture on the inside DMD window surface that masks structures of the DMD chip assembly from normal view, and is sized to anticipate several optical operating conditions. Overfill light illuminating the window aperture can create artifacts from the edge of the window aperture opening and other surface anomalies that may be visible on the screen. Design the illumination optical system to limit light flux incident anywhere on the window aperture from exceeding approximately 10% of the average flux level in the active area. Depending on the particular system optical architecture, overfill light may have to be further reduced below the suggested 10% level in order to be acceptable.

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7.6 Micromirror Array Temperature Calculation

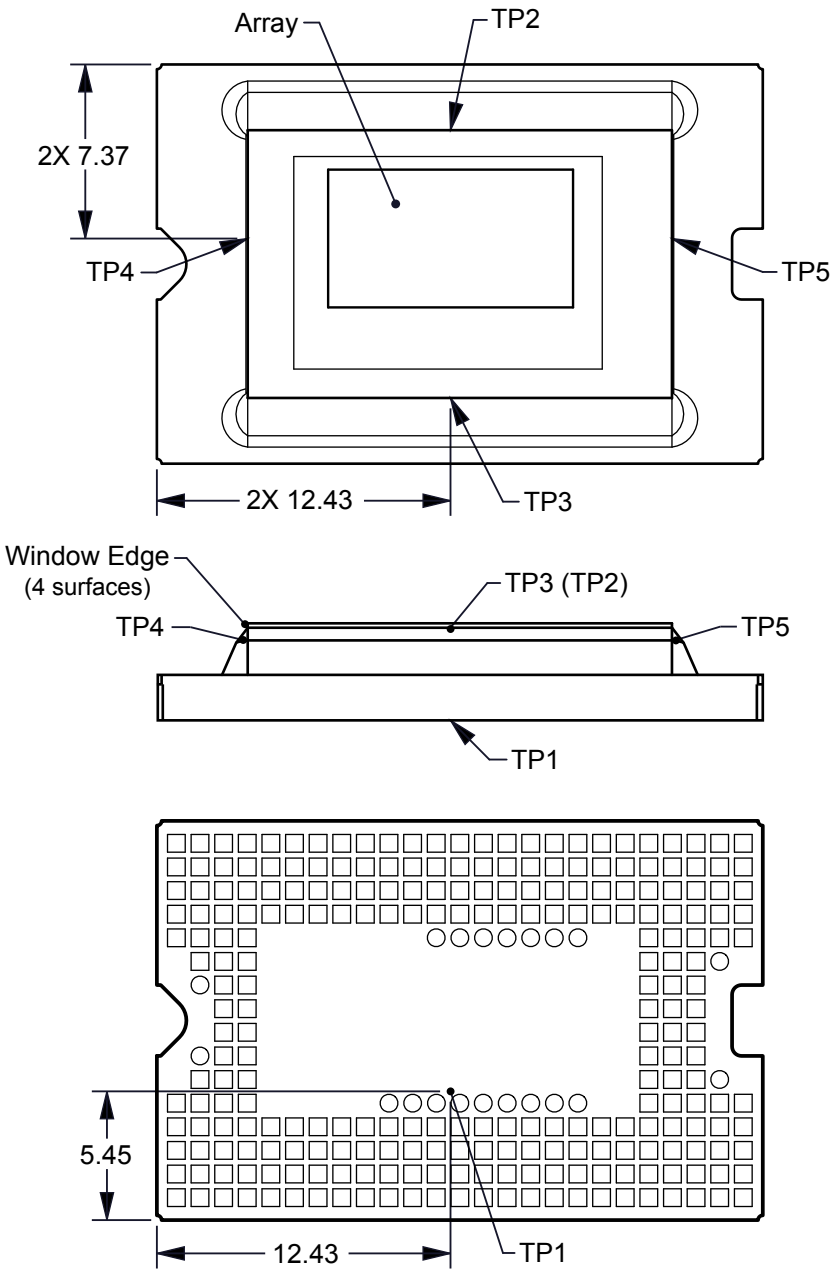


Figure 10. DMD Thermal Test Points

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Micromirror Array Temperature Calculation (continued)

Micromirror array temperature cannot be measured directly, therefore it must be computed analytically from measurement points on the outside of the package, the package thermal resistance, the electrical power, and the illumination heat load. The relationship between array temperature and the reference ceramic temperature (thermal test TP1 in Figure 10) is provided by the following equations:

$$T_{ARRAY} = T_{CERAMIC} + (Q_{ARRAY} \times R_{ARRAY\text{-}TO\text{-}CERAMIC})$$

$$Q_{ARRAY} = Q_{ELECTRICAL} + Q_{ILLUMINATION}$$

where

- T_{ARRAY} = Computed array temperature (°C)
- $T_{CERAMIC}$ = Measured ceramic temperature (°C) (TP1 location)
- $R_{ARRAY\text{-}TO\text{-}CERAMIC}$ = Thermal resistance of package specified in *Thermal Information* from array to ceramic TP1 (°C/Watt)
- Q_{ARRAY} = Total (electrical + absorbed) DMD power on the array (Watts)
- $Q_{ELECTRICAL}$ = Nominal electrical power
- $Q_{ILLUMINATION} = (C_{L2W} \times SL)$
- C_{L2W} = Conversion constant for screen lumens to power on DMD (Watts/Lumen)
- SL = Measured screen Lumens

The electrical power dissipation of the DMD is variable and depends on the voltages, data rates, and operating frequencies. A nominal electrical power dissipation to use when calculating array temperature is 1.3 W. The absorbed power from the illumination source is variable and depends on the operating state of the micromirrors and the intensity of the light source. The equations shown above are valid for a 1-chip DMD system with projection efficiency from the DMD to the screen of 87%.

The conversion constant C_{L2W} is calculated to be 0.00266 W/lm based on array characteristics. It assumes a spectral efficiency of 300 lumens/Watt for the projected light and illumination distribution of 83.7% on the active array, and 16.3% on the array border.

A sample calculation for a typical projection application is as follows:

SL = 1500 lm (measured)

$T_{CERAMIC}$ = 55.0°C (measured)

C_{L2W} = 0.00266 W/lm

$Q_{ELECTRICAL}$ = 1.3 W

Q_{ARRAY} = 1.3 W + (0.00266 W/lm × 1500 lm) = 5.29 W

T_{ARRAY} = 55.0°C + (5.29 W × 1.2°C/W) = 61.35°C

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7.7 Micromirror Landed-On/Landed-Off Duty Cycle

7.7.1 Definition of Micromirror Landed-On/Landed-Off Duty Cycle

The micromirror landed-on/landed-off duty cycle (landed duty cycle) denotes the amount of time (as a percentage) that an individual micromirror is landed in the ON state versus the amount of time the same micromirror is landed in the OFF state.

For example, a landed duty cycle of 75/25 indicates that the referenced pixel is in the ON state 75% of the time (and in the OFF state 25% of the time); whereas 25/75 would indicate that the pixel is in the ON state 25% of the time. Likewise, 50/50 indicates that the pixel is ON for 50% of the time (and OFF for 50% of the time).

Note that when assessing landed duty cycle, the time spent switching from one state (ON or OFF) to the other state (OFF or ON) is considered negligible and is thus ignored.

Since a micromirror can only be landed in one state or the other (ON or OFF), the two numbers (percentages) nominally add to 100.

7.7.2 Landed Duty Cycle and Useful Life of the DMD

Knowing the long-term average landed duty cycle (of the end product or application) is important because subjecting all (or a portion) of the DMD micromirror array (also called the active array) to an asymmetric landed duty cycle for a prolonged period of time can reduce the DMD useful life.

Note that it is the symmetry/asymmetry of the landed duty cycle that is of relevance. The symmetry of the landed duty cycle is determined by how close the two numbers (percentages) are to being equal. For example, a landed duty cycle of 50/50 is perfectly symmetrical whereas a landed duty cycle of 100/0 or 0/100 is perfectly asymmetrical.

7.7.3 Landed Duty Cycle and Operational DMD Temperature

Operational DMD temperature and landed duty cycle interact to affect DMD useful life, and this interaction can be exploited to reduce the impact that an asymmetrical landed duty cycle has on the DMD useful life. This is quantified in the de-rating curve shown in Figure 1. The importance of this curve is that:

- All points along this curve represent the same useful life.
- All points above this curve represent lower useful life (and the further away from the curve, the lower the useful life).
- All points below this curve represent higher useful life (and the further away from the curve, the higher the useful life).

In practice, this curve specifies the maximum operating DMD temperature for a given long-term average landed duty cycle.

7.7.4 Estimating the Long-Term Average Landed Duty Cycle of a Product or Application

During a given period of time, the nominal landed duty cycle of a given pixel follows from the image content being displayed by that pixel.

For example, in the simplest case, when displaying pure-white on a given pixel for a given time period, that pixel experiences a landed duty cycle very close to 100/0 during that time period. Likewise, when displaying pureblack, the pixel experiences a landed duty cycle very close to 0/100.

Between the two extremes (ignoring for the moment color and any image processing that may be applied to an incoming image), the landed duty cycle tracks one-to-one with the gray scale value, as shown in Table 5.

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Table 5. Grayscale Value and Landed Duty Cycle

GRAYSCALE VALUE	NOMINAL LANDED DUTY CYCLE
0%	0/100
10%	10/90
20%	20/80
30%	30/70
40%	40/60
50%	50/50
60%	60/40
70%	70/30
80%	80/20
90%	90/10
100%	100/0

Accounting for color rendition (but still ignoring image processing) requires knowing both the color intensity (from 0% to 100%) for each constituent primary color (red, green, and/or blue) for the given pixel as well as the color cycle time for each primary color, where “color cycle time” is the total percentage of the frame time that a given primary must be displayed in order to achieve the desired white point.

Use Equation 1 to calculate the landed duty cycle of a given pixel during a given time period

Landed Duty Cycle = (Red_Cycle_% × Red_Scale_Value) + (Green_Cycle_% × Green_Scale_Value) + (Blue_Cycle_% × Blue_Scale_Value) (1)

where

- Red_Cycle_%, represents the percentage of the frame time that red is displayed to achieve the desired white point
- Green_Cycle_% represents the percentage of the frame time that green is displayed to achieve the desired white point
- Blue_Cycle_%, represents the percentage of the frame time that blue is displayed to achieve the desired white point

For example, assume that the red, green, and blue color cycle times are 50%, 20%, and 30% respectively (in order to achieve the desired white point), then the nominal landed duty cycle for various combinations of red, green, blue color intensities would be as shown in Table 6 and Table 7.

Table 6. Example Landed Duty Cycle for Full-Color, Color Percentage

CYCLE PERCENTAGE		
RED	GREEN	BLUE
50%	20%	30%

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Table 7. Example Landed Duty Cycle for Full-Color

SCALE VALUE			NOMINAL LANDED DUTY CYCLE
RED	GREEN	BLUE	
0%	0%	0%	0/100
100%	0%	0%	50/50
0%	100%	0%	20/80
0%	0%	100%	30/70
12%	0%	0%	6/94
0%	35%	0%	7/93
0%	0%	60%	18/82
100%	100%	0%	70/30
0%	100%	100%	50/50
100%	0%	100%	80/20
12%	35%	0%	13/87
0%	35%	60%	25/75
12%	0%	60%	24/76
100%	100%	100%	100/0

The last factor to account for in estimating the landed duty cycle is any applied image processing. Within the DLPC6421 controllers, the gamma function affects the landed duty cycle.

Gamma is a power function of the form Output_Level = A × Input_Level^{Gamma}, where A is a scaling factor that is typically set to 1.

In the DLPC6421 controllers, gamma is applied to the incoming image data on a pixel-by-pixel basis. A typical gamma factor is 2.2, which transforms the incoming data as shown in Figure 11.

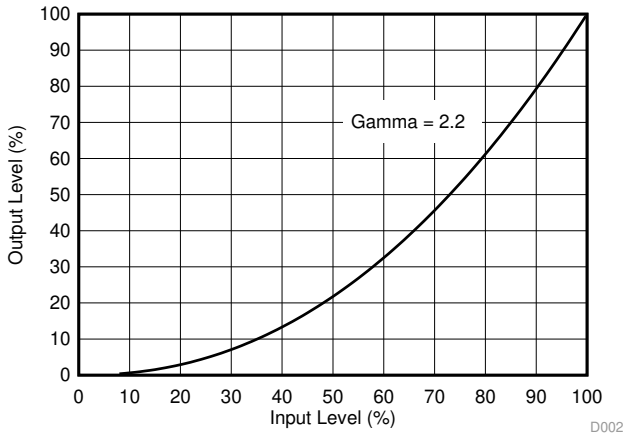


Figure 11. Example of Gamma = 2.2

From Figure 11, if the gray scale value of a given input pixel is 40% (before gamma is applied), then gray scale value is 13% after gamma is applied. Therefore,because gamma has a direct impact displayed gray scale level of a pixel, it also has a direct impact on the landed duty cycle of a pixel.

Consideration must also be given to any image processing which occurs before the DLPC3439 controllers.

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8 Application and Implementation

NOTE

Information in the following application sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

DMDs are spatial light modulators which reflect incoming light from an illumination source to one of two directions, with the primary direction being into a projection or collection optic. Each application is derived primarily from the optical architecture of the system and the format of the data coming into the dual DLPC6421 controllers. The high tilt pixel in the bottom-illuminated DMD increases brightness performance and enables a smaller system footprint for thickness constrained applications. Typical applications using the DLP470TP include mobile smart TV and digital signage.

The DLPA3005 strictly controls DMD power-up and power-down sequencing. Refer to the Power Supply Recommendations section for power-up and power-down specifications. To ensure reliable operation, the DLP470TP DMD must always be used with two DLPC6421 controllers and a DLPA3005 PMIC/LED driver.

8.2 Typical Application

The DLP470TP DMD combined with two DLPC6421 digital controllers and a power management device provides full 4K UHD resolution for bright, colorful display applications. See Figure 12, a block diagram showing the system components needed along with the LED configuration of the DLP 0.47" 4K UHD chipset. The components include the DLP470TP DMD, two DLPC6421 display controllers and the DLPA3005 PMIC and LED driver.

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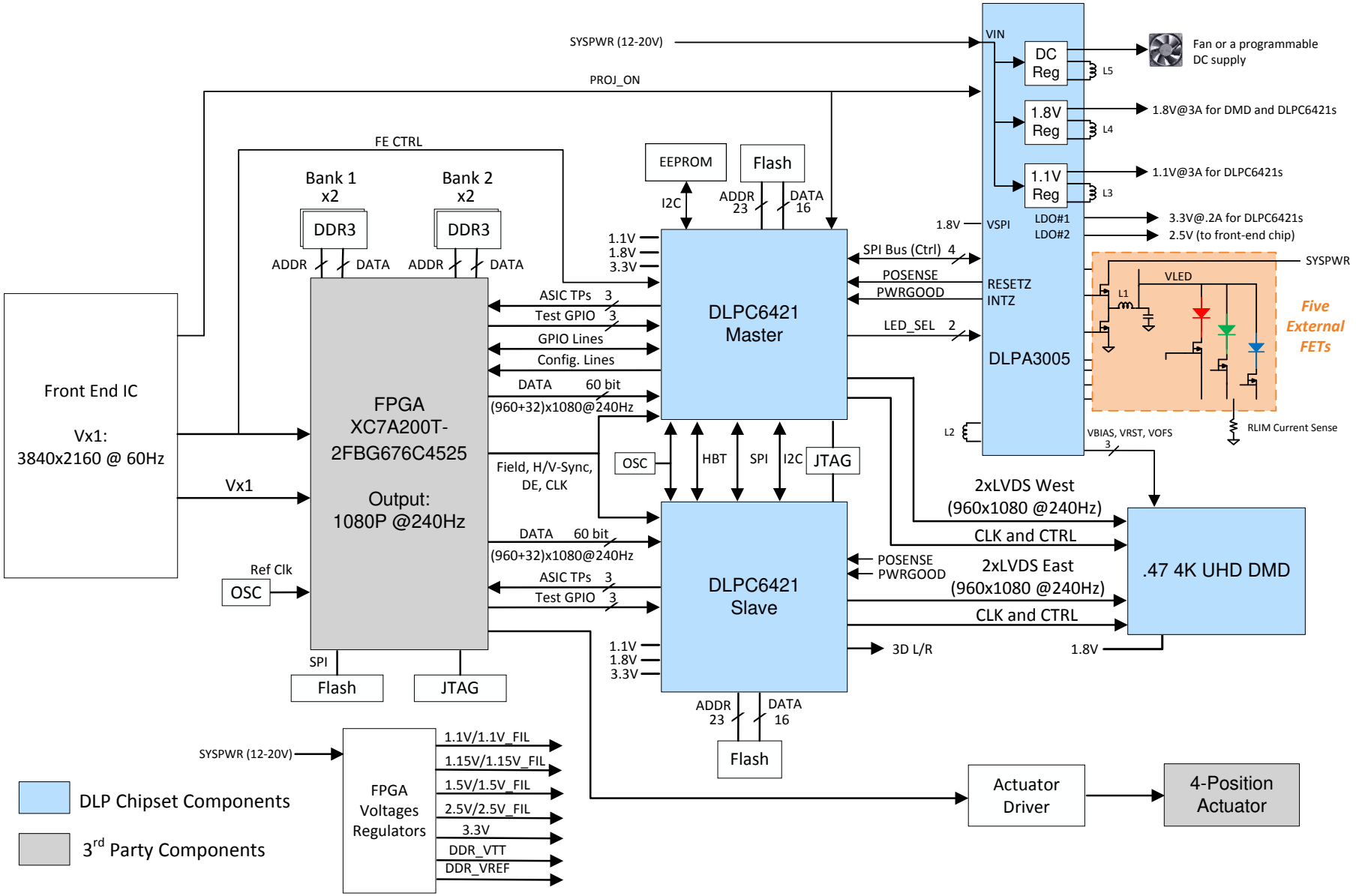


Figure 12. Typical 4K UHD LED Application Diagram

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8.2.1 Design Requirements

Other core components of the display system include an illumination source, an optical engine for the illumination and projection optics, other electrical and mechanical components, and software. The type of illumination used and desired brightness has a major effect on the overall system design and size.

The DLP470TP DMD is used as the core imaging device in the display system and contains a 0.47-inch array of micromirrors. The DLPC6421 controller is the digital interface between the DMD and the rest of the system, taking digital input from front end receiver and driving the DMD over a high speed interface. The DLPA3005 PMIC serves as a voltage regulator for the DMD, controller, and LED illumination functionality.

8.2.2 Detailed Design Procedure

For a complete DLP system, an optical module or light engine is required that contains the DLP470TP DMD, associated illumination sources, optical elements, and necessary mechanical components.

To ensure reliable operation, the DMD must always be used with two DLPC6421 display controllers and the DLPA3005 PMIC and LED driver. Refer to PCB Design Requirements for TI DLP Pico TRP Digital Micromirror Devices for the DMD board design and manufacturing handling of the DMD sub assemblies.

8.2.3 Application Curves

When LED illumination is utilized, typical LED-current-to-Luminance relationship is shown in Figure 13.

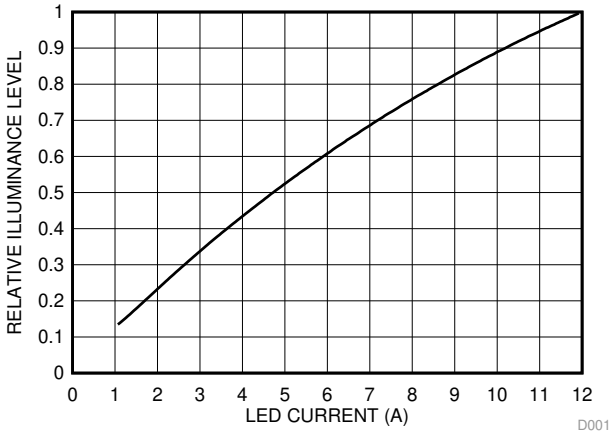


Figure 13. Luminance vs. Current

8.3 Temperature Sensor Diode

The software application contains functions to configure the TMP411 to read the DLP470TP DMD temperature sensor diode. This data can be leveraged by the customer to incorporate additional functionality in the overall system design such as adjusting illumination, fan speeds, etc. All communication between the TMP411 and the DLPC6421 controller operates over the I^2C interface. The TMP411 connects to the DMD via pins A16 and B14 as outlined in Figure 14 .

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Temperature Sensor Diode (continued)

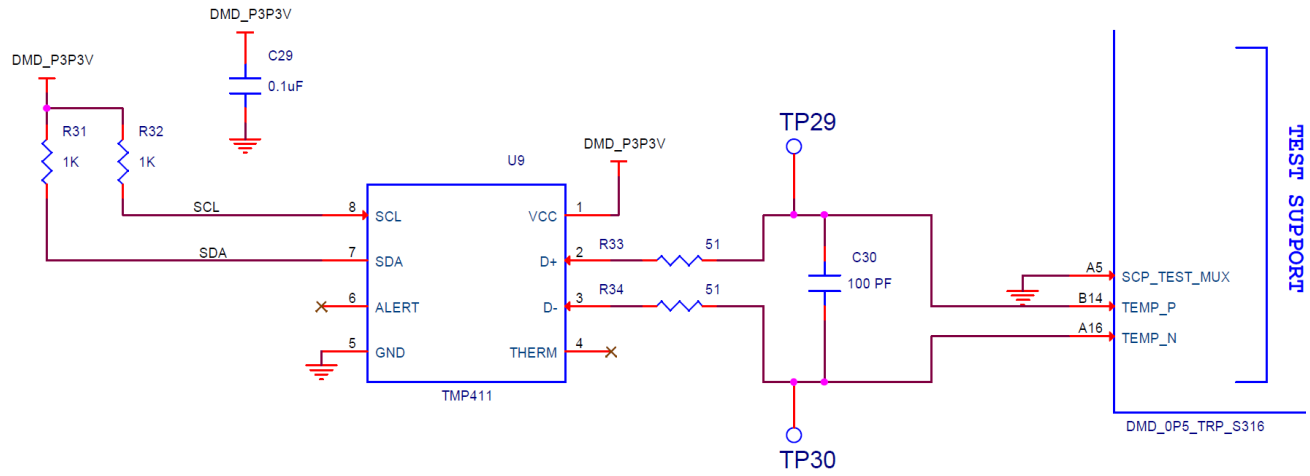


Figure 14. TMP411 Connection Schematic Example

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9 Power Supply Recommendations

The following power supplies are all required to operate the DMD:

- V_{SS}
- V_{BIAS}
- V_{CC}
- V_{OFFSET}
- V_{RESET}

DMD power-up and power-down sequencing is strictly controlled by the DLP display controller.

CAUTION

For reliable operation of the DMD, the following power supply sequencing requirements must be followed. Failure to adhere to any of the prescribed power-up and power-down requirements may affect device reliability. See the DMD power supply sequencing requirements in Figure 15.

V_{BIAS}, V_{CC}, V_{OFFSET}, and V_{RESET} power supplies must be coordinated during power-up and power-down operations. Failure to meet any of the below requirements results in a significant reduction in the DMD reliability and lifetime. Common ground V_{SS} must also be connected.

9.1 DMD Power Supply Power-Up Procedure

- During power-up, V_{CC} must always start and settle before V_{OFFSET} plus Delay1 specified in Table 8, V_{BIAS}, and V_{RESET} voltages are applied to the DMD.
- During power-up, it is a strict requirement that the voltage difference between V_{BIAS} and V_{OFFSET} must be within the specified limit shown in *Recommended Operating Conditions*.
- During power-up, there is no requirement for the relative timing of V_{RESET} with respect to V_{BIAS}.
- Power supply slew rates during power-up are flexible, provided that the transient voltage levels follow the requirements specified in *Absolute Maximum Ratings*, in *Recommended Operating Conditions*, and in Figure 15.
- During power-up, LVCMOS input pins must not be driven high until after V_{CC} have settled at operating voltages listed in *Recommended Operating Conditions*.

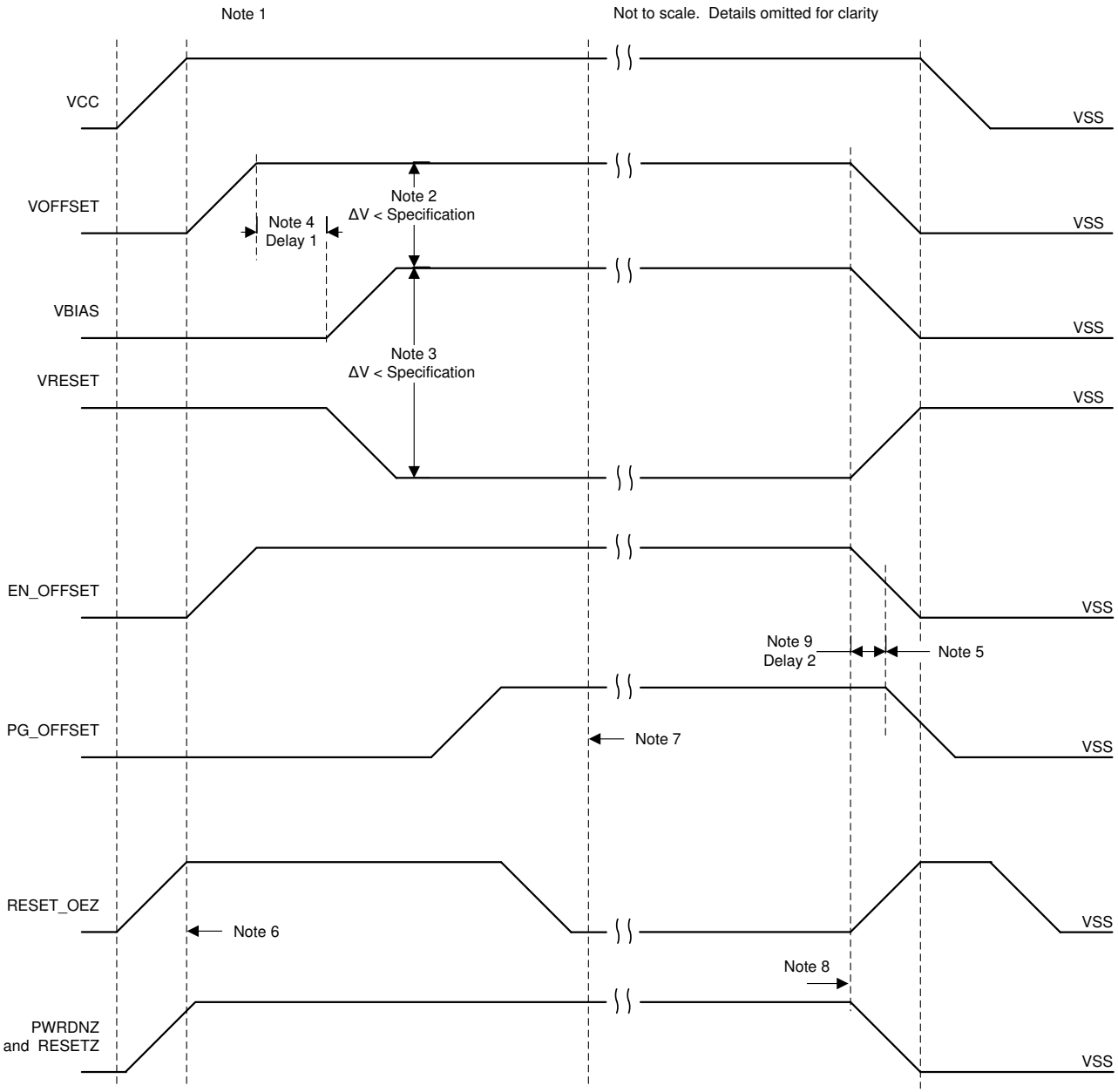
9.2 DMD Power Supply Power-Down Procedure

- During power-down, V_{CC} must be supplied until after V_{BIAS}, V_{RESET}, and V_{OFFSET} are discharged to within the specified limit of ground. See Table 8.
- During power-down, it is a strict requirement that the voltage difference between V_{BIAS} and V_{OFFSET} must be within the specified limit shown in *Recommended Operating Conditions*.
- During power-down, there is no requirement for the relative timing of V_{RESET} with respect to V_{BIAS}.
- Power supply slew rates during power-down are flexible, provided that the transient voltage levels follow the requirements specified in *Absolute Maximum Ratings*, in *Recommended Operating Conditions*, and in Figure 15.
- During power-down, LVCMOS input pins must be less than specified in *Recommended Operating Conditions*.

Table 8. DMD Power-Supply Requirements

PARAMETER	DESCRIPTION	MIN	NOM	MAX	UNIT
Delay1 (1)	Delay from V_{OFFSET} settled at recommended operating voltage to V_{BIAS} and V_{RESET} power up	1	2		ms
Delay2 (1)	PG_OFFSET hold time after EN_OFFSET goes low	100			ns

(1) See Figure 15.



(1) See *Recommended Operating Conditions* and the pin functions table.

(2) To prevent excess current, the supply voltage difference $|V_{OFFSET} - V_{BIAS}|$ must be less than the specified limit in *Recommended Operating Conditions*.

(3) To prevent excess current, the supply difference $|V_{BIAS} - V_{RESET}|$ must be less than the specified limit in the *Recommended Operating Conditions*.

(4) V_{BIAS} must power up after V_{OFFSET} has powered up, per the Delay1 specification in Table 8.

(5) PG_OFFSET must turn off after EN_OFFSET has turned off, per the Delay2 specification in Table 8.

(6) DLP controller software enables the DMD power supplies to turn on after RESET_OEZ is at logic high.

(7) DLP controller software initiates the global V_{BIAS} command.

(8) After the DMD micromirror park sequence is complete, the DLP controller software initiates a hardware power-down that activates PWRDNZ and disables V_{BIAS}, V_{RESET} and V_{OFFSET}.

(9) Under power-loss conditions where emergency DMD micromirror park procedures are being enacted by the DLP controller hardware, EN_OFFSET may turn off after PG_OFFSET has turned off. The OEZ signal goes high prior to PG_OFFSET turning off to indicate the DMD micromirror has completed the emergency park procedures.

Figure 15. DMD Power Supply Requirements

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10 Layout

10.1 Layout Guidelines

The DLP470TP DMD is part of a chipset that is controlled by two DLPC6421 display controllers in conjunction with the DLPA3005 PMIC and LED driver. These guidelines are targeted at designing a PCB board with the DLP470TP DMD. The DMD board is a high-speed multi-layer PCB, with primarily high-speed digital logic utilizing dual edge clock rates up to 400 MHz for DMD LVDS signals. The remaining traces are comprised of low speed digital LVTTL signals. TI recommends that mini power planes are used for V_{OFFSET}, V_{RESET}, and V_{BIAS}. Solid planes are required for Ground (V_{SS}). The target impedance for the PCB is 50 Ω ±10% with the LVDS traces being 100 Ω ±10% differential. TI recommends using an 8 layer stack-up as described in Table 9.

10.2 Layout Example

10.2.1 Layers

The layer stack-up and copper weight for each layer is shown in Table 9. Small sub-planes are allowed on signal routing layers to connect components to major sub-planes on top/bottom layers if necessary.

Table 9. Layer Stack-Up

LAYER NO.	LAYER NAME	COPPER WT. (oz.)	COMMENTS
1	Side A - DMD only	1.5	DMD, escapes, low frequency signals, power sub-planes
2	Ground	0.5	Solid ground plane (net GND)
3	Signal	0.5	50 Ω and 100 Ω differential signals
4	Signal/Power	0.5	50 Ω and 100 Ω differential signals / power
5	Ground	0.5	Solid ground plane (net GND)
6	Signal	0.5	50 Ω and 100 Ω differential signals
7	Ground	0.5	Solid ground plane (net GND)
8	Side B - All other Components	1.5	Discrete components, low frequency signals, power sub-planes

10.2.2 Impedance Requirements

Optimum layout practices requires the board to have a matched impedance of 50 Ω ±10% for all signals. Table 10 lists the exceptions to these imprdance requirements.

Table 10. Special Impedance Requirements

Signal Type	Signal Name	Impedance (Ω)
A, B, C, and D channel LVDS differential pairs	DDxP(0:15), DDxN(0:15)	100 ±10% differential across each pair
	DCLKx_P, DCLKx_N	
	SCTRL_CP, SCTRL_CN	

10.2.3 Trace Width, Spacing

Unless otherwise specified, TI recommends that all signals follow the 0.005”/0.005” design rule. Minimum trace clearance from the ground ring around the PWB has a 0.1” minimum. An analysis of impedance and stack-up requirements determine the actual trace widths and clearances.

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10.2.3.1 Voltage Signals

Table 11. Special Trace Widths, Spacing Requirements

SIGNAL NAME	MINIMUM TRACE WIDTH TO PINS (MIL)	LAYOUT REQUIREMENT
V_{SS}	15	Maximize trace width to connecting pin
V_{CC}	15	Maximize trace width to connecting pin
V_{OFFSET}	15	Create mini plane to DMD
V_{RESET}	15	Create mini plane to DMD
V_{BIAS}	15	Create mini plane to DMD

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11 Device and Documentation Support

11.1 Device Support

11.1.1 Device Nomenclature

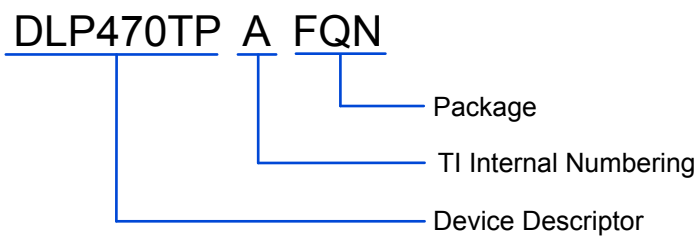


Figure 16. Part Number Description

11.1.2 Device Markings

The device marking includes both human-readable information and a 2-dimensional matrix code. The human-readable information is described in Figure 17 and includes the legible character string GHJJJJK DLP470TPAFQN. GHJJJJK is the lot trace code and DLP470TPAFQN is the device marking.

Example: GHJJJJK DLP470TPAFQN

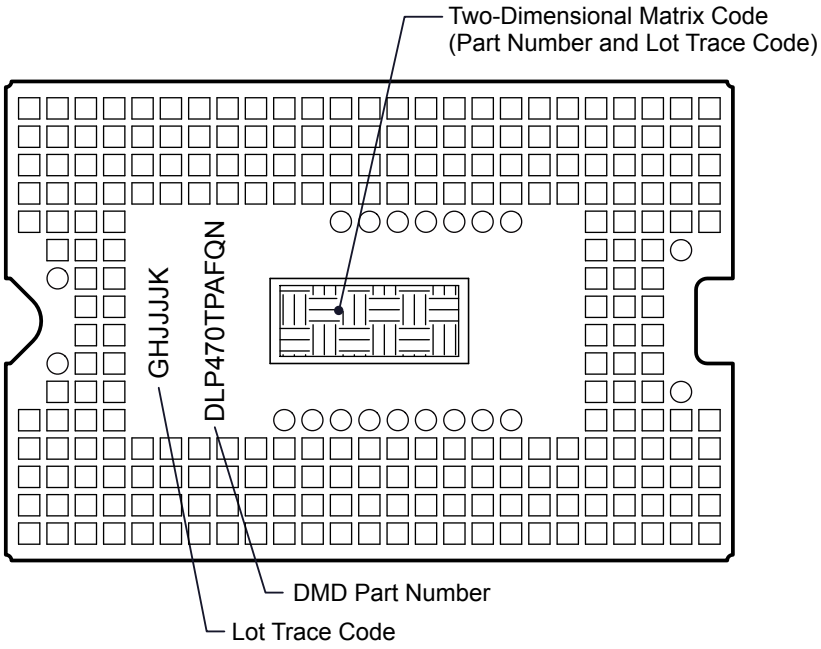


Figure 17. DMD Marking Locations

11.2 Documentation Support

11.2.1 Related Documentation

The following documents contain additional information related to the chipset components used with the DLP470TP DMD.

- DLPC6421 Display Controller Data Sheet
- DLPA3005 PMIC/LED Driver Data Sheet

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Community Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.5 Trademarks

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DLP is a registered trademark of Texas Instruments.

11.6 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

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12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DLP470TPAFQN	ACTIVE	CLGA	FQN	250	54	RoHS & Green	Call TI	N / A for Pkg Type			Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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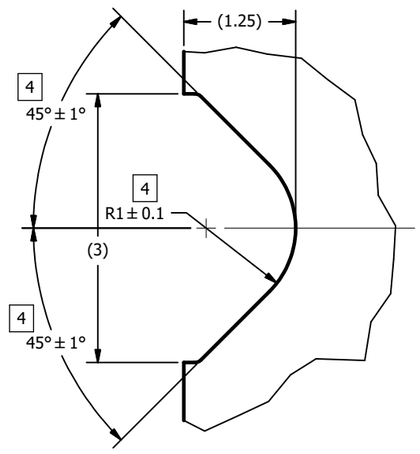
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REVISIONS

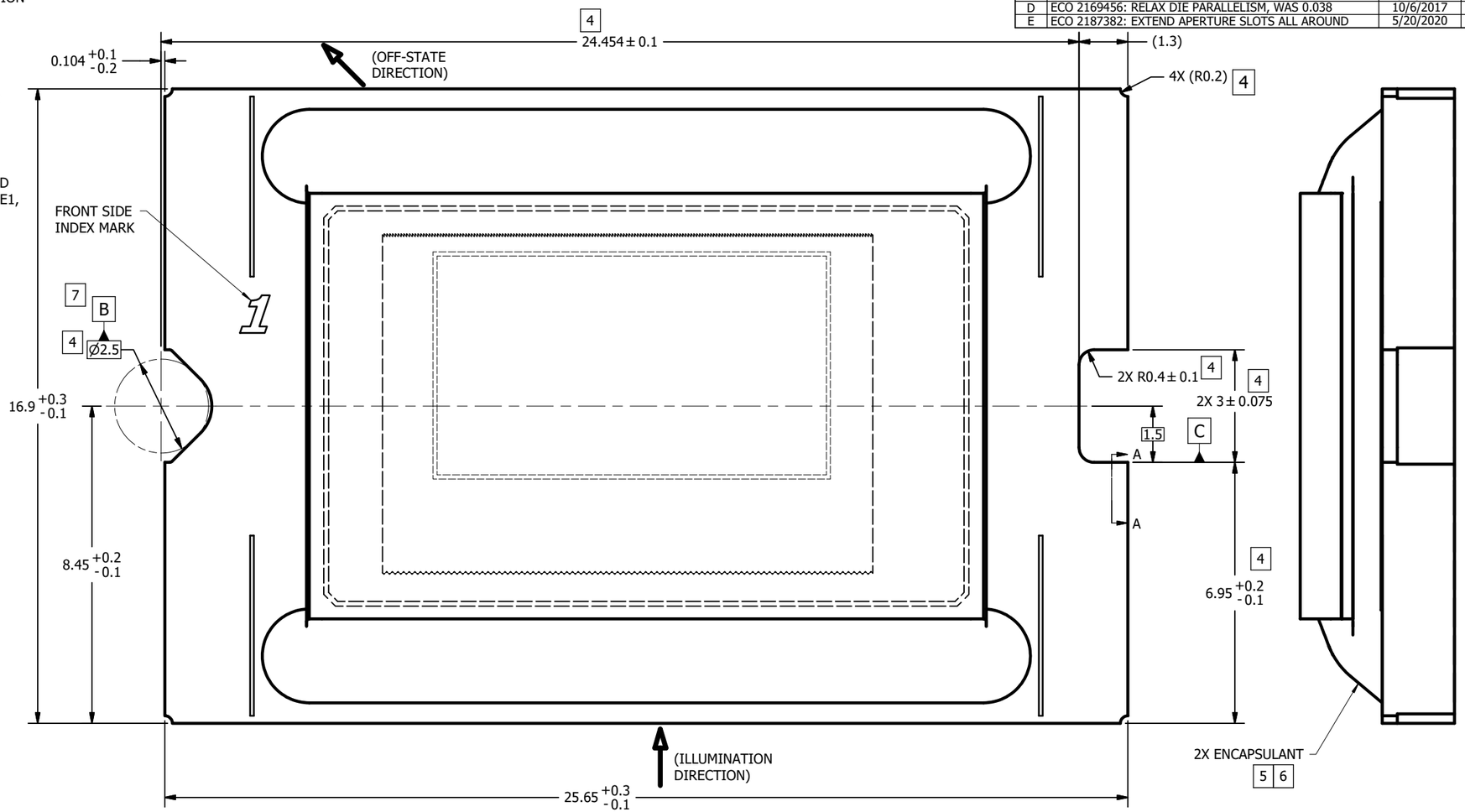
REV	DESCRIPTION	DATE	BY
A	ECO 2162276: INITIAL RELEASE	11/14/2016	BMH
B	ECO 2167828: CORRECT BACK SIDE MARKING; WAS 227-X	7/24/2017	BMH
C	ECO 2168706: ADD APERTURE SLOTS PICTORIALLY	9/14/2017	BMH
D	ECO 2169456: RELAX DIE PARALLELISM, WAS 0.038	10/6/2017	BMH
E	ECO 2187382: EXTEND APERTURE SLOTS ALL AROUND	5/20/2020	BMH

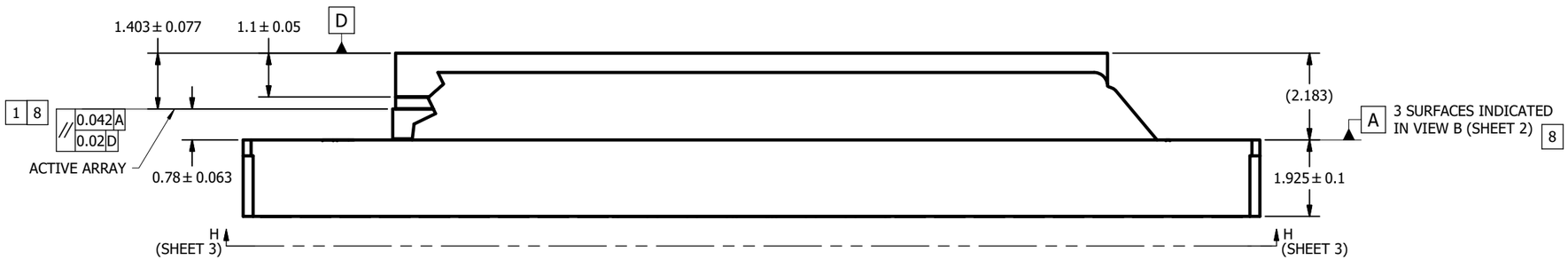
NOTES UNLESS OTHERWISE SPECIFIED:

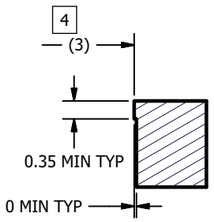
1. DIE PARALLELISM TOLERANCE APPLIES TO DMD ACTIVE ARRAY ONLY.
2. ROTATION ANGLE OF DMD ACTIVE ARRAY IS A REFINEMENT OF THE LOCATION TOLERANCE AND HAS A MAXIMUM ALLOWED VALUE OF 0.6 DEGREES.
3. BOUNDARY MIRRORS SURROUNDING THE DMD ACTIVE ARRAY.
4. NOTCH DIMENSIONS ARE DEFINED BY UPPERMOST LAYERS OF CERAMIC, AS SHOWN IN SECTION A-A.
5. ENCAPSULANT TO BE CONTAINED WITHIN DIMENSIONS SHOWN IN VIEW D (SHEET 3). NO ENCAPSULANT IS ALLOWED ON TOP OF THE WINDOW.
6. ENCAPSULANT NOT TO EXCEED THE HEIGHT OF THE WINDOW.
7. SEE DETAIL B FOR "V-NOTCH" DIMENSIONS.
8. WHILE ONLY THE THREE DATUM A TARGET AREAS A1, A2, AND A3 ARE USED FOR MEASUREMENT, ALL 4 CORNERS SHOULD BE CONTACTED, INCLUDING E1, TO SUPPORT MECHANICAL LOADS.



DETAIL B
V-NOTCH
SCALE 30 : 1







SECTION A-A
(ROTATED 90°)

	0314DA
NEXT ASSY	USED ON
APPLICATION	

THIRD ANGLE PROJECTION

UNLESS OTHERWISE SPECIFIED
- DIMENSIONS ARE IN MILLIMETERS
- TOLERANCES:
  - ANGLES ± 1°
  - 2 PLACE DECIMALS ± 0.25
  - 1 PLACE DECIMALS ± 0.50
- ~~DIMENSIONAL LIMITS APPLY BEFORE PROCESSES~~
- INTERPRET DIMENSIONS IN ACCORDANCE WITH ASME Y14.5M-1994
- ~~REMOVE ALL BURRS AND SHARP EDGES~~
- PARENTHETICAL INFORMATION FOR REFERENCE ONLY

		DATE
DRAWN	B. HASKETT	11/14/2016
ENGINEER	B. HASKETT	11/14/2016
QA/CE	P. KONRAD	11/14/2016
CM	S. SUSI	11/15/2016
	M. DORAK	11/17/2016
APPROVED	R. LONG	11/16/2016

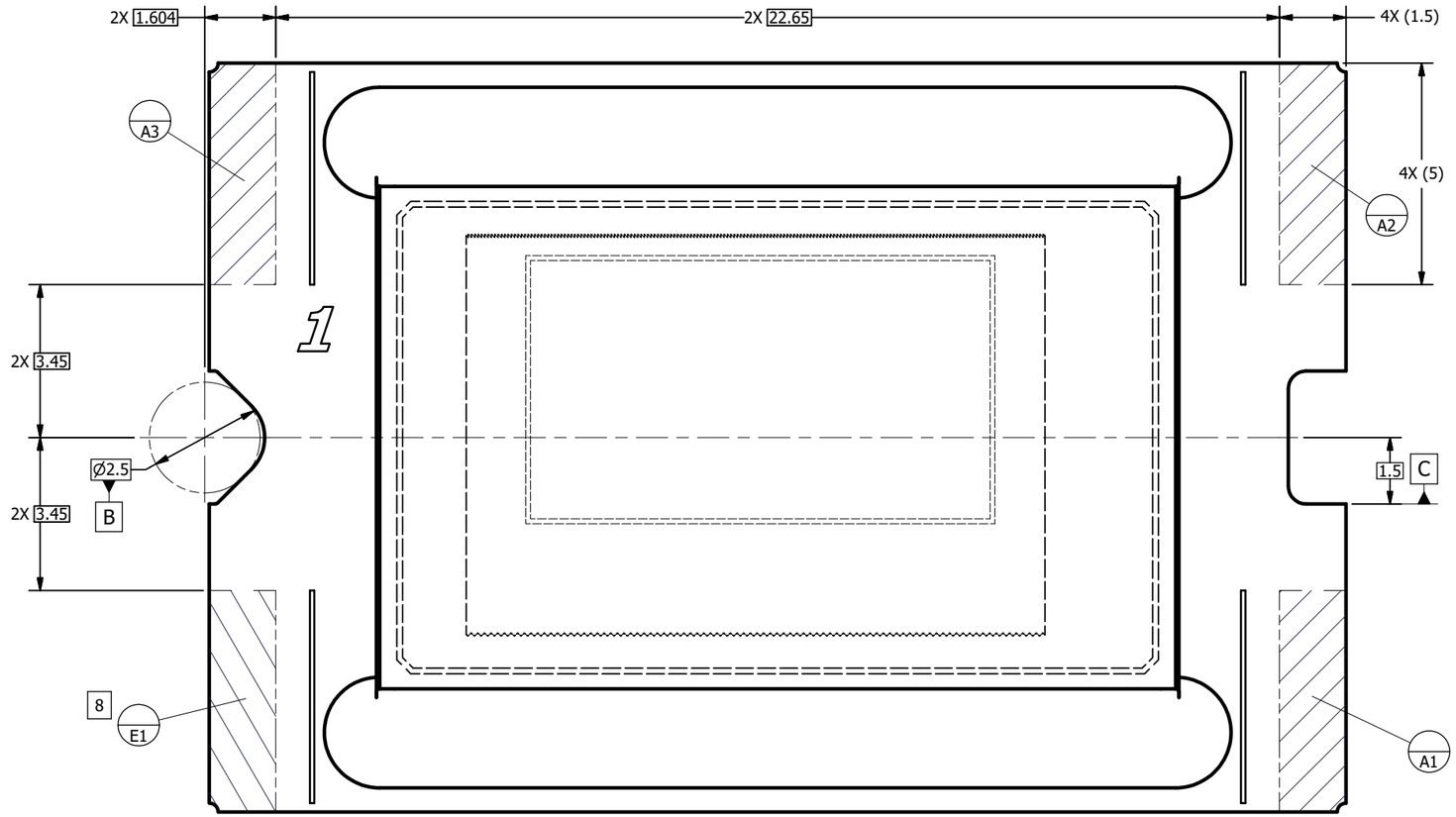
TEXAS INSTRUMENTS
Dallas Texas

TITLE: ICD, MECHANICAL, DMD, .47 4K SERIES 316 (FQN PACKAGE)

SIZE D | DWG NO 2515301 | REV E

SCALE 15:1 | SHEET 1 OF 5

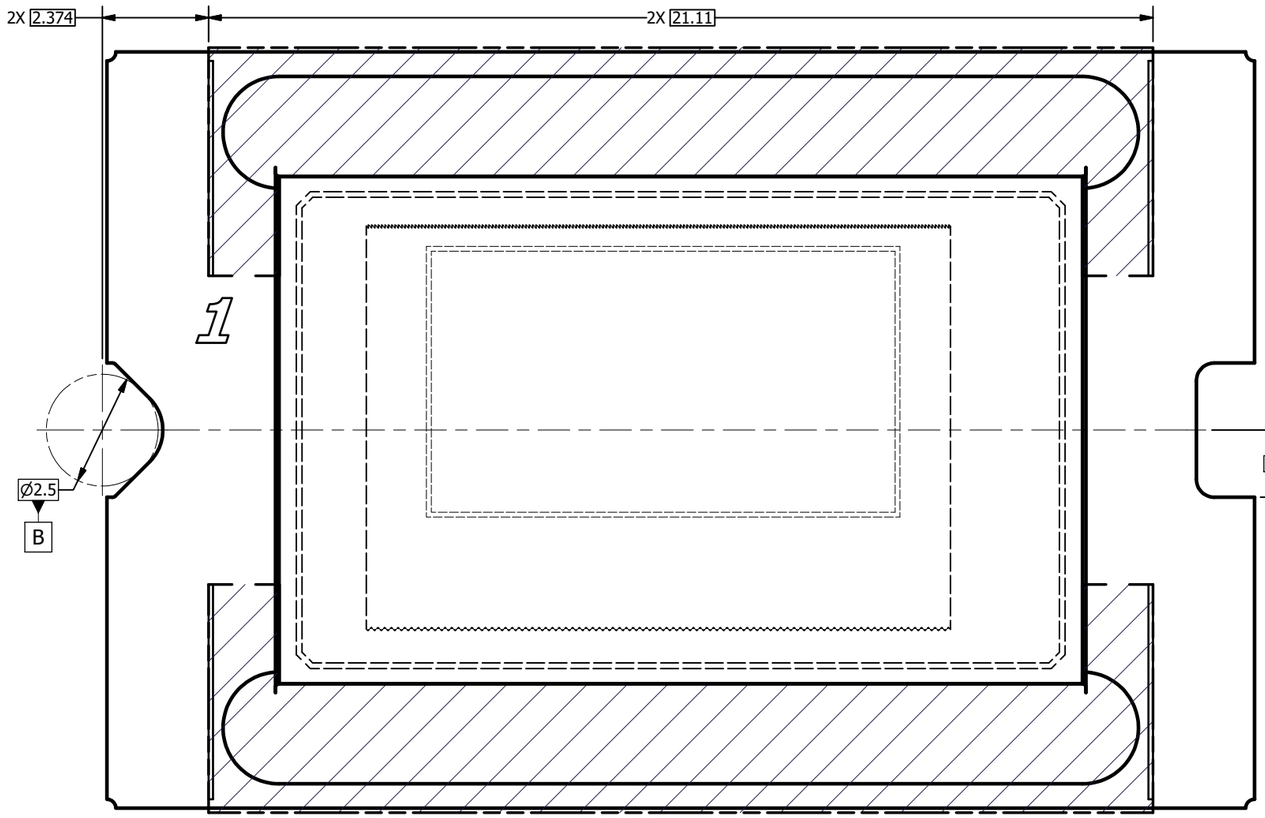
INV11-2006a



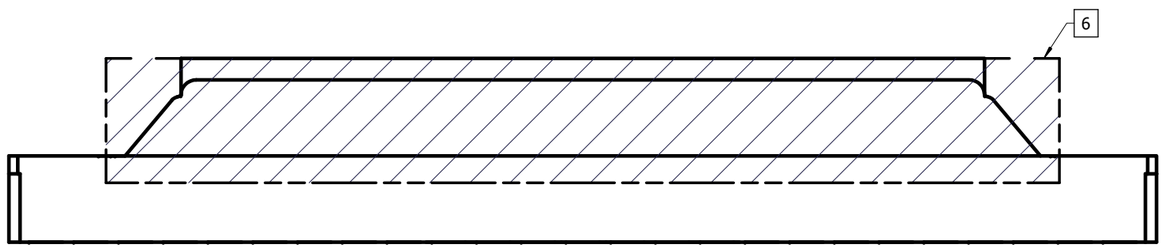
VIEW C
DATUMS A AND E
(FROM SHEET 1)

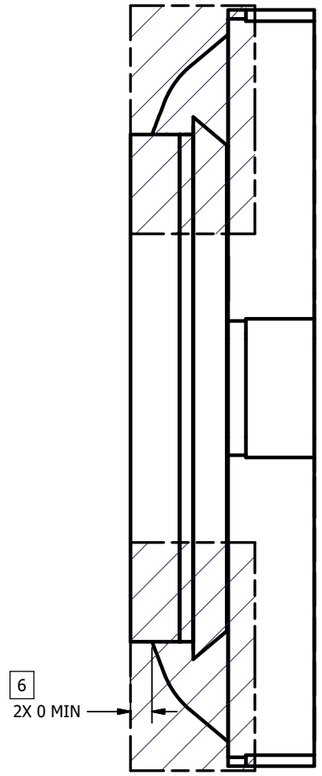
TEXAS INSTRUMENTS Dallas Texas	DRAWN B. HASKETT	DATE 11/14/2016	SIZE D		DWG NO 2515301	REV E
			SCALE		SHEET 2 OF 5	

INV11-2006a



VIEW D
ENCAPSULANT MAXIMUM X/Y DIMENSIONS 5
(FROM SHEET 1)

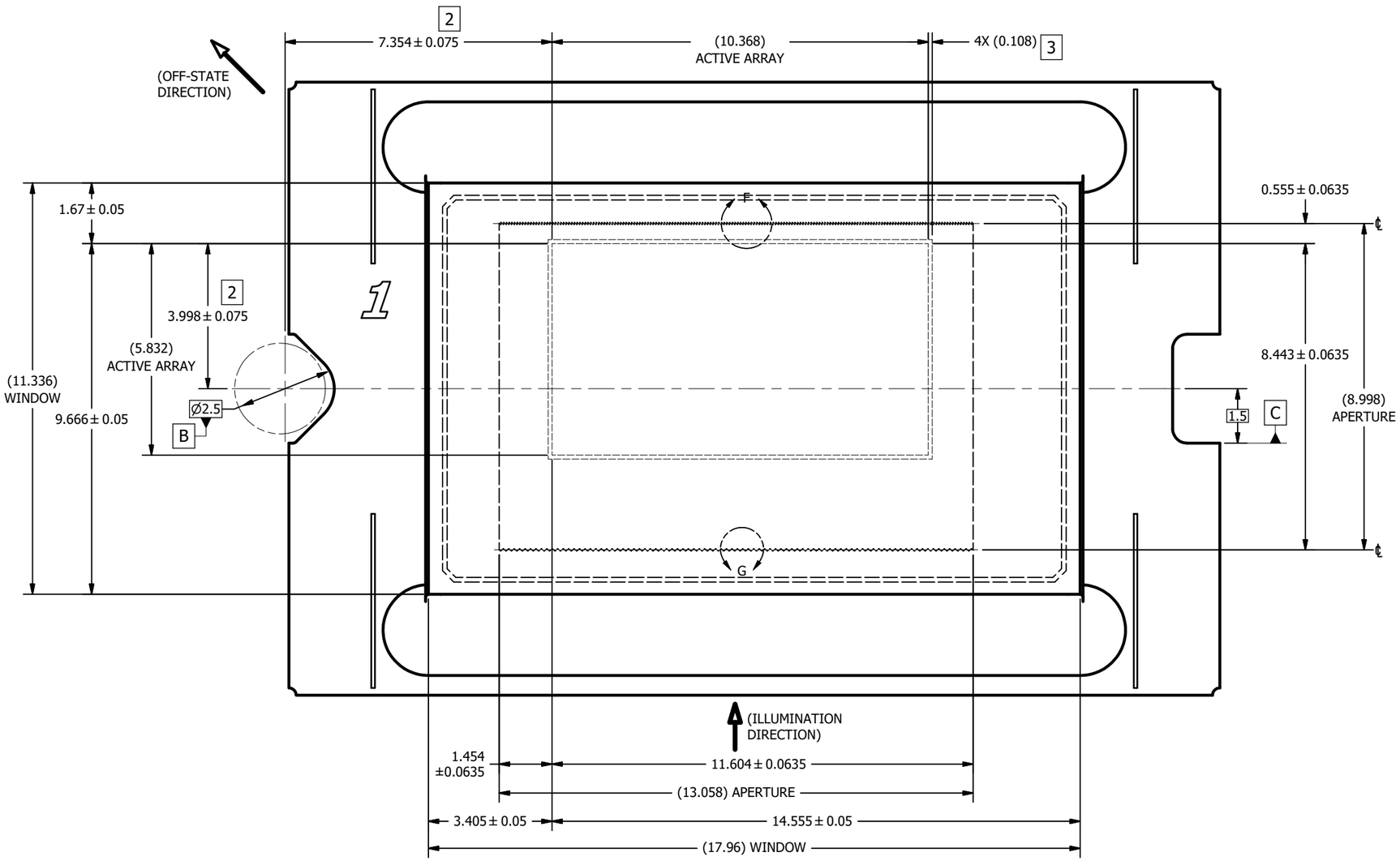




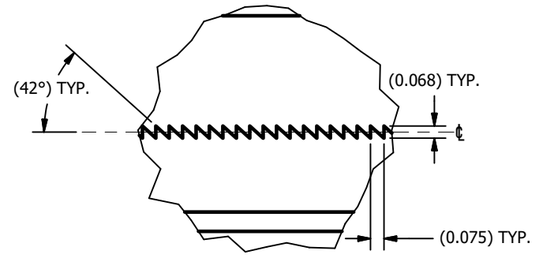
VIEW E
MAXIMUM ENCAPSULANT HEIGHT

Texas Instruments Dallas Texas	DRAWN B. HASKETT	DATE 11/14/2016	SIZE D	DWG NO 2515301 REV E
			SCALE	SHEET 3 OF 5

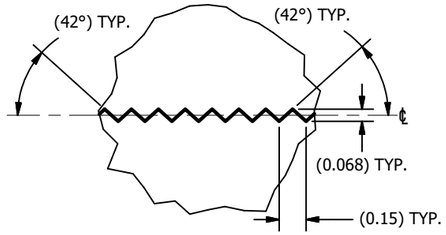
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VIEW E
WINDOW AND ACTIVE ARRAY
(FROM SHEET 1)



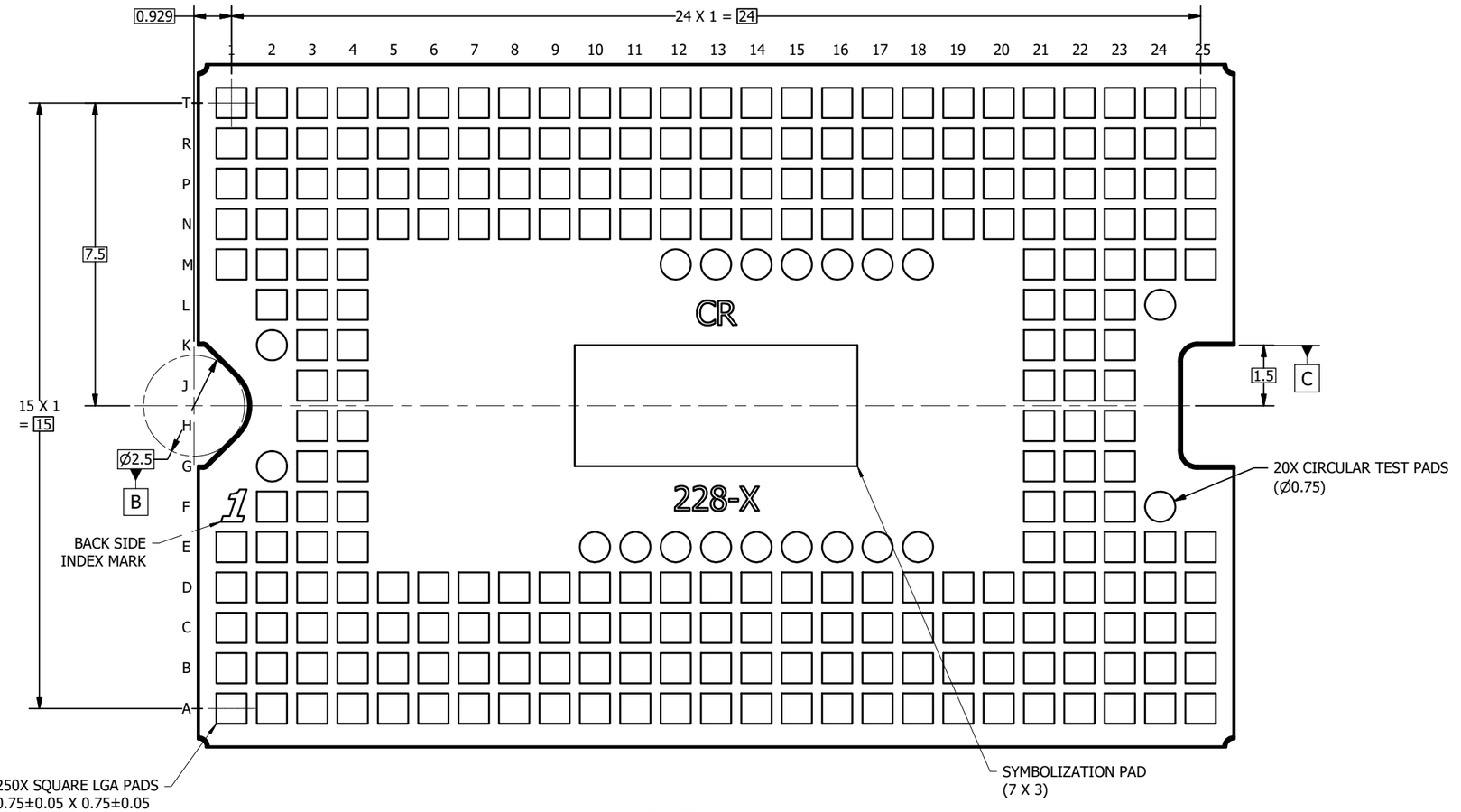
DETAIL F
APERTURE TOP EDGE
SCALE 60 : 1



DETAIL G
APERTURE BOTTOM EDGE
SCALE 60 : 1

TEXAS INSTRUMENTS Dallas Texas	DRAWN B. HASKETT	DATE 11/14/2016	SIZE D		DWG NO 2515301	REV E
			SCALE		SHEET 4 OF 5	

INV11-2006a



VIEW H-H
BACK SIDE METALLIZATION
(FROM SHEET 1)

Texas Instruments Dallas Texas	DRAWN B. HASKETT	DATE 11/14/2016	SIZE D	DWG NO 2515301 REV E
			SCALE	SHEET 5 OF 5

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