

SBOS229B – DECEMBER 2001 – REVISED JUNE 2003

192kHz Digital Audio Transmitter

FEATURES

- COMPLIANT WITH AES-3, IEC-60958, AND EIAJ CP1201 INTERFACE STANDARDS
- SUPPORTS SAMPLING RATES UP TO 192kHz
- SUPPORTS MONO-MODE OPERATION
- ON-CHIP DIFFERENTIAL LINE DRIVER
- FLEXIBLE AUDIO SERIAL INTERFACE:
  - -Master or Slave Mode Operation
  - -Supports I^2S, Left-Justified, and Right-Justified Data Formats
- SOFTWARE MODE VIA SERIAL CONTROL INTERFACE:
  - -Block Sized Buffer for Channel Status Data
  - -Auto Increment Mode for Block Sized Write and Read Operations
- HARDWARE MODE ALLOWS OPERATION WITHOUT A MICROCONTROLLER
- CRC CODE GENERATION FOR PROFESSIONAL MODE
- MASTER CLOCK RATE: $128f_S$, $256f_S$, $384f_S$, or $512f_S$
- +5V CORE SUPPLY (V_{DD})
- +2.7V TO V_{DD} LOGIC I/O SUPPLY (V_{IO})
- PACKAGE: TSSOP-28

APPLICATIONS

- DIGITAL MIXING CONSOLES
- DIGITAL MICROPHONES
- DIGITAL AUDIO WORKSTATIONS
- BROADCAST STUDIO EQUIPMENT
- EFFECTS PROCESSORS
- SURROUND-SOUND DECODERS AND ENCODERS
- A/V RECEIVERS
- DVD, CD, DAT, AND MD PLAYERS
- AUDIO TEST EQUIPMENT

DESCRIPTION

The DIT4192 is a digital audio transmitter designed for use in both professional and consumer audio applications. Transmit data rates up to 192kHz are supported. The DIT4192 supports both software and hardware operation, which makes it suitable for applications with or without a microcontroller. A flexible serial audio interface is provided, supporting standard audio data formats and easy interfacing to audio DSP serial ports.



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ABSOLUTE MAXIMUM RATINGS[1]

Power-Supply Voltage, V_{DD}	+6.5V
V_{IO}	+6.5V
Input Current	±10mA
Digital Input Voltage	–0.2V to +5.5V
Digital Output Voltage	–0.2V to (V_{DD} + 0.2V)
Power Dissipation	300mW
Operating Temperature Range	–40°C to + 85°C
Storage Temperature	–55°C to +125°C
Lead Temperature (soldering, 5s)	+260°C
Package Temperature (IR re-flow, 10s)	+235°C

NOTE: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR[1]	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
DIT4192	TSSOP-28	PW	–40°C to +85°C	DIT4192IPW	DIT4192IPW	Rails, 50
"	"	"	"	"	DIT4192IPWR	Tape and Reel, 2000

NOTE: (1) For the most current specifications and package information, refer to our web site at www.ti.com.

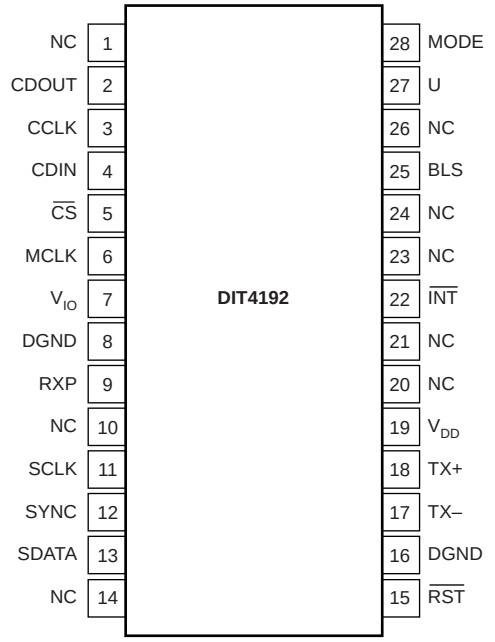
ELECTRICAL CHARACTERISTICS

All specifications at T_A = +25°C, V_{DD} = +5V, and V_{IO} = 3.3V unless otherwise noted.

PARAMETER	CONDITIONS	DIT4192IPW			UNITS
		MIN	TYP	MAX	
DIGITAL CHARACTERISTICS					
Applies to All Digital I/O Except TX+ and TX–					
High-Level Input Voltage, V_{IH}		0.7 • V_{IO}		V_{IO}	V
Low-Level Input Voltage, V_{IL}		0		0.2 • V_{IO}	V
High-Level Output Voltage, V_{OH}	I_O = –4mA	0.8 • V_{IO}			V
Low-Level Output Voltage, V_{OL}	I_O = +4mA	0		0.1 • V_{IO}	V
Input Leakage Current			1	10	µA
OUTPUT DRIVER CHARACTERISTICS					
Applies Only to TX+ and TX–					
High-Level Output Voltage, V_{OH}	I_O = –30mA	V_{DD} – 0.7	V_{DD} – 0.4	V_{DD}	V
Low-Level Output Voltage, V_{OL}	I_O = +30mA	0	0.4	0.7	V
SWITCHING CHARACTERISTICS					
Master Clock and Reset					
Master Clock (MCLK) Frequency				25	MHz
Master Clock (MCLK) Duty Cycle		40		60	%
Reset ($\overline{RST}$) Active Low Pulse Width		500			ns
Serial Control Port Timing					
CCLK Frequency					
Stereo Mode	f_S = Sampling Frequency			128 • f_S	MHz
Mono Mode	f_S = Sampling Frequency			64 • f_S	MHz
Serial Control Data Setup Time, t_{SDS}		12			ns
Serial Control Data Hold Time, t_{SDH}		8			ns
$\overline{CS}$ Falling to CCLK Rising, t_{CSCR}		15			ns
CCLK Falling to $\overline{CS}$ Rising, t_{CFCS}		12			ns
CCLK Falling to CDOUT Data Valid, t_{CFDO}				12	ns
$\overline{CS}$ Rising to CDOUT High Impedance, t_{CSZ}				10	ns
Audio Serial Interface Timing					
SYNC Frequency (or Frame Rate)				195.3050	kHz
SYNC Clock Period t_{SYNCP}		5.12			µs
SYNC High/Low Pulse Width, t_{SYNCHL}		2.56			µs
SCLK Frequency				25	MHz
SCLK Clock Period, t_{SCLKP}		40			ns
SCLK High/Low Pulse Width, t_{SCLKHL}		18			ns
SYNC Edge to SCLK Edge, t_{SYSK}		15			ns
Audio Data Setup Time, t_{ADS}		15			ns
Audio Data Hold Time, t_{ADH}		15			ns
C, U, and V Input Timing					
C/U/V Data Setup Time, t_{CUVS}		15			ns
C/U/V Data Hold Time, t_{CUVH}		15			ns
POWER-SUPPLY					
Operating Voltage					
V_{DD}		+4.5	+5	+5.5	V
V_{IO}		+2.7		V_{DD}	V
Supply Current					
I_{DD}, Quiescent	V_{DD} = +5V		25		µA
I_{DD}, Power-Down Mode	V_{DD} = +5V		2		µA
I_{DD}, Dynamic (at 192kHz operation)	V_{DD} = +5V		30		mA
I_{IO}, Quiescent	V_{IO} = +3.3V		15		µA
I_{IO}, Power-Down Mode	V_{IO} = +3.3V		15		µA
I_{IO}, Dynamic (at 192kHz operation)	V_{IO} = +3.3V		1.5		mA
I_{IO}, Power-Down Mode	V_{IO} = +5V		250		µA
I_{IO}, Quiescent	V_{IO} = +5V		250		µA
I_{IO}, Dynamic (at 192kHz operation)			3		mA
Power Dissipation					
PD, Quiescent	V_{DD} = +5V		100		µW
PD, Power-Down Mode	V_{DD} = +5V		100		µW
PD, Dynamic (at 192kHz operation)	V_{DD} = +5V		175		mW
TEMPERATURE RANGE					
Operating Range		–40		+85	°C
Storage Range		–55		+125	°C

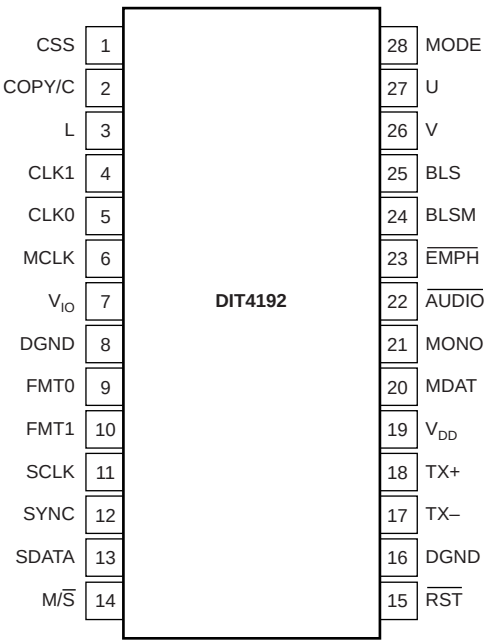
PIN CONFIGURATION: Software Mode (MODE = 0)

Top View TSSOP



PIN CONFIGURATION: Hardware Mode (MODE = 1)

Top View TSSOP



PIN DESCRIPTIONS: Software Mode

PIN	NAME	PIN DESCRIPTION
1	NC	No Connection
2	CDOUT	Control Port Data Output, Tri-State
3	CCLK	Control Port Data Clock Input
4	CDIN	Control Port Serial Data Input
5	$\overline{CS}$	Control Port Chip Select Input, Active LOW
6	MCLK	Master Clock Input
7	V_{IO}	Digital I/O Power Supply, +2.7V to V_{DD} Nominal
8	DGND	Digital Ground
9	RXP	AES-3 Encoded Data Input
10	NC	No Connection
11	SCLK	Audio Serial Port Data Clock I/O
12	SYNC	Audio Serial Port Frame SYNC Clock I/O
13	SDATA	Audio Serial Port Data Input
14	NC	No Connection
15	$\overline{RST}$	Reset Input, Active LOW
16	DGND	Digital Ground
17	TX–	Transmitter Line Driver Output
18	TX+	Transmitter Line Driver Output
19	V_{DD}	Digital Core Power Supply, +5V Nominal
20	NC	No Connection
21	NC	No Connection
22	$\overline{INT}$	Open Drain Interrupt Output, Active LOW. Requires 10kΩ pull-up resistor to V_{IO}.
23	NC	No Connection
24	NC	No Connection
25	BLS	Block Start I/O
26	NC	No Connection
27	U	User Data Input
28	MODE	Control Mode Input. Set MODE = 0 for Software Mode operation.

PIN DESCRIPTIONS: Hardware Mode

PIN	NAME	PIN DESCRIPTION
1	CSS	Channel Status Data Mode Input
2	COPY/C	Copy Protect Input or Channel Status Serial Data Input
3	L	Generation Status Input
4	CLK1	Master Clock Rate Selection Input
5	CLK0	Master Clock Rate Selection Input
6	MCLK	Master Clock Input
7	V_{IO}	Digital I/O Power Supply, +2.7V to V_{DD} Nominal
8	DGND	Digital Ground
9	FMT0	Audio Data Format Control Input
10	FMT1	Audio Data Format Control Input
11	SCLK	Audio Serial Port Data Clock I/O
12	SYNC	Audio Serial Port Frame SYNC Clock I/O
13	SDATA	Audio Serial Port Data Input
14	M/$\overline{S}$	Audio Serial Port Master/Slave Control Input
15	$\overline{RST}$	Reset Input, Active LOW
16	DGND	Digital Ground
17	TX–	Transmitter Line Driver Output
18	TX+	Transmitter Line Driver Output
19	VDD	Digital Core Power-Supply, +5V Nominal
20	MDAT	Mono Mode Channel Data Selection Input
21	MONO	Mono Mode Enable Input, Active HIGH
22	$\overline{AUDIO}$	Audio Data Valid Control Input, Active LOW
23	$\overline{EMPH}$	Pre-Emphasis Status Input, Active LOW
24	BLSM	Block Start Mode Control Input
25	BLS	Block Start I/O
26	V	Validity Data Input
27	U	User Data Input
28	MODE	Control Mode Input. Set MODE = 1 for Hardware Mode Operation.

GENERAL DESCRIPTION

The DIT4192 is a complete digital audio transmitter, suitable for both professional and consumer audio applications. Sampling rates up to 192kHz are supported. The DIT4192 complies with the requirements for the AES-3, IEC-60958, and EIAJ CP1201 interface standards.

Figures 1 and 2 show the block diagrams for the DIT4192 when used in Software and Hardware control modes. The MODE input (pin 28) determines the control model used to configure the DIT4192 internal functions. In Software mode, a serial control port is used to write and read on-chip control registers and status buffers. In Hardware mode, dedicated control pins are provided for configuration and status inputs.

The DIT4192 includes an audio serial port, which is used to interface to standard digital audio sources, such as Analog-to-Digital (A/D) converters, Digital Signal Processors (DSPs), and audio decoders. Support for Left-Justified, Right-Justified, and I^2S data formats is provided.

The AES-3 encoder creates a multiplexed bit stream, containing audio, status, and user data. See Figure 3 for the multiplexed data format. The data is then Bi-Phase Mark encoded and output to a differential line driver. The line driver outputs are connected to the transmission medium, be it cable or fiber optics. In the case of twisted-pair or coaxial cable, a transformer is commonly used to couple the driver outputs to the transmission line. This provides both isolation and improved common-mode rejection. For optical transmission, the TX+ (pin 18) driver output is connected to an optical transmitter module. See the Applications Information section of this data sheet for details regarding output driver circuit configurations.

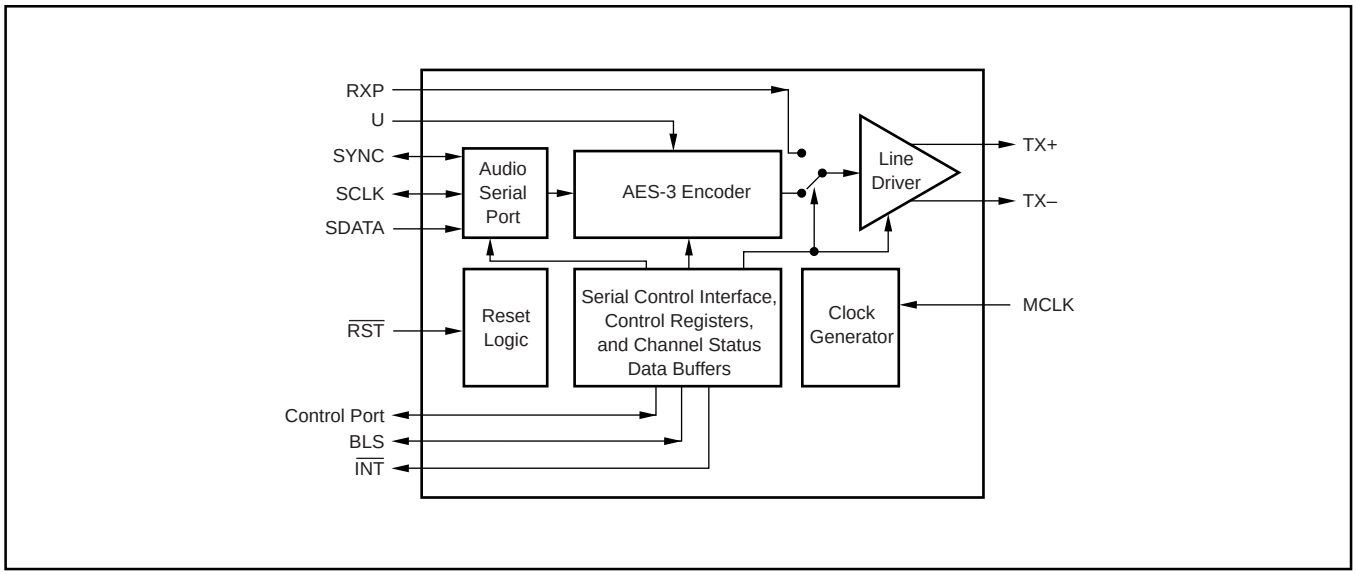


FIGURE 1. Software Mode Block Diagram.

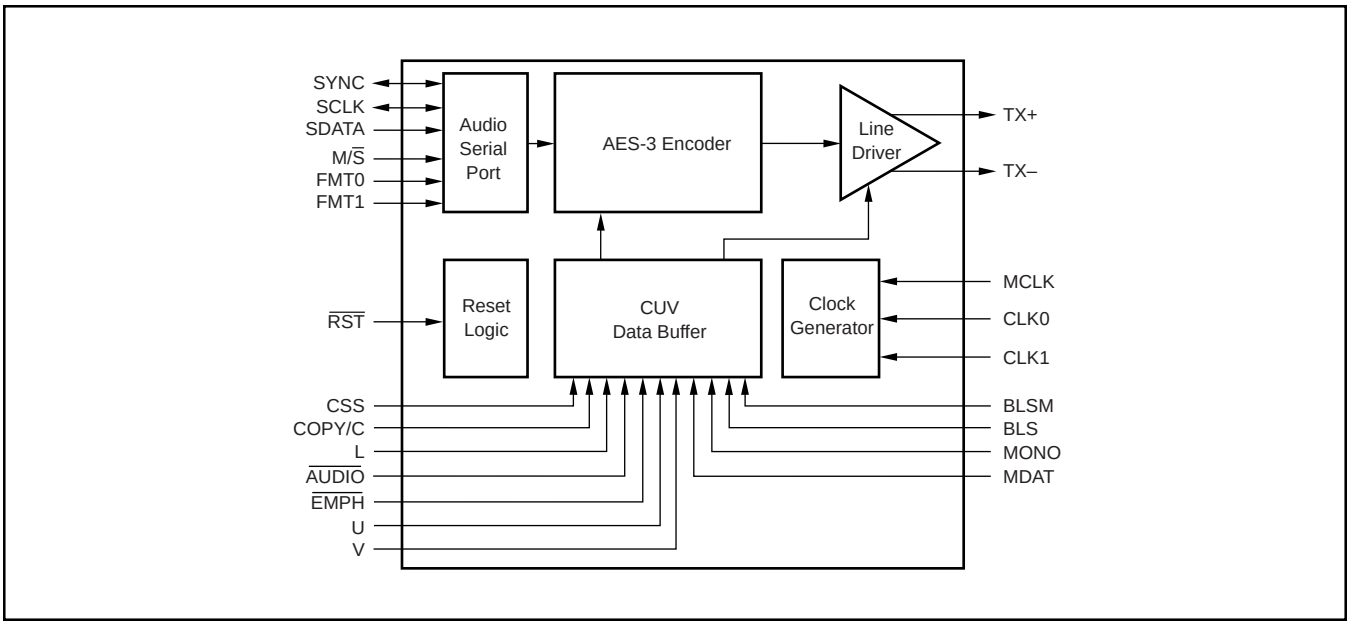


FIGURE 2. Hardware Mode Block Diagram.

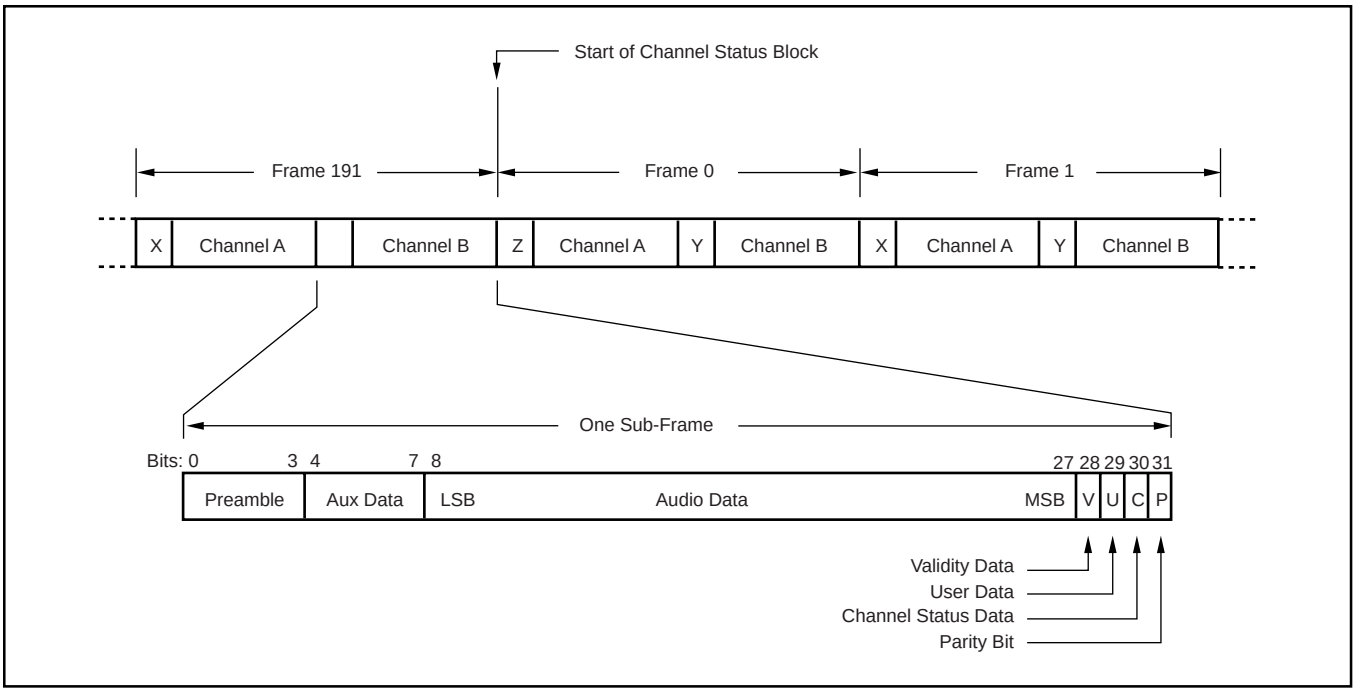


FIGURE 3. AES-3 Frame Format.

MASTER CLOCK

The DIT4192 requires a master clock for operation. This clock must be supplied at the MCLK input (pin 6). The maximum master clock frequency that may be supplied to MCLK is 25MHz. Table I shows master clock rates for common input sampling frequencies.

SAMPLING FREQUENCY (kHz)	MASTER CLOCK FREQUENCY (MHz)			
	128 • f_S	256 • f_S	384 • f_S	512 • f_S
22.05	n/a	5.6448	8.4672	11.2896
24	n/a	6.144	9.216	12.288
32	n/a	8.192	12.288	16.384
44.1	n/a	11.2896	16.9344	22.5792
48	n/a	12.288	18.432	24.576
88.2	n/a	22.5792	n/a	n/a
96	n/a	24.576	n/a	n/a
176.4	22.5792	n/a	n/a	n/a
192	24.576	n/a	n/a	n/a

TABLE I. Master Clock Frequencies for Common Sampling Rates.

For Software mode, the master clock frequency selection is programmed using the CLK0 and CLK1 bits in Control Register 02_H. For Hardware mode, the CLK0 (pin 5) and CLK1 (pin 4) inputs are used to select the master clock frequency. Table II shows the available MCLK frequency selections.

CONTROL BITS OR INPUT PINS		
CLK1	CLK0	MASTER CLOCK (MCLK) SELECTION
0	0	128 • f_S
0	1	256 • f_S
1	0	384 • f_S
1	1	512 • f_S

TABLE II. Master Clock Rate Selection for Software and Hardware Modes.

RESET AND POWER-DOWN OPERATION

The DIT4192 includes a reset input, $\overline{RST}$ (pin 15), which is used to force a reset sequence. When the DIT4192 is first powered up, the user must assert $\overline{RST}$ low in order to start the reset sequence. The $\overline{RST}$ input must be low for a minimum of 500ns. The $\overline{RST}$ input is then forced high to enable normal operation. For software mode, the reset sequence will force all internal registers to their default settings. In addition, the reset sequence will force all channel status bits to 0 in Software mode.

While the $\overline{RST}$ input is low, the transmitter outputs, TX– (pin 17) and TX+ (pin 18), are forced to ground.

Upon setting $\overline{RST}$ high, the TX– and TX+ outputs will remain low until the rising edge of the SYNC clock is detected at pin 12. Once this occurs, the TX– and TX+ outputs will become active and be driven by the output of the AES-3 encoder.

In Software mode, the DIT4192 also includes software reset and power-down bits, located in control register 02_H. The software reset bit, $\overline{RST}$, and the software power-down bit, PDN, are both active high.

AUDIO SERIAL PORT

The audio serial port is a 3-wire interface used to connect the DIT4192 to an audio source, such as an A/D converter or DSP. The port supports sampling frequencies up to 192kHz. The port signals include SDATA (pin 13), SYNC (pin 12), and SCLK (pin 11). The SDATA pin is the serial data input for the port. The SCLK pin may be either an input or output, and is used to clock serial data into the port. The SYNC pin may be either an input or output, and provides the frame synchroni-

zation clock for the port. The SYNC pin is also used as a data latch clock for the channel status, user, and validity data inputs in Hardware mode, and the user data input in Software mode.

SLAVE OR MASTER MODE OPERATION

The audio serial port supports both Slave and Master mode operation. In Slave mode, both SYNC and SCLK are configured as inputs. The audio source device must generate both the SYNC and SCLK clocks in Slave mode. In Master mode, both SYNC and SCLK are configured as outputs. The audio serial port generates the SYNC and SCLK clocks in Master mode, deriving both from the master clock (MCLK) input.

In Software mode, Master/Slave mode selection is performed using the M/$\overline{S}$ bit in Control Register 03_H (defaults to Slave mode). In Hardware mode, the M/S input (pin 14) is used to select the audio serial port mode. This is shown in Table III.

CONTROL BITS OR INPUT PIN	
M/$\overline{S}$	MASTER/SLAVE MODE SELECTION
0	Slave Mode, both SYNC and SCLK are inputs.
1	Master Mode, both SYNC and SCLK are outputs.

TABLE III. Master/Slave Mode Selection for Software or Hardware Mode.

SYNC AND SCLK FREQUENCIES

The SYNC clock rate is the same as the sampling frequency, or f_S. This holds true for both Slave and Master modes. The DIT4192 supports SYNC frequencies up to 192kHz.

The SCLK frequency in Slave mode must provide at least one clock cycle for each data bit that is input at SDATA. The maximum SCLK frequency is 128 • f_S, or 24.576MHz for f_S = 192kHz. The SCLK frequency in Master mode is set by the DIT4192 itself. For Software mode operation, the SCLK rate may be programmed to either 64 • f_S or 128 • f_S, using the SCLKR bit in Control Register 03_{HEX}. In Hardware mode, the SCLK frequency is fixed at 64 • f_S for Master mode.

AUDIO DATA FORMATS

The DIT4192 supports standard audio data formats, including Philips I²S, Left-Justified, and Right-Justified data.

Software mode provides the most flexible format selection, while Hardware mode supports a limited subset of the Software mode formats. Linear PCM audio data at the SDATA input is typically presented in Binary Two's Complement, MSB first format. Encoded or non-audio data may be provided as required by the encoding scheme in use. Figure 4 shows the common data formats used by the audio serial port.

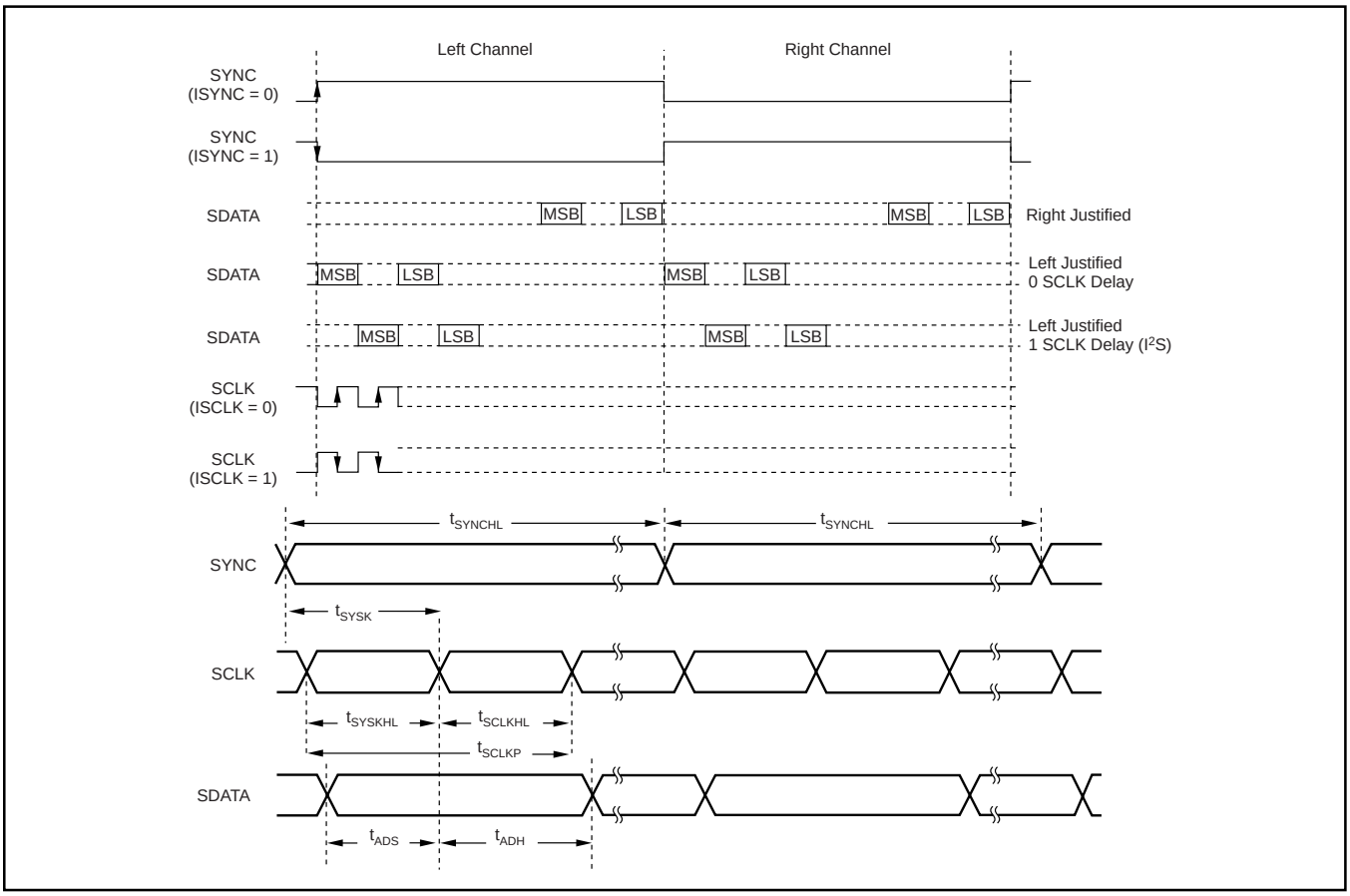


FIGURE 4. Audio Data Formats and Timing.

For Software mode, Control Register 03_H is used to set the audio data format selection. Data word length may be set to 16, 18, 20, or 24 bits using the WLEN0 and WLEN1 bits. Several format parameters, including SCLK sampling edge, data delay from the start of frame, and SYNC polarity may be programmed using this register. Table IV shows examples of register bit settings for three standard audio formats. SCLK sampling edges and SYNC polarity may differ from one system implementation to the next. Consult the audio source device data sheet or technical reference for details regarding the output data formatting.

For Hardware mode, the FMT0 (pin 9) and FMT1 (pin 10) inputs are utilized to select one of four audio data formats. Refer to Table V for the available format selections.

INPUT PINS		
FMT1	FMT0	FORMAT SELECTIONS
0	0	24-Bit Left-Justified
0	1	24-Bit I^2S
1	0	24-Bit Right-Justified
1	1	16-Bit Right-Justified

TABLE V. Audio Data Format Selection for Hardware Mode.

AES-3 ENCODER OPERATION

The AES-3 encoder performs the multiplexing of audio, channel status, user, and validity data. It also performs Bi-Phase Mark encoding of the multiplexed data stream. This section describes how channel status, user, and validity data are input to the encoder function.

BLOCK START INPUT/OUTPUT

The block start is used to indicate the start of a channel status data block, which starts with Frame 0 for the AES-3 data stream. For the DIT4192, the block start signal BLS (pin 25), may be either an input or output. In Software mode, the direction of BLS is set using the BLSM bit in control register 01_H (defaults to input). In Hardware mode, the direction of BLS is set by the BLSM input (pin 24). If BLSM = 0, the BLS pin is an input. If BLSM = 1, the BLS pin is an output.

For Software mode operation, the block start signal is synchronized to the audio serial port frame sync clock, SYNC (pin 12). When BLS is configured as an input pin, it is sampled on the rising edge of SYNC when the ISYNC bit in control register 03_H is set to 0. Otherwise, it is sampled on the falling edge of SYNC when the ISYNC bit is set to 1. If BLS is high when it is sampled, then a block start condition is indicated. When BLS is configured as an output and the ISYNC bit is set to 0, BLS will go high at every 192nd falling edge of SYNC for Stereo mode, or every 384th falling edge of SYNC for Mono mode. BLS will then go low on the following falling edge. If the ISYNC bit is set to 1, then BLS transitions on the rising edge of SYNC.

Hardware mode operation is similar to Software mode operation, with the exception that there are only a limited number of data formats available for the audio serial port. For Left- and Right-Justified formats, BLS behaves as it would in Software mode with ISYNC = 0. For the I^2S data format, BLS behaves as it would in Software mode with ISYNC = 1.

CHANNEL STATUS DATA INPUT

Channel status data input is determined by the control mode in use. In Software mode, the channel status data buffer is accessed through the serial control port. Buffer operations are described in detail in the section of this data sheet entitled Channel Status Buffer Operation (Software Mode Only). In Hardware mode, channel status data input is accomplished by one of two user-selectable methods.

THE CSS INPUT

In Hardware mode, the state of the CSS input (pin 1) determines the function of dedicated channel status inputs.

When CSS = 0, the COPY (pin 2), L (pin 3), $\overline{\text{AUDIO}}$ (pin 22), and $\overline{\text{EMPH}}$ (pin 23) inputs are used to set associated channel status data bits. The COPY and L inputs are used to set up copy protection for consumer operation, or indicate that the transmitter is operating in professional mode, without copy protection. The $\overline{\text{AUDIO}}$ input is utilized to indicate whether the data being transmitted is PCM audio data, or non-audio data. The $\overline{\text{EMPH}}$ input is used to indicate whether the PCM audio data has been pre-emphasized using the 50/15µs standard. See Table VI for the available options for these dedicated channel status inputs.

When CSS = 1, the channel status data is input in a serial fashion at the C input (pin 2). Data is clocked on the rising and falling edges of the SYNC input (pin 12). All channel status data bits can be written in this mode, allowing greater flexibility than the previous Hardware mode case with CSS = 0. See Figure 5 for the C input timing diagram.

AUDIO DATA FORMATS	CONTROL REGISTER 03_H BIT SETTINGS							
	Bit Name	Function	Bit Name	Function	Bit Name	Function	Bit Name	Function
	JUS	Justification	DELAY	SCLK Delay	ISCLK	Sampling Edge	ISYNC	Phase
Philips I^2S	0	Left-Justified	1	1 SCLK Delay	0	Rising Edge	1	Inverted
Left-Justified	0	Left-Justified	0	0 SCLK Delay	0	Rising Edge	0	Noninverted
Right-Justified	1	Right-Justified	0	0 SCLK Delay	0	Rising Edge	0	Noninverted

TABLE IV. Audio Data Format Selection in Software Mode.

INPUT	FUNCTION		
COPY L	**Copy Status** **Generation Status**		
	COPY	L	Status
	0	0	Consumer Mode, PRO = 0, COPY = 0, L = 0
	0	1	Consumer Mode, PRO = 0, COPY = 0, L = 1
	1	0	Consumer Mode, PRO = 0, COPY = 1, L = 0
	1	1	Professional Mode, PRO = 1, No Copy Protection
$\overline{\text{AUDIO}}$	**Audio Data Status**		
	$\overline{\text{AUDIO}}$	Status	
	0	Digital (or Linear PCM) Audio Data	
	1	Non-Audio or Encoded Audio Data	
$\overline{\text{EMPH}}$	**Pre-Emphasis Status**		
	$\overline{\text{EMPH}}$	Status	
	0	Pre-emphasis bits are set to indicate 50/15µs Pre-emphasis has been applied.	
	1	Pre-emphasis bits are set to indicate that no Pre-emphasis has been applied.	

TABLE VI. Channel Status Data Input for Hardware Mode with CSS = 0.

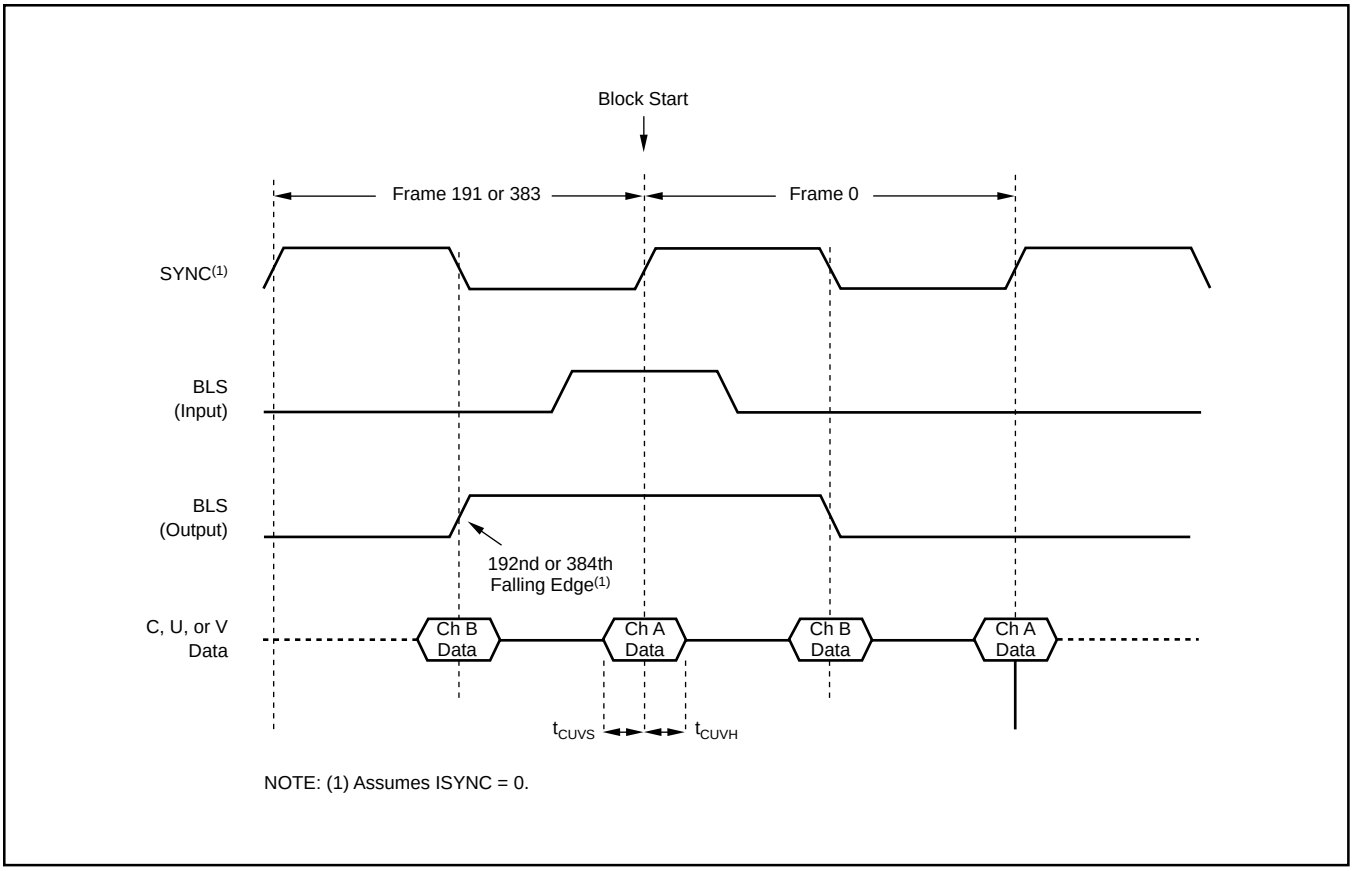


FIGURE 5. C, U, and V Data Timing.

USER AND VALIDITY DATA INPUT

The user data bits in the AES-3 data stream allow for a convenient way to transfer user-defined or application specific data to another device containing an AES-3 receiver. The U input (pin 27) is used in both Software and Hardware mode to input the user data in a serial fashion. Figure 5 shows the U input timing diagram.

Validity data is used to indicate that a sample is error-free audio data, or that the sample is defective and is not suitable for further processing. In Software mode, the VAL bit in control register 01_H is utilized to write the validity data. In Hardware mode, the V input (pin 26) is used to input the validity data in serial fashion. Refer to Figure 5 for V input timing for Hardware Mode.

When VAL or V = 0, this indicates that the audio data is valid and suitable for further processing. When VAL or V = 1, then the audio sample is defective and should not be used.

LINE DRIVER OUTPUTS

The DIT4192 includes a balanced line driver. The line driver outputs are TX– (pin 17) and TX+ (pin 18). In Software mode, the line driver input is taken from either the output of the on-chip AES-3 encoder, or from an external AES-3 encoded source input at RXP (pin 9). The input source is selected using the BYPASS bit in control register 01_H (defaults to the on-chip AES-3 encoder). In Hardware mode, the line driver source is always the on-chip AES-3 encoder.

The outputs of the line driver will follow the AES-3 encoded data source in normal operation. During a hardware or software reset, or when the device is in power-down mode, the line driver outputs will be forced to ground. The outputs can also be forced to ground at any time in Software mode by setting the TXOFF bit to 1 in control register 01_H.

CONTROL PORT OPERATION (SOFTWARE MODE ONLY)

For Software mode operation, the DIT4192 includes a serial control port, which is used to write and read control registers and the channel status data buffer. Port signals include $\overline{CS}$ (pin 5), CDIN (pin 4), CDOUT (pin 2), and CCLK (pin 3).

$\overline{CS}$ is the active low chip select. This signal must be driven low in order to write or read control registers and the channel status data buffer.

CDIN is the serial data input, while CDOUT serves as the serial data output. The CDOUT pin is a tri-state output, which is set to a high-impedance state when not performing a Read operation, or when $\overline{CS}$ = 1.

CCLK is the data clock for the serial control interface. Data is clocked in at CDIN on the rising edge of CCLK, while data is clocked out at CDOUT on the falling edge of CCLK. Data is clocked MSB first for both CDIN and CDOUT.

WRITE OPERATION

Figure 6 illustrates the write operation for the control port. You may write one register or buffer address at a time, or use the auto-increment capability built into the control port to perform block writes. The register or buffer data is preceded by a 16-bit header, with the first byte being used to configure control port operation and set the starting register or buffer address. The second byte of the header is comprised of “don’t care” bits, which can be set to either 0 or 1 without affecting port operation.

The first byte of the header contains two control bits, R/$\overline{W}$ and STEP, followed by a 6-bit address. For write operations, R/$\overline{W}$ = 0. The STEP bit determines the address step size for the auto-increment operation. When STEP = 0, the address is incremented by 1. When STEP = 1, the address is incremented by 2. Incrementing by 1 is useful when writing multiple control registers in sequence, or when writing both left and right channel status data in sequence. Incrementing by 2 is useful when writing just one channel of status data in sequence.

The third byte contains the 8-bit data for the register or buffer address pointed to by the first byte of the header. To write a single address location, $\overline{CS}$ is brought high after the least significant bit of the third byte is clocked into the port. For auto increment mode, $\overline{CS}$ is kept low to write successive register or buffer addresses.

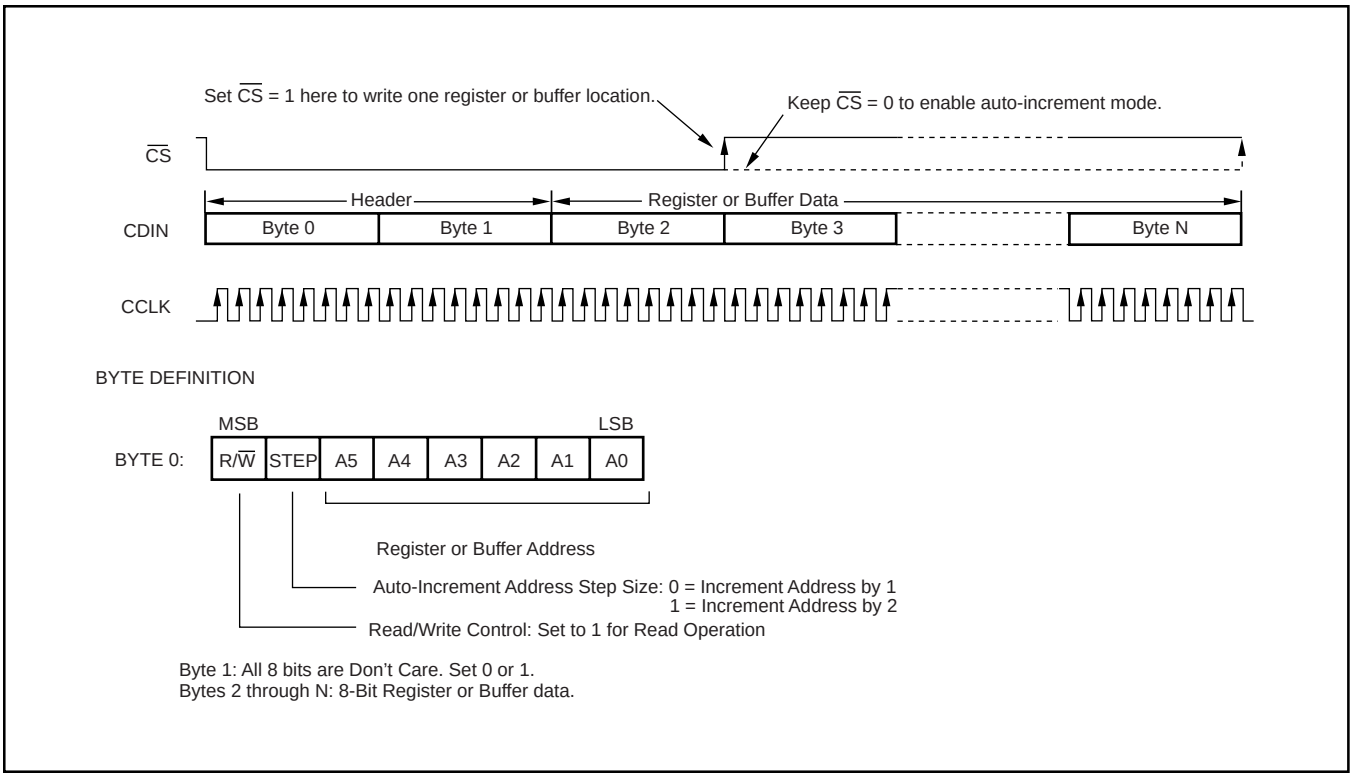


FIGURE 6. Write Operation Format.

READ OPERATION

Figure 7 shows an illustration of the read operation for the control port. You may read one register or buffer address at a time, or use the auto-increment capability built into the control port to perform block reads. A 16-bit header is first written to the port, with the first byte being used to configure control port operation and set the starting register or buffer address. The second byte of the header is comprised of "don't care" bits, which can be set to either 0 or 1 without affecting port operation.

The first byte of the header contains two control bits, R/$\overline{W}$ and STEP, followed by a 6-bit address. For read operations, R/$\overline{W}$ = 1. The STEP bit determines the address step size for the auto-increment operation. When STEP = 0, the address is incremented by 1. When STEP = 1, the address is incremented by 2. Incrementing by 1 is useful when reading multiple control registers in sequence, or when reading both left and right channel status data in sequence. Incrementing by 2 is useful for reading just one channel of status data in sequence.

The first output data byte occurs immediately after the 16-bit header has been written. This byte contains the 8-bit data for the register or buffer address pointed to by the first byte of the header. To read a single address location, $\overline{CS}$ is brought high after the least significant bit of the first data byte is clocked out of the port. For auto-increment mode, $\overline{CS}$ is kept low to read successive register or buffer addresses.

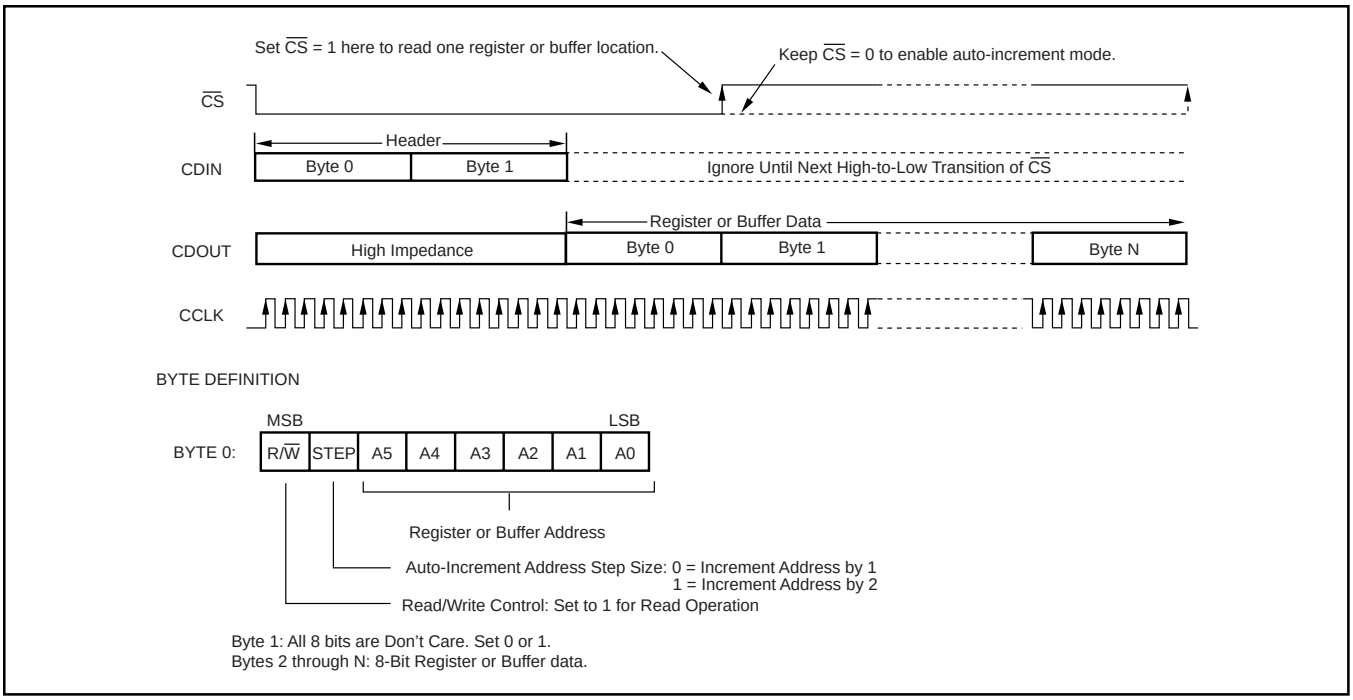


FIGURE 7. Read Operation Format.

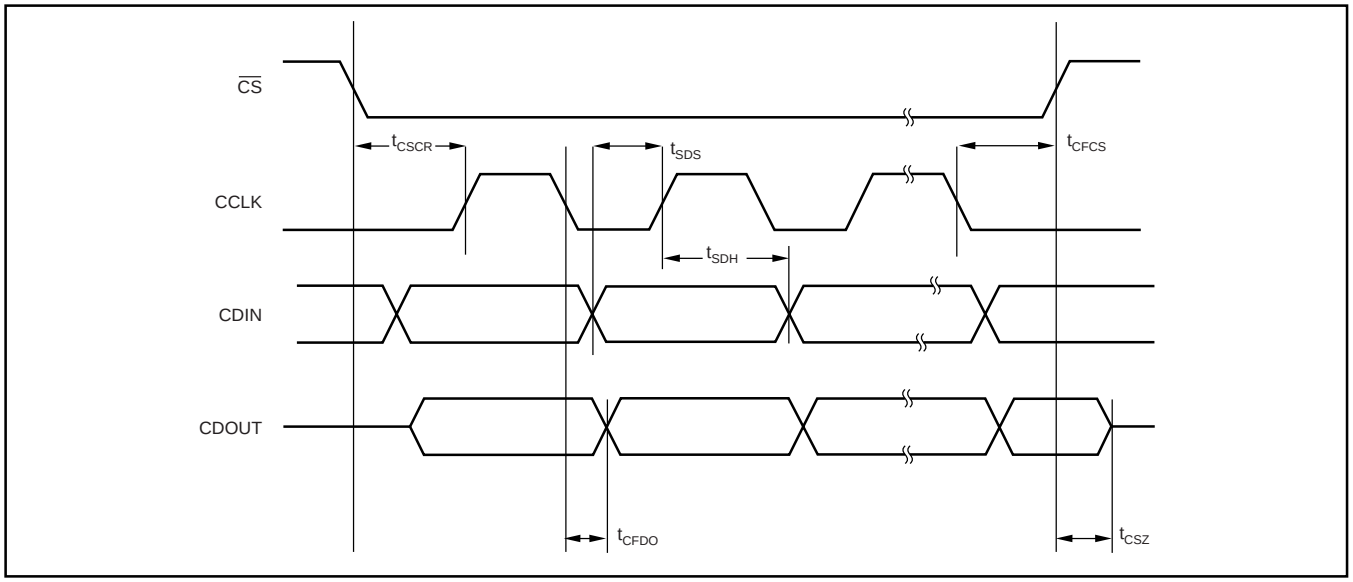


FIGURE 8. Serial Port Timing.

CONTROL REGISTER DEFINITIONS (SOFTWARE MODE ONLY)

This section defines the control registers used to configure the DIT4192, as well as the status register used to indicate an interrupt source.

Register 00_H: Reserved for Factory Use

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
0	0	0	0	0	0	0	0

BLSM **Block Start Mode (Defaults to 0)**

When set to 0, BLS (pin 25) is configured as an input pin.

When set to 1, BLS (pin 25) is configured as an output pin.

VAL **Audio Data Valid (Defaults to 0)**

When set to 0, valid Linear PCM audio data is indicated.

When set to 1, invalid audio data or non-PCM data is indicated.

Register 01_H: Transmitter Control Register

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
TXOFF	MCSD	MDAT	MONO	BYPAS	MUTE	VAL	BLSM

MUTE **Transmitter Mute (Defaults to 0)**

When set to 0, the mute function is disabled.

When set to 1, the mute function is enabled, with Channel A and B audio data set to all 0's.

BYPASS **Transmitter Bypass—AES-3 Data Source for the Output Driver (Defaults to 0)**

When set to 0, AES-3 encoded data is taken from the output of the on-chip encoder.

When set to 1, RXP (pin 9) is used as the source for AES-3 encoded data.

MONO **Mono Mode Control (Defaults to 0)**

When set to 0, the transmitter is set to Stereo mode.

When set to 1, the transmitter is set to Mono mode.

MDAT **Data Selection Bit (Defaults to 0)**

(0 = Left Channel, 1 = Right Channel)

When MONO = 0 and MCSD = 0, the MDAT bit is ignored.

When MONO = 0 and MCSD = 1, the MDAT bit is used to select the source for Channel Status data.

When MONO = 1 and MCSD = 0, the MDAT bit is used to select the source for Audio data.

When MONO = 1 and MCSD = 1, the MDAT bit is used to select the source for both Audio and Channel Status data.

MCSD **Channel Status Data Selection (Defaults to 0)**

When set to 0, Channel A data is used for the A sub-frame, while Channel B data is used for the B sub-frame.

When set to 1, use the same channel status data for both A and B sub-frames. Channel status data source is selected using the MDAT bit.

TXOFF **Transmitter Output Disable (Defaults to 0)**

When set to 0, the line driver outputs, TX– (pin 17) and TX+ (pin 18) are enabled.

When set to 1, the line driver outputs are forced to ground.

Register 02_H: Power-Down and Clock Control Register

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
0	0	0	0	RST	CLK1	CLK0	PDN

PDN **Power-Down (Defaults to 1)**

When set to 0, the DIT4192 operates normally.

When set to 1, the DIT4192 is powered down, with the line driver outputs forced to ground.

CLK[1:0] **MCLK Rate Selection**

These bits are used to select the master clock frequency applied to the MCLK input (pin 6).

CLK1	CLK0	MCLK Rate
0	0	128 • f_S
0	1	256 • f_S (default)
1	0	384 • f_S
1	1	512 • f_S

RST **Software Reset (Defaults to 0)**

When set to 0, the DIT4192 operates normally.
When set to 1, the DIT4192 is reset.

Register 03_H: Audio Serial Port Control Register

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
ISYNC	ISCLK	DELAY	JUS	WLEN1	WLEN0	SCLKR	M/S

M/S **Master/Slave Mode (Defaults to 0)**

When set to 0, the audio serial port is set for Slave operation.

When set to 1, the audio serial port is set for Master operation.

SCLKR **Master Mode SCLK Frequency (Defaults to 0)**

When set to 0, the SCLK frequency is set to 64 • f_S.

When set to 1, the SCLK frequency is set to 128 • f_S.

WLEN[1:0] **Audio Data Word Length**

These bits are used to set the audio data word length for both Left and Right channels.

WLEN1	WLEN0	Length
0	0	24 Bits (default)
0	1	20 Bits
1	0	18 Bits
1	1	16 Bits

JUS **Audio Data Justification (Defaults to 0)**

When set to 0, the audio data is Left-Justified with respect to the SYNC edges.

When set to 1, the audio data is Right-Justified with respect to the SYNC edges.

DELAY **Audio Data Delay from the Start of Frame (Defaults to 0)**

This applies primarily to I^2S and DSP frame formats, which use Left-Justified audio data.

When set to 0, audio data starts with the SCLK period immediately following the SYNC edge which starts the frame. This is referred to as a zero SCLK delay.

When set to 1, the audio data starts with the second SCLK period following the SYNC edge which starts the frame. This is referred to as a one SCLK delay. This is used primarily for the I^2S data format.

ISCLK **SCLK Sampling Edge (Defaults to 0)**

When set to 0, audio serial data at SDATA (pin 13) is sampled on rising edge of SCLK.

When set to 1, audio serial data at SDATA (pin 13) is sampled on falling edge of SCLK.

ISYNC **SYNC Polarity (Defaults to 0)**

When set to 0, Left channel data occurs when the SYNC clock is HIGH.

When set to 1, Left channel data occurs when the SYNC clock is LOW.

For both cases, Left channel data always precedes the Right channel data in the audio frame.

Register 04_H: Interrupt Status Register

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
0	0	0	0	0	0	TSLIP	BTI

BTI **Buffer Transfer Interrupt Status—Active High**

When User Access (UA) to Transmitter Access (TA) buffer transfers are enabled, and the BTI interrupt is unmasked, this bit will go HIGH when a UA to TA buffer transfer has completed. This will also cause the $\overline{INT}$ output (pin 22) to be driven Low, indicating that an interrupt has occurred.

TSLIP **Transmitter Source Data Slip Interrupt Status—Active High**

This bit will go HIGH when either a Data Slip or Block Start condition is detected, and the TSLIP interrupt is unmasked. This will also cause the $\overline{INT}$ output (pin 22) to be driven LOW, indicating that an interrupt has occurred. The function of this bit is selected using the BSSL bit in control register 05_H (defaults Data Slip).

The MBTI and MTSLIP bits are used to mask the BTI and TSLIP interrupts. When masked, these interrupt sources are disabled.

Register 05_H: Interrupt Mask Register

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
0	0	0	0	0	BSSL	MTSLIP	MBTI

MBTI **BTI Interrupt Mask. Set to '0' to mask BTI (Defaults to 0).**

MTSLIP **TSLIP Interrupt Mask. Set to '0' to mask TSLIP (Defaults to 0).**

BSSL **TSLIP Interrupt Select (Defaults to 0)**

When set to 0, the Data Slip condition is used to trigger a TSLIP interrupt.

When set to 1, the Block Start condition is used to trigger a TSLIP interrupt.

Register 06_H: Interrupt Mode Register

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
0	0	0	0	TSLIPM1	TSLIPM0	BTIM1	BTIM0

BTIM[1:0] **BTI Interrupt Mode**

TSLIPM[1:0] **TSLIP Interrupt Mode**

These bits are used to select the active state for interrupt operation.

BTIM1 or TSLIPM1	BTIM0 or TSLIPM0	Interrupt Operation
0	0	Rising Edge Active (default)
0	1	Falling Edge Active
1	0	Level Active
1	1	Reserved

BTD **Buffer Transfer Disable (Defaults to 0)**

When set to 0, User Access (UA) to Transmitter Access (TA) Buffer transfers are enabled.

When set to 1, User Access (UA) to Transmitter Access (TA) Buffer transfers are disabled.

Register 07_H: Channel Status Buffer Control Register

bit 7 (MSB)	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0 (LSB)
0	0	0	0	0	0	0	BTD

CHANNEL STATUS DATA BUFFER OPERATION (SOFTWARE MODE ONLY)

The DIT4192 contains two buffers for the channel status data. These are referred to as the Transmitter Access (TA) buffer and the User Access (UA) buffer. Each buffer is 48 bytes long, containing 24 bytes each for channels A and B. The 24 bytes per channel correspond to the channel status block defined in the AES-3 and IEC-60958 specifications. Channel A and B data are interleaved within the buffers, see Tables VII and VIII.

The AES-3 encoder internally accesses the TA buffer to obtain the channel status data that is multiplexed into the AES-3 data stream. The user accesses the UA buffer through the control port in order to update the channel status data when needed. The transfer of data from the UA buffer to the TA buffer is managed internally by the DIT4192, but it may be enabled or disabled by the user via a control register.

The master clock input (MCLK) and the frame synchronization clock input (SYNC) must be active in order to update the channel status buffer in Software mode. When the DIT4192 is initially powered up, the device defaults to power-down mode. When the PDN bit in Register 2 is set to 0 to power up the device, there must be a delay between the time that PDN is set to 0 and the first access to the channel status buffer. This delay allows the SYNC clock to synchronize the AES3 encoder block with the audio serial port. It is recommended that Register 2 be the last control register written in the initialization sequence, followed by a delay (10 milliseconds or longer) before attempting to access the channel status buffer.

UPDATING THE CHANNEL DATA STATUS BUFFER

Updating the channel status data buffer involves disabling and enabling the UA to TA buffer transfer using the BTD bit in control register 07_H. Figure 9 shows the proper flow for updating the buffer.

The BTD bit is normally set to 0, which enables the UA to TA buffer transfer. In order to update the channel status data, the user must write to the UA buffer. To avoid UA to TA data transfer while the UA buffer is being updated, the BTD bit is set to 1, which disables UA to TA buffer transfers. While BTD = 1, the user writes new channel status data to the UA buffer via the control port. Once the UA buffer update is complete, the BTD bit is reset to 0. A new UA to TA buffer transfer will occur during one of the frames 184 through 191,

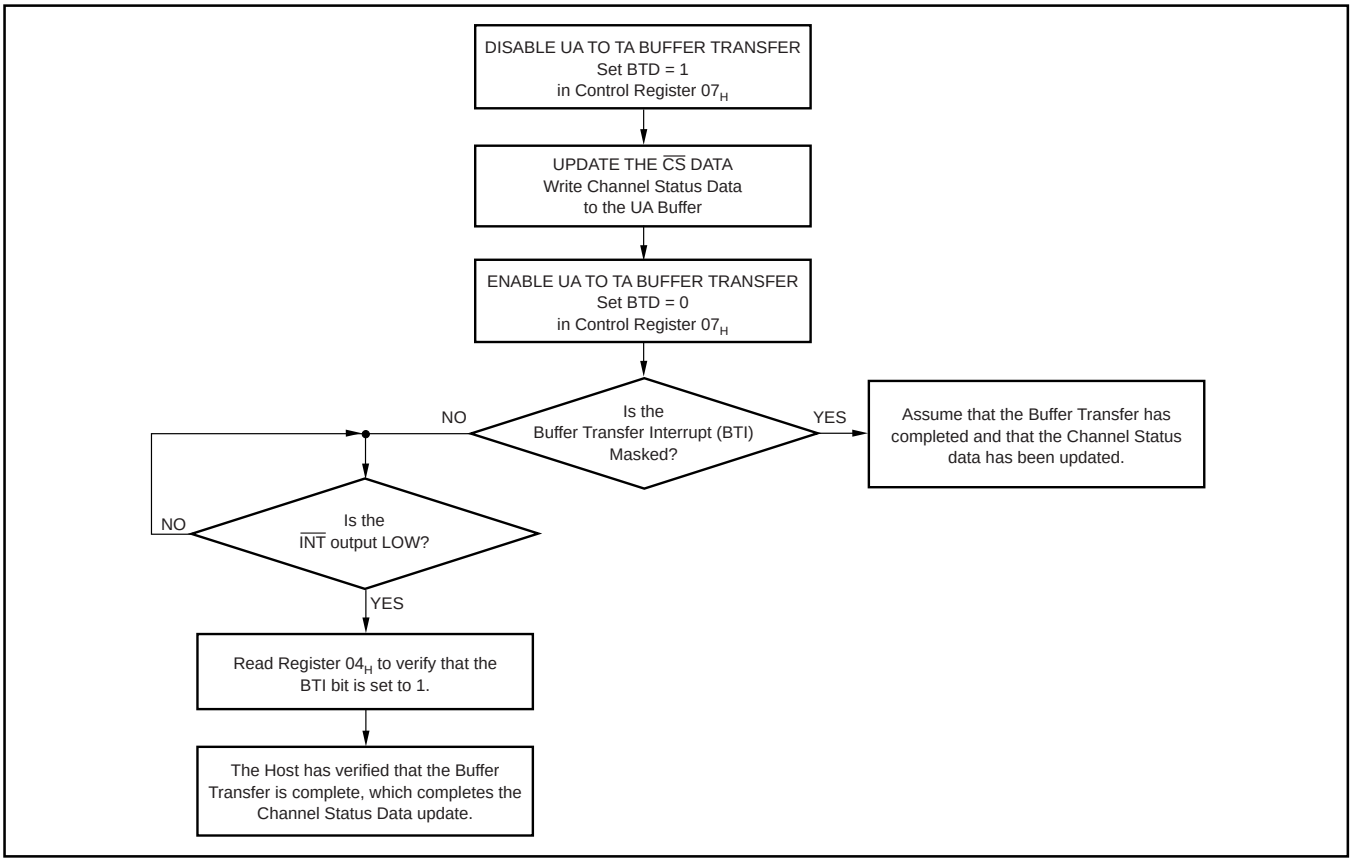


FIGURE 9. Flowchart for Updating the Channel Status Buffer.

ADDRESS	$\overline{CS}$	BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
(HEX)	Byte	MSB							LSB
08	A0	PRO	$\overline{\text{AUDIO}}$	$\overline{\text{EMPH}}$	$\overline{\text{EMPH}}$	$\overline{\text{EMPH}}$	LOCK	f_S	f_S
09	B0	PRO	$\overline{\text{AUDIO}}$	$\overline{\text{EMPH}}$	$\overline{\text{EMPH}}$	$\overline{\text{EMPH}}$	LOCK	f_S	f_S
0A	A1	CH MODE	CH MODE	CH MODE	CH MODE	U BIT MGT	U BIT MGT	U BIT MGT	U BIT MGT
0B	B1	CH MODE	CH MODE	CH MODE	CH MODE	U BIT MGT	U BIT MGT	U BIT MGT	U BIT MGT
0C	A2	AUX	AUX	AUX	WLEN	WLEN	WLEN	reserved	reserved
0D	B2	AUX	AUX	AUX	WLEN	WLEN	WLEN	reserved	reserved
0E	A3	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
0F	B3	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
10	A4	REF	REF	reserved	reserved	reserved	reserved	reserved	reserved
11	B4	REF	REF	reserved	reserved	reserved	reserved	reserved	reserved
12	A5	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
13	B5	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
14	A6	Alphanumeric Channel Origin Data (7-Bit ASCII0) for Channel A							
15	B6	Alphanumeric Channel Origin Data (7-Bit ASCII0) for Channel B							
16	A7	Alphanumeric Channel Origin Data (7-Bit ASCII0) for Channel A							
17	B7	Alphanumeric Channel Origin Data (7-Bit ASCII0) for Channel B							
18	A8	Alphanumeric Channel Origin Data (7-Bit ASCII0) for Channel A							
19	B8	Alphanumeric Channel Origin Data (7-Bit ASCII0) for Channel B							
1A	A9	Alphanumeric Channel Origin Data (7-Bit ASCII0) for Channel A							
1B	B9	Alphanumeric Channel Origin Data (7-Bit ASCII0) for Channel B							
1C	A10	Alphanumeric Channel Destination Data (7-Bit ASCII) for Channel A							
1D	B10	Alphanumeric Channel Destination Data (7-Bit ASCII) for Channel B							
1E	A11	Alphanumeric Channel Destination Data (7-Bit ASCII) for Channel A							
1F	B11	Alphanumeric Channel Destination Data (7-Bit ASCII) for Channel B							
20	A12	Alphanumeric Channel Destination Data (7-Bit ASCII) for Channel A							
21	B12	Alphanumeric Channel Destination Data (7-Bit ASCII) for Channel B							
22	A13	Alphanumeric Channel Destination Data (7-Bit ASCII) for Channel A							
23	B13	Alphanumeric Channel Destination Data (7-Bit ASCII) for Channel B							
24	A14	Local Sample Address Code (32-Bit Binary) for Channel A							
25	B14	Local Sample Address Code (32-Bit Binary) for Channel B							
26	A15	Local Sample Address Code (32-Bit Binary) for Channel A							
27	B15	Local Sample Address Code (32-Bit Binary) for Channel B							
28	A16	Local Sample Address Code (32-Bit Binary) for Channel A							
29	B16	Local Sample Address Code (32-Bit Binary) for Channel B							
2A	A17	Local Sample Address Code (32-Bit Binary) for Channel A							
2B	B17	Local Sample Address Code (32-Bit Binary) for Channel B							
2C	A18	Time of Day Code (32-Bit Binary) for Channel A							
2D	B18	Time of Day Code (32-Bit Binary) for Channel B							
2E	A19	Time of Day Code (32-Bit Binary) for Channel A							
2F	B19	Time of Day Code (32-Bit Binary) for Channel B							
30	A20	Time of Day Code (32-Bit Binary) for Channel A							
31	B20	Time of Day Code (32-Bit Binary) for Channel B							
32	A21	Time of Day Code (32-Bit Binary) for Channel A							
33	B21	Time of Day Code (32-Bit Binary) for Channel B							
34	A22	reserved	reserved	reserved	reserved	Rel Flags	Rel Flags	Rel Flags	Rel Flags
35	B22	reserved	reserved	reserved	reserved	Rel Flags	Rel Flags	Rel Flags	Rel Flags
36	A23	CRC Check Character for Channel A							
37	B23	CRC Check Character for Channel B							

TABLE VII. Channel Status Buffer Map for Professional Mode (PRO = 1).

ADDRESS	$\overline{CS}$	BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
(HEX)	Byte	MSB							LSB
8	A0	PRO = 0	$\overline{AUDIO}$	COPY	$\overline{EMPH}$	$\overline{EMPH}$	$\overline{EMPH}$	MODE	MODE
09	B0	PRO = 0	$\overline{AUDIO}$	COPY	$\overline{EMPH}$	$\overline{EMPH}$	$\overline{EMPH}$	MODE	MODE
0A	A1	CAT CODE	CAT CODE	CAT CODE	CAT CODE	CAT CODE	CAT CODE	CAT CODE	L
0B	B1	CAT CODE	CAT CODE	CAT CODE	CAT CODE	CAT CODE	CAT CODE	CAT CODE	L
0C	A2	SOURCE	SOURCE	SOURCE	SOURCE	CH NUM	CH NUM	CH NUM	CH NUM
0D	B2	SOURCE	SOURCE	SOURCE	SOURCE	CH NUM	CH NUM	CH NUM	CH NUM
0E	A3	f_S	f_S	f_S	f_S	CLK ACC	CLK ACC	reserved	reserved
0F	B3	f_S	f_S	f_S	f_S	CLK ACC	CLK ACC	reserved	reserved
10	A4	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
11	B4	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
12	A5	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
13	B5	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
14	A6	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
15	B6	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
16	A7	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
17	B7	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
18	A8	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
19	B8	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
1A	A9	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
1B	B9	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
1C	A10	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
1D	B10	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
1E	A11	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
1F	B11	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
20	A12	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
21	B12	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
22	A13	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
23	B13	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
24	A14	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
25	B14	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
26	A15	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
27	B15	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
28	A16	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
29	B16	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
2A	A17	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
2B	B17	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
2C	A18	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
2D	B18	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
2E	A19	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
2F	B19	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
30	A20	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
31	B20	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
32	A21	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
33	B21	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
34	A22	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
35	B22	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
36	A23	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
37	B23	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved

TABLE VIII. Channel Status Buffer for Consumer Mode (PRO = 0).

whichever is the first frame to occur after the BTD bit is reset to 0. Once the UA to TA buffer transfer is completed, the buffer transfer interrupt (BTI) will occur, as long as it is unmasked.

The transmitter will ignore any attempt to access the UA buffer during a UA to TA buffer transfer. In addition, the BTD bit may be set to 1 to stop a UA to TA buffer transfer that maybe in progress, if so desired.

CHANNEL STATUS BUFFER MAP

The channel status buffer is organized in accordance with the AES-3 and IEC-60958 standards. See Table VII for the memory map for the UA channel status data buffer for Professional mode. Table VIII shows the memory map for the UA channel status data buffer for Consumer mode.

INTERRUPT SOURCES (SOFTWARE MODE ONLY)

The DIT4192 can be programmed to generate interrupts for up to three predefined conditions. The interrupt output, $\overline{INT}$ (pin 22), is set low when a valid interrupt occurs. The interrupt status register, 04_H, is then read to determine the source of the interrupt. Status register bits and the $\overline{INT}$ output pin remain active until the status register is read. Once read, status bits are cleared and the $\overline{INT}$ pin is pulled high by an external pull-up resistor to V_{IO}.

Interrupts may be masked using control register 05_H. When masked, the interrupt mechanism associated with a particular status bit is disabled.

CHANNEL STATUS BUFFER TRANSFER INTERRUPT

This interrupt occurs when a channel status buffer transfer has been completed. The buffer transfer process was described in detail in the previous section of this data sheet. This interrupt may be used by the host to trigger an event to occur after a channel status buffer update. The BTI bit in status register 04_H is used to indicate the occurrence of the buffer transfer. The BTI bit, like all other status bits, is active high and remains set until the status register is read.

DATA SLIP AND BLOCK START INTERRUPTS

Unlike the BTI interrupt, which has only one function, the TSLIP interrupt can be set to one of two modes. This is accomplished using the BSSL bit in control register 05_H. When BSSL = 0, the TSLIP interrupt is set to indicate a data slip condition. When BSSL = 1, the TSLIP interrupt is set to indicate a block start condition. The TSLIP bit, like all other status bits, is active high and remains set until the status register is read.

A data slip condition may occur in cases where the master clock, MCLK (pin 6), is asynchronous to the audio data source. When BSSL = 0, the TSLIP bit will be set to 1 every time a data sample is dropped or repeated.

A block start condition occurs when a block start signal is generated either internally by the DIT4192, or when an external block start is received at the BLS input (pin 25).

APPLICATIONS INFORMATION

This section provides practical information pertinent for designing the DIT4192 into a target application. Circuit schematics are provided as needed.

TYPICAL APPLICATION DIAGRAMS

Figures 10 and 11 illustrate the typical application schematics for the DIT4192 when used in Software and Hardware modes. Figure 10 shows a typical Software mode application, where a microprocessor or DSP interface is used to communicate with the DIT4192 via the serial control port. See Figure 11 for a typical Hardware mode configuration, where the control pins are either hardwired or driven by digital logic in a stand-alone application.

The recommended component values for power-supply bypass capacitors are shown in Figures 10 and 11. These capacitors should be located as close to the DIT4192 power-supply pins as physically possible.

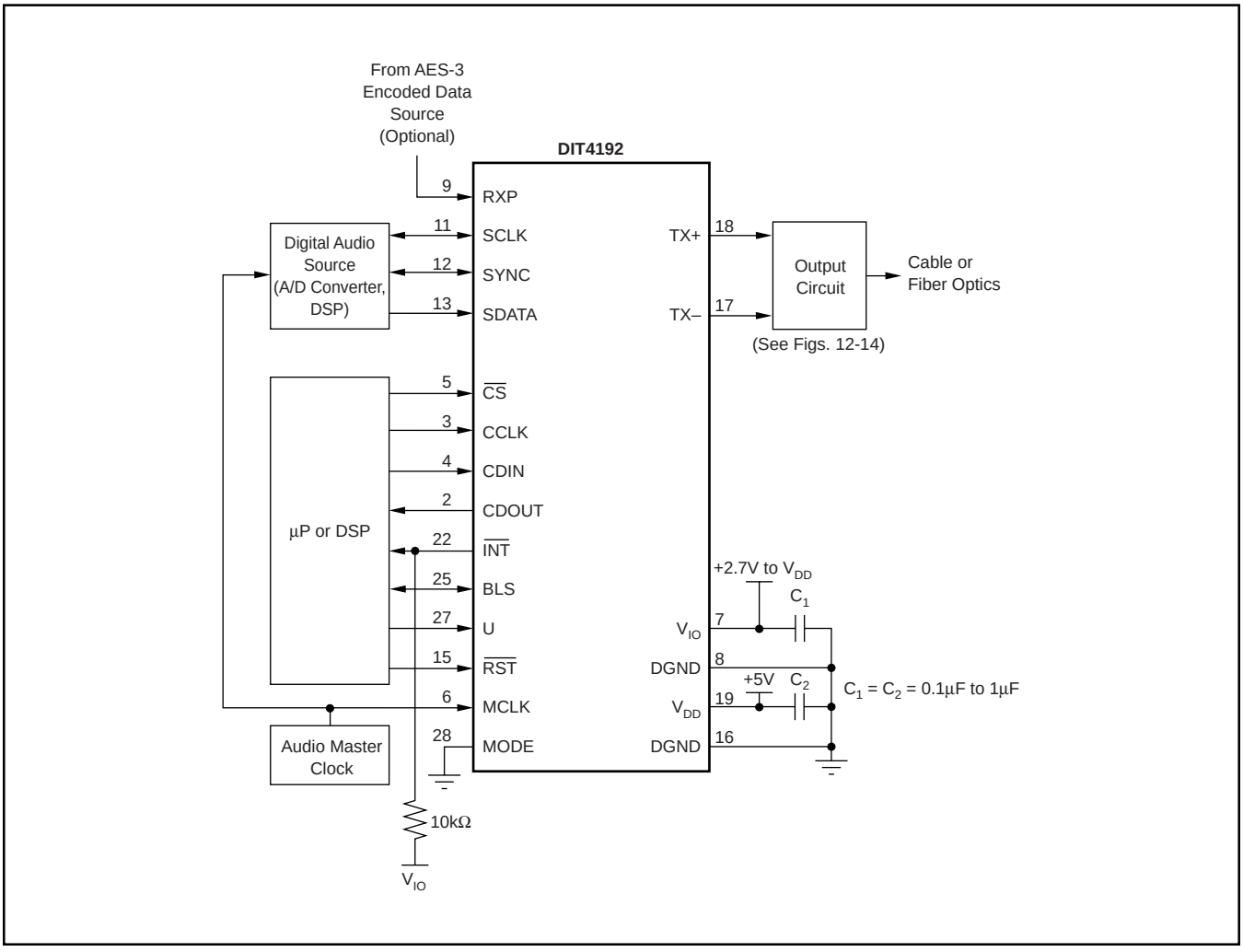


FIGURE 10. Typical Circuit Configuration, Software Mode.

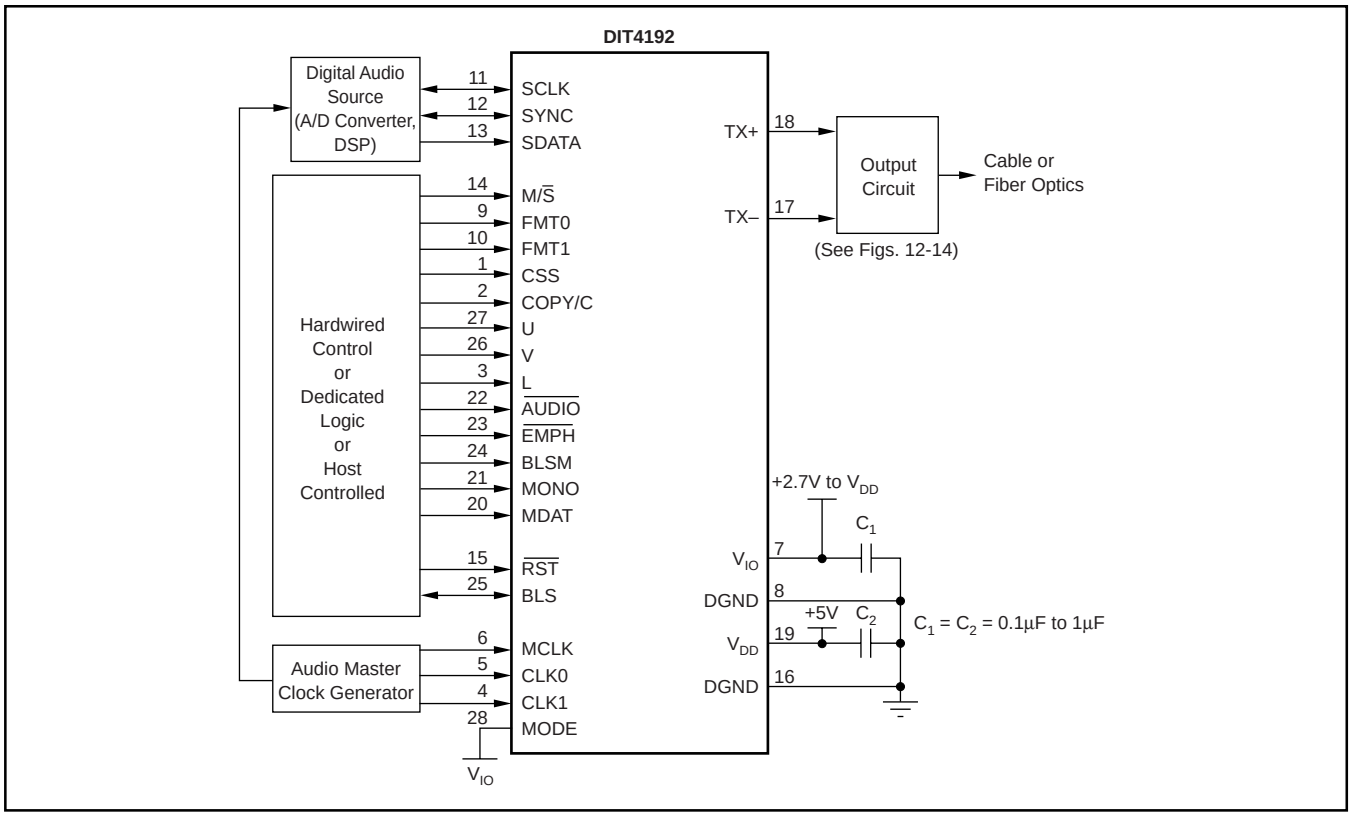


FIGURE 11. Typical Circuit Configuration, Hardware Mode.

The line driver outputs may be connected to cable or fiber optic transmission media in the target application. Figures 12 and 13 show typical connections for driving either balanced twisted-pair or unbalanced coaxial cable. Either of these connections will support rates up to 192kHz.

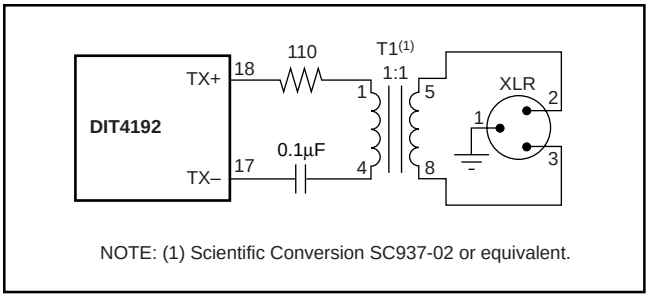


FIGURE 12. Recommended Transmitter Output Circuit for Balanced, 110Ω Twisted-Pair Transmission.

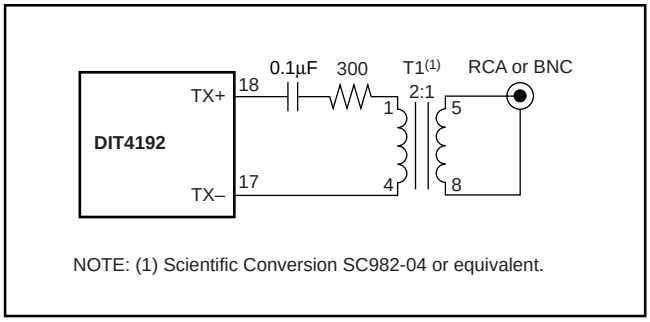


FIGURE 13. Recommended Transmitter Output Circuit for Unbalanced, 75Ω Coaxial Cable Transmission.

Figure 14 illustrates the connection to an optical transmitter module, used primarily in consumer applications, such as CD or DVD players. The optical transmitter data rate is limited to 6Mb/s, so it will not support 192kHz data rates. The optical interface is typically reserved for lower rate transmission, such as 44.1kHz or 48kHz.

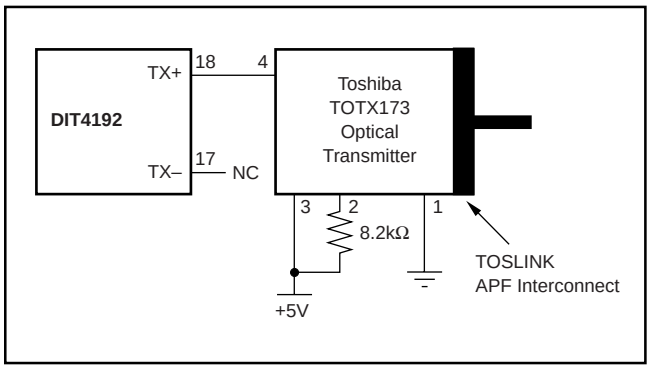


FIGURE 14. Recommended Transmitter Output Circuit for TOSLINK Optical Transmission Over All Plastic Fiber (APF).

DUAL-WIRE OPERATION USING MONO MODE

In order to support stereo 192kHz transmission for legacy systems, which utilize AES-3 receivers that operate up to a maximum of 96kHz, it is necessary to use two DIT4192 transmitters in what is referred to as a Dual-Wire configuration. Each transmitter carries data for only one channel in this configuration.

Dual-Wire operation requires that each DIT4192 operates in Mono mode, which is supported in both Software and Hardware control modes. In Mono mode, the DIT4192 transmits two consecutive samples of a single channel for both the Channel A and Channel B sub-frames, effectively doubling the sampling rate. The audio serial port channel used for sampling audio and channel status data is selectable in both Software and Hardware control modes.

In Software mode, the MONO, MDAT, and MCSD bits in control register 01_H are used to select mono mode, as well as the source channel for audio and channel status data. Refer to the register definition for details regarding the setting of these bits.

In Hardware mode, the MONO (pin 21) and MDAT (pin 20) inputs are used to enable mono mode, as well as selecting the source channel for audio and channel status data. Table IX shows the available options for MONO and MDAT selection. Figure 15 illustrates a simple Hardware mode configuration for implementing Dual-Channel operation using two DIT4192 transmitters.

INPUT	FUNCTION		
MONO	**Stereo/Mono Mode Selection**		
	MONO	Status	
	0	Stereo Mode	
	1	Mono Mode	
MDAT	**Mono Mode Audio and Channel Status Data Selection**		
	MDAT	Status	
	0	Source is Left Channel for Audio data, and Channel A for $\overline{CS}$ data.	
	1	Source is Right Channel for Audio data, and Channel B for $\overline{CS}$ data.	

TABLE IX. Mono Mode Configuration Settings for Hardware Mode Operation.

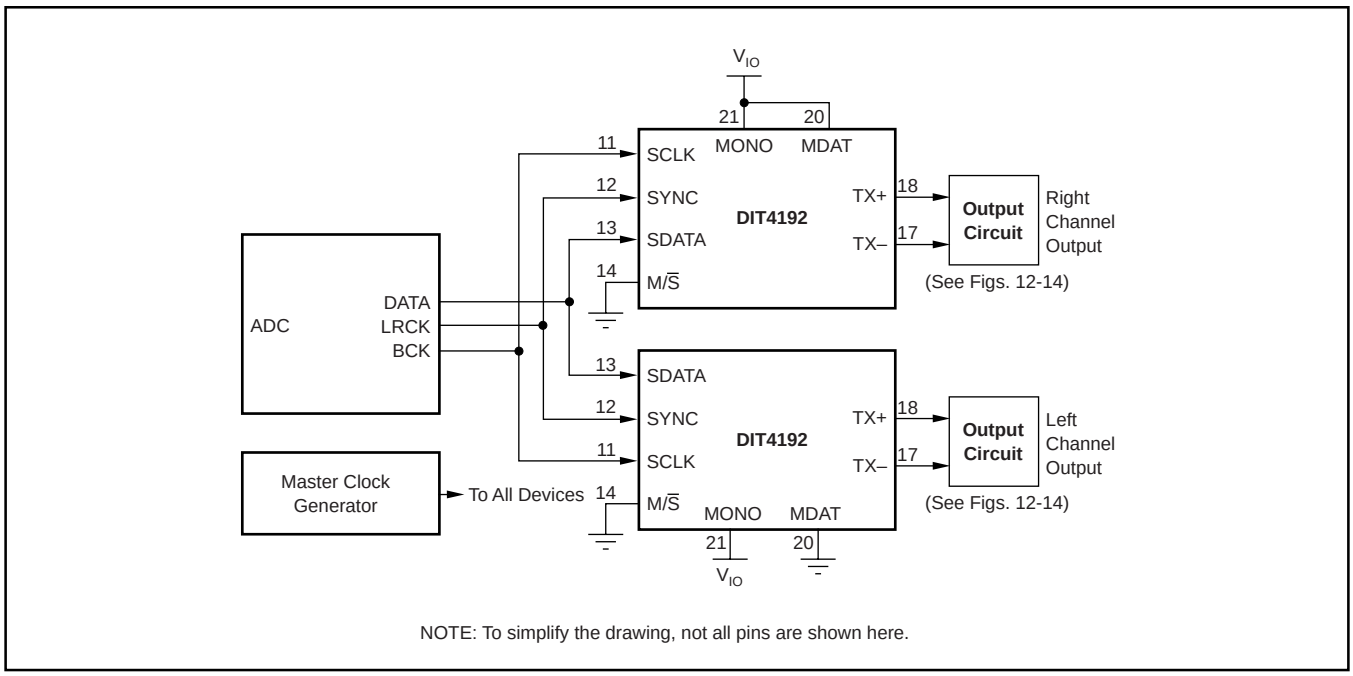
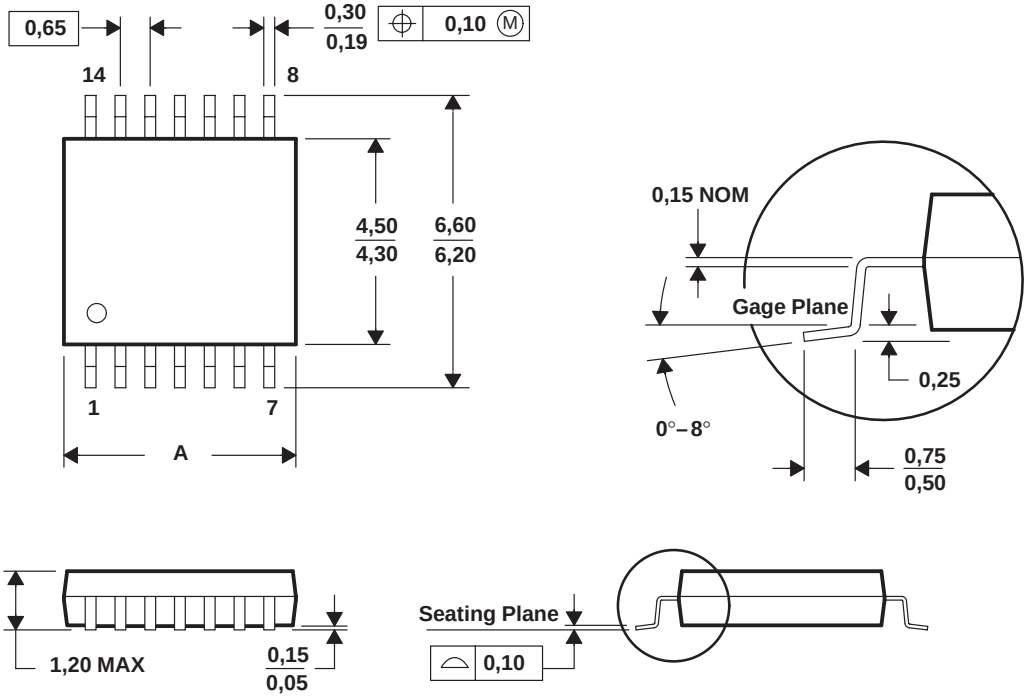


FIGURE 15. Hardware Mode Example for Dual-Channel Transmitter Operation.

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DIT4192IPW	ACTIVE	TSSOP	PW	28	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DIT4192I	Samples
DIT4192IPWR	ACTIVE	TSSOP	PW	28	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DIT4192I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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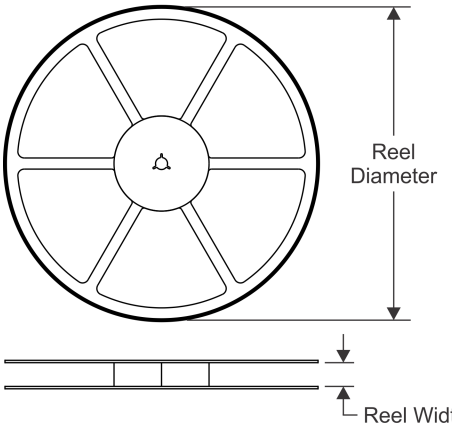
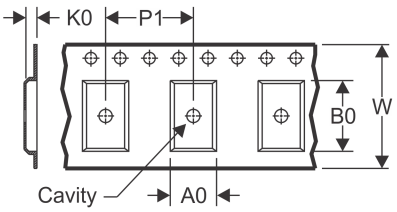
TAPE AND REEL INFORMATION

REEL DIMENSIONS

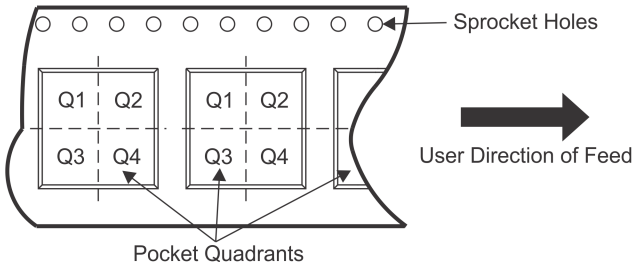


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

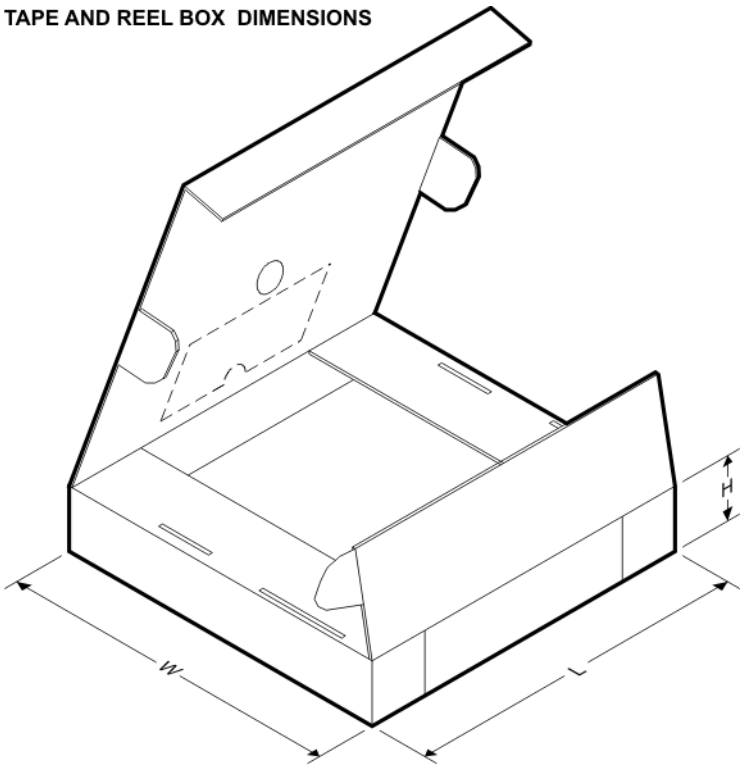
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DIT4192IPWR	TSSOP	PW	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

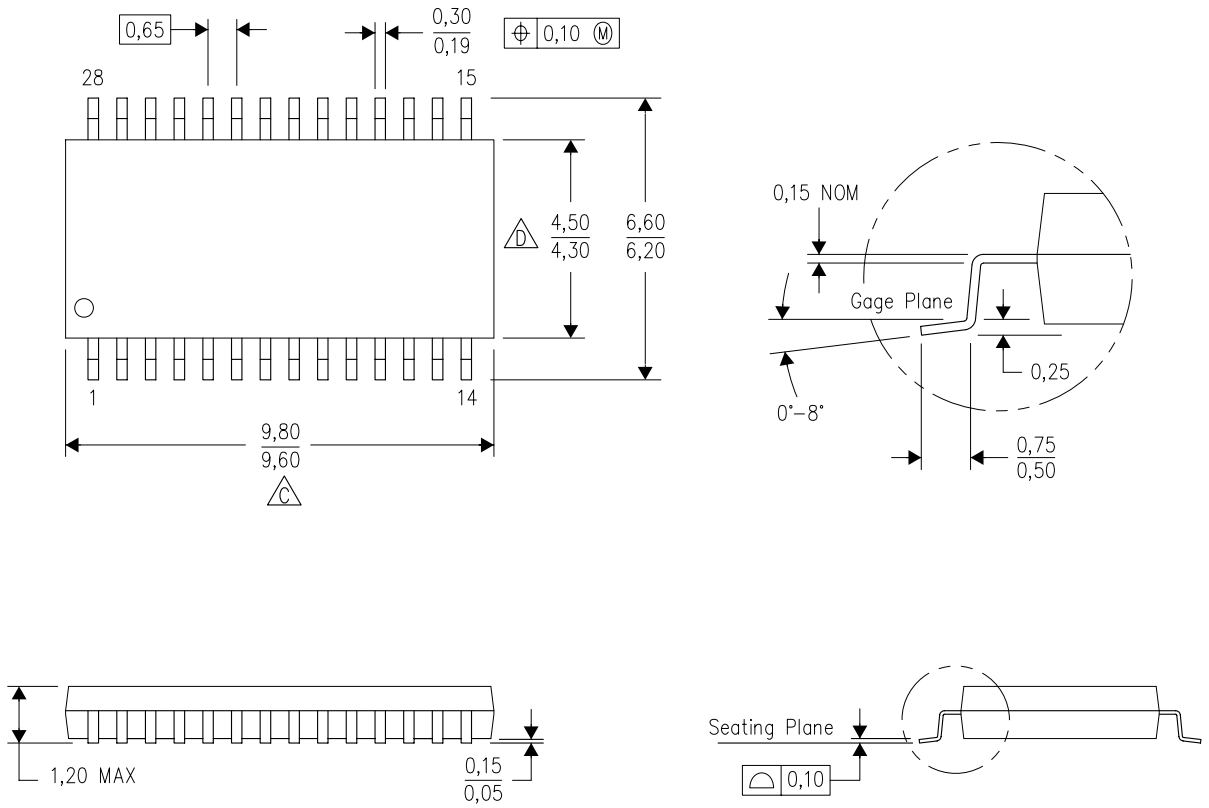
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DIT4192IPWR	TSSOP	PW	28	2000	350.0	350.0	43.0

PW (R–PDSO–G28) PLASTIC SMALL OUTLINE



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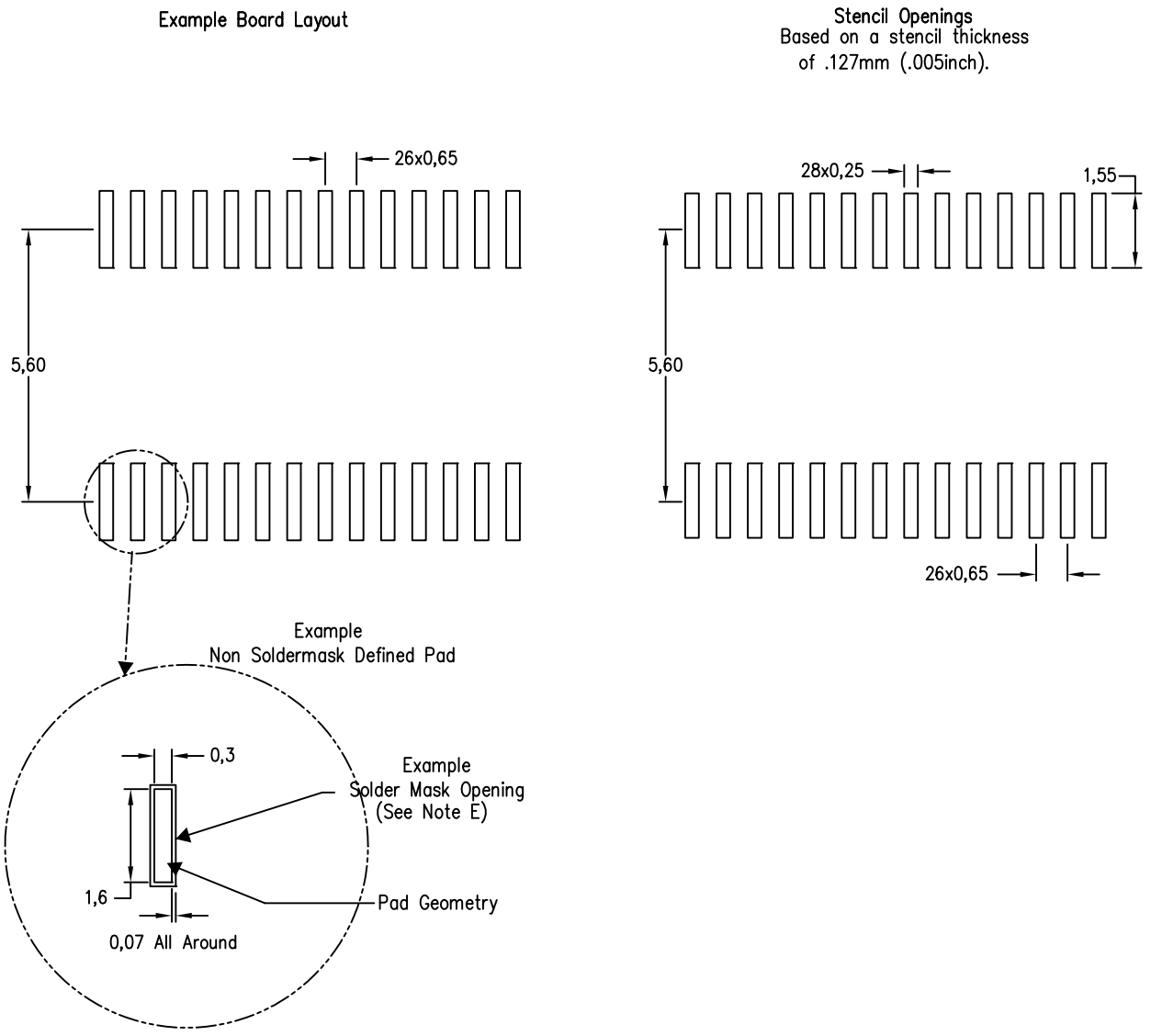
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G28) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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