Design Idea DI-53
DPA-Switch™
50 W DC-DC Dual Output Converter

Application	Device	Power Output	Input Voltage	Output Voltage	Topology
Telecom	DPA425R	50 W	36-75 VDC	5 V & 3.3 V	Forward Sync. Rect.

Design Highlights

- High efficiency: 90% at 36 VDC using synchronous rectification
- Dual output with tight cross-regulation ±4% from zero to full load on both outputs
- Output overload, open loop and thermal protection
- 300 kHz switching frequency to allow sufficient transformer reset time with sync rectification
- 3.85 x 2.25 x 0.6 inch (~9.62 W/in^3)

Operation

DPA-Switch greatly simplifies the design compared to a discrete implementation. This design uses a coupled output inductor and synchronous rectification to achieve excellent cross-regulation and high efficiency.

Resistor R1 programs the under/over voltages and linearly reduces the maximum duty cycle with input voltage to prevent core saturation during load transients. Components D1, D2, C9 and L2 implement a resonant clamp circuit to catch and recirculate the transformer leakage energy during normal operation, with Zener VR1 providing absolute clamping for transient conditions.

Capacitor C21 charges the gate of Q2, the forward synchronous rectifier MOSFET of the 5 V output. Resistor R21 limits gate oscillation and R22 provides gate pull-down. Zener diode VR20 limits the Q2 gate voltage during conduction and also reverse charges C21 during the Q2 off time. The same drive technique is used for the forward synchronous rectifier MOSFET (Q4) of the 3.3 V output (with C22, R24, R25, and VR21).

MOSFETs Q1 and Q3 are driven via resistors R23 and R26 from the transformer (T1) reset voltage and operate only when Q2 and Q4 are off. Diodes D20 and D21 provide a conduction path for the output inductor (L4) current when the transformer reset is complete.

A winding on the coupled inductor L4, along with diode D4 and capacitor C9, provide the *DPA-Switch* bias voltage.

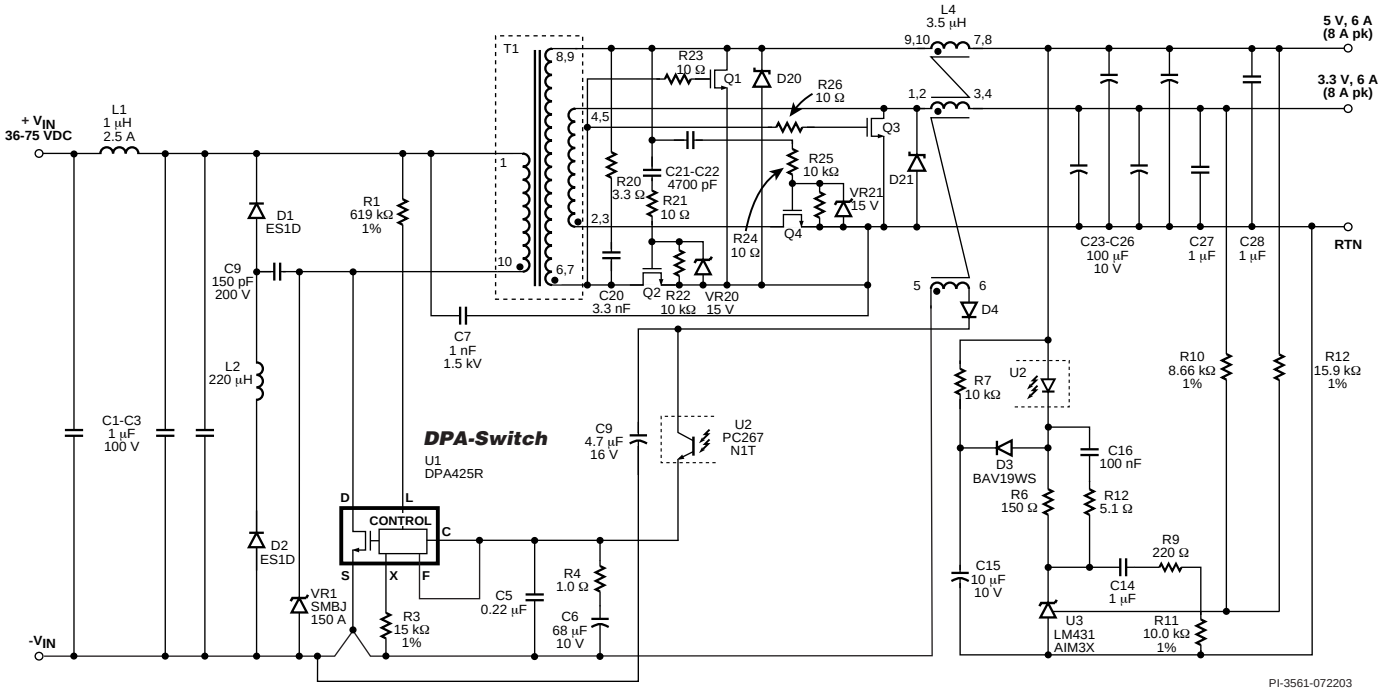


Figure 1. DPA425R - 50 W, 5 V, 6 A and 3.3 V, 6 A DC-DC Converter.

Key Design Points

- Capacitors C20, C_{Q1gs} and C_{Q3gs} will all load transformer reset. Choose values to ensure sufficient reset at low line and safe maximum drain voltage at high line. Also use 300 kHz operation for longest reset time.
- Capacitors C21 and C22 will capacitively drive MOSFET gate capacitances C_{Q2gs} and C_{Q4gs} (respectively). C21 and C22 should be chosen to ensure that gate drive voltage attains turn-on threshold of MOSFET (Vg_{TH}), at worst case conditions (low line for forward MOSFET).
- Reduce transformer leakage inductance by filling each winding layer across the entire width of the bobbin.
- Higher efficiency (+1%) can be acheived by using a DPA426R and increasing R3 to reduce the internal current limit.

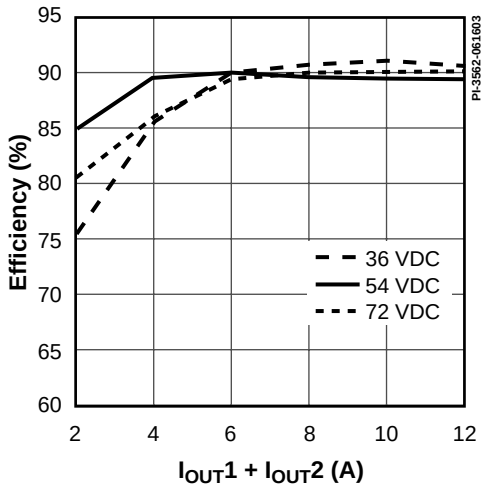


Figure 2. Efficiency vs. Output Power.

TRANSFORMER PARAMETERS	
Core Material	Ferroxcube P/N: EFD25-3F3, ungapped
Bobbin	10-pin EFD25 surface mount bobbin
Winding Details	Primary 11T, 4 x 28 AWG 3.3 V 2T, 2 x 4 x 26 AWG 5 V 3T, 2 x 4 x 26 AWG
Winding Order and Pin Numbers	5 V (6, 7-8, 9), Primary (1-10), 3.3 V (4.5-2.3)
Primary Inductance	250 µH ±25% at 300 kHz
Primary Resonant Frequency	3.8 MHz (minimum)
Leakage Inductance	0.8 µH (maximum)

Table 1. Transformer Design Parameters.

INDUCTOR PARAMETERS	
Core Material	Ferroxcube P/N: EFD25-3F3 ungapped
Bobbin	10-pin EFD20 surface mount bobbin
Winding Details	5 V 6T, 2 x 4 x 26 AWG 3.3 V 4T, 2 x 4 x 26 AWG Bias 12T, 1 x 30 TIW
Winding Order and Pin Numbers	5 V (9, 10-7, 8), 3.3 V (1, 2-3, 4), Bias (FL1-FL2)
Inductance	Pin (1, 2-3, 4): 3.5 µH ±10% at 300 kHz

Table 1. Inductor Design Parameters.

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