Single 16-Ch/Differential 8-Ch CMOS Analog Multiplexers

(Obsolete for non-hermetic. Use DG406/407 as pin-for-pin replacements.)

FEATURES

- Low On-Resistance: 240 Ω
- TTL and CMOS Logic Compatible
- Low Power: 30 mW
- Break-Before-Make Switching
- 44-V Power Supply Rating
- Transition Time: 600 ns

BENEFITS

- Easily Interfaced
- Low Power Consumption
- Low System Crosstalk
- Wide Analog Signal Range

APPLICATIONS

- Communication Systems
- ATE
- Data Acquisition Systems
- Audio Signal Routing and Multiplexing
- Medical Instrumentation

MIL QUALIFIED

DESCRIPTION

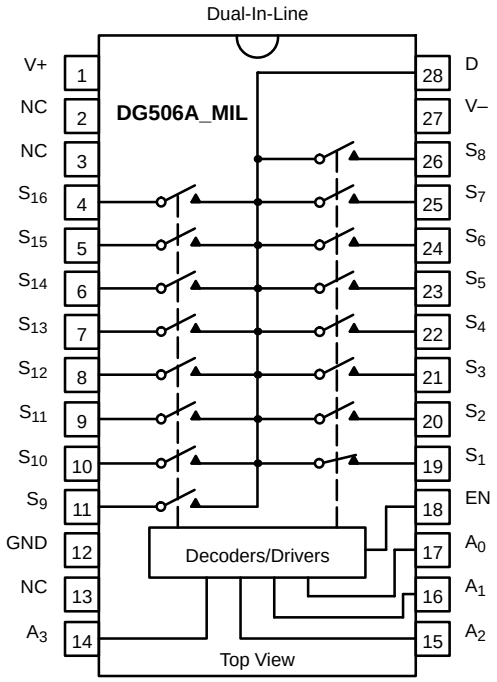
A channel in the on state conducts current equally well in both directions. In the off state each channel blocks voltages up to the power supply rails, normally 30 V peak-to-peak. An enable (EN) function allows for device selection when several multiplexers are used. All control inputs, address (A_X) and enable (EN) are TTL or CMOS compatible over the full specified operating temperature range.

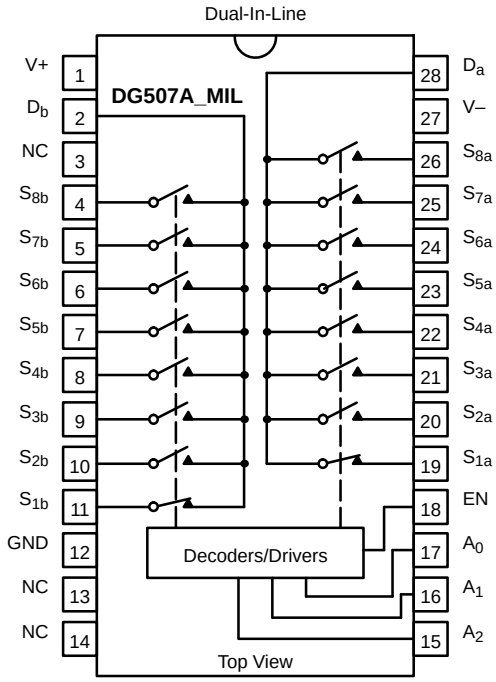
The DG506A_MIL/507A_MIL are fabricated in the Vishay Siliconix PLUS-40 process, which includes improved ESD protection for ruggedness. An epitaxial layer prevents latch up.

The DG506A_MIL/507A_MIL are available in hermetic packages. For plastic packages, use the DG406/407 as pin-for-pin replacements.

For wideband/video multiplexing, the DG536 is recommended.

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION





TRUTH TABLES AND ORDERING INFORMATION

TRUTH TABLE — DG506A_MIL

A_3	A_2	A_1	A_0	EN	On Switch
X	X	X	X	0	None
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16

ORDERING INFORMATION — DG506A_MIL

Temp Range	Package	Part Number
–55 to 125°C	28-Pin CerDIP	DG506AAK
		DG506AAK/883
	28-Pin Sidebraze	JM38510/19001BXC
	LCC-28*	DG506AAZ/883

*Block Diagram and Pin Configuration not shown.

TRUTH TABLE — DG507A_MIL

A_2	A_1	A_0	EN	On Switch
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

Logic “0” = $V_{AL} \leq 0.8$ V
Logic “1” = $V_{AH} \geq 2.4$ V
X = Don’t Care

ORDERING INFORMATION — DG507A_MIL

Temp Range	Package	Part Number
–55 to 125°C	28-Pin CerDIP	DG507AAK
		DG507AAK/883
	28-Pin Sidebraze	JM38510/19003BXC
	28-Pin LCC	DG507AAZ/883

ABSOLUTE MAXIMUM RATINGS

Voltage Referenced to V–
V+ . . . . . 44 V
GND . . . . . 25 V
Digital Inputs[a], V_S, V_D . . . . . (V–) –2 V to (V+) +2 V or 20 mA, whichever occurs first
Current (Any Terminal, Except S or D) . . . . . 30 mA
Continuous Current, S or D . . . . . 20 mA
Peak Current, S or D
(Pulsed at 1 ms, 10% Duty Cycle Max) . . . . . 40 mA
Storage Temperature (CerDIP) . . . . . –65 to 150°C
(Plastic DIP) . . . . . –65 to 125°C

Power Dissipation (Package)[b]
28-Pin CerDIP and Sidebraze . . . . . 1200 mW
28-Pin PLCC[NO TAG] . . . . . 1200 mW
LCC-20,28[c] . . . . . 1000 mW

Notes:
a. Signals on S_X, D_X or IN_X exceeding V+ or V– will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads soldered or welded to PC board.
c. Derate 14 mW/°C above 75°C.

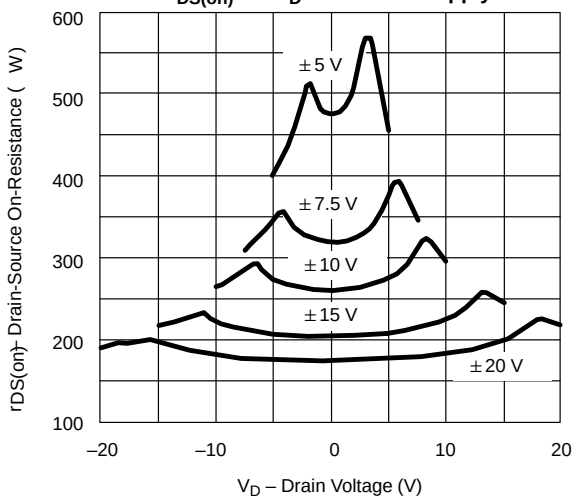
SPECIFICATIONS[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V– = –15 V V_{IN} = 2.4 V, 0.8 V[f]		Temp[b]	A Suffix –55 to 125°C Min[d]	Typ[c]	Max[d]	Unit
Analog Switch								
Analog Signal Range[e]	V_{ANALOG}			Full	–15		15	V
Drain-Source On-Resistance	$r_{DS(on)}$	V_D = ±10 V, I_S = –200 µA		Room Full		240	400 500	Ω
$r_{DS(on)}$ Matching[g]	$\Delta r_{DS(on)}$	–10 V < V_S < 10 V		Room		6		%
Source Off Leakage Current	$I_{S(off)}$	V_S = ±10 V, V_D = ∓10 V V_{EN} = 0 V		Room Full	–1 –50		1 50	nA
Drain Off Leakage Current	$I_{D(off)}$	V_D = ∓10 V V_S = ±10 V V_{EN} = 0 V	DG506A_MIL	Room Full	–10 –300		10 300	
			DG507A_MIL	Room Full	–5 –200		5 200	
Drain On Leakage Current	$I_{D(on)}$	V_S = V_D = ±10 V	DG506A_MIL	Room Full	–10 –300		10 300	
			DG507A_MIL	Room Full	–5 –200		5 200	
Digital Control								
Logic Input Current Input Voltage High	I_{AH}	V_A = 2.4 V		Room Full	–10 –30			µA
		V_A = 15 V		Room Full			10 30	
Logic Input Current Input Voltage Low	I_{AL}	V_{EN} = 0 V, 2.4 V, V_A = 0 V		Room Full	–10 –30			
Dynamic Characteristics								
Transition Time	t_{TRANS}	See Figure 2		Room		0.6	1.0	µs
Break-Before-Make Time	t_{OPEN}	See Figure 4		Room		0.2		
Enable Turn-On Time	$t_{ON(EN)}$	See Figure 3		Room		1	1.5	
Enable Turn-Off Time	$t_{OFF(EN)}$			Room		0.4	1.0	
Charge Injection	Q			Room		6		pC
Off Isolation[h]	OIRR	V_{EN} = 0 V, R_L = 1 kΩ, C_L = 15 pF V_S = 7 V_{RMS}, f = 500 kHz		Room		68		dB
Source Off Capacitance	$C_{S(off)}$	V_{EN} = 0 V, V_S = 0 V, f = 140 kHz		Room		6		pF
Drain Off Capacitance	$C_{D(off)}$	V_{EN} = 0 V V_D = 0 V f = 140 kHz	DG506A_MIL	Room		45		
			DG507A_MIL	Room		23		
Power Supplies								
Positive Supply Current	I+	V_{EN} = 0 V, V_A = 0 V		Room		1.3	2.4	mA
Negative Supply Current	I–			Room	–1.5	–0.7		

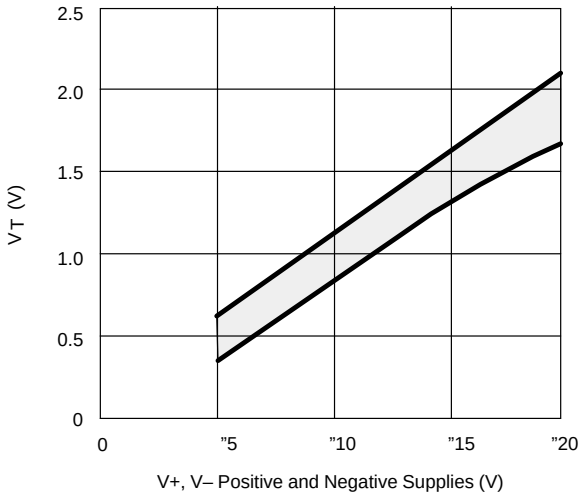
Notes:
a. Refer to PROCESS OPTION FLOWCHART.
b. Room = 25°C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
e. Guaranteed by design, not subject to production test.
f. V_{IN} = input voltage to perform proper function.
g. $\Delta r_{DS(on)} = \left(\frac{r_{DS(on)}MAX - r_{DS(on)}MIN}{r_{DS(on)}AVE} \right)$
h. Off isolation = 20 log $\frac{V_D}{V_S}$, V_S = input to off switch, V_D = output due to V_S.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

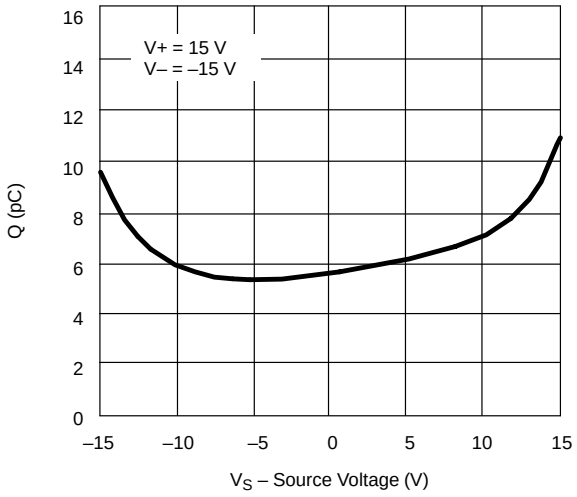
$r_{DS(on)}$ vs. V_D and Power Supply



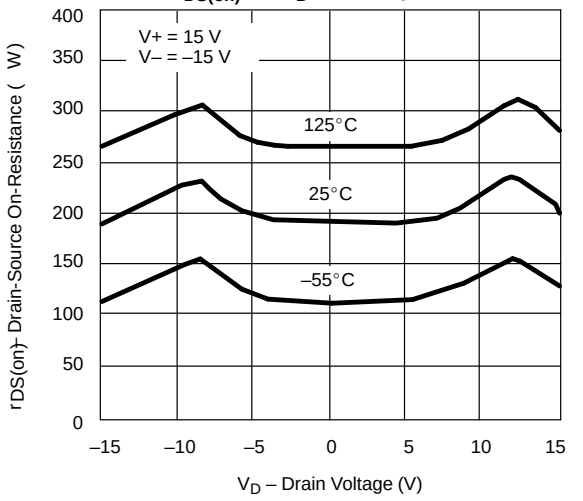
Input Switching Threshold vs. V+ and V– Supply Voltages



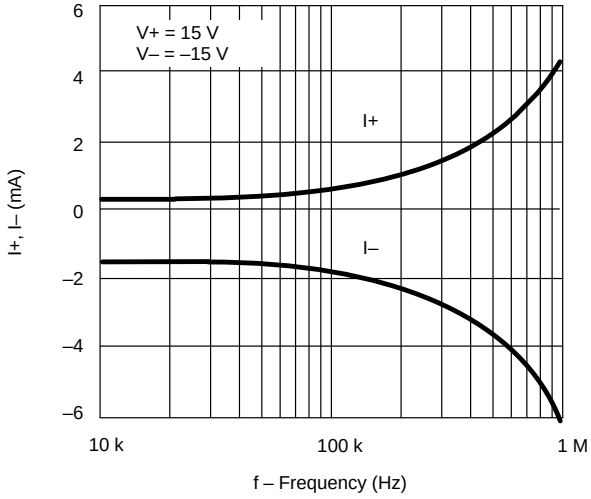
Charge Injection vs. Analog Voltage



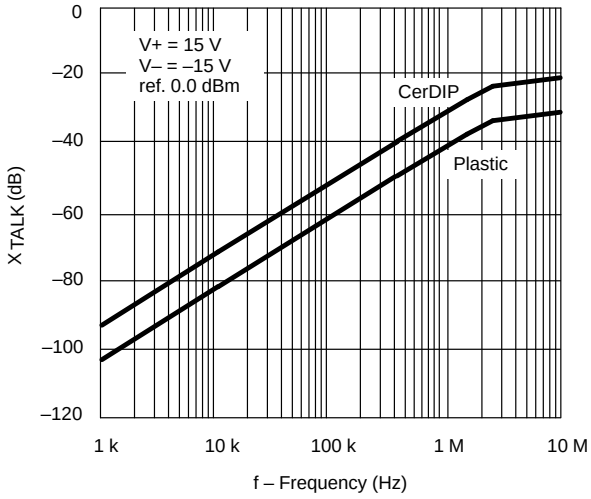
$r_{DS(on)}$ vs. V_D and Temperature



Supply Current vs. Switching Frequency

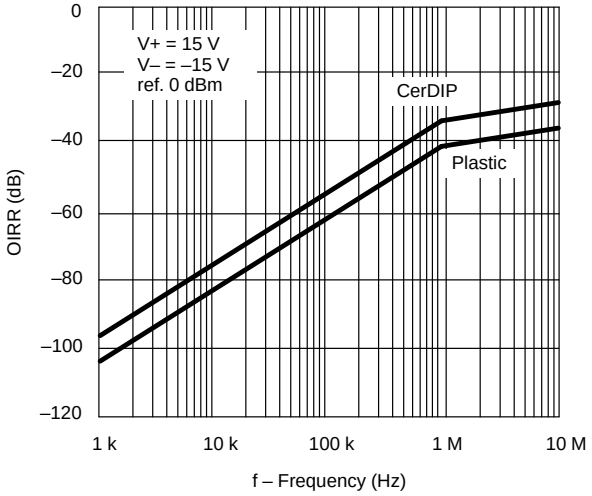


Crosstalk vs. Frequency

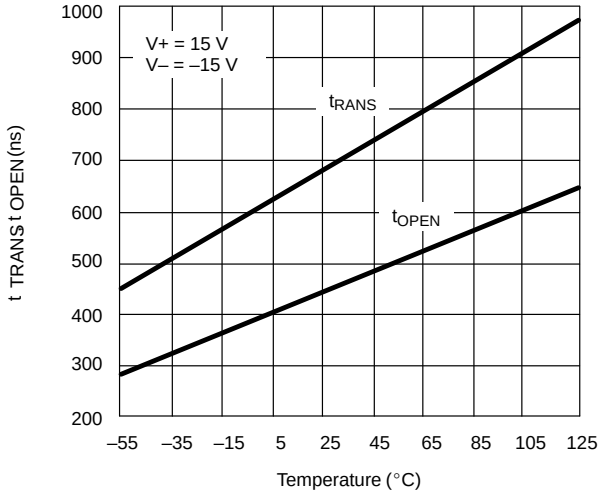


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

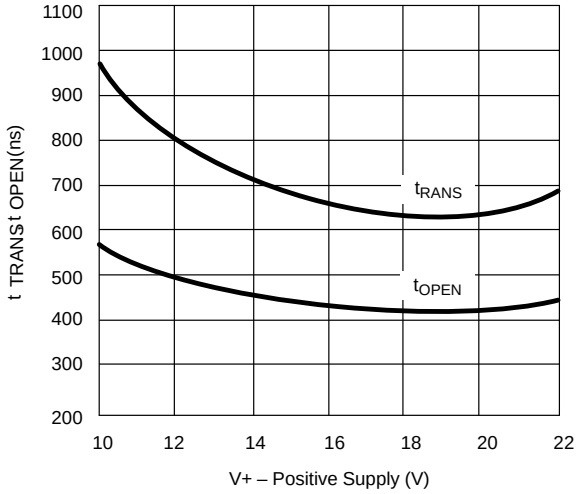
Off Isolation vs. Frequency



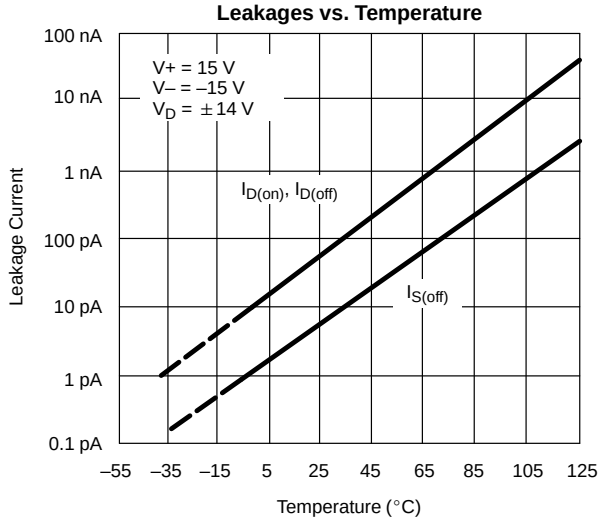
Switching Time vs. Temperature



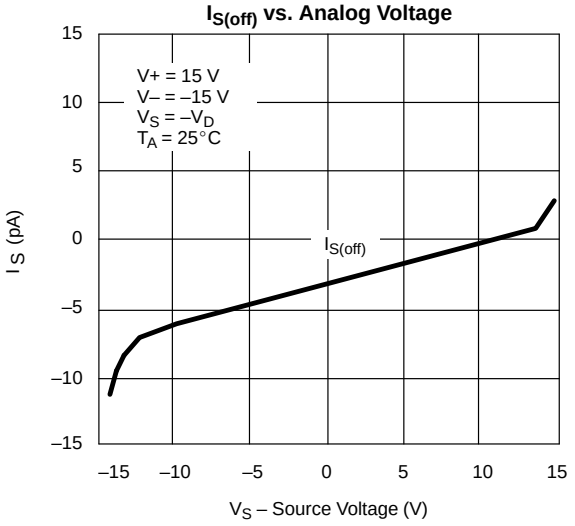
Switching Time vs. Positive Supply Voltage



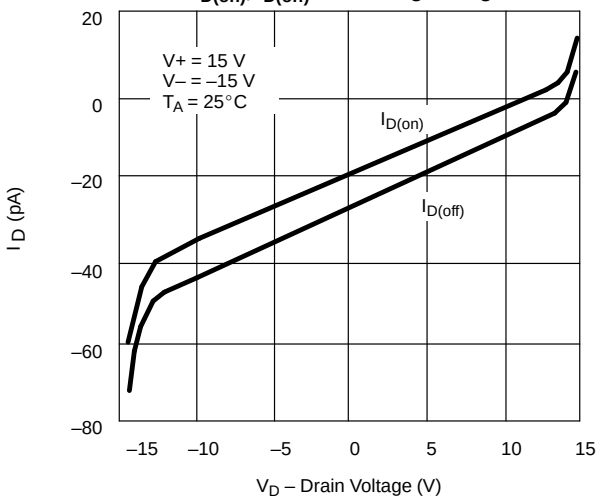
Leakages vs. Temperature



$I_{S(off)}$ vs. Analog Voltage



$I_{D(on)}$, $I_{D(off)}$ vs. Analog Voltage



SCHEMATIC DIAGRAM (TYPICAL CHANNEL)

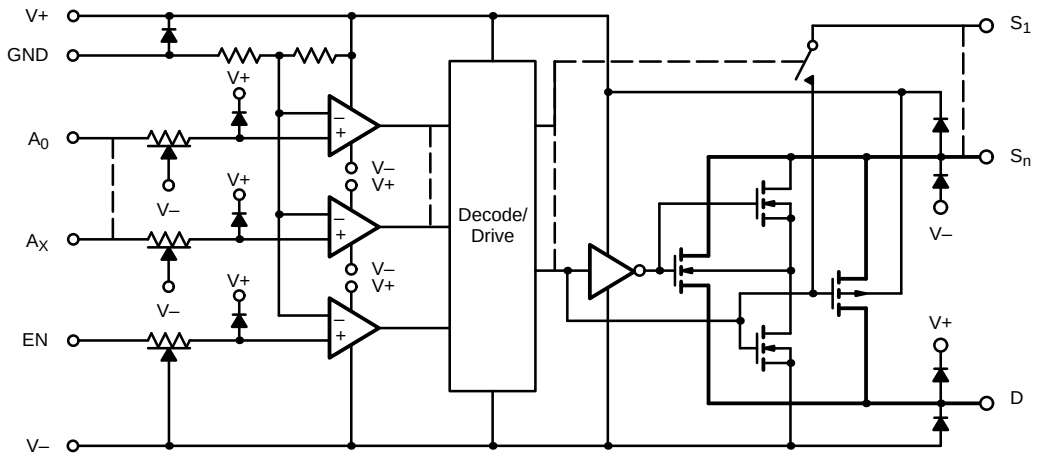
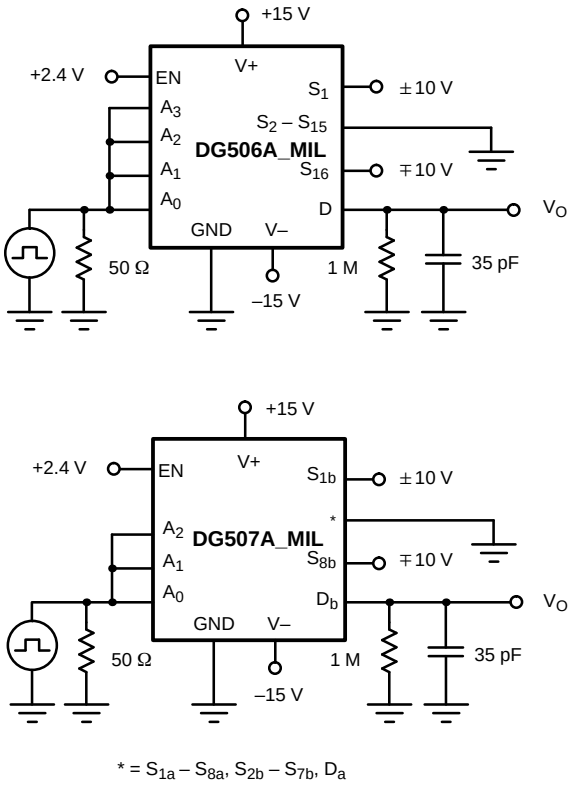


FIGURE 1.

TEST CIRCUITS



* = $S_{1a} – S_{8a}$, $S_{2b} – S_{7b}$, D_a

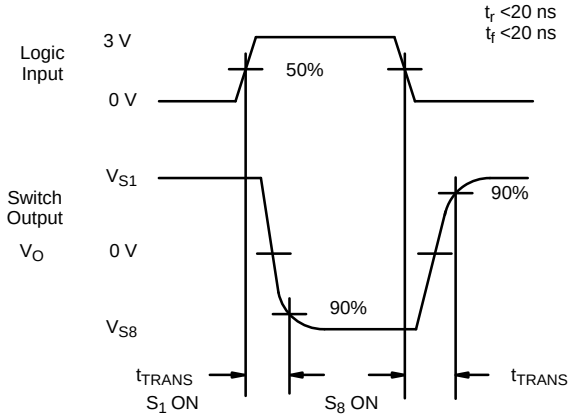


FIGURE 2. Transition Time

TEST CIRCUITS

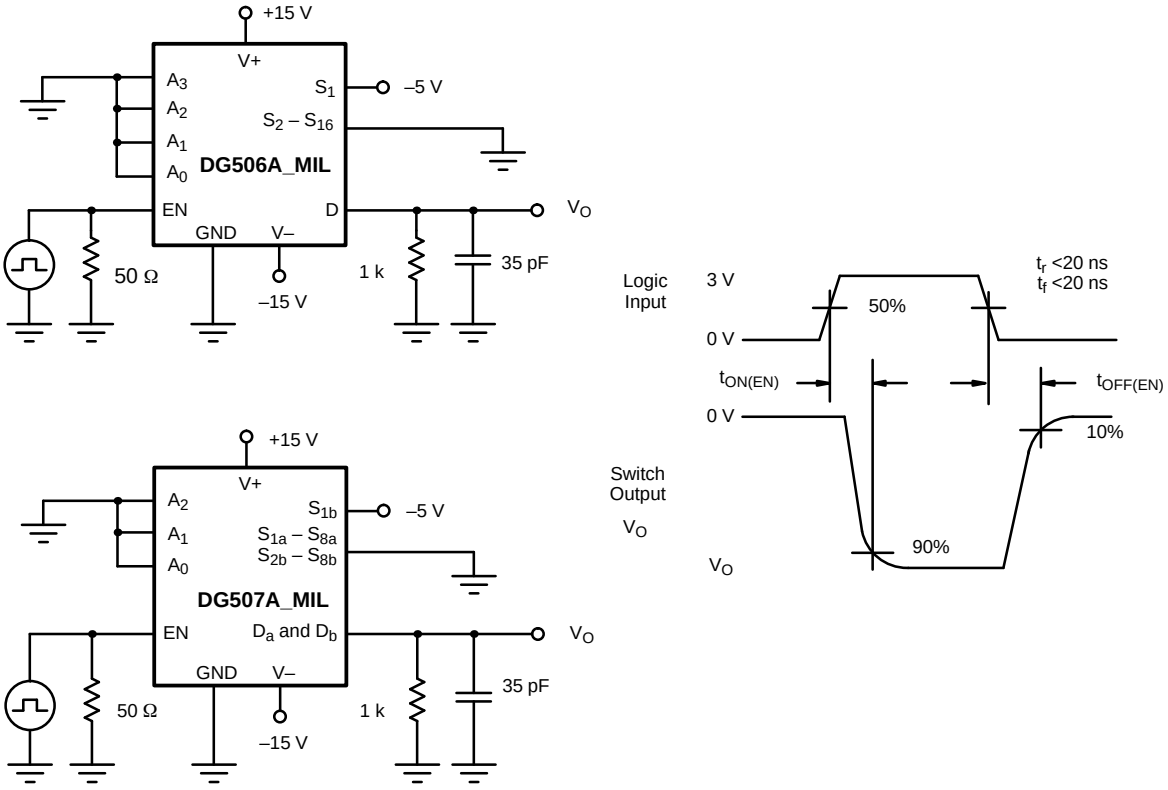


FIGURE 3. Enable Switching Time

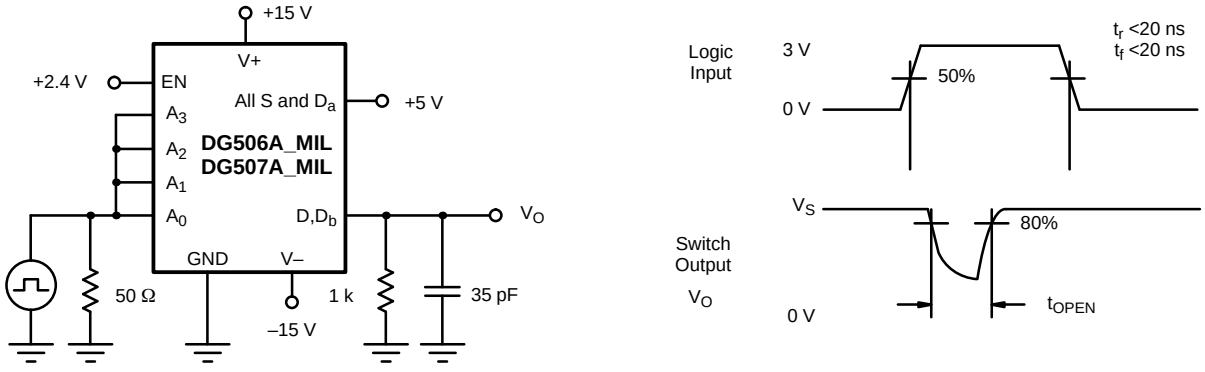


FIGURE 4. Break-Before-Make Interval

APPLICATION HINTS[a]			
V+ Positive Supply Voltage (V)	V– Negative Supply Voltage (V)	V_{IN} Logic Input Voltage $V_{INH(min)}/V_{INL(max)}$ (V)	V_S or V_D Analog Voltage Range (V)
15[b]	–15	2.4/0.8	–15 to 15
12	–12	2.4/0.8	–12 to 12
10	–10	2.2/0.6	–10 to 10
8[c]	–8	2.0/0.5	–8 to 8

Notes:
a. Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.
b. Electrical Parameter Chart based on V+ = 15 V, V– = –15 V.
c. Operation below ±8 V is not recommended due to shift in $V_{INL(MAX)}$.

Overvoltage Protection

A very convenient form of overvoltage protection consists of adding two small signal diodes (1N4148, 1N914 type) in series with the supply pins (see Figure 5). This arrangement effectively blocks the flow of reverse currents. It also floats the supply pin above or below the normal V+ or V– value. In this case the overvoltage signal actually becomes the power supply of the IC. From the point of view of the chip, nothing has changed, as long as the difference between V_S and the V– rail doesn't exceed +44 V. The addition of these diodes will reduce the analog signal range to 1 V below V+ and 1 V above V–, but it preserves the low channel resistance and low leakage characteristics.

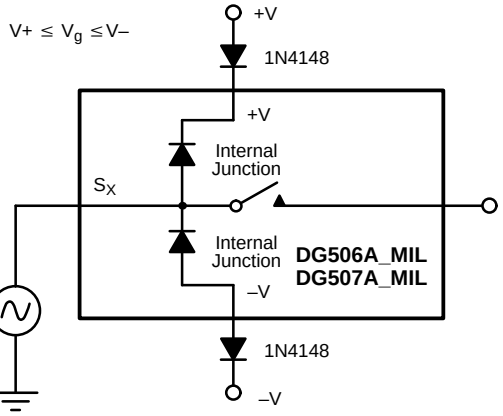


FIGURE 5. Overvoltage Protection Using Blocking Diodes

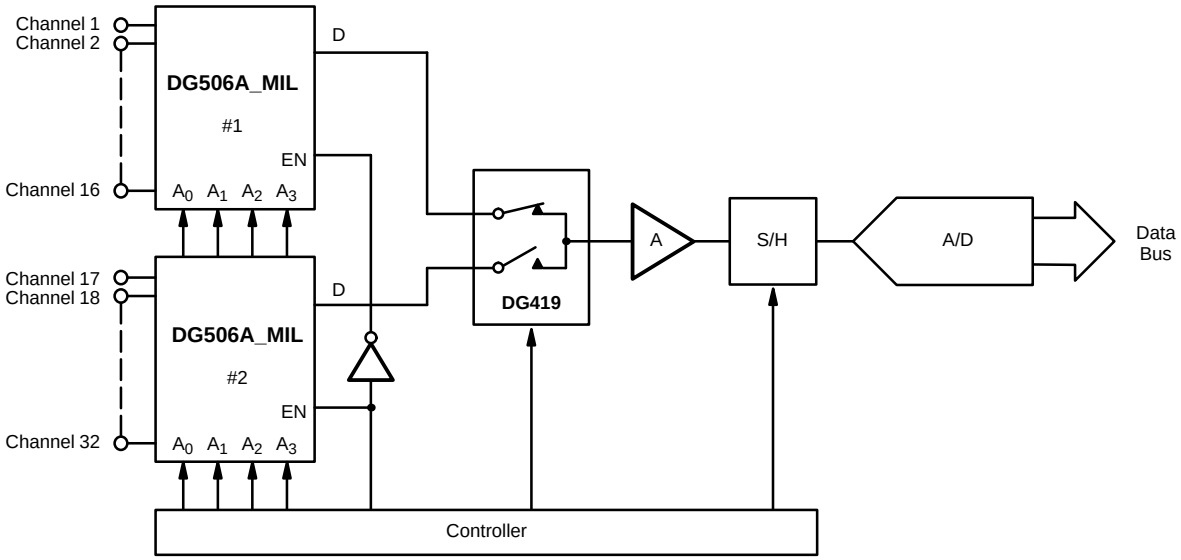


FIGURE 6. A 32-Channel Data Acquisition System

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