Low-Voltage Single SPDT Analog Switch

FEATURES

- Low Voltage Operation (1.8 V to 5.5 V)
- Low On-Resistance - r_{ON}: 3 Ω
- Fast Switching - t_{ON} : 20 ns, t_{OFF}: 10 ns
- Low Leakage - I_{COM}: 0.2-nA
- Low Charge Injection - Q_{INJ}: 5 pC
- Low Power Consumption
- TTL/CMOS Compatible
- ESD Protection > 2000 V (Method 3015.7)
- TSOP-6 Package

BENEFITS

- Reduced Power Consumption
- Simple Logic Interface
- High Accuracy
- Reduce Board Space

APPLICATIONS

- Cellular Phones
- Communication Systems
- Portable Test Equipment
- Battery Operated Systems
- Sample and Hold Circuits

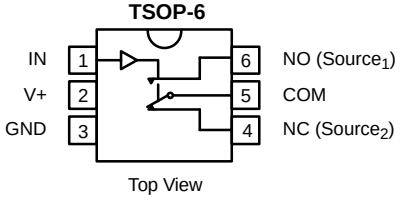
DESCRIPTION

The DG2001 is a single-pole/double-throw monolithic CMOS analog switch designed for high performance switching of analog signals. Combining low power, high speed, low on-resistance and small physical size, the DG2001 is ideal for portable and battery powered applications requiring high performance and efficient use of board space.

The DG2001 is built on Vishay Siliconix's low voltage JI2 process. The DG2001 has a minimum 2000-V, ESD protection, per Method 3015.7. An epitaxial layer prevents latchup. Break-before-make is guaranteed.

The switch conducts equally well in both directions when on, and blocks up to the power supply level when off.

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



Top View

TRUTH TABLE		
Logic	**NC**	**NO**
0	ON	OFF
1	OFF	ON

ORDERING INFORMATION		
Temp Range	**Package**	**Part Number**
-40 to 85°C	TSOP-6	DG2001DV

ABSOLUTE MAXIMUM RATINGS

Reference to GND
V+ . . . . . -0.3 to +6 V
IN, COM, NC, NO[a] . . . . . -0.3 to (V+ + 0.3 V)
Continuous Current (Any terminal) . . . . . ±50 mA
Peak Current . . . . . ±200 mA
(Pulsed at 1 ms, 10% duty cycle)
ESD (MIL-STD-883B, Method 3015.7) . . . . . > 2000 V

Storage Temperature (D Suffix) . . . . . -65 to 125°C
Power Dissipation (Packages)[b]
TSOP-6[c] . . . . . 570 mW

Notes:
a. Signals on NC, NO, or COM or IN exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC Board.
c. Derate 7.0 mW/°C above 25°C

SPECIFICATIONS (V+ = 2.0 V)

Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 2.0 V, ±10%, V_{IN} = 0.4 or 1.6 V[e]	Temp[a]	Limits –40 to 85°C Min[b]	Typ[c]	Max[b]	Unit
Analog Switch							
Analog Signal Range[d]	V_{NO}, V_{NC}, V_{COM}		Full	0		V+	V
On-Resistance	r_{ON}	V+ = 1.8 V, V_{COM} = 1.0 V, I_{NO}, I_{NC} = 10 mA	Room Full		15 17	30 32	Ω
r_{ON} Flatness[d]	r_{ON} Flatness	V+ = 1.8 V, V_{COM} = 0 to V+, I_{NO}, I_{NC} = 10 mA	Room		5		
Switch Off Leakage Current[g]	$I_{NO(off)}$, $I_{NC(off)}$	V+ = 2.2 V V_{NO}, V_{NC} = 0.5 V/1.5 V, V_{COM} = 1.5 V/0.5 V	Room Full	–300 –3.5		300 3.5	pA nA
	$I_{COM(off)}$		Room Full	–300 –3.5		300 3.5	pA nA
Channel-On Leakage Current[g]	$I_{COM(on)}$	V+ = 2.2 V, V_{NO}, V_{NC} = V_{COM} = 0.5 V/1.5 V	Room Full	–350 –3.5		300 3.5	pA nA
Digital Control							
Input High Voltage	V_{INH}		Full	1.6			V
Input Low Voltage	V_{INL}		Full			0.4	
Input Capacitance	C_{in}		Full		4		pF
Input Current	I_{INL} or I_{INH}	V_{IN} = 0 or V+	Full	1		1	µA
Dynamic Characteristics							
Turn-On Time	t_{ON}	V_{NO} or V_{NC} = 1.5 V, R_L = 300 Ω, C_L = 35 pF	Room Full		30	50 53	ns
Turn-Off Time	t_{OFF}		Room Full		15	30 33	
Break-Before-Make Time	t_d		Room	1	15		
Charge Injection[d]	Q_{INJ}	C_L = 1 nF, V_{GEN} = 0 V, R_{GEN} = 0 Ω	Room		1	10	pC
Off-Isolation[d]	OIRR	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz	Room		–71		dB
Crosstalk[d]	X_{TALK}		Room		–70		
N_O, N_C Off Capacitancen[d]	$C_{NO(off)}$, $C_{NC(off)}$	V_{IN} = 0 or V+, f = 1 MHz	Room		17		pF
Channel-On Capacitance[d]	C_{ON}		Room		50		
Power Supply							
Power Supply Range	V+			1.8		2.20	V
Power Supply Current	I+	V_{IN} = 0 or V+			0.01	1.0	µA
Power Consumption	P_C					2.2	µW

SPECIFICATIONS (V+ = 3 V)

Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 3 V, ±10%, V_{IN} = 0.4 or 2.0 V[e]	Temp[a]	Limits –40 to 85°C Min[b]	Typ[c]	Max[b]	Unit
Analog Switch							
Analog Signal Range[d]	V_{NO}, V_{NC}, V_{COM}		Full	0		V+	V
On-Resistance	r_{ON}	V+ = 2.7 V, V_{COM} = 1.5 V, I_{NO}, I_{NC} = 10 mA	Room Full		5 6	9.2 10.2	Ω
r_{ON} Flatness[d]	r_{ON} Flatness	V+ = 2.7 V V_{COM} = 0 to V+, I_{NO}, I_{NC} = 10 mA	Room		3		Ω
Switch Off Leakage Current[g]	$I_{NO(off)}$, $I_{NC(off)}$	V+ = 3.3 V, V_{NO}, V_{NC} = 1 V/3 V V_{COM} = 3 V/1 V	Room Full	–400 –4.5		400 4.5	pA nA
	$I_{COM(off)}$		Room Full	–400 –4.5		400 4.5	pA nA
Channel-On Leakage Current[g]	$I_{COM(on)}$	V+ = 3.3 V, V_{NO}, V_{NC} = V_{COM} = 1 V/3 V	Room Full	–450 –4.5		450 4.5	pA nA
Digital Control							
Input High Voltage	V_{INH}		Full	2			V
Input Low Voltage	V_{INL}		Full			0.4	V
Input Capacitance	C_{in}		Full		4		pF
Input Current	I_{INL} or I_{INH}	V_{IN} = 0 or V+	Full	1		1	µA
Dynamic Characteristics							
Turn-On Time	t_{ON}	V_{NO} or V_{NC} = 2.0 V, R_L = 300 Ω, C_L = 35 pF	Room Full		24	45 48	ns
Turn-Off Time	t_{OFF}		Room Full		12	30 33	ns
Break-Before-Make Time	t_d		Room	1	13		ns
Charge Injection[d]	Q_{INJ}	C_L = 1 nF, V_{GEN} = 0 V, R_{GEN} = 0 Ω	Room		3	10	pC
Off-Isolation[d]	OIRR	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz	Room		–71		dB
Crosstalk[d]	X_{TALK}		Room		–70		dB
N_O, N_C Off Capacitance[d]	$C_{NO(off)}$, $C_{NC(off)}$	V_{IN} = 0 or V+, f = 1 MHz	Room		17		pF
Channel-On Capacitance[d]	C_{ON}		Room		50		pF
Power Supply							
Power Supply Range	V+			2.7		3.3	V
Power Supply Current	I+	V_{IN} = 0 or V+			0.01	1.0	µA
Power Consumption	P_C					3.3	µW

SPECIFICATIONS (V+ = 5 V)

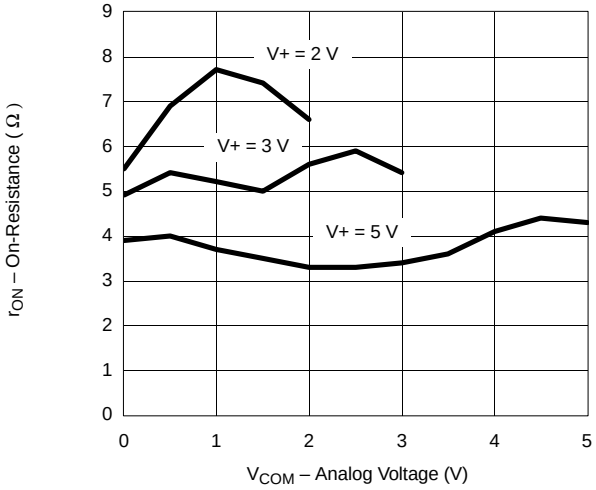
Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 5 V, ±10%, V_{IN} = 0.8 or 2.4 V[e]	Temp[a]	Limits –40 to 85°C Min[b]	Typ[c]	Max[b]	Unit
Analog Switch							
Analog Signal Range[d]	V_{NO}, V_{NC}, V_{COM}		Full	0		V+	V
On-Resistance	r_{ON}	V+ = 4.5 V, V_{COM} = 3 V, I_{NO}, I_{NC} = 10 mA	Room Full		3 4	7.0 8.0	Ω
r_{ON} Flatness[d]	r_{ON} Flatness	V+ = 4.5 V, V_{COM} = 0 to V+, I_{NO}, I_{NC} = 10 mA	Room		2		Ω
Switch Off Leakage Current[g]	$I_{NO(off)}$, $I_{NC(off)}$	V+ = 5.5 V V_{NO}, V_{NC} = 1 V/4.5 V, V_{COM} = 4.5 V/1 V	Room Full	–900 –5.5		900 5.5	pA nA
	$I_{COM(off)}$		Room Full	–900 –5.5		900 5.5	pA
Channel-On Leakage Current[g]	$I_{COM(on)}$	V+ = 5.5 V, V_{NO}, V_{NC} = V_{COM} = 1 V/4.5 V	Room Full	–1000 –5.5		1000 5.5	pA nA
Digital Control							
Input High Voltage	V_{INH}		Full	2.4			V
Input Low Voltage	V_{INL}		Full			0.8	V
Input Capacitance	C_{in}		Full		4		pF
Input Current	I_{INL} or I_{INH}	V_{IN} = 0 or V+	Full	1		1	µA
Dynamic Characteristics							
Turn-On Time	t_{ON}	V_{NO} or V_{NC} = 3 V, R_L = 300 Ω, C_L = 35 pF	Room Full		20	37 40	ns
Turn-Off Time	t_{OFF}		Room Full		10	27 30	ns
Break-Before-Make Time	t_d		Room	1	10		ns
Charge Injection[d]	Q_{INJ}	C_L = 1 nF, V_{GEN} = 0 V, R_{GEN} = 0 Ω	Room		7	10	pC
Off-Isolation[d]	OIRR	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz	Room		–71		dB
Crosstalk[d]	X_{TALK}		Room		–70		dB
Source-Off Capacitance[d]	$C_{NO(off)}$, $C_{NC(off)}$	V_{IN} = 0 or V+, f = 1 MHz	Room		17		pF
Channel-On Capacitance[d]	C_{ON}		Room		50		pF
Power Supply							
Power Supply Range	V+			4.5		5.5	V
Power Supply Current	I+	V_{IN} = 0 or V+			0.01	1.0	µA
Power Consumption	P_C					5.5	µW

Notes:

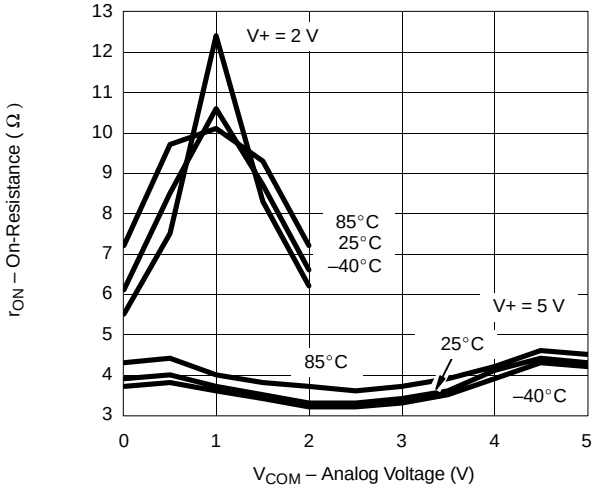
a. Room = 25°C, Full = as determined by the operating suffix.
b. Typical values are for design aid only, not guaranteed nor subject to production testing.
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
d. Guarantee by design, nor subjected to production test.
e. V_{IN} = input voltage to perform proper function.
f. Guaranteed by 5-V leakage testing, not production tested.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

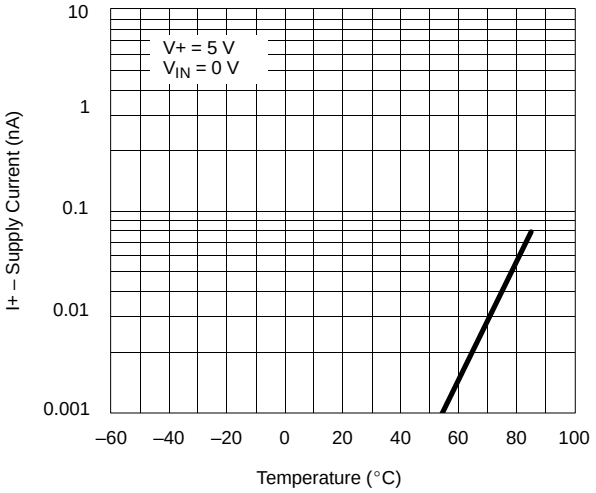
r_{ON} vs. V_{COM} and Supply Voltage



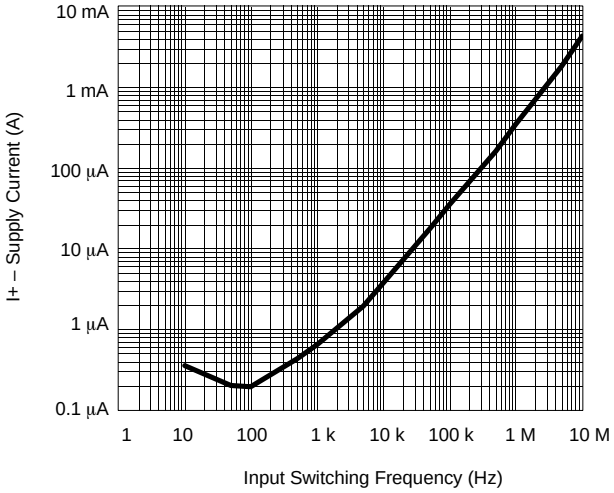
r_{ON} vs. Analog Voltage and Temperature



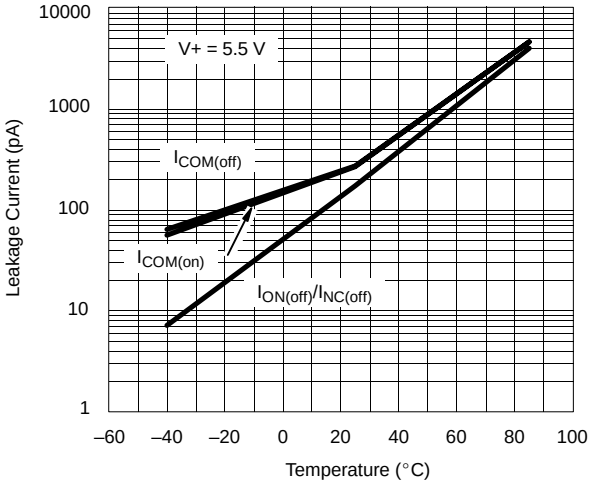
Supply Current vs. Temperature



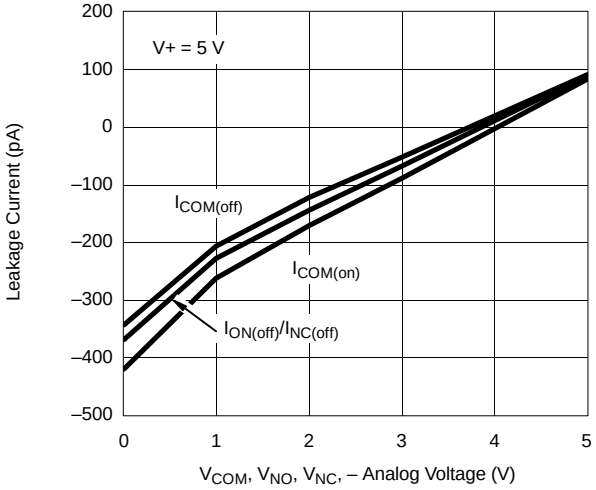
Supply Current vs. Input Switching Frequency



Leakage Current vs. Temperature

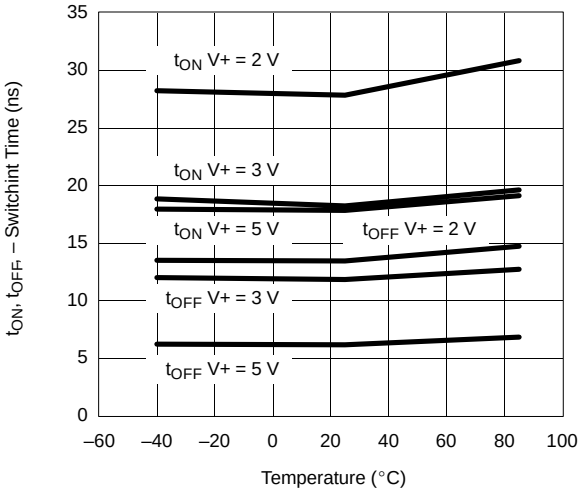


Leakage vs. Analog Voltage

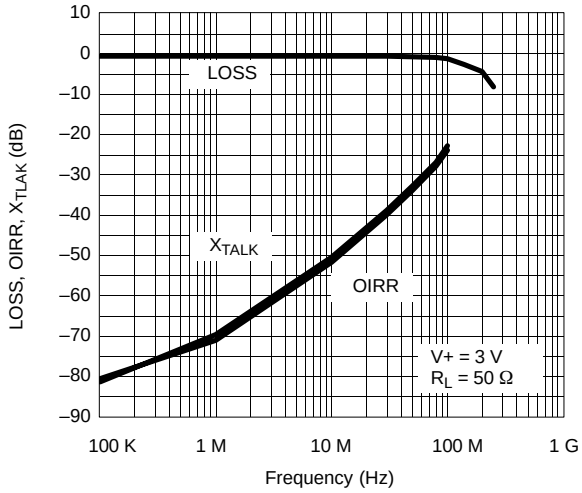


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

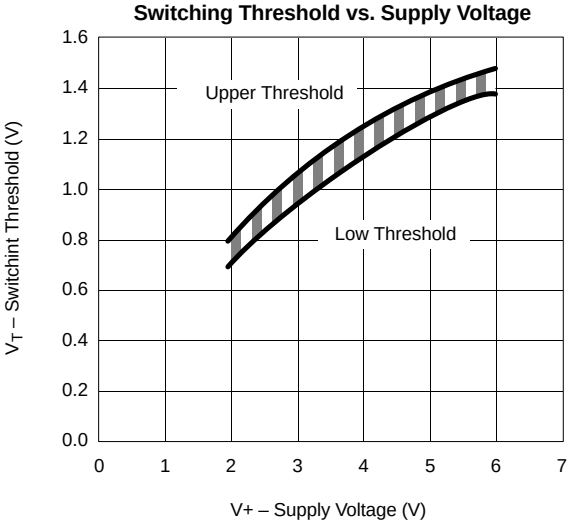
Switching Time vs. Temperature and Supply Voltage



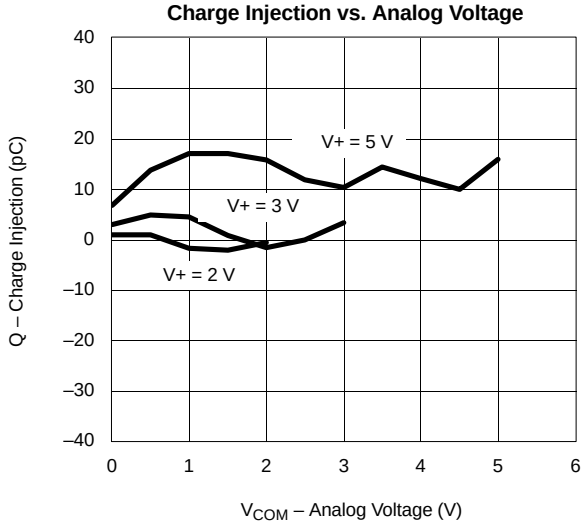
Insertion Loss, Off-Isolation, Crosstalk vs. Frequency



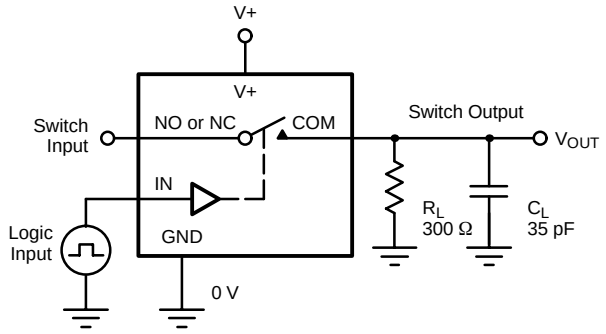
Switching Threshold vs. Supply Voltage



Charge Injection vs. Analog Voltage

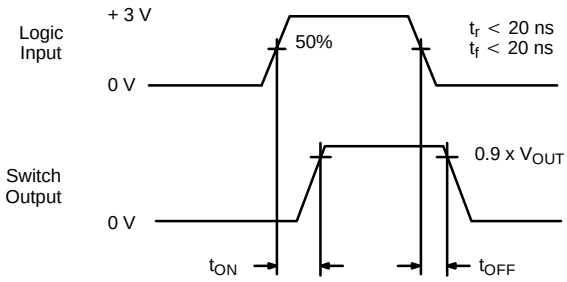


TEST CIRCUITS



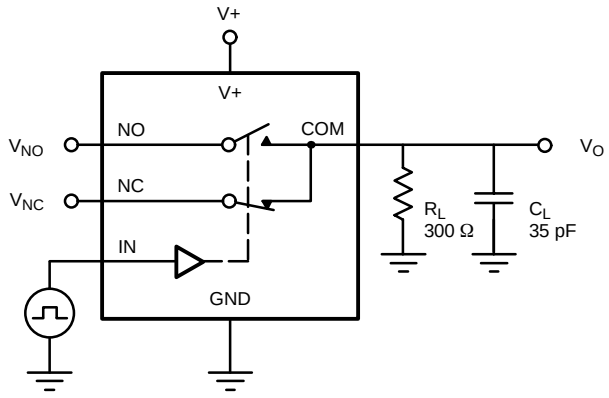
C_L (includes fixture and stray capacitance)

$$V_{OUT} = V_{COM}\left(\frac{R_L}{R_L + R_{ON}}\right)$$



Logic "1" = Switch On
Logic input waveforms inverted for switches that have the opposite logic sense.

FIGURE 1. Switching Time



C_L (includes fixture and stray capacitance)

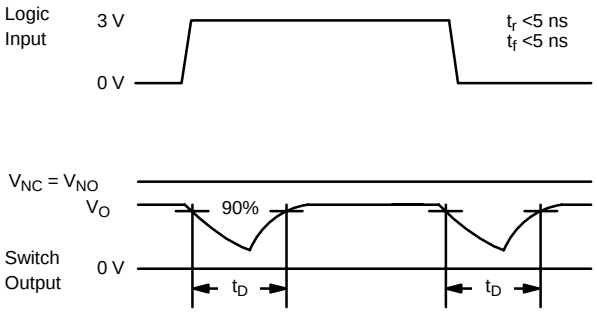
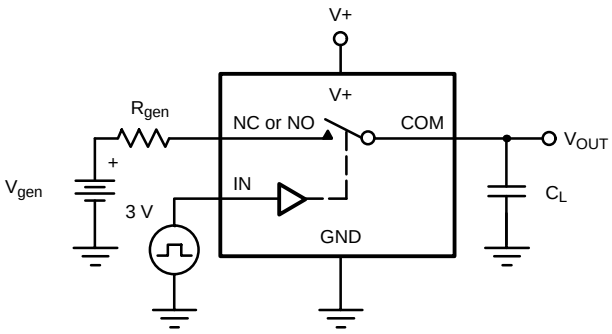
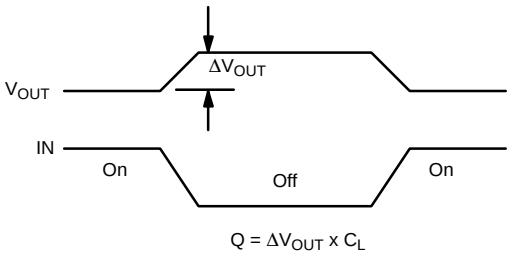


FIGURE 2. Break-Before-Make Interval





$Q = \Delta V_{OUT} \times C_L$

IN depends on switch configuration: input polarity determined by sense of switch.

FIGURE 3. Charge Injection

TEST CIRCUITS

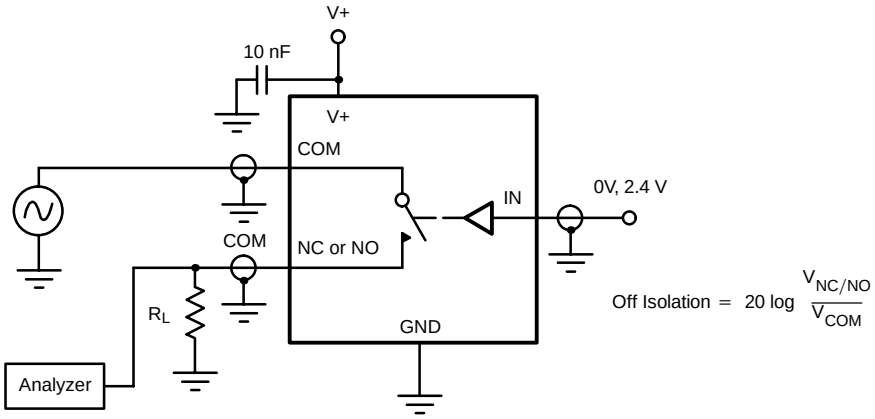


FIGURE 4. Off-Isolation

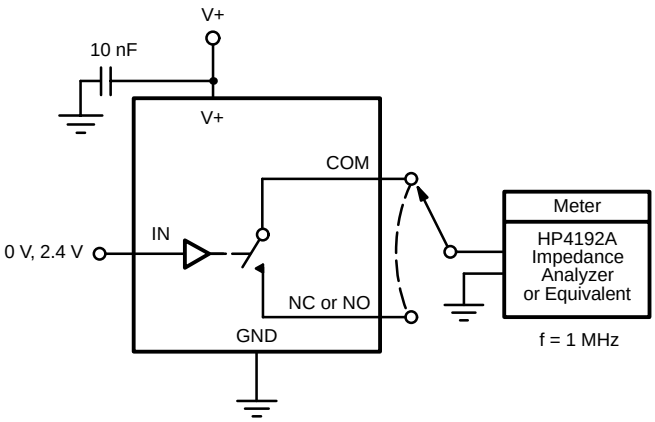


FIGURE 5. Channel Off/On Capacitance