Display Elektronik GmbH

DATA SHEET

LCD MODULE

DEM 16216 SYH-PY

Product specification ***Version: 4***

09.04.2003

GENERAL SPECIFICATION

MODULE N0. :

DEM 16216 SYH-PY

CUSTOMER P / N

VERSION NO.	CHANGE DESCRIPTION	DATE
0	ORIGINAL VERSION	2001/01/16
1	CHANGE AS KS0070B	2001/01/18
2	CHANGE LCD AND BACKLIGHT	2001/01/31
3	ADD VERSION	2002/10/14
4	ADD MODEL	2002/11/15

PREPARED BY: ZXD DATE: 15.11.2002

APPROVED BY: MH DATE: 09.04.2003

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1. FUNCTIONS & FEATURES

- DEM 16216-SERIES type:

MODULE	LCD-TYPE	LCD TYPE
DEM 16216 SYH-PY	STN Yellow/Green	Transflective Positive Mode

- Viewing Direction : 6 O'clock
- Driving Scheme : 1/16 Duty Cycle, 1/5 Bias
- Power Supply Voltage : 2.7V to 5.5V (typ. 5V)
- V_{LCD} Adjustable for Best Contrast : 4.5V (typ.)
- Backlight : Yellow/Green (lightpipe/lightguide)
- Display Format : 16 x 2 Characters (5 x 8 dots, Format : 192 Kinds)
- Internal Memory : CGROM (8,320 bits)
  : CGRAM (64 x 8 bits)
  : DDRAM (80 x 8 bits for Digits)
- Interface : Easy Interface with a 4 - bit or 8 - bit MPU

2. MECHANICAL SPECIFICATIONS

- Character Pitch : 3.55(w) x 5.95(h) mm
- Character Size : 2.95(w) x 5.55(h) mm
- Character Font : 5 x 8 dots
- Dot Size : 0.55(w) x 0.65(h) mm
- Dot Pitch : 0.60(w) x 0.70(h) mm

3. BLOCK Diagram

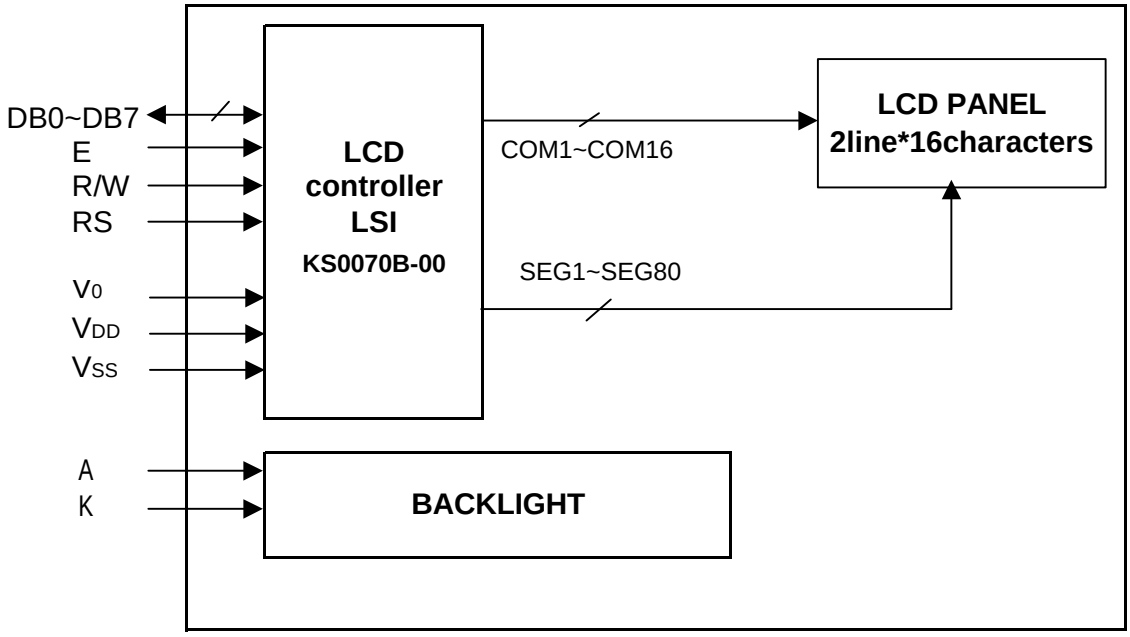


Figure 1.0

4. External Dimensions

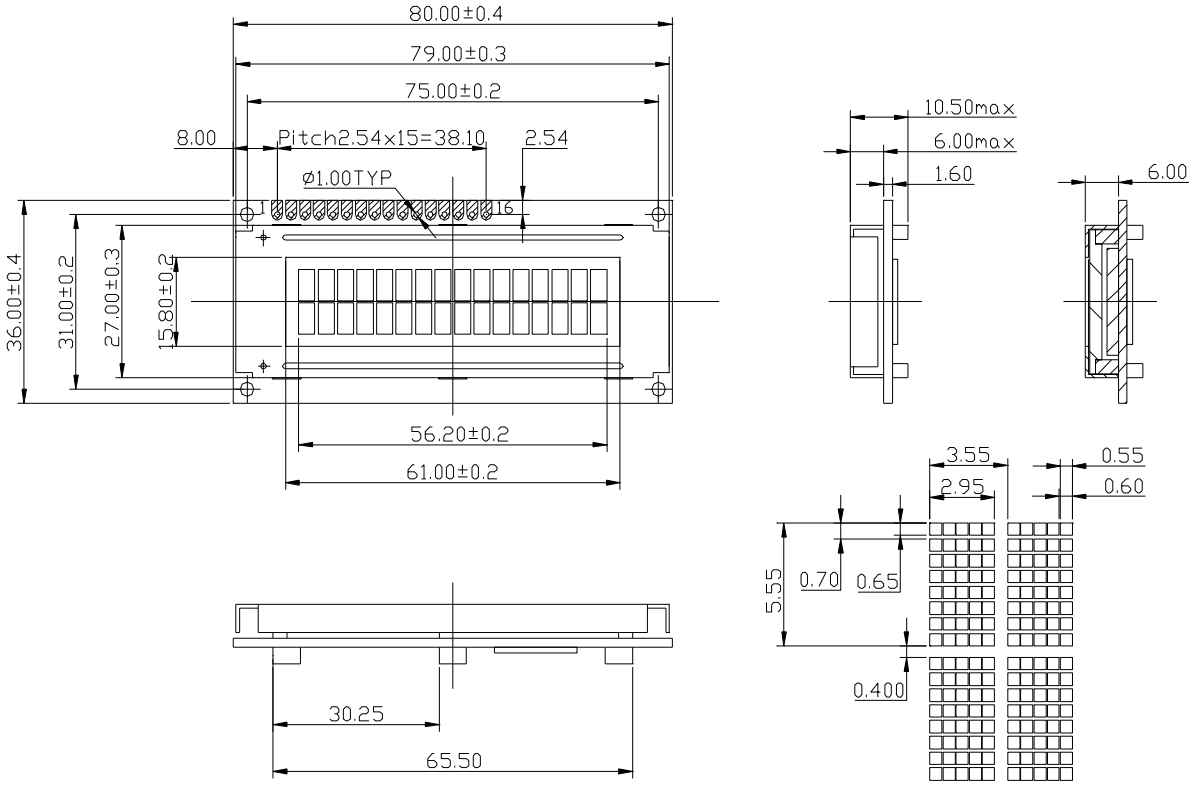


Figure 2.0

5. PIN Assignment

Pin No.	Symbol	Function
1	V_{SS}	Ground terminal of module
2	V_{DD}	Supply terminal of module 2.7 to 5.5 V
3	V_0	Power Supply for Liquid crystal Drive
4	RS	Register Select RS = 0… Instruction Register RS = 1… Data Register
5	R/W	Read / Write R/W = 1 (Read) R/W = 0 (Write)
6	E	Enable
7	DB0	Bi-directional Data Bus, Data Transfer is performed once , thru DB0~DB7 , in the case of interface data . Length is 8-bits; and twice , thru DB4~DB7 in the case of interface data length is 4-bits . Upper four bits first then lower four bits .
8	DB1	
9	DB2	
10	DB3	
11	DB4	
12	DB5	
13	DB6	
14	DB7	
15	LED - (K)	Please also refer to 6.1 PCB drawing and description .
16	LED + (A)	Please also refer to 6.1 PCB drawing and description .

6.1 PCB DRAWING AND DESCRIPTION

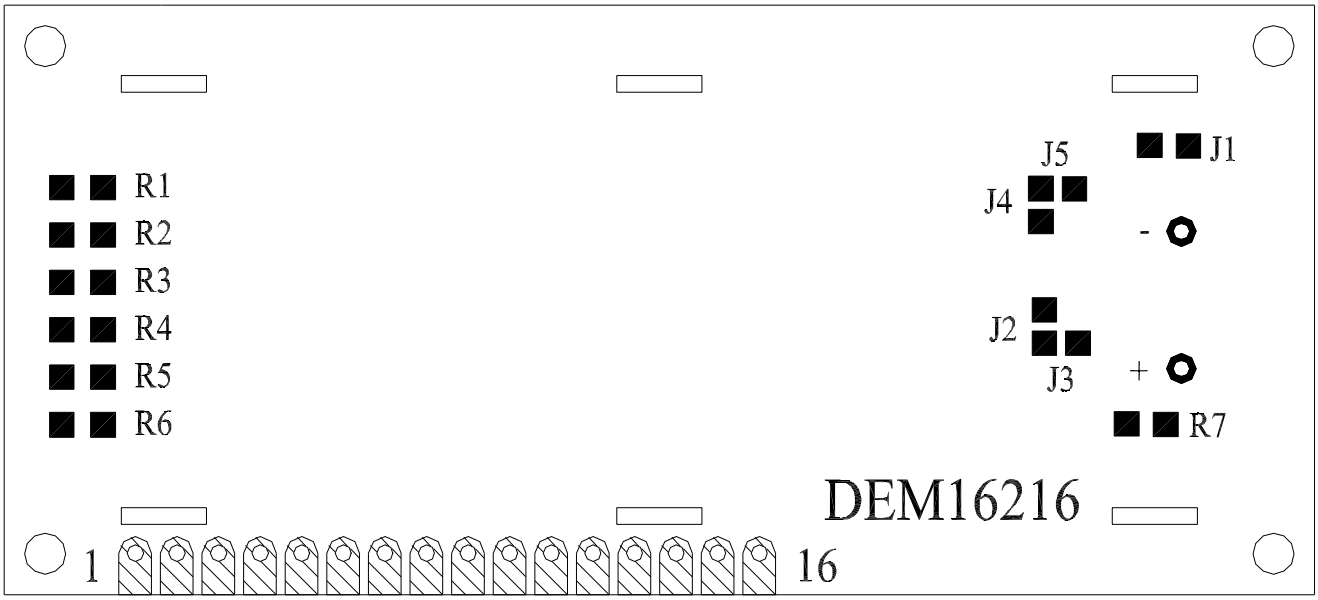


Figure 3.0

Description :

6-1-1.The polarity of the pin 15 and the pin 16

Symbol / State		J3,J5	J2,J4	LED Polarity	
				15 Pin	16 Pin
J2,J4	Each Solder- Bridge	Each Open	———	Anode	Cathode
J3,J5	Each Solder- Bridge	———	Each Open	Cathode	Anode

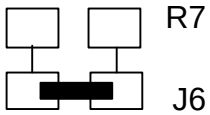
6-1-2. The metal-bezel should be on gronud when the J1 is Solder- Bridge .

6-1-3. The LED Resistor should be bridged when the J6 is Solder-Bridge .

6-1-4. The R7 is the LED Resistor. (R7=24 Ohm)

6.2 Example application

6-2-1 The LED resistor should be bridged as following .



6-2-2 The 15 pin is the Anode and the 16 pin is the cathode as following .



6-2-3 The 15 pin is the cathode and the 16 pin is the Anode as following .



6-2-4 The metal-bezel is on ground as following .



6.3 The module No. Is printed on the PCB .

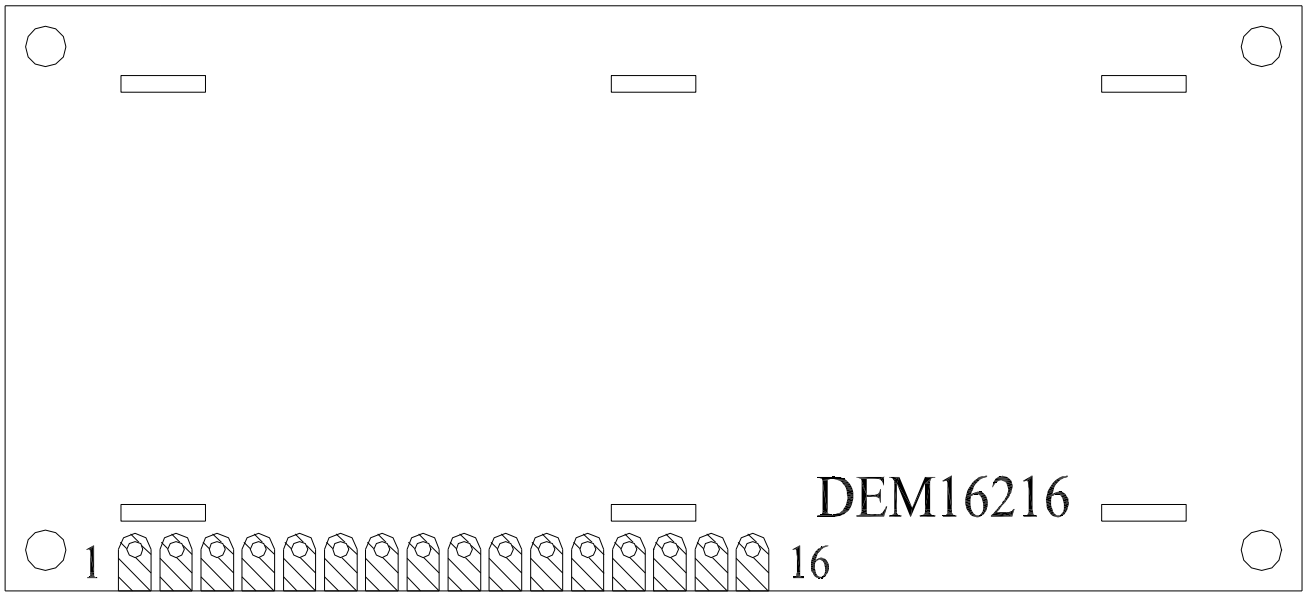


Figure 4.0

7. BACKLIGHT &SWITCH (Ta = -25 ~ +75°C)

Item	Symbol	Standard Value	Unit	Applicable Terminal
Backlight Voltage	V	5	V	LED+ / LED-
Backlight Current	I	~33	mA	

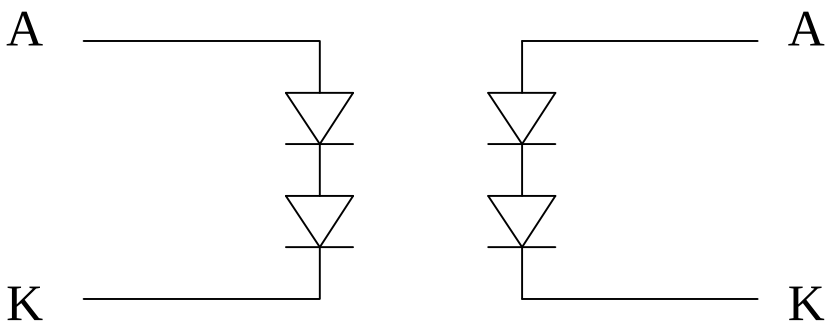


Figure 5.0

8. DISPLAY DATA RAM (DDRAM)

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F

← DISPLAY POSITION
← DDRAM ADDRESS

9. INSTRUCTION DESCRIPTION

Outline

To overcome the speed difference between the internal clock of KS0070B and the MPU clock, KS0070B performs internal operations by storing control information to IR or DR. The internal operation is determined according to the signal from MPU, composed of read/write and data bus (Refer to Table 5).

Instruction can be divided largely into four kinds .

(1) KS0070B function set instructions (set display methods, set data length, etc.)

(2) address set instruction to internal RAM

(3) data transfer instructions with internal ram

(4) others .

The address of the internal RAM is automatically increased or decreased by 1 .

*NOTE : During internal operation, Busy Flag (DB7) is read "1". Busy Flag check must be preceded by the next instruction .

When you make an MPU program with checking the Busy Flag (DB7), it must be necessary 1/2 Fosc for executing the next instruction by falling E signal after the Busy Flag (DB7) goes to "0" .

Contents

1) Clear Display

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1

Clear all the display data by writing "20H" (space code) to all DRAM addresses, and set the DRAM addresses to "00H" in the AC (address counter). Return cursor to original status, namely, bring the cursor to the left edge on first line of the display . Make entry mode increment (I/D = "1") .

2) Return Home

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	x

Return Home is the cursor return home instruction .

Set DRAM address to "00H" in the address counter. Return cursor to its original site and return display to its original status, if shifted, Contents of DDRAM does not change .

3) Entry Mode Set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	I/D	SH

Set the moving direction of cursor and display .

I/D : Increment/decrement of DDRAM address (cursor or blink)

When I/D = "1" , cursor/blink moves to right and DDRAM address is increased by 1.

When I/D = "0" , cursor/blink moves to left and DDRAM address is increased by 1.

*CGRAM operates the same as DDRAM , when reading from or writing to CGRAM .

SH: Shift of entire display

When DDRAM is in read (CGRAM read/write) operation or SH = "0" , shift of entire display is not performed .

If SH = "1" and in DDRAM write operation, shift of entire display is performed according to I/D value (I/D = "1" : shift left, I/D = "0" : shift right).

4).Display ON/OFF CONTROL

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	D	C	B

Control display/cursor/blink ON/OFF 1 bit register.

D : Display ON/OFF control bit

When D = "1" , entire display is turned on .

When D = "0" , display is turned off, but display data is remained in DDRAM .

C : Cursor ON/OFF control bit

When C = "1" , cursor is turned on.

When C = "0" , cursor is disappeared in current display, but I/D register remains its data .

B : Cursor Blink ON/OFF control bit

When B = "1" , cursor blink is on , that performs alternate between all the "1" data and display character at the cursor position.

When B = "0" , blink is off.

5).Cursor or Display Shift

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	S/C	R/L	X	X

Without writing or reading of display data , Shift right/left cursor position or display

This instruction is used to correct or search display data . (Refer to Table 4)

During 2-line mode display, cursor moves to the 2nd line after 40th digit of 1st line .

Note that display shift is performed simultaneously in all the line .

When displayed data is shifted repeatedly, each line shifted individually .

When displayed shift is performed, the contents of address counter are not changed .

Table 4 Shift patterns according to S/C and R/L bits

S/C	R/L	Operation
0	0	Shift cursor to the left, AC is decreased by 1
0	1	Shift cursor to the right, AC is decreased by 2
1	0	Shift all the display to the left, cursor moves according to the display
1	1	Shift all the display to the right, cursor moves according to the display

6).Function Set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	DL	N	F	X	X

DL : Interface data length control bit

When DL = "1" , it means 8-bit bus mode with MPU.

When DL = "0" , it means 4-bit bus mode with MPU. So to speak, DL is a signal to select 8-bit or 4-bit bus mode .

When 4-bit bus mode, it needs to transfer 4-bit data in two parts .

N : Display line number control bit

When N = "1" , 2-Line display mode is set .

When N = "0" , 1-Line display mode is set .

F : Display font type control bit

When F = "0" , 5 X 7 dots format display mode .

When F = "1" , 5 X 10 dots format display mode .

7).Set CGRAM Address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0

Set CGRAM Address to AC .

This instruction makes CGRAM data available from MPU.

8).Set DDRAM Address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0

Set DDRAM Address to AC .

This instruction makes DDRAM data available from MPU.

In 1-line display mode (N=0, NW=0), DDRAM address is from "00H" to "4FH".

In 2-line display mode (N=1, NW=0), DDRAM address in the 1st line is from "00H" to "27H",and DDRAM address in the 2nd line is from "40H" to "67H".

9) Read Busy Flag & Address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0

This instruction shows whether KS0070B is in internal operation or not. If the resultant BF is High, the internal operation is in progress and should wait until BF to become "Low", which by then the next instruction can be performed. In this instruction value of address counter can also be read.

10) Write data to RAM

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	D7	D6	D5	D4	D3	D2	D1	D0

Write binary 8-bit data to DRAM/CRAM/SEAGRAM.

The selection of RAM from DRAM, CRAM or SEAGRAM, is set by the previous address set instruction: DDRAM address set, CGRAM address set, SEGRAM address set, RAM set instruction can also determines the AC direction to RAM.

After write operation, the address is automatically increased/decreased by 1, according to the entry mode.

11) Read data from RAM

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	D7	D6	D5	D4	D3	D2	D1	D0

Read binary 8-bit data to DDRAM/CRAM .

The selection of RAM is set by the previous address set instruction. If address set instruction of RAM is not performed before this instruction, the data that read first is invalid, as the direction of AC is not determined. If the RAM data is read several times without RAM address set instruction before read operation, the correct RAM data from the second, but the first data would be incorrect, as there is not time to transfer RAM data. In case of DDRAM read operation, cursor shift instruction plays the same role as DDRAM address set instruction: it also transfer RAM data to output data register.

After read operation address counter is automatically increased/decreased by 1 according to the entry mode.

After CGRAM read operation, display shift may not be executed correctly.

*In case of RAM write operation, AC is increased/decreased by 1 like read operation after this. In this time, AC indicates the next address position, but the previous data can only by read instruction.

(CONTINUED)

Table 5. Instruction Set

Instruction	Instruction code										Execution time (fosc =270KHz)	Description
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
clear Display	0	0	0	0	0	0	0	0	0	1	1.53ms	Write "20H" to DDRAM. And set DDRAM address to "00H" from AC .
Return home	0	0	0	0	0	0	0	0	1	X	1.53ms	Set DDRAM address to "00H" from AC and return cursor to its original position if shifted.
Entry mode set	0	0	0	0	0	0	0	1	I/D	SH	39us	Assign cursor moving direction and enable the shift of entire display
Display on/ off control	0	0	0	0	0	0	1	D	C	B	39us	Set display (D), cursor (C), and blinking of cursor (B) on/off control bit .
Cursor or Display shift	0	0	0	0	0	1	S/C	R/L	X	X	39us	Set cursor moving and display shift control bit , and the direction , without changing of DRAM data .
Function Set	0	0	0	0	1	DL	N	F	X	X	39us	Set interface data length (DL : 4-bit/8-bit), numbers of display line (N : 1-line/2-line, Display font type (F: 0…)
Set CGRAM Address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	39us	Set CGRAM address in address counter.
Set DDRAM Address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	39us	Set DDRAM address in address counter.
Read Busy flag and Address	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	0us	Whether during internal operation or not can be known by reading BF. The contents of address counter can also be read .
Write Data to RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	43us	Write data into internal RAM (DDRAM/CGRAM)
Read Data from RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	43us	Read data into internal RAM (DDRAM/CGRAM)

NOTE : When you make an MPU program with checking the Bus Flag (DB7), it must be necessary 1/2F osc for executing the next instruction by falling E signal after the Busy Flag (DB7) goes to "0" .

10. INTERFACE WITH MPU IN BUS MODE

1). Interface with 8-bit MPU

When interface data length are 8-bits , transfer is performed all at once through 8 ports. From DB0 to DB7 .
An Example of timing sequence is shown below .

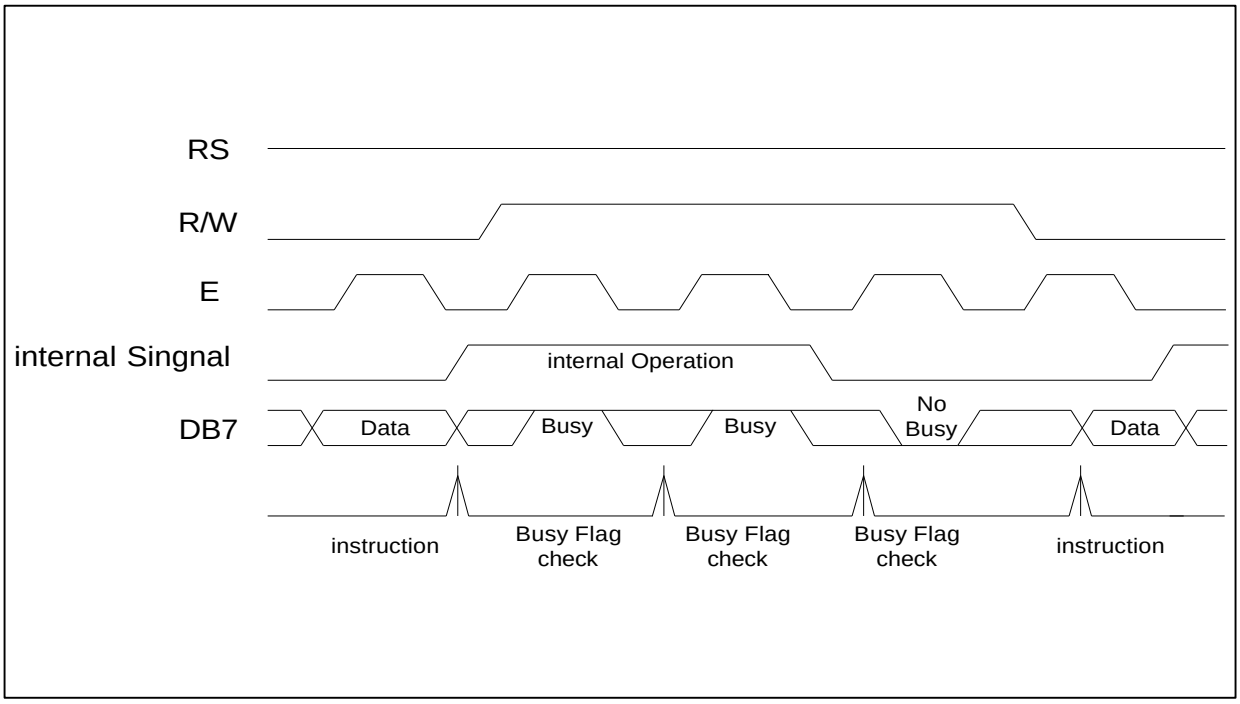


Figure 6.0. Example of 8-bit bus mode timing Diagram

2) Interface with 4-bits MPU

When interfacing data length aref 4-bits , only 4 ports, from DB4 to DB7 , are used as data bus .
At first, higher 4-bit (in case of 8-bit bus mode, the contents of DB4~DB7) are transferred, and then the lower 4-bit (in case of 8-bit bus mode, the contents of DB0~DB3) are transferred. So transfer is performed in two parts. Busy Flag outputs"1" after the second transfer are ended.
Example of timing sequence is shown below .

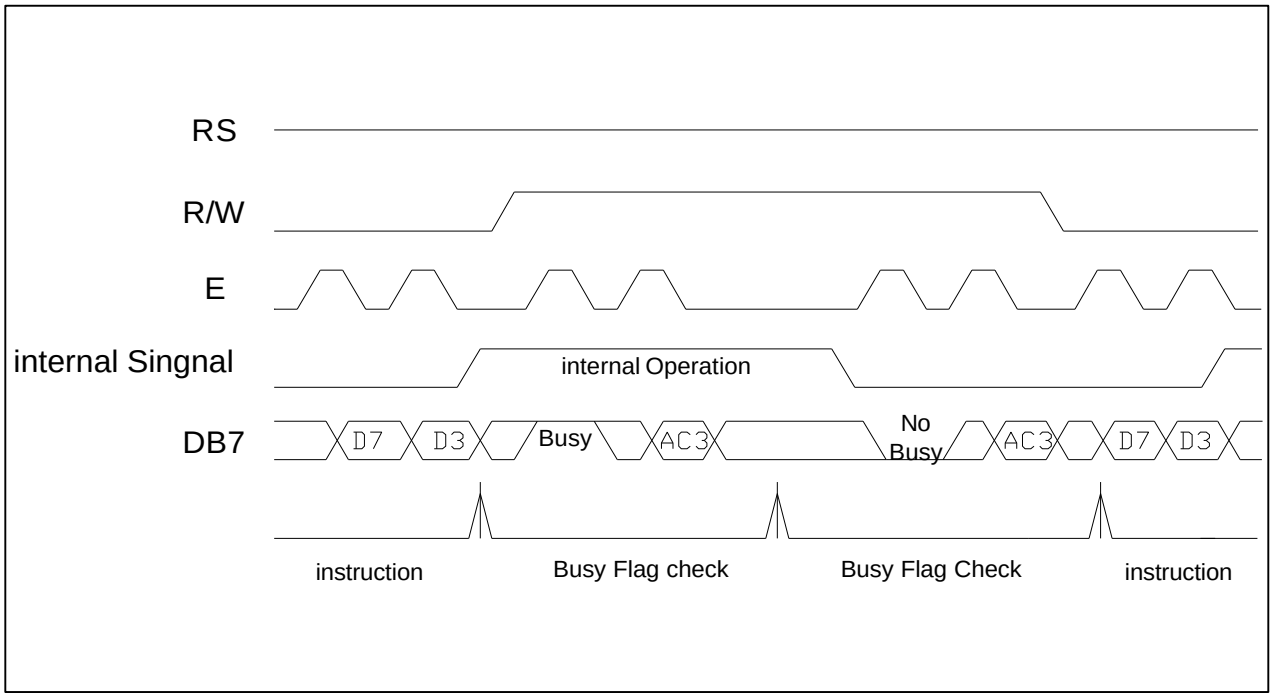
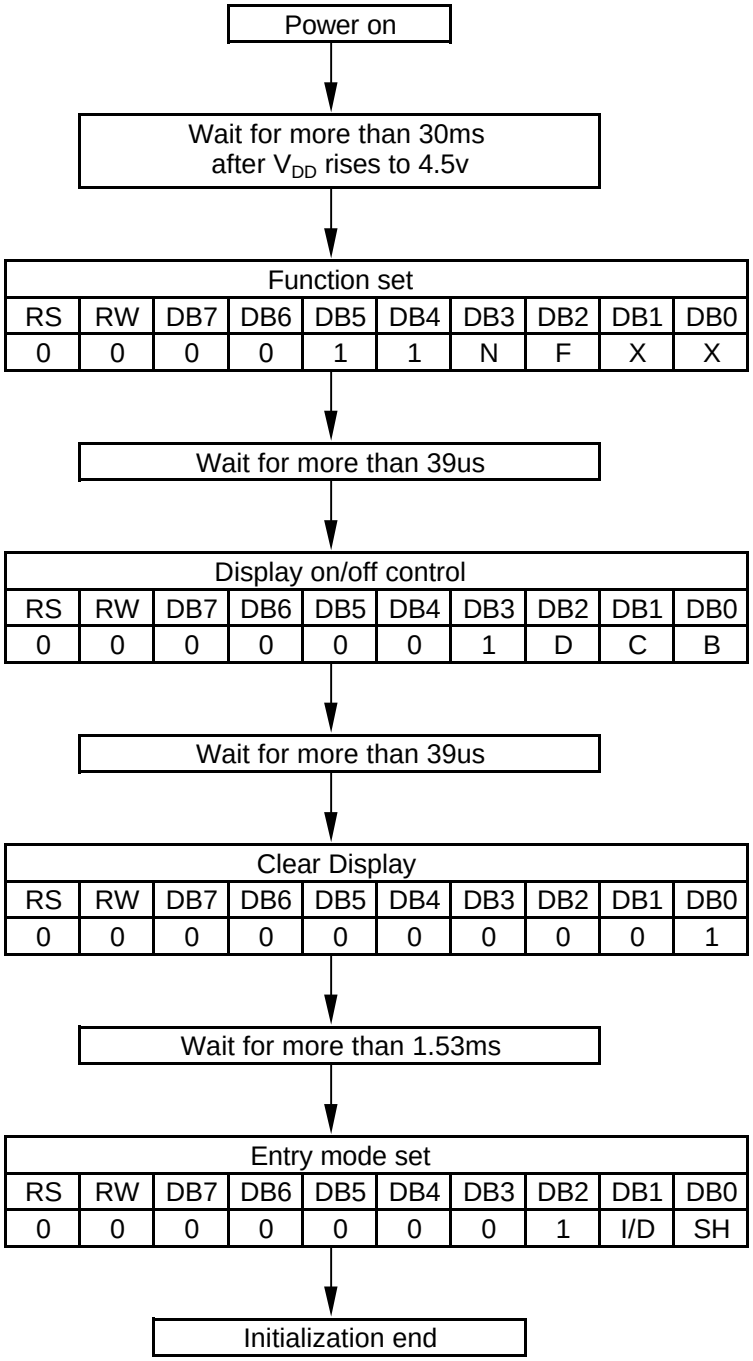


Figure 7.0 Example of 4-bit bus mode timing Diagram

11. INITIALIZING BY INSTRUCTION

11-1 8-bit interface mode



Condition : fosc=270kHz

N	0	1-line mode
	1	2-line mode

F	0	5 x 7 dots
	1	5 x 10 dots

D	0	display off
	1	display on

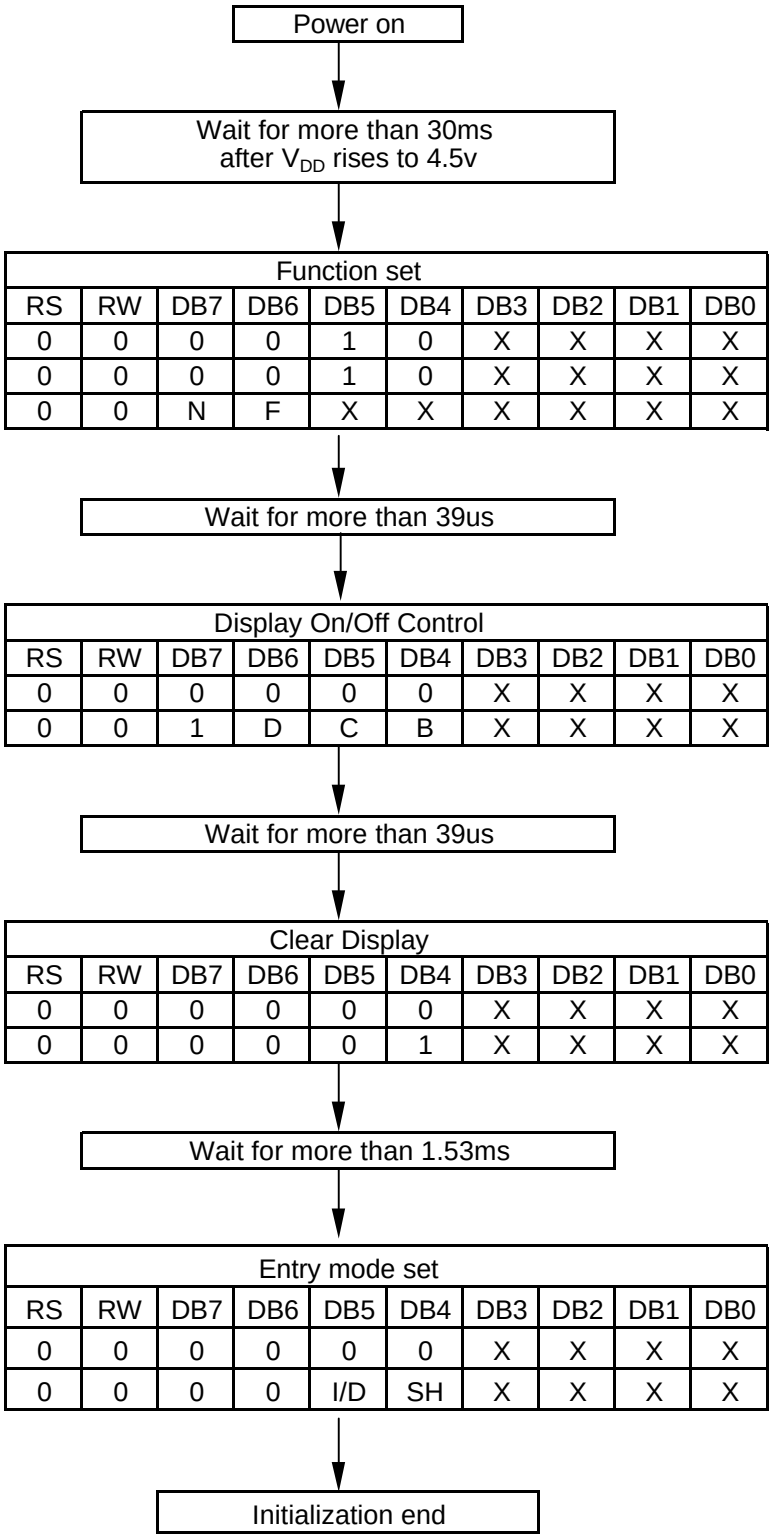
C	0	cursor off
	1	cursor on

B	0	blink off
	1	blink on

I/D	0	decrement mode
	1	increment mode

SH	0	entire shift off
	1	entire shift on

11-2 4-bit interface mode



Condition : fosc=270kHz

N	0	1-line mode
	1	2-line mode
F	0	5 x 7 dots
	1	5 x 10 dots
D	0	display off
	1	display on
C	0	cursor off
	1	cursor on
B	0	blink off
	1	blink on
I/D	0	decrement mode
	1	increment mode
SH	0	entire shift off
	1	entire shift on

12. MAXIMUM ABSOLUTE POWER RATINGS (Ta = 25°C)

Item	Symbol	Standard value	Unit
Power supply voltage(1)	V_{DD}	-0.3 ~ +7.0	V
Power supply voltage(2)	V_0	V_{DD}-15.0 ~ V_{DD}+0.3	V
Input voltage	V_{IN}	-0.3 ~ V_{DD}+0.3	V
Operating temperature	T_{opr}	-20 ~ +70	°C
Storage temperature	T_{stg}	-30 ~ +80	°C

13. Electrical Characteristics

13-1-1. DC Characteristics (V_{DD} = 4.5V ~ 5.5V, Ta = -20 ~ +70°C)

Characteristic	Symbol	Standard Value			Test Condition	Unit
		MIN	TYP	MAX		
Operating Voltage	V_{DD}	4,5	—	5,5	—	V
Supply Current	I_{DD1}		0,7	1.0	ceramic resonator fosc = 250kHz	mA
	I_{DD2}	—	0.4	0.6	Resistor oscillation external clock operation fosc = 270kHz	
Input Voltage(1) (except OSC1)	V_{IH1}	2.2	—	V_{DD}	—	V
	V_{IL1}	-0,3	—	0,6	—	
Input Voltage(2) (OSC1)	V_{IH2}	V_{DD}-1.0	—	V_{DD}	—	V
	V_{IL2}	-0.2	—	1.0	—	
Output Voltage (1) (DB0 TO DB7)	V_{OH1}	2,4	—	—	I_{OH}=-0.205mA	V
	V_{OL1}	—	—	0,4	I_{OL}=1.2uA	
Output Voltage (2) (except DB0 TO DB7)	V_{OH2}	0.9V_{DD}	—	—	I_{OH}=-40uA	V
	V_{OL2}	—	—	0.1V_{DD}	I_{OL}=40uA	
Voltage Drop	Vd_{COM}	—	—	1	I_O = ±0.1mA	V
	Vd_{SEG}	—	—	1		
Input Leakage Current	I_{IL}	-1	—	1	V_{IN}=0 V to V_{DD}	uA
Low Input Current	I_{IN}	-50	-125	-250	V_{IN}=0V,V_{DD}=5V(pull up)	
Internal Clock (external Rf)	f_{OSC}	190	270	350	Rf = 91k ± 2% (V_{DD}=5V)	kHz
External Clock	f_{EC}	150	250	350	—	kHz
	duty	45	50	55		%
	t_R,t_F	—	—	0,2		us
LCD Driving Voltage	V_{LCD}	4.6	—	10.0	V_{DD}-V_5 (1/5 Bias)	V

(CONTINUED)

(V_{DD} = 2.7V ~ 5.5V; Ta = -20 ~ +70°C)

Characteristic	Symbol	Standard Value			Test Condition	Unit
		MIN	TYP	MAX		
Operating Voltage	V_{DD}	2.7	—	5,5	—	V
Supply Current	I_{DD1}	—	0.3	0.5	ceramic resonator fosc = 250kHz	mA
	I_{DD2}	—	0.17	0.3	Resistor oscillation external clock operation fosc = 270kHz	
Input Voltage(1) (except OSC1)	V_{IH1}	0.7V_{DD}	—	V_{DD}	—	V
	V_{IL1}	-0,3	—	0.4	—	
Input Voltage(2) (OSC1)	V_{IH2}	0.7V_{DD}	—	V_{DD}	—	V
	V_{IL2}		—	0.2V_{DD}	—	
Output Voltage (1) (DB0 TO DB7)	V_{OH1}	2	—	—	I_{OH}=-0.1mA	V
	V_{OL1}	—	—	0,4	I_{OL}=0.1mA	
Output Voltage (2) (except DB0 TO DB7)	V_{OH2}	0.8V_{DD}	—	—	I_{OH}=-40uA	V
	V_{OL2}	—	—	0.2V_{DD}	I_{OL}=40uA	
Voltage Drop	Vd_{COM}	—	—	1	I_O = ±0.1mA	V
	Vd_{SEG}	—	—	1,5		
Input Leakage Current	I_{IL}	-1	—	1	V_{IN}=0 V to V_{DD}	uA
Low Input Current	I_{IN}	-10	-50	-120	V_{IN}=0V,V_{DD}=5V(pull up)	
Internal Clock (external Rf)	f_{OSC}	190	250	350	Rf = 75k ± 2% (V_{DD}=3V)	kHz
External Clock	f_{EC}	125	270	350	—	kHz
	duty	45	50	55		%
	t_R,t_F	—	—	0,2		us
LCD Driving Voltage	V_{LCD}	3.0	—	10.0	V_{DD}-V_5 (1/5 Bias)	V

13-2-1 AC Characteristics

(V_{DD} = 4.5V ~ 5.5V, Ta = -20 ~ +70°C)

Mode	Item	Symbol	Min	Typ	Max	Unit
(1) Write Mode (refer to Figure 8.0)	E Cycle Time	t_C	500	—	—	ns
	E Rise/Fall Time	t_R,t_F	—	—	25	
	E Pulse Width (High, Low)	t_w	220	—	—	
	R/W and RS Setup Time	t_{su1}	40	—	—	
	R/W and RS Hold Time	t_{H1}	10	—	—	
	Data Setup Time	t_{su2}	60	—	—	
	Data Hold Time	t_{H2}	10	—	—	
(2) Read Mode (refer to Figure 9.0)	E Cycle Time	t_C	500	—	—	ns
	E Rise/Fall Time	t_R,t_F	—	—	25	
	E Pulse Width (High, Low)	t_w	220	—	—	
	R/W and RS Setup Time	t_{su}	40	—	—	
	R/W and RS Hold Time	t_H	10	—	—	
	Data Out Delay Time	t_D	—	—	120	
	Data Hold Time	t_{DH}	20	—	—	

(V_{DD} = 2.7V ~ 5.5V, Ta = -20 ~ +70°C)

Mode	Item	Symbol	Min	Typ	Max	Unit
(3) Write Mode (refer to Figure 8.0)	E Cycle Time	t_C	1400	—	—	ns
	E Rise/Fall Time	t_R,t_F	—	—	25	
	E Pulse Width (High, Low)	t_w	400	—	—	
	R/W and RS Setup Time	t_{su1}	60	—	—	
	R/W and RS Hold Time	t_{H1}	20	—	—	
	Data Setup Time	t_{su2}	140	—	—	
	Data Hold Time	t_{H2}	10	—	—	
(4) Read Mode (refer to Figure 9.0)	E Cycle Time	t_C	1400	—	—	ns
	E Rise/Fall Time	t_R,t_F	—	—	25	
	E Pulse Width (High, Low)	t_w	450	—	—	
	R/W and RS Setup Time	t_{su}	60	—	—	
	R/W and RS Hold Time	t_H	20	—	—	
	Data Out Delay Time	t_D	—	—	360	
	Data Hold Time	t_{DH}	5	—	—	

13-2-2. Write Mode

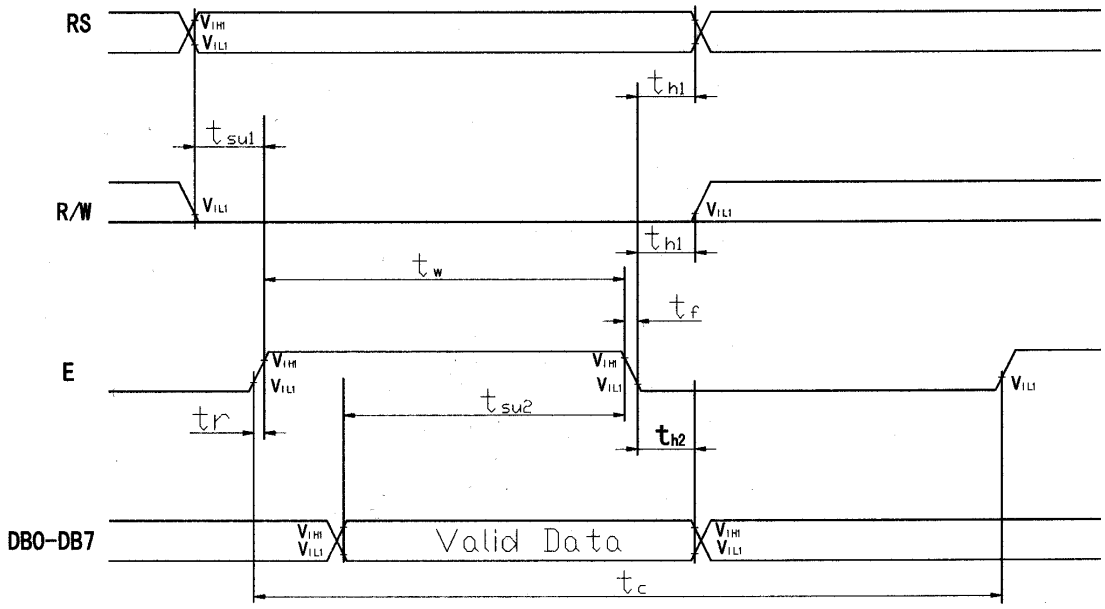


Figure 8.0

13-2-3. Read Mode

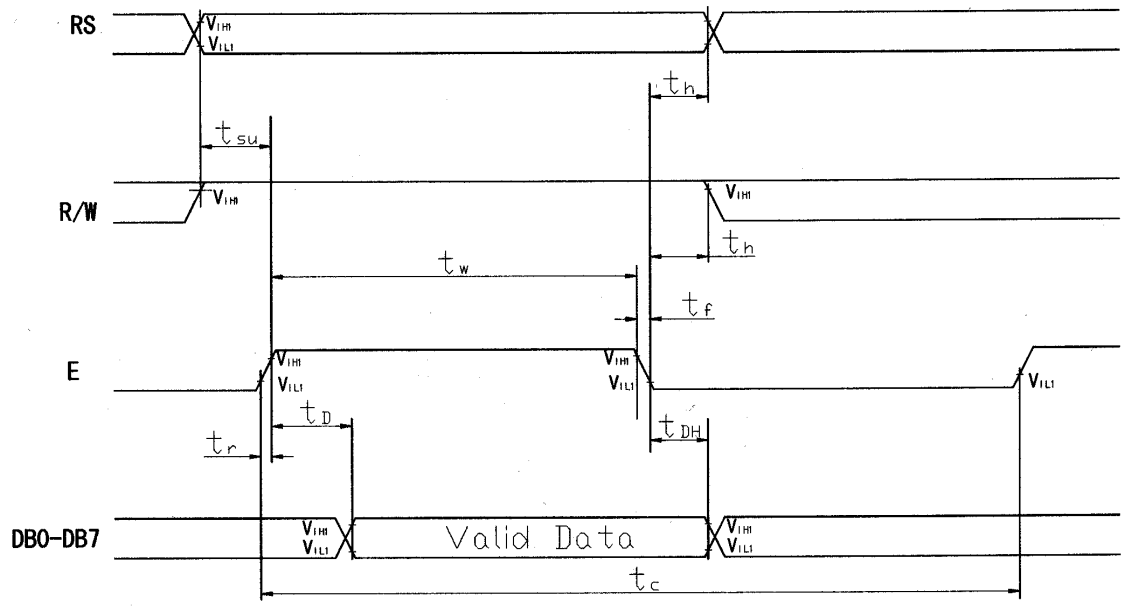


Figure 9.0

14. STANDARD CHARACTER PATTERN

Lower(4bit) \ Upper(4bit)	LLLL	LLLH	LLHL	LLHH	LHLL	LHLH	LHHL	LHHH	HLLL	HLLH	HLHL	HLHH	HHLL	HHLH	HHHL	HHHH
LLLL	CG RAM (1)															
LLLH	(2)															
LLHL	(3)															
LLHH	(4)															
LHLL	(5)															
LHLH	(6)															
LHHL	(7)															
LHHH	(8)															
HLLL	(1)															
HLLH	(2)															
HLHL	(3)															
HLHH	(4)															
HHLL	(5)															
HHLH	(6)															
HHHL	(7)															
HHHH	(8)															

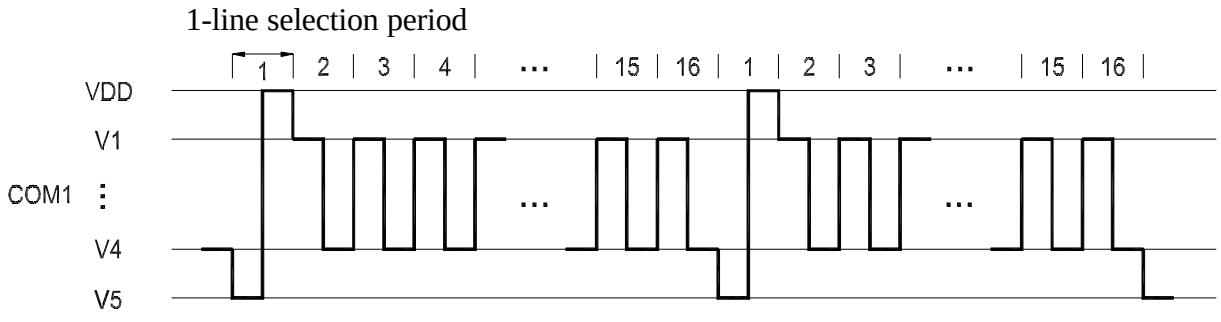
Table 3. Relationship Between character Code (DDRAM) and Character Pattern (CGRAM)

Character Code (DDRAM data)								CGRAM Address						CGRAM Data								Pattern
D7	D6	D5	D4	D3	D2	D1	D0	A5	A4	A3	A2	A1	A0	P7	P6	P5	P4	P3	P2	P1	P0	number
0	0	0	0	x	0	0	0	0	0	0	0	0	0	x	x	x	0				0	Pattern 1
											0	0	1					0	0	0		
											0	1	0					0	0	0		
				⋮						⋮	0	1	1		⋮							
											1	0	0					0	0	0		
											1	0	1					0	0	0		
											1	1	0					0	0	0		
											1	1	0					0	0	0		
											1	1	1				0	0	0	0	0	
				⋮						⋮								⋮				Pattern 8
0	0	0	0	x	1	1	1	1	1	1	0	0	0	x	x	x		0	0	0		
											0	0	1					0	0	0		
											0	1	0					0	0	0		
				⋮						⋮	0	1	1		⋮							
											1	0	0					0	0	0		
											1	0	1					0	0	0		
											1	1	0					0	0	0		
											1	1	1				0	0	0	0	0	

"x": don't care

15. FRAME FREQUENCY (1/16 duty cycle)

A-type Waveform



Item	Clock / Frequency
Line selection period	200 clocks
Frame frequency	84.4 Hz

* fosc = 270 kHz (1 clock = 3.7 us)

Figure 10.0

16. LCD Modules Handling precautions

- The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place ,etc.
- If the display panel is damaged and the liquid crystal substance inside it leaks out , do not get any in your mouth . If the substance come into contact with your skin or clothes promptly wash it off using soap and water.

- Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

- The polarizer covering the display surface of the LCD module is soft and easily scratched. handle this polarize carefully

- To prevent destruction of the elements by static electricity , be careful to maintain an optimum work environment.
  -Be sure to ground the body when handling the LCD Modules.
  -Tools required for assembly, such as soldering irons, must be properly grounded.
  -To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.
  -The LCD Module is coated with a film to protect the display surface. Exercise care when peeling off this protective film since static electricity may be generated.

- Storage Precautions
  When storing the LCD Modules, avoid exposure to direct sunlight or to the light of fluorescent lamps. Keep the modules in bags designed to prevent static electricity charging under low temperature / normal humidity conditions (avoid high temperature / high humidity and low temperatures below 0°C).Whenever possible, the LCD Modules should be stored in the same conditions in which they were shipped from our company.

17. Others

- Liquid crystals solidify at low temperature (below the storage temperature range) leading to defective orientation of liquid crystal or the generation of air bubbles (black or white). Air bubbles may also be generated if the module is subjected to a strong shock at a low temperature.

- If the LCD Modules have been operating for a long time showing the same display patterns the display patterns may remain on the screen as ghost images and a slight contrast irregularity may also appear. Abnormal operating status can be resumed to be normal condition by suspending use for some time.
  It should be noted that this phenomena does not adversely affect performance reliability.

- To minimize the performance degradation of the LCD Modules resulting from caused by static electricity , etc . Exercise care to avoid holding the following sections when handling the modules:
  -Exposed area of the printed circuit board
  -Terminal electrode sections