Device
Engineering
Incorporated

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DEI1148
OCTAL ARINC 429 LINE RECEIVER

FEATURES

- Octal ARINC 429 to TTL/CMOS logic line receivers
- Operates from single +5 V ± 10% or 3.3 V ± 10% power supply
- Operates in high noise environment
  - Input Common Voltage Range: ± 20 V
  - 2 V minimum Input hysteresis
- ARINC inputs internally protected to lightning requirements of DO-160 Level A3
- Withstands inadvertent short to 115 Vac on inputs
- Package: 44L MQFP, 13.9mm footprint

PINOUT

PIN	NAME	DESCRIPTION
15, 13, 11, 9, 2, 44, 42, 40	IN[8:1]A	429 INPUTS. ARINC 429 format serial digital data "A" inputs.
16, 14, 12, 10, 3, 1, 43, 41	IN[8:1]B	429 INPUTS. ARINC 429 format serial digital data "B" inputs.
5	TESTAA	LOGIC INPUT. Test input A (+) for odd channels.
6	TESTAB	LOGIC INPUT. Test input A (-) for odd channels.
7	TESTBA	LOGIC INPUT. Test input B (+) for even channels.
8	TESTBB	LOGIC INPUT. Test input B (-) for even channels.
19, 21, 23, 25, 32, 34, 36, 38	OUT[8:1]A	LOGIC OUTPUTS. CMOS/TTL format serial digital data "A" outputs.
18, 20, 22, 24, 31, 33, 35, 37	OUT[8:1]B	LOGIC OUTPUTS. CMOS/TTL format serial digital data "B" outputs.
29	VDD	POWER INPUT. 5 V OR 3.3 V.
27	VSS	POWER INPUT. Ground.

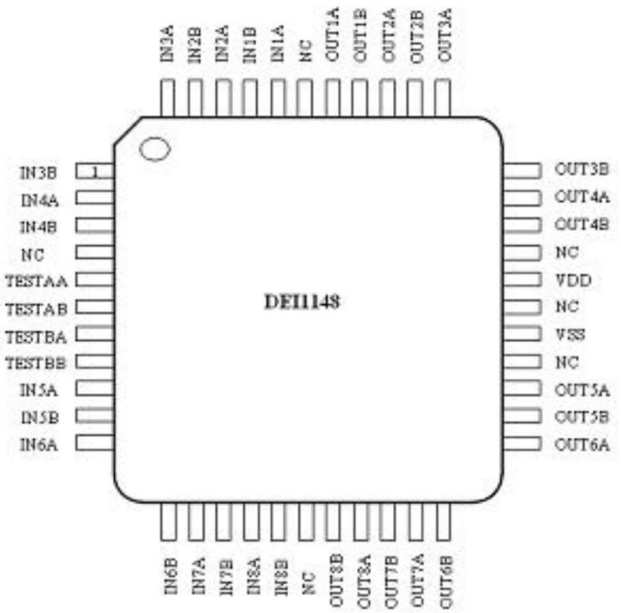


Figure 1 DEI1148 Pinout

FUNCTIONAL DESCRIPTION

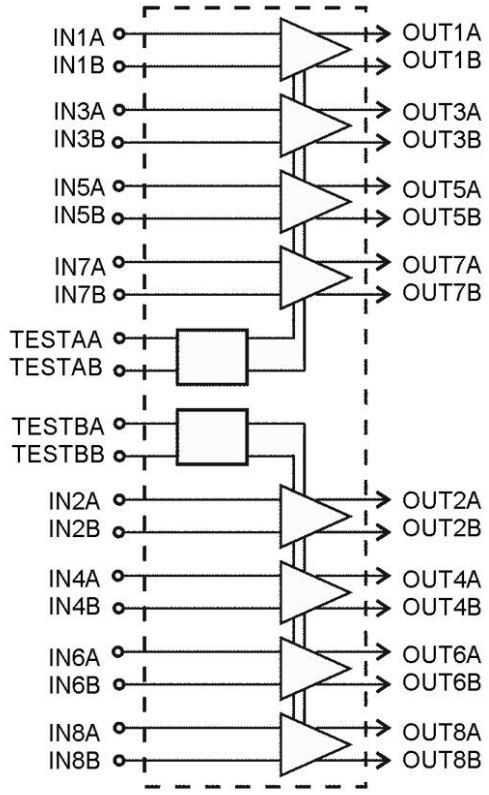
The DEI1148 is a BiCMOS device which contains eight differential line receivers. Each receiver channel translates incoming ARINC 429 data bus signals (tri-level RZ bipolar differential modulation) to a pair of TTL/CMOS logic outputs. Each channel operates independently and meets the requirements of the ARINC 429 Digital Information Transfer Standard. Refer to Figure 2 DEI1148 Block Diagram and Truth Table.

The device is designed to operate in a high noise environment. Inputs are accepted over a ±20 V common mode voltage range and the receivers provide over 2 Volts of hysteresis. Circuit speed is optimized to reject high frequency transients.

The DEI1148 device provides logic level TEST inputs for built in system test. There are two TEST input ports, each force the outputs of four receivers to the specified ZERO, ONE or NULL state. The ARINC inputs are ignored when the device is in test mode.

The ARINC inputs incorporate on-chip lightning protection by use of high value resistors on the inputs to minimize IR heating. The resistors have dielectric isolation to withstand the voltage transients. The inputs withstand lightning induced transients up to and including DO160 Level 3 pin injection levels. Higher levels can be achieved with the addition of external TVS devices between the inputs and VSS, or alternately, TVS devices in combination with series current limiting resistors between the ARINC bus and the IC/TVS node. The series resistors reduce the power requirement and size of the TVS. Resistor values up to 10K ohms are feasible.

The ARINC inputs withstand inadvertent short to 115 Vac aircraft power without sustaining damage.



INPUTS			OUTPUTS		
TEST INPUTS (TTL/CMOS)		ARINC INPUTS	TTL/CMOS		
TESTA	TESTB	INA - INB	OUTA	OUTB	Logic
0	0	Logic +1	1	0	ONE
0	0	Logic -1	0	1	ZERO
0	0	NULL	0	0	NULL
0	1	X	0	1	ZERO
1	0	X	1	0	ONE
1	1	X	0	0	NULL

Figure 2 DEI1148 Block Diagram and Truth Table

ELECTRICAL DESCRIPTION

Table 1: Absolute Maximum Rating

PARAMETER	MIN	MAX	UNITS
Supply Voltage (with respect to VSS)	-0.3	7.0	V
Storage Temperature	-65	+150	°C
Input Voltage, continuous (ARINC Inputs)		115	Vac
Power Dissipation @ 85 °C		800	mW
Junction Temperature, Tjmax (limited by molding compound Tg)		145	°C
Peak Body Temperature		260	°C
Lightning Protection (ARINC 429 Channel Inputs) Waveform 3 (2) Waveform 4, 5A, 5B (2) (3)	 -720 -360	 +720 +360	 V V
ESD JS-001-2017 HBM	1B		Class

Notes:

1. Stresses above these limits can cause permanent damage.
2. Per DO160, Sect 22 Level 3 pin injection. See Figures 5 – 7.
3. Inputs can be protected to withstand higher stress by adding series resistors and shunt TVS on inputs. Inputs withstand 1500 V Waveform 5A when clipped ≤ 600 V.

Table 2: Recommended Operating Conditions

PARAMETER	SYMBOL	CONDITIONS
Supply Voltage	VDD	+5 V ±10% +3.3 V ±10%
Logic Input Levels	TESTA/B	0 to VDD
Operating Temperature -QES -QMS	Ta	 -55 to +85 °C -55 to +125 °C

Table 3: Electrical Characteristics

Conditions: Temperature: -55 °C to +85 °C (-QES); -55 °C to +125 °C (-QMS)
VDD = +5 V ±10% or 3.3 V ±10%

PARAMETER	TEST CONDITION	SYMBOL	MIN	MAX	UNITS
ARINC INPUTS					
$V_A - V_B$ = Logic +1	OUTA = 1	V_{+1}	6.5	13	V
$V_A - V_B$ = Logic -1	OUTB = 1	V_{-1}	-6.5	-13	V
$V_A - V_B$ = Logic Null	OUTA = 0 OUTB = 0	V_{NULL}	-2.5	2.5	V
Input Hysteresis		V_{HY}	2.0	4.0	V
Input Common Mode Voltage Range	Logic +1, Null, Logic -1	V_{CM}	-20	+20	V
Input Resistance IN_A to IN_B	VDD open, Shorted to VSS or +5 V (1)	R_{IN}	280		kΩ
Input Resistance IN_A or IN_B to V_{SS}	VDD open, Shorted to VSS or +5 V	R_S	140		kΩ
Input Capacitance IN_A to IN_B	VDD open, Shorted to VSS or +5 V (1)	C_{IN}		10	pF
Input Capacitance IN_A or IN_B to V_{SS}	VDD open, Shorted to VSS or +5 V (1)	C_S		10	pF
LOGIC INPUTS					
Logic 0 Voltage		V_{IL}		0.8	V
Logic 1 Voltage		V_{IH}	2.0		V
Logic 0 Current	V_{IL} = 0.8	I_{IL}		25	µA
Logic 1 Current	V_{IH} = 2.0	I_{IH}		25	µA
LOGIC OUTPUTS					
OUTPUT HIGH VOLTAGE TTL	I_{OH} = -5 mA (VDD = 5.0 V) I_{OH} = -5 mA (VDD = 3.3 V) TTL Compatible	V_{OH}	2.4		V
OUTPUT LOW VOLTAGE TTL	I_{OL} = 5mA (VDD = 5.0 V)	V_{OL}		0.4	V
OUTPUT HIGH VOLTAGE CMOS	I_{OH} = 100 µA CMOS Compatible	V_{OH}	V_{DD} – 50mV		V
OUTPUT LOW VOLTAGE CMOS	I_{OL} = 100 µA CMOS Compatible	V_{OL}		V_{SS} + 50mV	V
SUPPLY CURRENT					
VDD Current	Data Rate = 0 MHZ, INA/B = open, OUTA/B = open, VDD = 5.5 V or 3.63 V	I_{DD}	1.5	8.5	mA

Notes:
1. Guaranteed by design, not production tested.
2. Current flowing into device is positive. Current flowing out of device is negative. All voltages are with respect to VSS unless otherwise noted.

Table 4: Switching Characteristics

PARAMETER	TEST CONDITION (1,2)	SYMBOL	MAX VDD 3.3V	MAX VDD 5V	UNITS
INA/B to OUTA/B Prop Delay	TESTA = TESTB = 0 C_L = 50 pF	t_{LH}	1000	900	ns
INA/B to OUTA/B Prop Delay	TESTA = TESTB = 0 C_L = 50 pF	t_{HL}	1000	900	ns
OUTA/B rise time	10% to 90%, C_L = 50 pF	t_r	50	25	ns
OUTA/B fall time	10% to 90%, C_L = 50 pF	t_f	50	25	ns
TESTA/B to OUTA/B Prop delay	C_L = 50 pF	t_{TOH}	100	60	ns
TESTA/B to OUTA/B Prop delay	C_L = 50 pF	t_{TOL}	100	60	ns

Notes:
1. Refer to Figures 3 - 4.
2. Sample tested

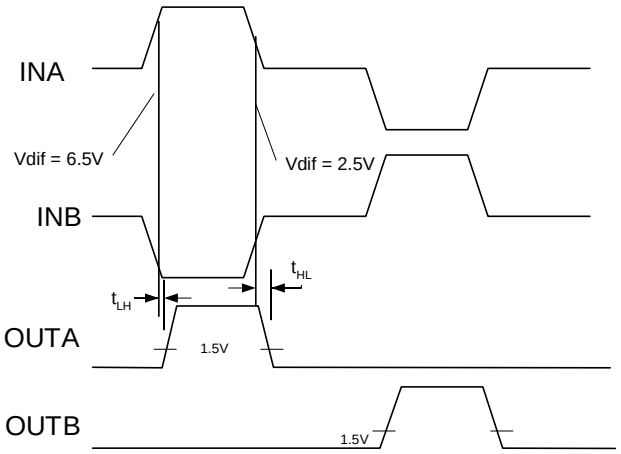


Figure 3 ARINC 429 Input to Logic Output Switching Waveform

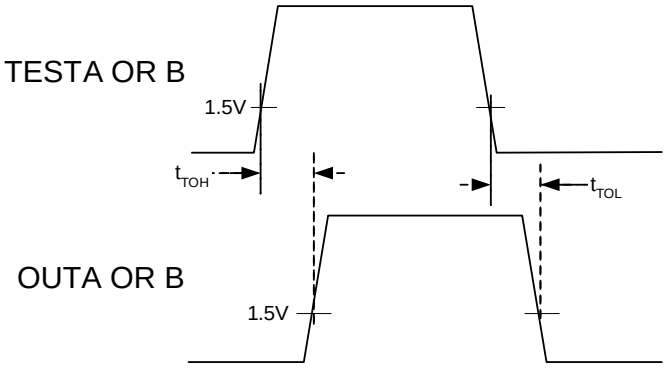


Figure 4 TEST Input to Logic Output Switching Waveform

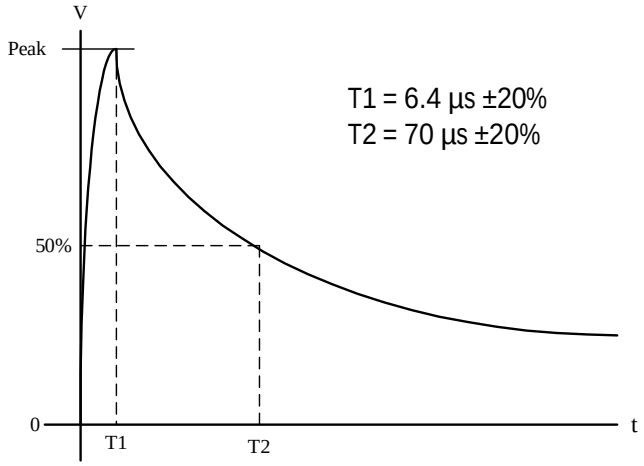


Figure 5 DO160 Lightning Induced Transient Voltage Waveform #4 Pin Injection
Voc = 300 V, Isc = 60 A.

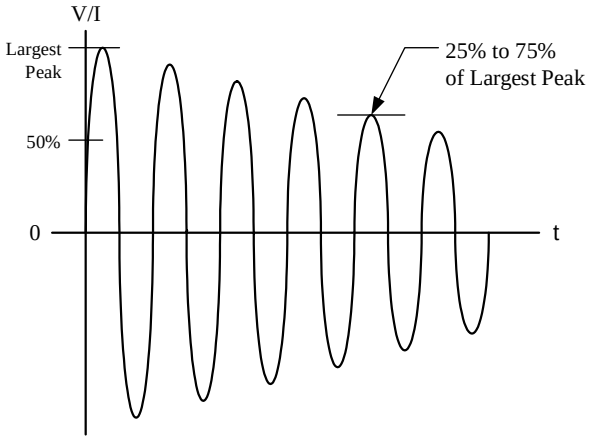


Figure 6 DO160 Lightning Induced Transient Voltage Waveform #3 Pin Injection
Voc = 600 V, Isc = 24 A. Freq = 1 MHZ ±20%

LIGHTNING TRANSIENT NOTES:

1. Voc = Peak Open Circuit Voltage available at the calibration point.
2. Isc = Peak Short Circuit Current available at the calibration point.
3. Amplitude tolerances: +10%, -0%.
4. The ratio of Voc to Isc is the generator source impedance to be used for generating the waveforms.

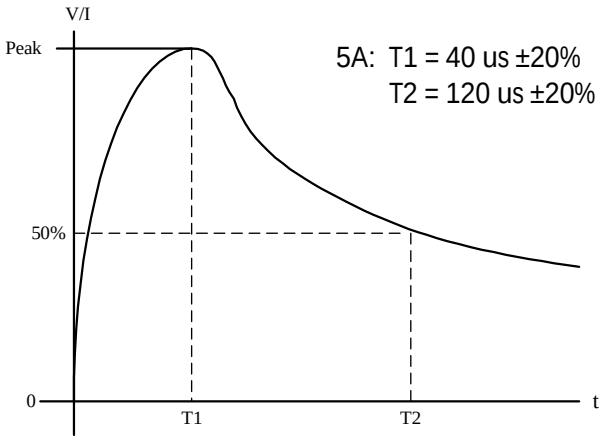


Figure 5 DO160 Lightning Induced Transient Voltage Waveform #5A Pin Injection.
Voc = 300 V, Isc = 300 A

ORDERING INFORMATION

Table 5: Ordering Information

DEI PN	MARKING (1)	TEST INPUTS	TEMPERATURE RANGE	PACKAGE	SCREENING
DEI1148-QES-G	DEI1148-QES (e3)	YES	-55/+85 °C	44L MQFP G	Standard
DEI1148-QMS-G	DEI1148-QMS (e3)	YES	-55/+125 °C	44L MQFP G	Standard

Notes:
1. All packages marked with Lot Code and Date Code. (e3) after Date Code denotes Pb Free category.

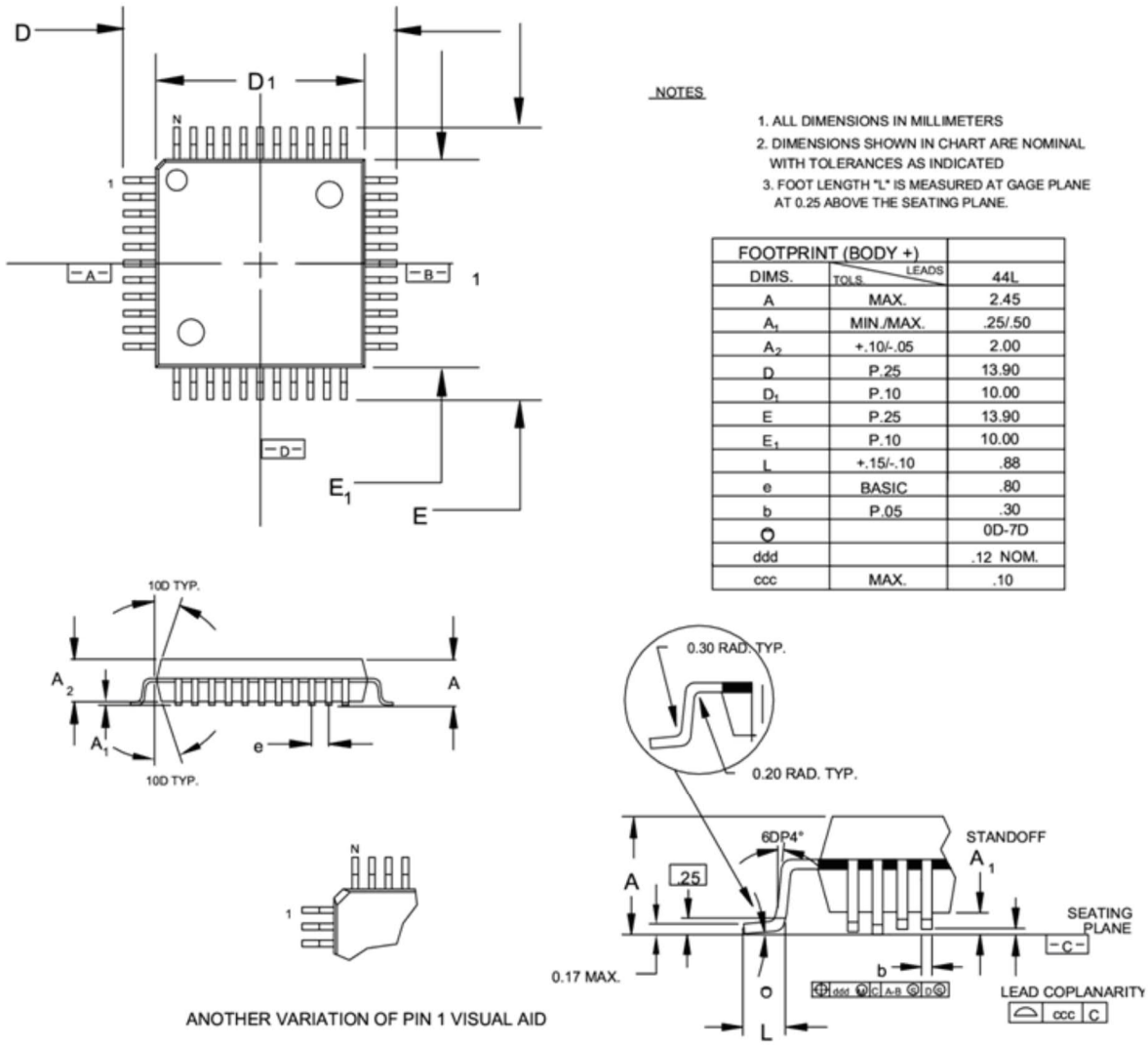
Table 6: Screening Process

SCREENING	STANDARD
ELECTRICAL TEST:	
ROOM TEMPERATURE	100%
HIGH TEMPERATURE	100% @ 85 °C or 125 °C
LOW TEMPERATURE	0.65% AQL @ -55 °C

PACKAGE DESCRIPTION

Table 7: Package Characteristics

CHARACTERISTIC	VALUE
REFERENCE	44L MQFP G
Θ_{JA} (4 layer PCB with Power Planes)	52 °C/W
Θ_{JC}	12 °C/W
JEDEC MOISTURE SENSITIVITY LEVEL (MSL)	MSL 3 / 260 °C
LEAD FINISH MATERIAL / JEDEC Pb-free CODE	Matte Sn e3
Pb-Free DESIGNATION	RoHS Compliant
JEDEC REFERENCE	MO-112 VAR AA-11



NOTES

1. ALL DIMENSIONS IN MILLIMETERS
2. DIMENSIONS SHOWN IN CHART ARE NOMINAL WITH TOLERANCES AS INDICATED
3. FOOT LENGTH "L" IS MEASURED AT GAGE PLANE AT 0.25 ABOVE THE SEATING PLANE.

FOOTPRINT (BODY +)		
DIMS.	TOLS. / LEADS	44L
A	MAX.	2.45
A_1	MIN./MAX.	.25/.50
A_2	+.10/-.05	2.00
D	P.25	13.90
D_1	P.10	10.00
E	P.25	13.90
E_1	P.10	10.00
L	+.15/-.10	.88
e	BASIC	.80
b	P.05	.30
O		0D-7D
ddd		.12 NOM.
ccc	MAX.	.10

Figure 6 44L PQFP Mechanical Outline

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