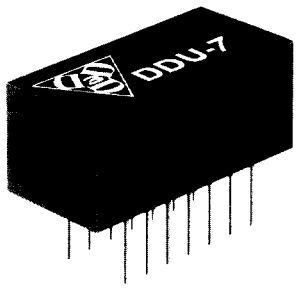
Digital Delay Units

SERIES DDU-7

10 Taps (14 pins DIP)
T²L Interfaced

data delay devices, inc.



(Military Type)

Features:

- **Completely interfaced for TTL and DTL application**
- **No external components required**
- **P.C. board space economy achieved**
- **Fits standard 14 pins DIP socket**
- **Operates over full military temperature range**

Specifications:

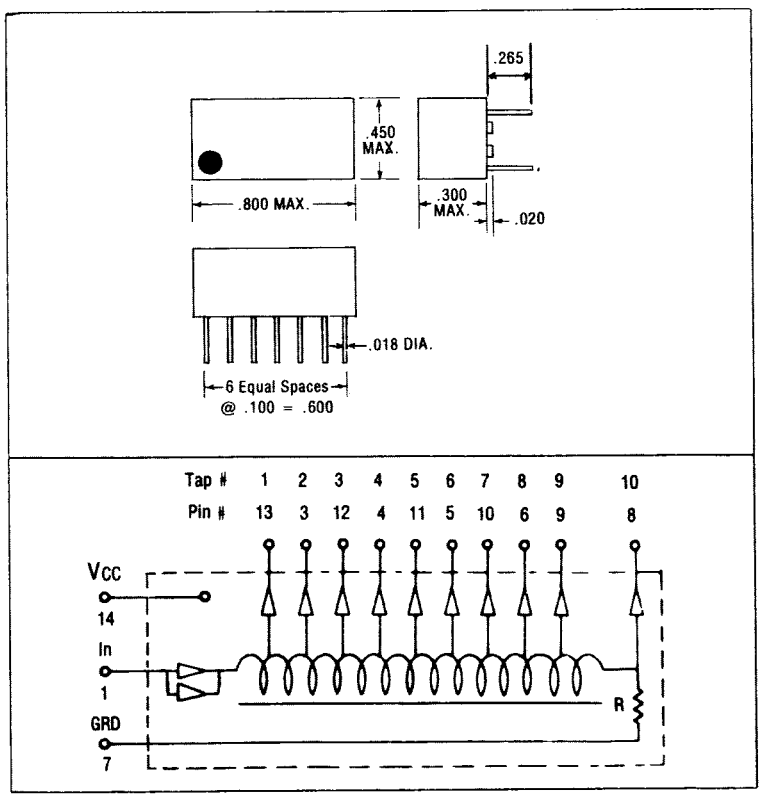
- **No. Taps:** 10 equally spaced taps
- **Total Delay Tolerance:** ±5% or better, or 2 NS whichever is greater.
- **Rise-time:** 4 NS typically
- **Temperature coefficient:** 100 PPM/°C
- **Temperature range:** −55°C to +125°C
- **Supply voltage:** 4.5 to 5.5 Vdc.
- **Logic 1 input current:** 100 μa max.
- **Logic 0 input current:** −4 ma. max.
- **Logic 1 V out:** 2.5 V min.
- **Logic 0 V out:** 0.5 V max.
- **Logic 1 Fan-out:** 20/tap max.
- **Logic 0 Fan-out:** 10/tap max.
- **Power Dissipation:** 740 MW max.

Test Conditions:

- Input Pulse Width: ⩾150% of total delay.
- Time delay measured @ 1.5 V on rising edge.
- Unless otherwise specified all time-delays are referenced to input of delay line.
- Rise-time is measured from .75 V to 2.4 V of leading edge.
- All measurements made @ V_{CC} = 5V; T_A = +25°C.

Part No.	Total Delay NS	Delay Per Tap NS
*DDU-7-10	9	1 ± .4
*DDU-7-20	18	2 ± .5
*DDU-7-25	22.5	2.5 ± .7
*DDU-7-50	45	5.0 ±1.5
DDU-7-100	100	10.0 ±2.0
DDU-7-150	150	15.0 ±2.0
DDU-7-200	200	20.0 ±2.0
DDU-7-250	250	25.0 ±2.0
DDU-7-300	300	30.0 ±3.0
DDU-7-400	400	40.0 ±4.0
DDU-7-500	500	50.0 ±5.0

*Time delay referenced to 1st tap. Two (2) gates in parallel for input buffer. 6 NS ± 1 NS inherent delay.



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