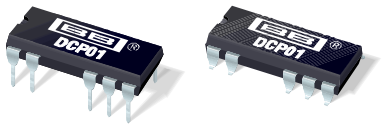
Burr-Brown Products
from Texas Instruments



SBVS012B − DECEMBER 2000 − REVISED OCTOBER 2004

Miniature, 1W Isolated UNREGULATED DC/DC CONVERTERS

FEATURES

- **Up To 85% Efficiency**
- **Thermal Protection**
- **Device-to-Device Synchronization**
- **Short-Circuit Protection**
- **EN55022 Class B EMC Performance**
- **UL1950 Recognized Component**
- **JEDEC DIP-14 and SOP-14 Packages**

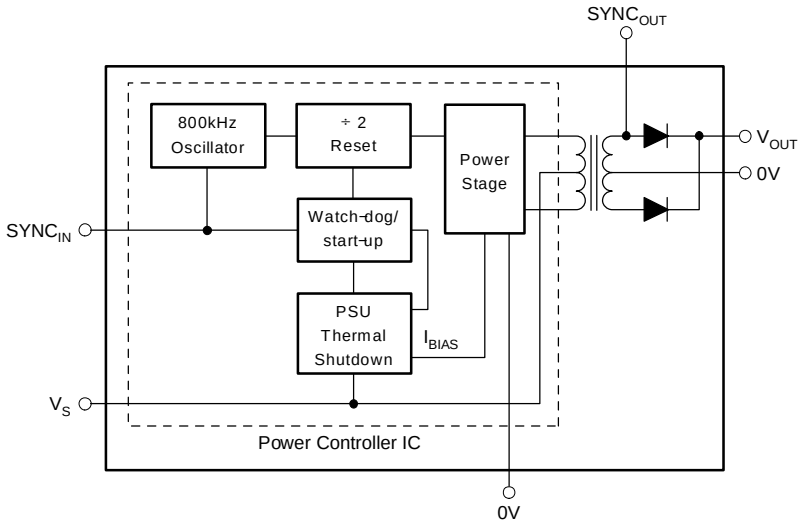
APPLICATIONS

- **Point-of-Use Power Conversion**
- **Ground Loop Elimination**
- **Data Acquisition**
- **Industrial Control and Instrumentation**
- **Test Equipment**

DESCRIPTION

The DCP01B series is a family of 1W, unregulated, isolated DC/DC converters. Requiring a minimum of external components and including on-chip device protection, the DCP01B series provides extra features such as output disable and synchronization of switching frequencies.

The use of a highly-integrated package design results in highly reliable products with a power density of 40W/in^3 (2.4W/cm^3). This combination of features and small sizes makes the DCP01B suitable for a wide range of applications.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

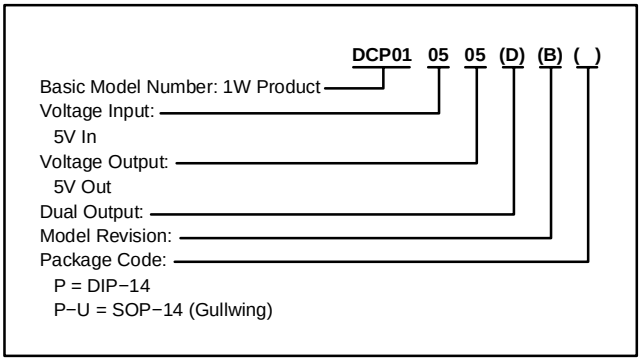
ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

		DCP01B SERIES	UNIT
Input voltage	5V models	7	V
	15V models	18	V
	24V models	29	V
Storage temperature		−40 to +125	°C
Lead temperature (soldering, 10s)		+270	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

SUPPLEMENTAL ORDERING INFORMATION



ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER(2)	TRANSPORT MEDIA
SINGLE VOLTAGE(3)						
DCP010505	DIP-14	NVA	−40°C to +100°C	DCP010505BP	DCP010505BP	Rails
	SOP-14(4)	DUA	−40°C to +100°C	DCP010505BP−U	DCP010505BP−U/700	Tape and Reel
DCP010512	DIP-14	NVA	−40°C to +100°C	DCP010512BP	DCP010512BP	Rails
	SOP-14(4)	DUA	−40°C to +100°C	DCP010512BP−U	DCP010512BP−U/700	Tape and Reel
DCP010515	DIP-14	NVA	−40°C to +100°C	DCP010515BP	DCP010515BP	Rails
	SOP-14(4)	DUA	−40°C to +100°C	DCP010515BP−U	DCP010515BP−U/700	Tape and Reel
DCP012405	DIP-14	NVA	−40°C to +100°C	DCP012405BP	DCP012405BP	Rails
	SOP-14(4)	DUA	−40°C to +100°C	DCP012405BP−U	DCP012405BP−U/700	Tape and Reel
DUAL VOLTAGE(3)						
DCP010505	DIP-14	NVA	−40°C to +100°C	DCP010505DBP	DCP010505DBP	Rails
	SOP-14(4)	DUA	−40°C to +100°C	DCP010505DBP−U	DCP010505DBP−U/700	Tape and Reel
DCP010512	DIP-14	NVA	−40°C to +100°C	DCP010512DBP	DCP010512DBP	Rails
	SOP-14(4)	DUA	−40°C to +100°C	DCP010512DBP−U	DCP010512DBP−U/700	Tape and Reel
DCP010515	DIP-14	NVA	−40°C to +100°C	DCP010515DBP	DCP010515DBP	Rails
	SOP-14(4)	DUA	−40°C to +100°C	DCP010515DBP−U	DCP010515DBP−U/700	Tape and Reel
DCP011512	DIP-14	NVA	−40°C to +100°C	DCP011512DBP	DCP011512DBP	Rails
	SOP-14(4)	DUA	−40°C to +100°C	DCP011512DBP−U	DCP011512DBP−U/700	Tape and Reel
DCP011515	DIP-14	NVA	−40°C to +100°C	DCP011515DBP	DCP011515DBP	Rails
	SOP-14(4)	DUA	−40°C to +100°C	DCP011515DBP−U	DCP011515DBP−U/700	Tape and Reel
DCP012415	DIP-14	NVA	−40°C to +100°C	DCP012415DBP	DCP012415DBP	Rails
	SOP-14(4)	DUA	−40°C to +100°C	DCP012415DBP−U	DCP012415DBP−U/700	Tape and Reel

(1) All devices also available in tray quatities. For the most current package and ordering information, see the Package Option Addendum at the end of this data sheet, or refer to our web site at www.ti.com.
(2) Models with a (*/*) are available only in Tape and Reel in the quantities indicated (for example, ***/700*** indicates 700 devices per reel). Ordering 700 pieces of "DCP010505BP−U/700" will get a single 700-piece Tape and Reel.
(3) Single voltage versions have six active pins; dual voltage versions have seven active pins.
(4) SOP package is gullwing surface-mount.

ELECTRICAL CHARACTERISTICS

At T_A = +25°C, V_S = nominal, C_{IN} = 2.2µF, and C_{OUT} = 0.1µF, unless otherwise noted.

PARAMETER	TEST CONDITIONS	DCP01B SERIES MIN	DCP01B SERIES TYP	DCP01B SERIES MAX	UNITS
Output					
Power	100% full load		0.97		W
Ripple	O/P capacitor = 1µF, 50% load		20		mV_{PP}
Voltage vs Temperature	Room to cold		0.046		%/°C
	Room to hot		0.016		%/°C
Input					
Voltage range on V_S		−10		+10	%
Isolation					
Voltage	1s flash test	1			kVrms
	60s test, UL1950(1)	1			kVrms
Line Regulation					
Voltage Source (V_S)	Minimum $V_S \le I_O$ constant ≤ typical V_S Typical $V_S \le I_O$ constant ≤ maximum V_S		1	15(2)	% change of V_S
Switching/Synchronization					
Oscillator frequency (f_{OSC})	Switcing frequency = $f_{OSC}/2$		800		kHz
Sync input low				0.4	V
Sync input current	V_{SYNC} = +2V		75		µA
Disable time			2		µs
Capacitance loading on $SYNC_{IN}$ pin	External			3	pF
Reliability					
Demonstrated	MSL 3−(U) versions T_A = +55°C	−40		+70	°C
Thermal Shutdown					
IC temperature at shutdown			+150		°C
Shutdown current			3		mA
Temperature Range					
Operating		−40		+100	°C

(1) During UL1950 recognition tests only.
(2) Line regulation is measured at constant load current. Line regulation = (V_{OUT} at I_{OUT} fixed)/V_S. Variation % = V_S min to V_S typ, V_S typ to V_S max.

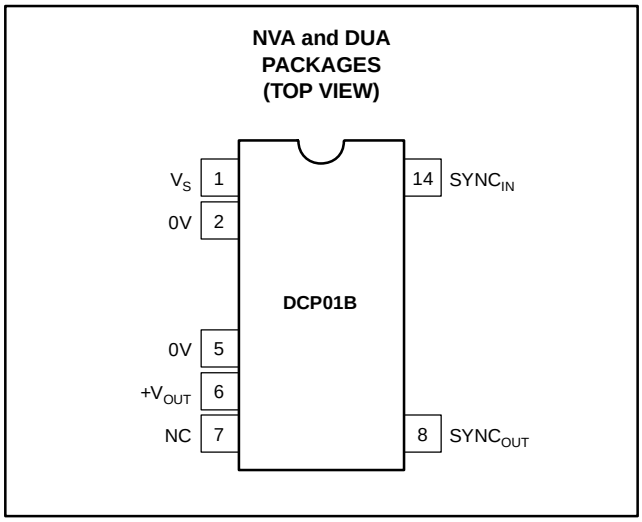
ELECTRICAL CHARACTERISTICS PER DEVICE

At T_A = +25°C, V_S = nominal, C_{IN} = 2.2µF, and C_{OUT} = 0.1µF, unless otherwise noted.

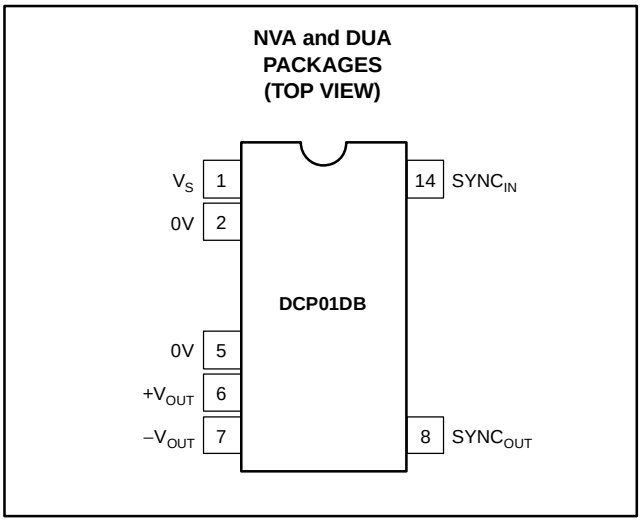
	INPUT VOLTAGE (V)			OUTPUT VOLTAGE (V)			LOAD REGULATION (%)		NO LOAD CURRENT (mA)	EFFICIENCY (%)	BARRIER CAPACITANCE (pF)
	V_S			$V_{NOM} = V_S$ Typical					I_Q		C_{ISO}
				75% LOAD(3)			10% TO 100% LOAD(4)		0% LOAD	100% LOAD	$V_{ISO} = 750V_{RMS}$
PRODUCT	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**TYP**	**MAX**	**TYP**	**TYP**	**TYP**
DCP010505B	4.5	5	5.5	4.75	5	5.25	19	31	20	80	3.6
DCP010505DB	4.5	5	5.5	±4.25	±5	±5.75	18	32	22	81	3.8
DCP010512B	4.5	5	5.5	11.4	12	12.6	21	38	29	85	5.1
DCP010512DB	4.5	5	5.5	±11.4	±12	±12.6	19	37	40	82	4.0
DCP010515B	4.5	5	5.5	14.25	15	15.75	26	42	34	82	3.8
DCP010515DB	4.5	5	5.5	±14.25	±15	±15.75	19	41	42	85	4.7
DCP011512DB	13.5	15	16.5	±11.4	±12	±12.6	11	39	19	78	2.5
DCP011515DB	13.5	15	16.5	±14.25	±15	±15.75	12	39	20	80	2.5
DCP012405B	21.6	24	26.4	4.75	5	5.25	13	23	14	77	2.5
DCP012415DB	21.6	24	26.4	±14.25	±15	±15.75	10	35	17	76	3.8

(3) 100% load current = 1W/V_S typical.
(4) Load regulation = (V_{OUT} at 10% load − V_{OUT} at 100% load)/V_{OUT} at 75% load.

PIN ASSIGNMENTS (Single Voltage Version)



PIN ASSIGNMENTS (Dual Voltage Version)



Terminal Functions (Single Voltage)

TERMINAL NAME	NO.	I/O	DESCRIPTION
V_S	1	I	Voltage input
0V	2	I	Input side common
0V	5	O	Output side common
$+V_{OUT}$	6	O	+Voltage out
NC	7		Not connected
$SYNC_{OUT}$	8	O	Unrectified transformer output
$SYNC_{IN}$	14	I	Synchronization pin

NOTE: I = input and O = output.

Terminal Functions (Dual Voltage)

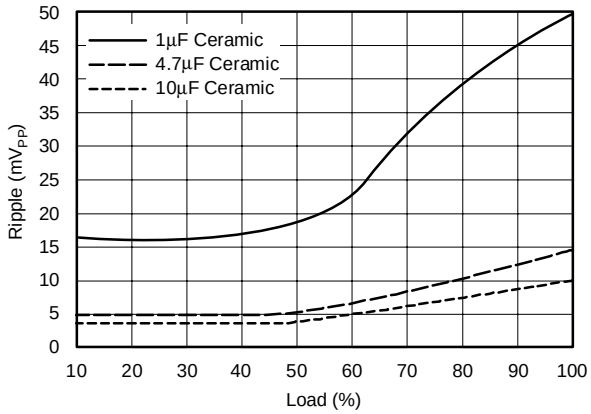
TERMINAL NAME	NO.	I/O	DESCRIPTION
V_S	1	I	Voltage input
0V	2	I	Input side common
0V	5	O	Output side common
$+V_{OUT}$	6	O	+Voltage out
$-V_{OUT}$	7	O	−Voltage out
$SYNC_{OUT}$	8	O	Unrectified transformer output
$SYNC_{IN}$	14	I	Synchronization pin

NOTE: I = input and O = output.

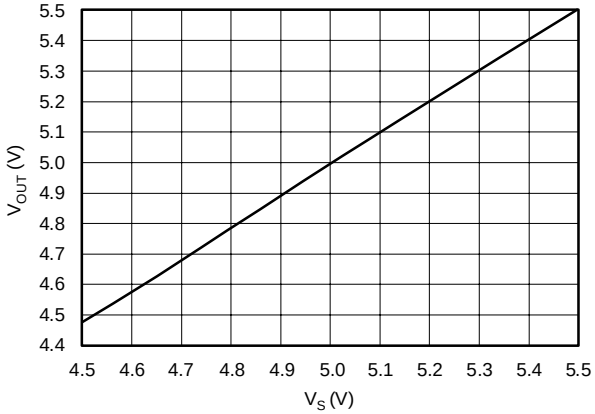
TYPICAL CHARACTERISTICS

At T_A = 25°C, unless otherwise noted.

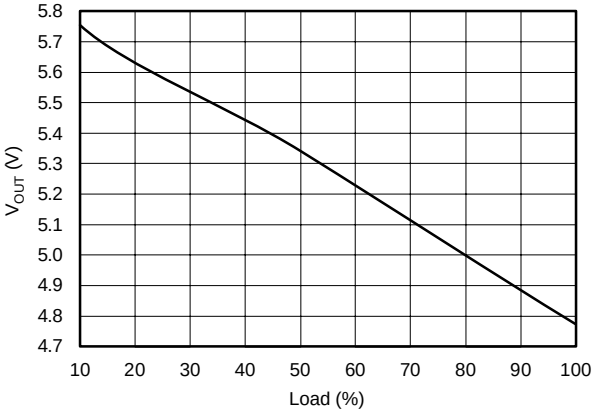
DCP010505B
OUTPUT RIPPLE vs LOAD (20MHz BW)



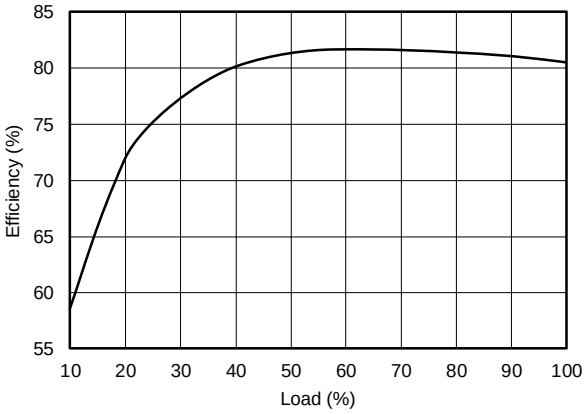
DCP010505B V_{OUT} vs V_S



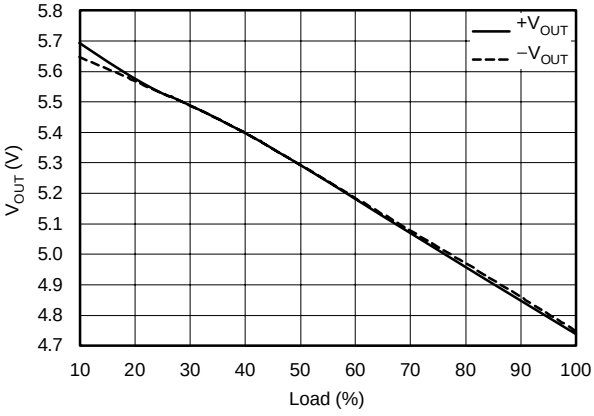
DCP010505B V_{OUT} vs LOAD



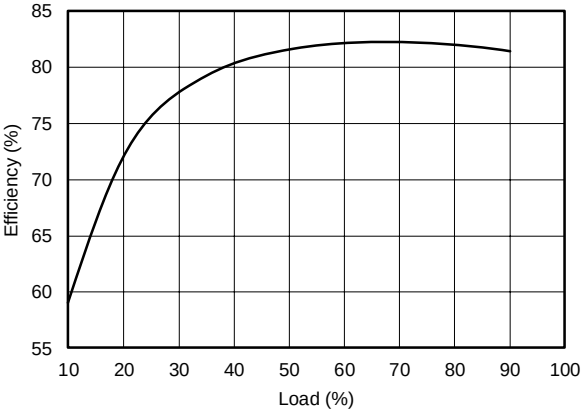
DCP010505B EFFICIENCY vs LOAD



DCP010505DB V_{OUT} vs LOAD



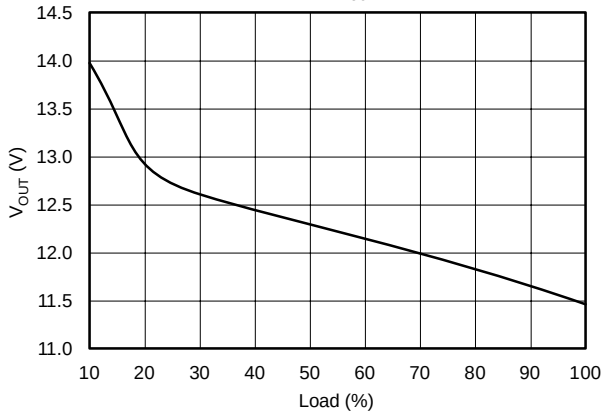
DCP010505DB EFFICIENCY vs LOAD



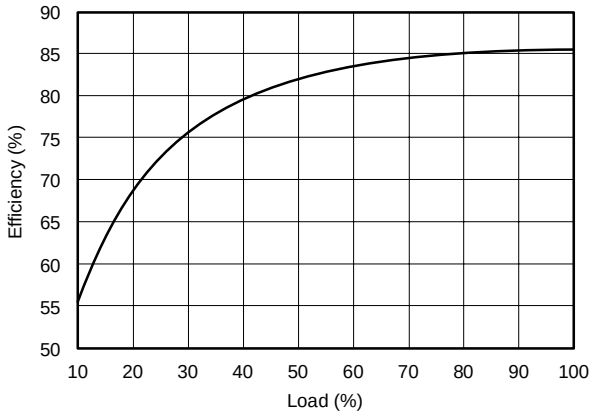
TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C, unless otherwise noted.

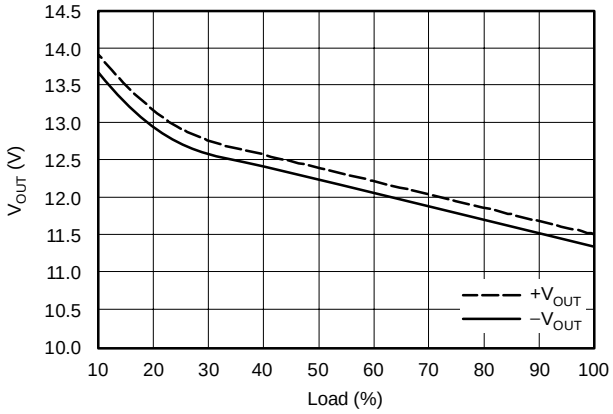
DCP010512B V_{OUT} vs LOAD



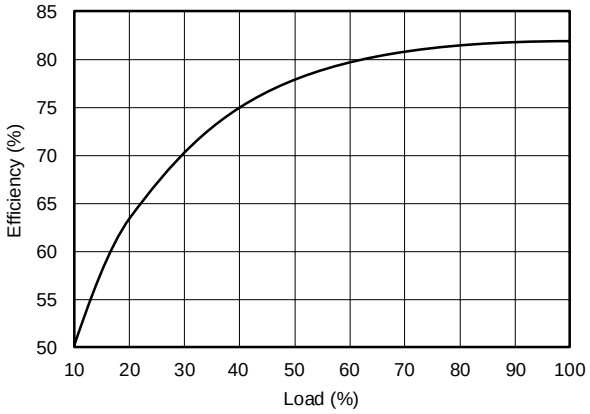
DCP010512B EFFICIENCY vs LOAD



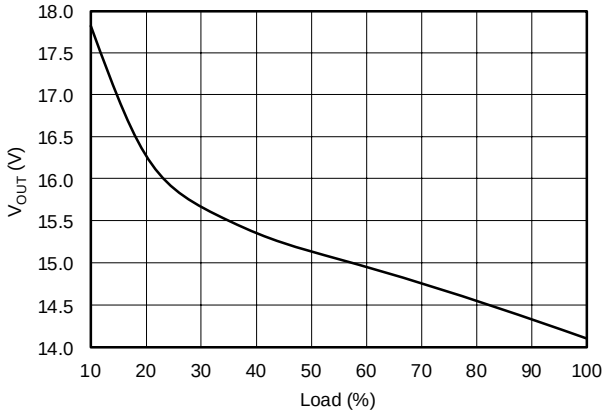
DCP010512DB V_{OUT} vs LOAD



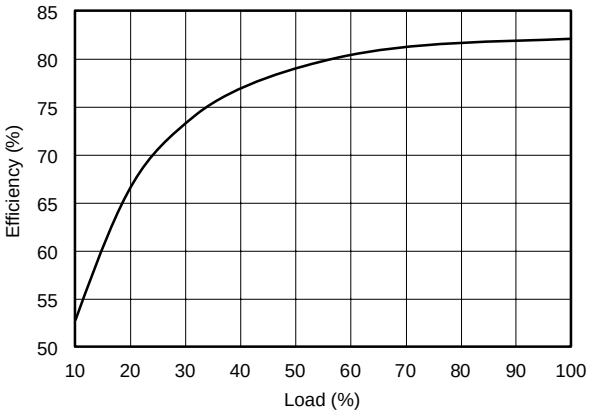
DCP010512DB EFFICIENCY vs LOAD



DCP010515B V_{OUT} vs LOAD



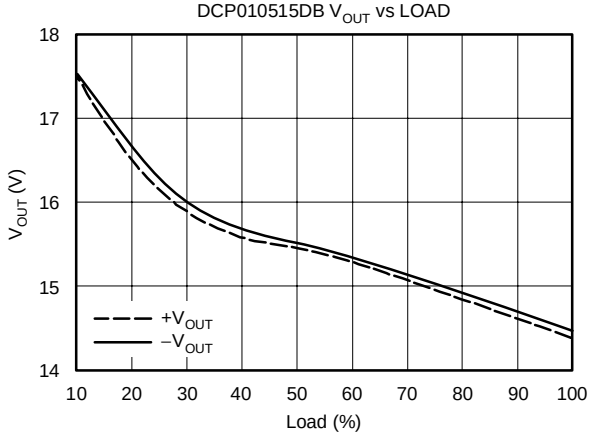
DCP010515B EFFICIENCY vs LOAD



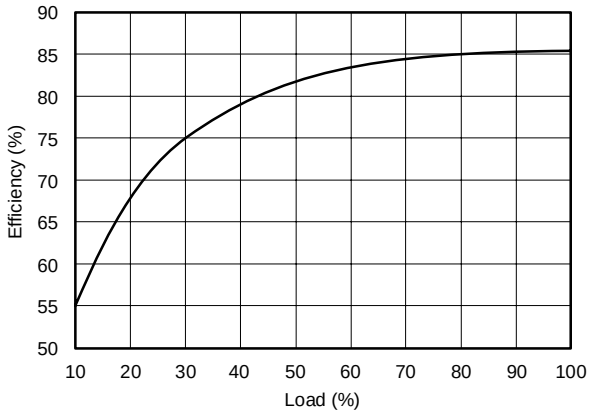
TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C, unless otherwise noted.

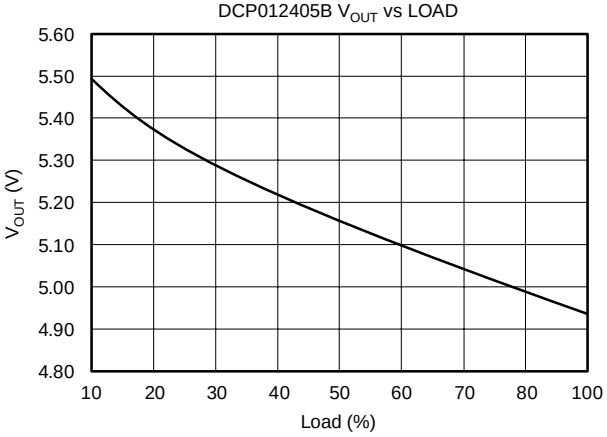
DCP010515DB V_{OUT} vs LOAD



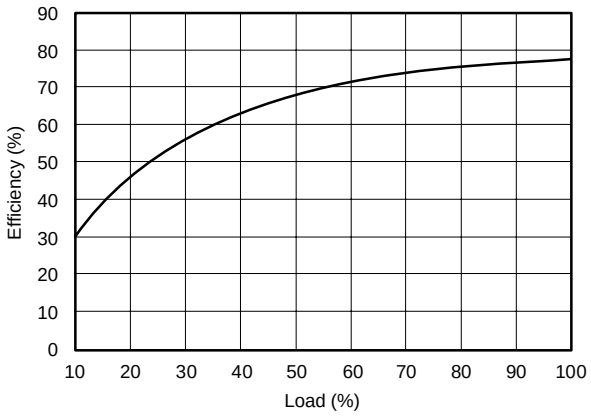
DCP010515DB EFFICIENCY vs LOAD



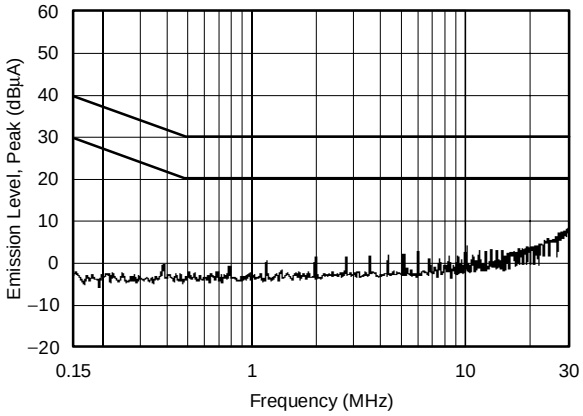
DCP012405B V_{OUT} vs LOAD



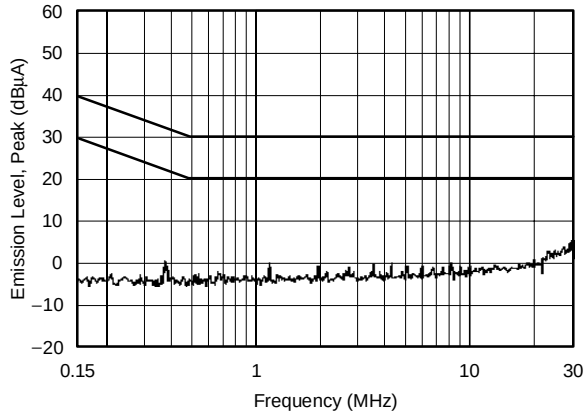
DCP012405B EFFICIENCY vs LOAD



DCP010505B
CONDUCTED EMISSIONS (125% Load)



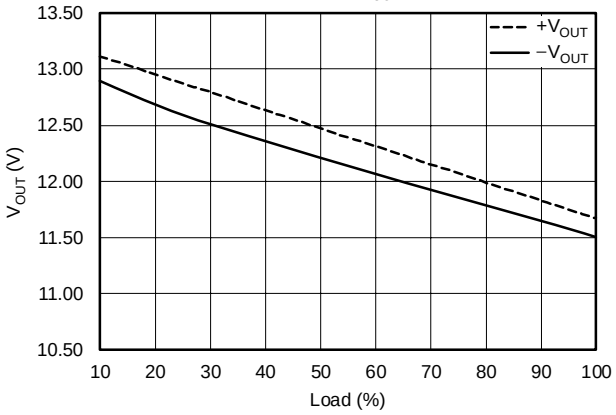
DCP010505B
CONDUCTED EMISSIONS (8% Load)



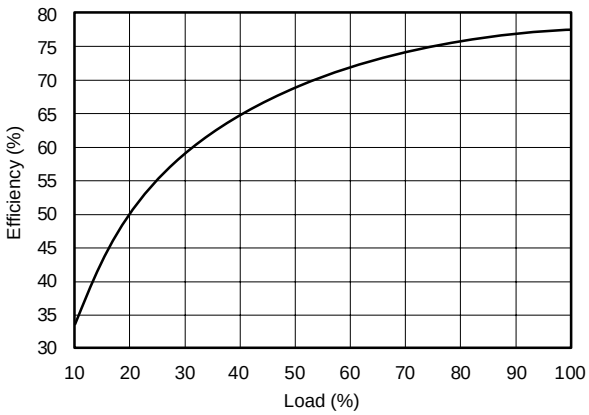
TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C, unless otherwise noted.

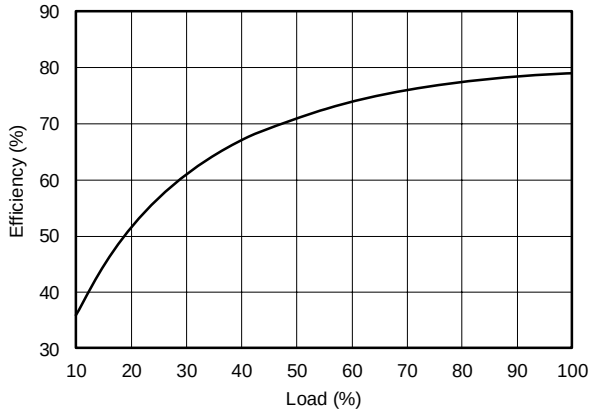
DCP011512DBP V_{OUT} vs LOAD



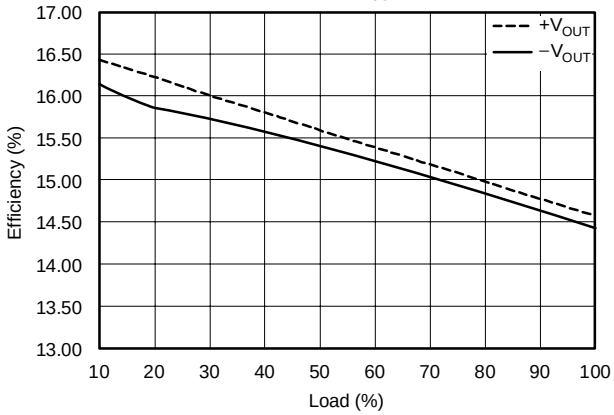
DCP011512DBP
EFFICIENCY vs LOAD



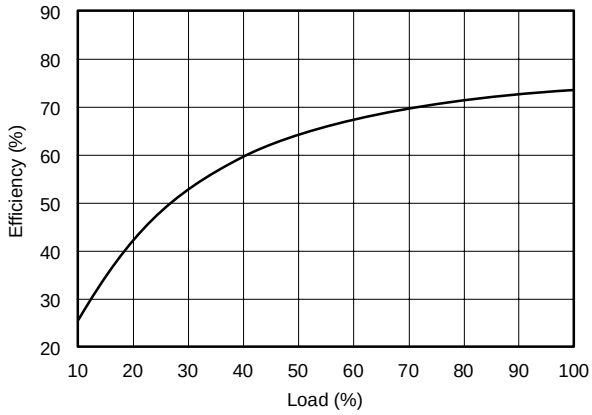
DCP011515DBP
EFFICIENCY vs LOAD



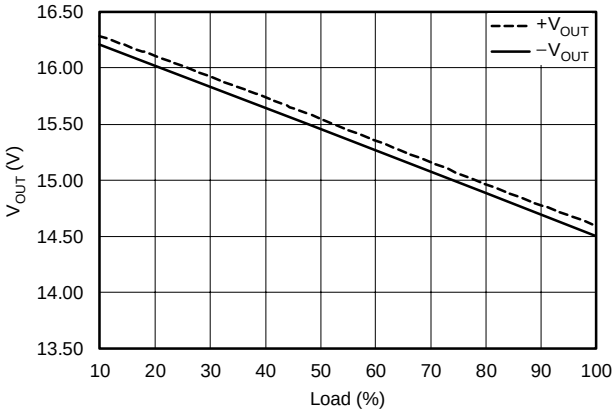
DCP011515DBP V_{OUT} vs LOAD



DCP012415DBP EFFICIENCY vs LOAD



DCP012415DBP V_{OUT} vs LOAD



FUNCTIONAL DESCRIPTION

OVERVIEW

The DCP01B offers up to 1W of unregulated output power with a typical efficiency of up to 85%. This is achieved through highly integrated packaging technology and the implementation of a custom power stage and control IC. The circuit design uses an advanced BiCMOS/DMOS process. For additional information, refer to the application notes located in the DCP01B product folder at www.ti.com.

POWER STAGE

This uses a push-pull, center-tapped topology switching at 400kHz (divide-by-2 from 800kHz oscillator).

OSCILLATOR AND WATCHDOG

The onboard 800kHz oscillator generates the switching frequency via a divide-by-2 circuit. The oscillator can be synchronized to other DCP01B circuits or an external source, and is used to minimize system noise.

A watchdog circuit checks the operation of the oscillator circuit. The oscillator can be stopped by pulling the SYNC pin low. The output pins will be tri-stated. This will occur in 2µs.

THERMAL SHUTDOWN

The DCP01B is protected by a thermal shutdown circuit. If the on-chip temperature exceeds 150°C, the device will shut down. Once the temperature falls below 150°C, normal operation will resume. If the thermal condition continues, operation will randomly cycle on and off. This will continue until the temperature is reduced.

SYNCHRONIZATION

In the event that more than one DC/DC converter is needed onboard, beat frequencies and other electrical interference can be generated. This is due to the small variations in switching frequencies between the DC/DC converters.

The DCP01B overcomes this by allowing devices to be synchronized to one another. Up to eight devices can be synchronized by connecting the $SYNC_{IN}$ pins together, taking care to minimize the stray capacitance. Stray capacitance (> 3pF) will have the effect of reducing the switching frequency, or even stopping the oscillator circuit.

If synchronized devices are used, it should be noted that at startup, all devices will draw maximum current simultaneously. This can cause the input voltage to dip. If it dips below the minimum input voltage (4.5V), the devices may not start up. A 2.2µF capacitor should be connected close to the input pins.

If more than eight devices are to be synchronized, it is recommended that the $SYNC_{IN}$ pins are driven by an external device. Details are contained in Application Report SBAA035, *External Synchronization of the DCP01/02 Series of DC/DC Converters*, available for download at www.ti.com.

CONSTRUCTION

The DCP01B basic construction is the same as standard ICs. There is no substrate within the molded package. The DCP01B is constructed using an IC, rectifier diodes, and a wound magnetic toroid on a leadframe. Since there is no solder within the package, the DCP01B does not require any special PCB assembly processing. This results in an isolated DC/DC converter with inherently high reliability.

ADDITIONAL FUNCTIONS

DISABLE/ENABLE

The DCP01B can be disabled or enabled by driving the SYNC pin using an open drain CMOS gate. If the $SYNC_{IN}$ pin is pulled low, the DCP01B will be disabled. The disable time depends upon the external loading; the internal disable function is implemented in 2µs. Removal of the pull-down will cause the DCP01B to be enabled.

Capacitive loading on the $SYNC_{IN}$ pin should be minimized in order to prevent a reduction in the oscillator frequency.

DECOUPLING

Ripple Reduction

A high switching frequency of 400kHz allows simple filtering. To reduce ripple, it is recommended that at least a 1µF capacitor is used on V_{OUT}. Dual outputs should have both the positive and negative buses decoupled to V_{OUT} ground (pin 5). The required 2.2µF low equivalent series resistance (ESR) ceramic capacitor on the input of the 5V to 15V versions, and the ≥ 0.47µF low-ESR ceramic capacitor on the 24V versions help reduce ripple and noise. See Application Bulletin SBVA012, *DC-to-DC Converter Noise Reduction*, available for download at www.ti.com.

Connecting the DCP01B in Series

Multiple DCP01B isolated 1W DC/DC converters can be connected in series to provide nonstandard voltage rails. This is possible by using the floating outputs provided by the DCP01B galvanic isolation.

Connect the positive V_{OUT} from one DCP01B to the negative V_{OUT} (0V) of another, as shown in Figure 1. If the $SYNC_{IN}$ pins are tied together, the self-synchronization feature of the DCP01B will prevent beat frequencies on the voltage rails. The $SYNC_{IN}$ feature of the DCP01B allows easy connection in series, which reduces separate filtering components.

The outputs on dual output DCP01B versions can also be connected in series to provide two times the magnitude of V_{OUT}, as shown in Figure 2. For example, a dual 15V DCP01B could be connected to provide a 30V rail.

Connecting the DCP01B in Parallel

If the output power from one DCP01B is not sufficient, it is possible to parallel the outputs of multiple DCP01B converters (see Figure 3). Again, the $SYNC_{IN}$ feature allows easy synchronization to prevent power-rail beat frequencies at no additional filtering cost.

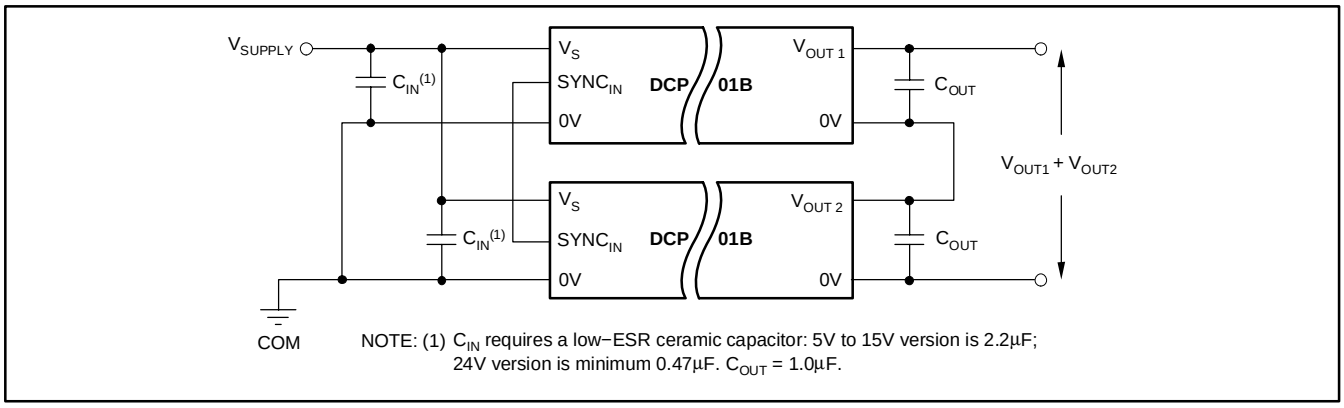


Figure 1. Connecting the DCP01B in Series

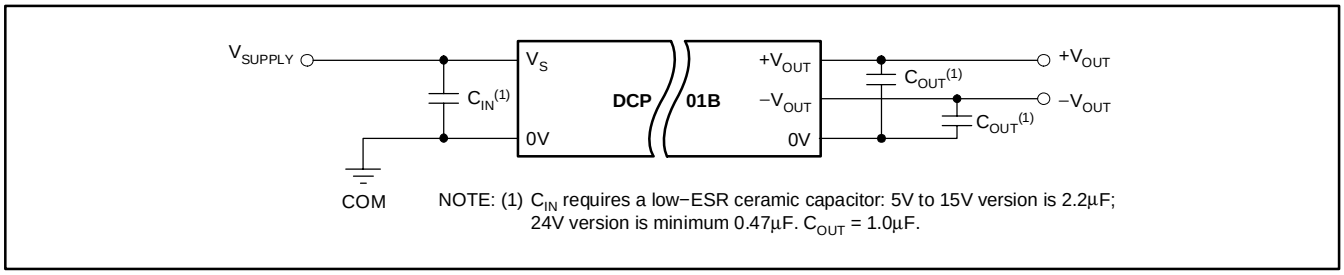


Figure 2. Connecting Dual Outputs in Series

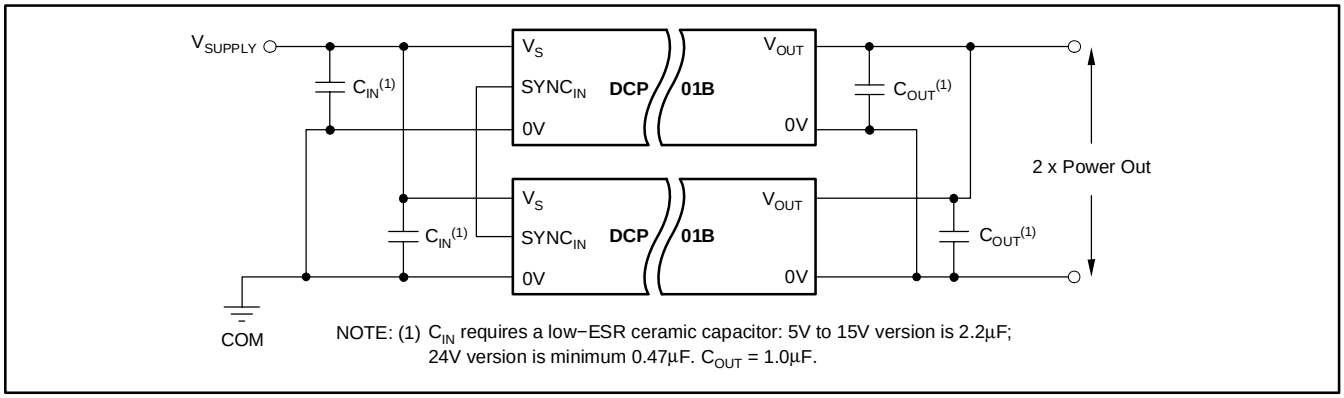


Figure 3. Connecting Multiple DCP01Bs in Parallel

APPLICATION INFORMATION

The DCP01B, DCV01, and DCP02 are three families of miniature DC/DC converters providing an isolated unregulated voltage output. All are fabricated using a CMOS/DMOS process with the DCP01B replacing the familiar DCP01 family that was fabricated from a bipolar process. The DCP02 is essentially an extension of the DCP01B family providing a higher power output with a significantly improved load regulation, and the DCV01 is tested to a higher isolation voltage.

TRANSFORMER DRIVE CIRCUIT

Transformer drive transistors have a characteristically low value of transistor *on* resistance (R_{DS}); thus, more power is transferred to the transformer. The transformer drive circuit is limited by the base current available to switch on the power transistors driving the transformer and their characteristic current gain (beta), resulting in a slower turn-on time. Consequently, more power is dissipated within the transistor. This results in a lower overall efficiency, particularly at higher output load currents.

SELF-SYNCHRONIZATION

The input synchronizations facility ($SYNC_{IN}$), allows for easy synchronizing of multiple devices. If two to eight devices (maximum) have their respective $SYNC_{IN}$ pins connected together, then all devices will be synchronized.

Each device has its own onboard oscillator. This is generated by charging a capacitor from a constant current and producing a ramp. When this ramp passes a threshold, an internal switch is activated that discharges the capacitor to a second threshold before the cycle is repeated.

When several devices are connected together, all the internal capacitors are charged simultaneously.

When one device passes its threshold during the charge cycle, it starts the discharge cycle. All the other devices sense this falling voltage and, likewise, initiate a discharge cycle so that all devices discharge together. A subsequent charge cycle is only restarted when the last device has finished its discharge cycle.

OPTIMIZING PERFORMANCE

Optimum performance can only be achieved if the device is correctly supported. By the very nature of a switching converter, it requires power to be instantly available when it switches on. If the converter has DMOS switching transistors, the fast edges will create a high current demand on the input supply. This transient load placed on the input is supplied by the external input decoupling capacitor, thus maintaining the input voltage. Therefore, the input supply does not see this transient (this is an analogy to high-speed digital circuits). The positioning of the capacitor is critical and must be placed as close as possible to the input pins and connected via a low-impedance path.

The optimum performance is primarily dependent on two factors:

1. Connection of the input and output circuits for minimal loss.
2. The ability of the decoupling capacitors to maintain the input and output voltages at a constant level.

PCB Design

The copper losses (resistance and inductance) can be minimized by the use of mutual ground and power planes (tracks) where possible. If that is not possible, use wide tracks to reduce the losses. If several devices are being powered from a common power source, a star-connected system for the track must be deployed; devices must not be connected in series, as this will cascade the resistive losses. The position of the decoupling capacitors is important. They must be as close to the devices as possible in order to reduce losses. See the *PCB Layout* section for more details.

Decoupling Ceramic Capacitors

All capacitors have losses due to their internal equivalent series resistance (ESR), and to a lesser degree their equivalent series inductance (ESL). Values for ESL are not always easy to obtain. However, some manufacturers provide graphs of Frequency versus Capacitor Impedance. These will show the capacitors' impedance falling as frequency is increased (see Figure 4). As the frequency is increased, the impedance will stop decreasing and begin to rise. The point of minimum impedance indicates the capacitors' resonant frequency. This frequency is where the components of capacitance and inductance reactance are of equal magnitude. Beyond this point, the capacitor is not effective as a capacitor.

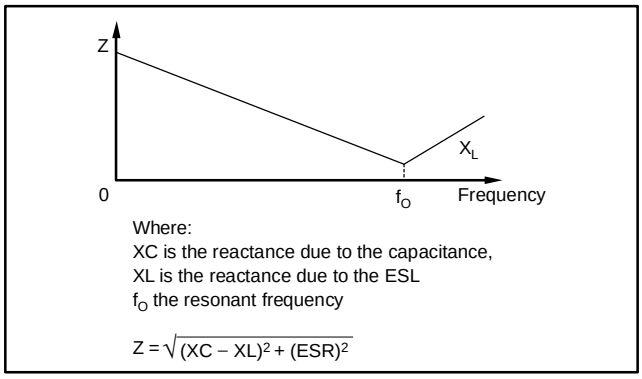


Figure 4. Capacitor Impedance vs Frequency

At f_O, $X_C = X_L$; however, there is a 180° phase difference resulting in cancellation of the imaginary component. The resulting effect is that the impedance at the resonant point is the real part of the complex impedance; namely, the value of the ESR. The resonant frequency must be well above the 800kHz switching frequency of the DCP and DCVs.

The effect of the ESR is to cause a voltage drop within the capacitor. The value of this voltage drop is simply the product of the ESR and the transient load current, as shown in Equation (1):

$$V_{IN} = V_{PK} - (ESR \times I_{TR}) \quad (1)$$

Where:

V_{IN} is the voltage at the device input.

V_{PK} is the maximum value of the voltage on the capacitor during charge.

I_{TR} is the transient load current.

The other factor that affects the performance is the value of the capacitance. However, for the input and the full wave outputs (single-output voltage devices), the ESR is the dominant factor.

Input Capacitor and the effects of ESR

If the input decoupling capacitor is not ceramic with < 20mΩ ESR, then at the instant the power transistors switch on, the voltage at the input pins will fall momentarily. Should the voltage fall below approximately 4V, the DCP will detect an under-voltage condition and switch the DCP drive circuits to the off state. This is carried out as a precaution against a genuine low input voltage condition that could slow down or even stop the internal circuits from operating correctly. This would result in the drive transistors being turned on too long, causing saturation of the transformer and destruction of the device.

Following detection of a low input voltage condition, the device switches off the internal drive circuits until the input voltage returns to a safe value. Then the device tries to restart. If the input capacitor is still unable to maintain the input voltage, shutdown recurs. This process is repeated until the capacitor is charged sufficiently to start the device correctly. Otherwise, the device will be caught up in a loop.

Normal startup should occur in approximately 1ms from power being applied to the device. If a considerably longer startup duration time is encountered, it is likely that either (or both) the input supply or the capacitors are not performing adequately.

For 5V to 15V input devices, a 2.2µF low-ESR ceramic capacitor will ensure a good startup performance, and for the remaining input voltage ranges, 0.47µF ceramic capacitors are good. Tantalum capacitors are not recommended, since most do not have low-ESR values and will degrade performance. If tantalum capacitors must be used, close attention must be paid to both the ESR and voltage as derated by the vendor.

Output Ripple Calculation Example

DCP020505: Output voltage 5V, Output current 0.4A. At full output power, the load resistor is 12.5Ω. Output capacitor of 1µF, ESR of 0.1Ω. Capacitor discharge time 1% of 800kHz (ripple frequency):

$t_{DIS} = 0.0125\mu s$

$t = C \times R_{LOAD}$

$t = 1 \times 10^{-6} \times 12.5 = 12.5\mu s$

$V_{DIS} = V_O(1 - EXP(-t_{DIS}/\tau))$

$V_{DIS} = 5mV$

By contrast the voltage dropped due to the ESR:

$V_{ESR} = I_{LOAD} \times ESR$

$V_{ESR} = 40mV$

Ripple voltage = 45mV

Clearly, increasing the capacitance will have a much smaller effect on the output ripple voltage than reducing the value of the ESR for the filter capacitor.

DUAL OUTPUT VOLTAGE DCP AND DCVs

The voltage output for the dual DCPs is half wave rectified; therefore, the discharge time is 1.25µs. Repeating the above calculations using the 100% load resistance of 25Ω (0.2A per output), the results are shown below:

τ = 25µs

T_{DIS} = 1.25µs.

V_{DIS} = 244mV

V_{ESR} = 20mV

Ripple Voltage = 266mV

This time, it is the capacitor discharging that is contributing to the largest component of ripple. Changing the output filter to 10µF, and repeating the calculations:

Ripple Voltage = 45mV.

This value is composed of almost equal components.

The above calculations are given only as a guide. Capacitor parameters usually have large tolerances and can be susceptible to environmental conditions.

PCB LAYOUT

Figure 5 and Figure 6 illustrate a printed circuit board (PCB) layout for the two conventional (DCP01/02, DCV01), and two SO-28 surface-mount packages (DCP02U). Figure 7 shows the schematic.

Input power and ground planes have been used, providing a low-impedance path for the input power. For the output, the common or 0V has been connected via a ground plane, while the connections for the positive and negative voltage outputs are conducted via wide traces in order to minimize losses.

The location of the decoupling capacitors in close proximity to their respective pins ensures low losses due to the effects of stray inductance; thus, improving the ripple performance. This is of particular importance to the input decoupling capacitor as this supplies the transient current associated with the fast switching waveforms of the power drive circuits.

The Sync pin, when not being used, is best left as a floating pad. A ground ring or annulus connected around the pin will prevent noise being conducted onto the pin. If the Sync pin is being connected to one or more Sync pins, then the linking trace should be narrow and must be kept short in length. In addition, no other trace should be in close proximity to this trace because that will increase the stray capacitance on this pin, and that will effect the performance of the oscillator.

Ripple and Noise

Careful consideration should be given to the layout of the PCB, in order that the best results can be obtained.

The DCP01B is a switching power supply and as such can place high peak current demands on the input supply. In order to avoid the supply falling momentarily during the fast switching pulses, ground and power planes should be used to connect the power to the input of DCP01B. If this is not possible, then the supplies must be connected in a star formation with the traces made as wide as possible.

If the $SYNC_{IN}$ pin is being used, then the trace connection between device $SYNC_{IN}$ pins should be short to avoid stray capacitance. If the $SYNC_{IN}$ pin is not being used, it is advisable to place a guard ring (connected to input ground) around this pin to avoid any noise pick up.

The output should be taken from the device using ground and power planes; this ensures minimum losses.

A good quality low-ESR ceramic capacitor placed as close as practical across the input will reduce reflected ripple and ensure a smooth startup.

A good quality low-ESR capacitor (ceramic preferred) placed as close as practical across the rectifier output terminal and output ground gives the best ripple and noise performance. See SBVA012 for more information on noise rejection.

THERMAL MANAGEMENT

Due to the high power density of this device, it is advisable to provide ground planes on the input and output.

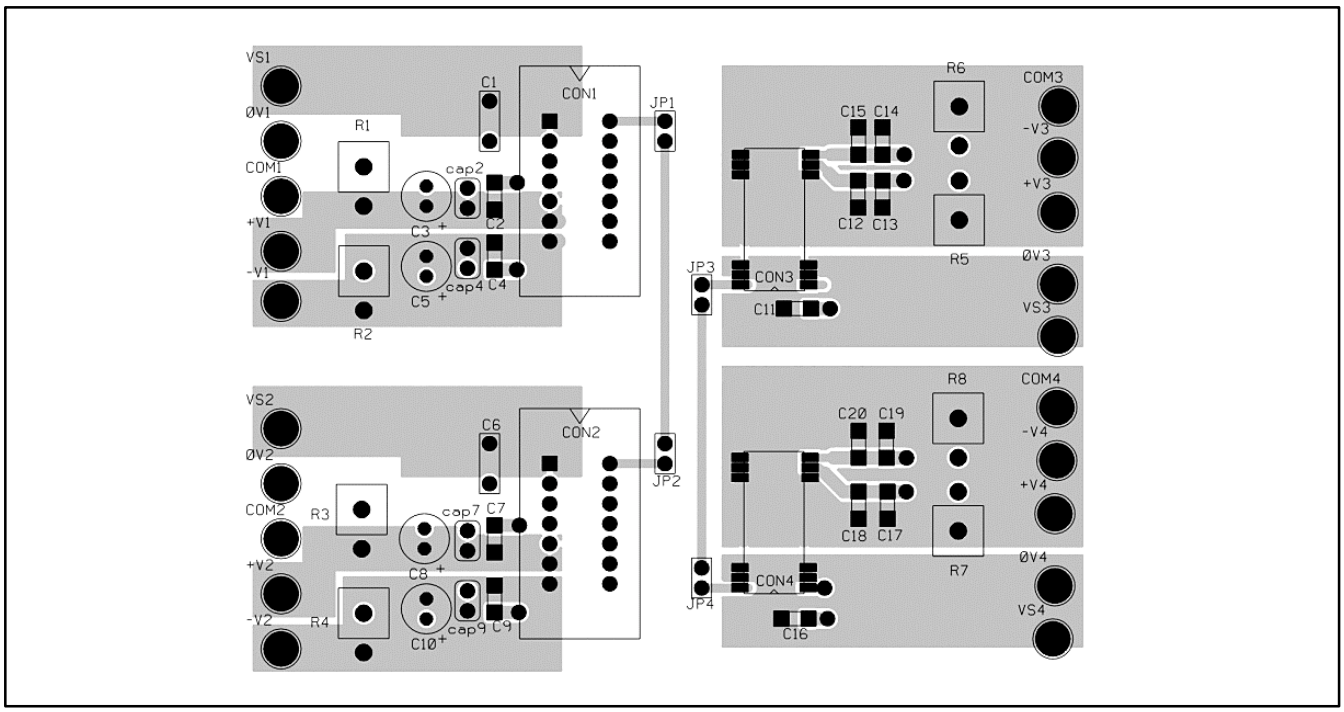


Figure 5. Example of PCB Layout, Component-Side View

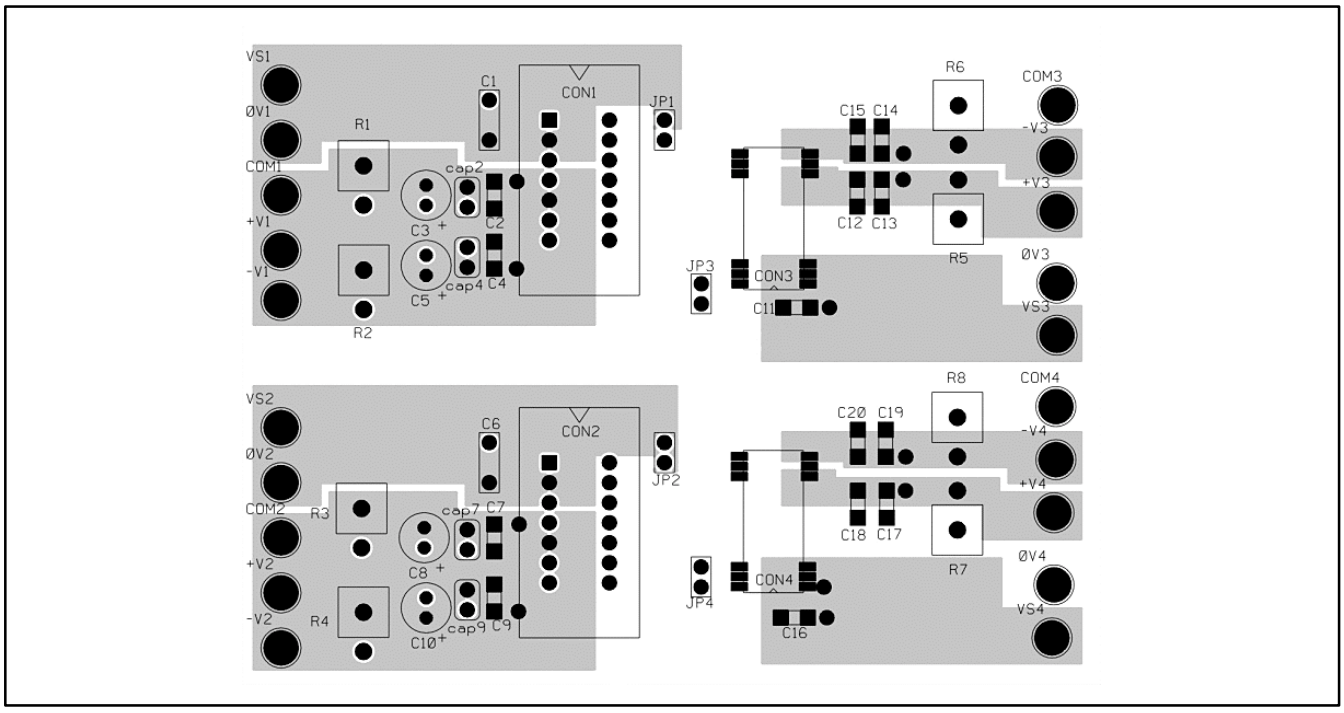
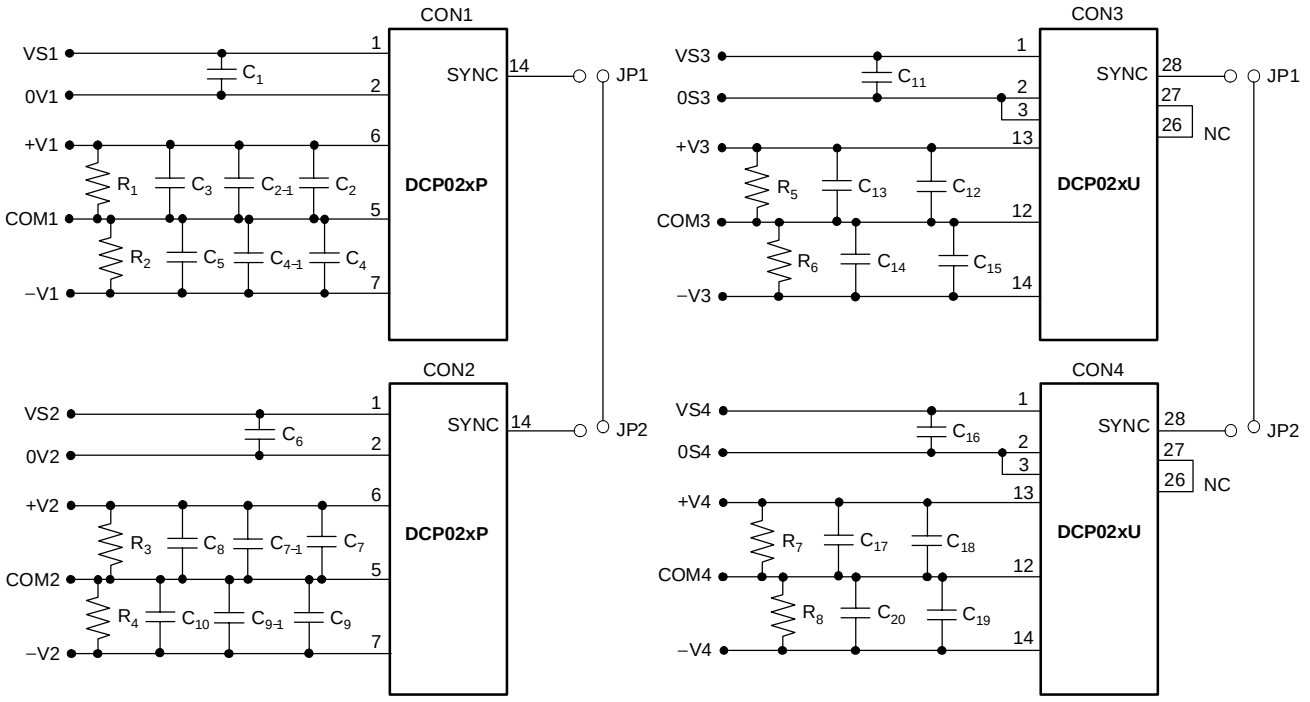


Figure 6. Example of PCB Layout, Non-component-Side View



(1) Capacitors C2−1, C4−1, C7−1, and C9−1 are through-hole plated components connected in parallel with C2, C4, C7 and C9 (1206 SMD), respectively.
(2) For optimum low-noise performance, use low-ESR capacitors.
(3) Do not connect the SYNC pin jumper (JP1−JP4) if the SYNC function is not being used.
(4) Connections to the power input should be made with a minimum wire of 16/0.2 twisted pair, with the length kept short.
(5) VSx and 0Vx are input supply and ground respecively (x represents the channel).
(6) +Vx and −Vx are the positive and negative outputs, referenced to a common ground COMx.
(7) JPx are the links used for self-synchronization; if this facility is not being used, the links should be unconnected.
(8) R1−R8 are the power output loads; do not fit these if an external load is connected.
(9) CON1 and CON2 are DIL-14; CON3 and CON4 are SO-28 packages.
(10) NC = not connected.

Figure 7. Example of PCB Layout, Schematic Diagram

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
DCP010505BP	ACTIVE	PDIP	NVA	7	25	TBD	CU SNPB	Level-NA-NA-NA
DCP010505BP-U	ACTIVE	SOP	DUA	7	25	TBD	CU SNPB	Level-3-240C-168 HR
DCP010505BP-U/700	ACTIVE	SOP	DUA	7	700	TBD	CU SNPB	Level-3-240C-168 HR
DCP010505DBP	ACTIVE	PDIP	NVA	7	25	TBD	CU SNPB	Level-NA-NA-NA
DCP010505DBP-U	ACTIVE	SOP	DUA	7	25	TBD	CU SNPB	Level-3-240C-168 HR
DCP010505DBP-U/700	ACTIVE	SOP	DUA	7	700	TBD	CU SNPB	Level-3-240C-168 HR
DCP010512BP	ACTIVE	PDIP	NVA	7	25	TBD	CU SNPB	Level-NA-NA-NA
DCP010512BP-U	ACTIVE	SOP	DUA	7	25	TBD	CU SNPB	Level-3-240C-168 HR
DCP010512BP-U/700	ACTIVE	SOP	DUA	7	700	TBD	CU SNPB	Level-3-240C-168 HR
DCP010512DBP	ACTIVE	PDIP	NVA	7	25	TBD	CU SNPB	Level-NA-NA-NA
DCP010512DBP-U	ACTIVE	SOP	DUA	7	25	TBD	CU SNPB	Level-3-240C-168 HR
DCP010512DBP-U/700	ACTIVE	SOP	DUA	7	700	TBD	CU SNPB	Level-3-240C-168 HR
DCP010515BP	ACTIVE	PDIP	NVA	7	25	TBD	CU SNPB	Level-NA-NA-NA
DCP010515BP-U	ACTIVE	SOP	DUA	7	25	TBD	CU SNPB	Level-3-240C-168 HR
DCP010515BP-U/700	ACTIVE	SOP	DUA	7	700	TBD	CU SNPB	Level-3-240C-168 HR
DCP010515DBP	ACTIVE	PDIP	NVA	7	25	TBD	CU SNPB	Level-NA-NA-NA
DCP010515DBP-U	ACTIVE	SOP	DUA	7	25	TBD	CU SNPB	Level-3-240C-168 HR
DCP010515DBP-U/700	ACTIVE	SOP	DUA	7	700	TBD	CU SNPB	Level-3-240C-168 HR
DCP011512DBP	ACTIVE	PDIP	NVA	7	25	TBD	CU SNPB	Level-NA-NA-NA
DCP011512DBP-U	ACTIVE	SOP	DUA	7	25	TBD	CU SNPB	Level-3-240C-168 HR
DCP011512DBP-U/700	ACTIVE	SOP	DUA	7	700	TBD	CU SNPB	Level-3-240C-168 HR
DCP011515DBP	ACTIVE	PDIP	NVA	7	25	TBD	CU SNPB	Level-NA-NA-NA
DCP011515DBP-U	ACTIVE	SOP	DUA	7	25	TBD	CU SNPB	Level-3-240C-168 HR
DCP011515DBP-U/700	ACTIVE	SOP	DUA	7	700	TBD	CU SNPB	Level-3-240C-168 HR
DCP012415DBP	ACTIVE	PDIP	NVA	7	25	TBD	CU SNPB	Level-NA-NA-NA
DCP012415DBP-U	ACTIVE	SOP	DUA	7	25	TBD	CU SNPB	Level-3-240C-168 HR
DCP012415DBP-U/700	ACTIVE	SOP	DUA	7	700	TBD	CU SNPB	Level-3-240C-168 HR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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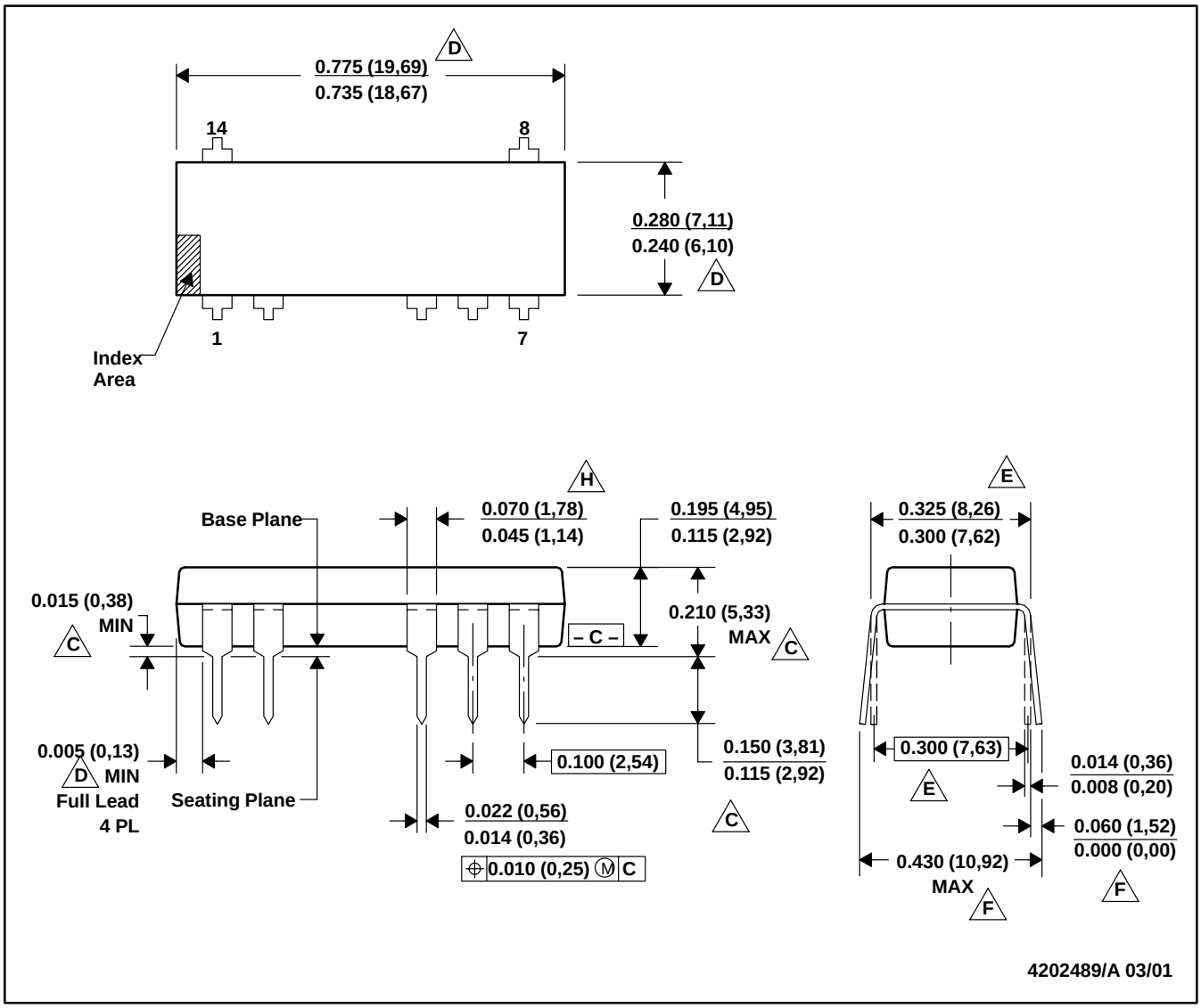
MPDI058 – APRIL 2001

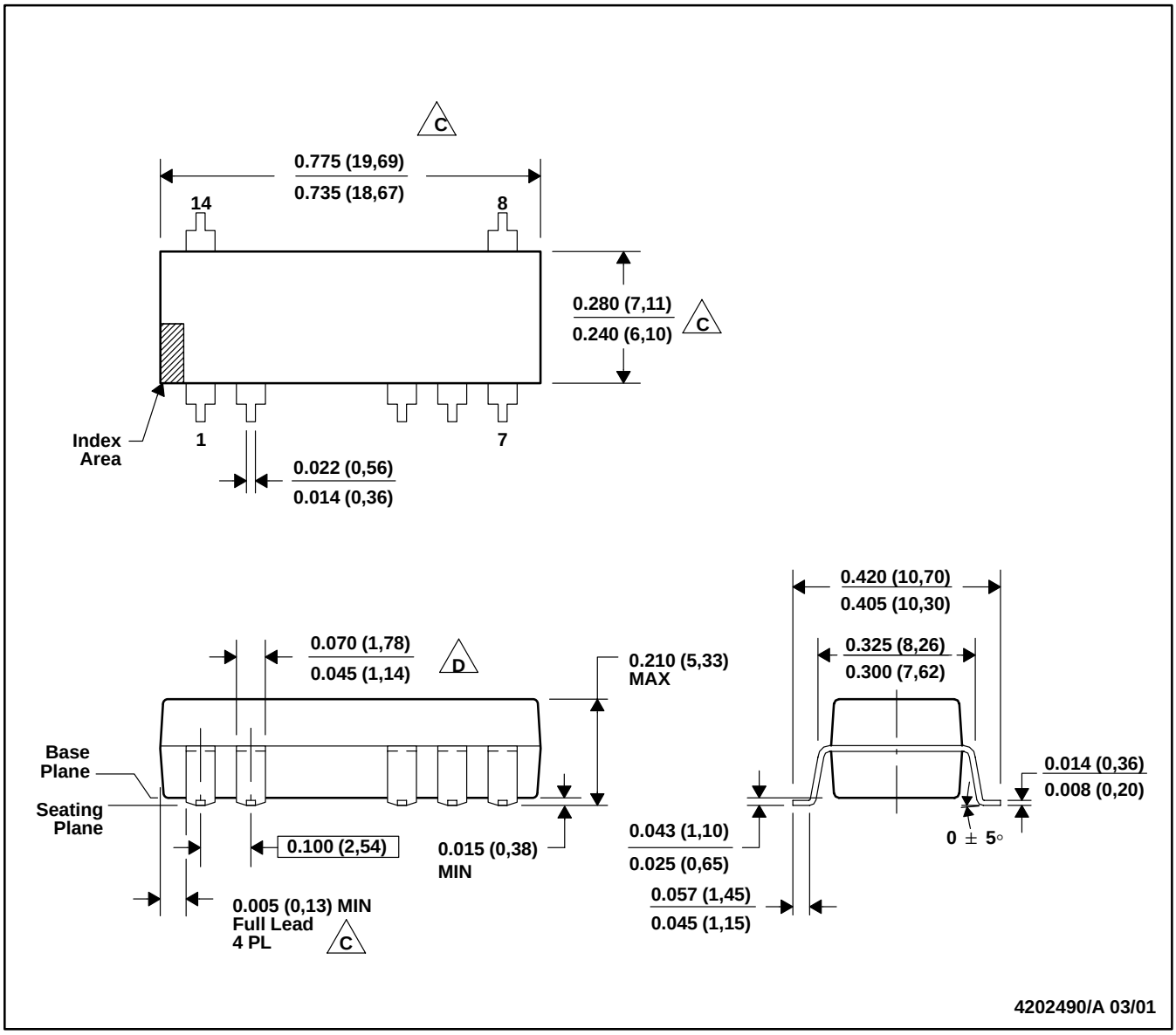
NVA (R-PDIP-T7/14) **PLASTIC DUAL-IN-LINE**



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Dimensions are measured with the package seated in JEDEC seating plane gauge GS-3.
D. Dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 (0,25).
E. Dimensions measured with the leads constrained to be perpendicular to Datum C.
F. Dimensions are measured at the lead tips with the leads unconstrained.
G. Pointed or rounded lead tips are preferred to ease insertion.
H. Lead shoulder maximum dimension does not include dambar protrusions. Dambar protrusions shall not exceed 0.010 (0,25).
I. Distance between leads including dambar protrusions to be 0.005 (0,13) minumum.
J. A visual index feature must be located within the cross–hatched area.
K. For automatic insertion, any raised irregularity on the top surface (step, mesa, etc.) shall be symmetrical about the lateral and longitudinal package centerlines.
L. Falls within JEDEC MS-001-AA.

MPDS097 – APRIL 2001

DUA (R-PDSO-G7/14) **PLASTIC SMALL-OUTLINE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 (0,25).
D. Lead shoulder maximum dimension does not include dambar protrusions. Dambar protrusions shall not exceed 0.010 (0,25).
E. Distance between leads including dambar protrusions to be 0.005 (0,13) minimum.
F. A visual index feature must be located within the cross–hatched area.
G. For automatic insertion, any raised irregularity on the top surface (step, mesa, etc.) shall be symmetrical about the lateral and longitudinal package centerlines.

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