DESCRIPTION

The LTC1606 is a 250Ksps ADC that draws only 75mW from a Single +5V Supply.

Demonstration circuit 379 provides the user a means of evaluating the performance of the device mounted on a PCB that is intended to demonstrate recommended placement, routing and bypassing.

For best performance, the area immediately surrounding the ADC should be used as a guideline for placement as well as interconnection of analog and digital planes.

Gerber files of this board are available online. Consult factory or LTC sales for access.

QUICK START PROCEDURE

DC379 requires +5V at approximately 30mA and +/- 15V to power amplifier U4.

Even if you do not use buffer/amplifier U4 (see jumper JP4) you must provide +/-15V, as otherwise, the input circuitry in U4 will load your signal source and cause distortion.

The +5V supply powers the ADC directly without any protection for reverse bias, and no regulation. **Poor regulation will compromise results; reverse bias will damage the ADC**. If you do not intend to use the amplifier, you may remove it, in which case, only +5V is required.

J1

You must provide a low jitter logic level clock source to J1. The rising edge of this signal defines the aperture of the converter. Slow rising edges or unterminated cables may compromise SNR of the converter in the presence of high-amplitude higher-frequency input signals. This input is not terminated, as a result, if you use a signal generator intended to drive 50-ohm loads, you must use a 50-ohm through-terminator at the input. Poor cables, clip leads, may or will compromise results.

The demo board incorporates an edge detector circuit in the form of an inverter (U6A) followed by a 500nsec delay, feeding, along with the original clock source, a two input NAND gate (U3). This will generate an approximate 500nsec active low pulse at the ADC if the clock high time is greater than 500nsec. A 50% duty cycle clock at 250KHz is typically used to test these demo boards. Shorter duty cycle (active High at J1) can be used to a minimum of 40nsec.

Logic can be used to drive **J1** if located close to the board, in which case, the through terminator is not required. Note that slow CMOS buffers will translate supply fluctuations into variation in propagation delay, and will appear as clock jitter.

Parallel data output from this board, if not used by a target system, must be acquired by a logic analyzer, and subsequently imported into a spreadsheet, or mathematical package depending on what form of digital signal processing is desired.

JP5 allows output buffer/latch to be operated as a transparent buffer, or as a latch. The choice is arbitrary, in many cases. However, JP5 can potentially be used to decimate the output, or for example latching only a given sample in a sequence to feed a DAC

Evaluations in some cases may be best performed by feeding the output of the converter to a 16-bit DAC, the output of which is used to subsequently drive a spectrum analyzer, or a scope. The limitations of the DAC must be recognized and accounted for in an evaluation of this type. If the signals of interest are channels in a time domain multiplexed sequence, or a brief transient feature on a complex recurring waveform, the subsequent waveform at the output of a DAC latching only that channel may be much easier to

interpret than the original signal. By placing a given frequency on the channel of interest, and a different frequency on another channel will allow you via the DAC, feeding a spectrum analyzer to see cross talk mechanisms in multiplexers. You can also use this technique to evaluate the effects of transient steps preceding the acquisition period.

The demo board is typically shipped with Byte (**JP2**) and CS (**JP3**) tied to ground. If you intend to operate this device in a fashion that involves these lines, you can use the jumpers as a means of introducing these signals from an external source.

JP1 allows you to select between an on chip reference (INT) or an external LT1019A-2.5. The typical drift specifications of this reference are similar to the on chip reference, but The LT1019 has guaranteed maximums.

The demo board is shipped with **JP4** in the out position, in which case, the input amplifier is not in the signal path. With **JP4** in the "IN" position, U4 (LT1468) provides a gain of 9dB, to allow a signal generator with 2.5V RMS output levels to drive the converter to full scale. This amplifier does not compromise the SNR or distortion performance of the converter.

The input noise density of the LT1468 itself is 5nV/•Hz.

In the circuit as configured, the feedback network impedance, and the amplifier's input noise current contribute noise power to produce an input referred noise density of 7.44nV//•Hz; With a gain of 2.82, this produces in the 675Khz bandwidth imposed by the converter, 17uV RMS, or a signal to noise ratio of 112dB at full scale.

This is of course not verifiable at the output of the ADC.

With JP4 in the "out" position, the input impedance at J2 is 10K-ohms. With JP4 in the "IN" position, the input impedance is very high.

If J2 is driven by a generator intended to drive a 50-ohm impedance, you may want to use a 50-ohm through-terminator. If a higher impedance source is to be evaluated, you will see better results with the amplifier in the signal path.

If you want to evaluate the amplifier in unity gain, remove R10, or solder a low value resistor in parallel with R9. If you want to evaluate the amplifier with higher gain, you may reduce the value of R10. If you use very high quality resistors, you should be able to increase the gain to 50 before the noise floor of the converter rises discernibly. A voltage gain of 10 should result in the typical SNR of 90dB dropping to 89.9dB. A voltage gain of 50 should give approx 88.7dB, and a gain of 100 would give approximately 86dB SNR. THD will increase but with a gain of 50, the THD of the LT1468 is still typically in the range of -90dB.

If the amplifier is configured for high gain, ground potential differences between the various instruments on your bench top may be found to develop a differential component at the input to the demo board. Transformer isolation may be required to produce good results with a gain of 50. The system used for data collection may have a negative effect on how well the demo board performs, if it produces significant ground current through the demo board.

This demo board is tested in house by duplicating the FFT plot shown in the lower left of page 6 of the LTC1606 data sheet. This involves using a low jitter, 250KHz clock source for the encode clock, (for example a 50MHz Oscillator divided by 200), along with a low noise, low distortion sinusoidal generator at a frequency in the neighborhood of 1KHz.

The FFT shown in the data sheet is a 4K point FFT, with the input frequency at precisely 1037.5976Hz. This frequency is "coherent" (produces an integral number of cycles of the fundamental within the window) for a 250KHz clock frequency, and Prime (17 cycles). A prime number of integral cycles exercises the greatest number of possible input codes. Note that a 4K transform does not exercise all codes in a 16-bit converter.

Other sample rates require different input frequencies.

There are a number of scenarios that can produce misleading results in evaluating an ADC. One that is not uncommon is that of feeding the converter with a frequency that is a sub-multiple of the sample rate, and which will only exercise a small subset of the possible output codes.

Note that the demo board does not have anti-aliasing filtering. Following jumper JP4, is an 800KHz first order low pass filter. (R4, and C16)

This does not appreciably change the –3dB point of the converter, which is typically 675KHz.

Hence, R4, and C16 do not constitute an anti-aliasing filter. If you require an anti-aliasing filter in your evaluation, it should generally be placed prior to the LT1468, or an external amplifier. If you have frequency components that are above Nyquist (1/2 fs), and up to and beyond 675KHz they will fold back into the DC-125KHz base band, and become indistinguishable from signals in this band.

The amplifier is “In” for the in-house test, and the signal is approx –1dBfs.

If you do not have a signal generator capable of PPM levels of frequency accuracy, you can use an FFT with windowing to reduce the “leakage” or spreading of the fundamental, to get a close approximation of the performance parameters. If an amplifier or clock source with poor phase noise is used, the windowing will not improve the SNR.

The signal source typically used is a B&K 1051. The clock source used is an HP8644 at 2.5MHz, followed by a PECL programmable divider set to a divide ratio of 10, producing a 400ns positive going pulse.

As with any high performance ADC, this part is sensitive to layout. The demo board is a good implementation for a case where the link between analog, and digital ground can be made at the ADC. The area immediately surrounding the ADC should be used as a guideline for placement, and routing to the ground plane, and the various capacitors associated with the ADC. Cases where the link cannot be made under the ADC require careful thought with respect to ground currents, and the signals that may be developed across the planes or interconnections.

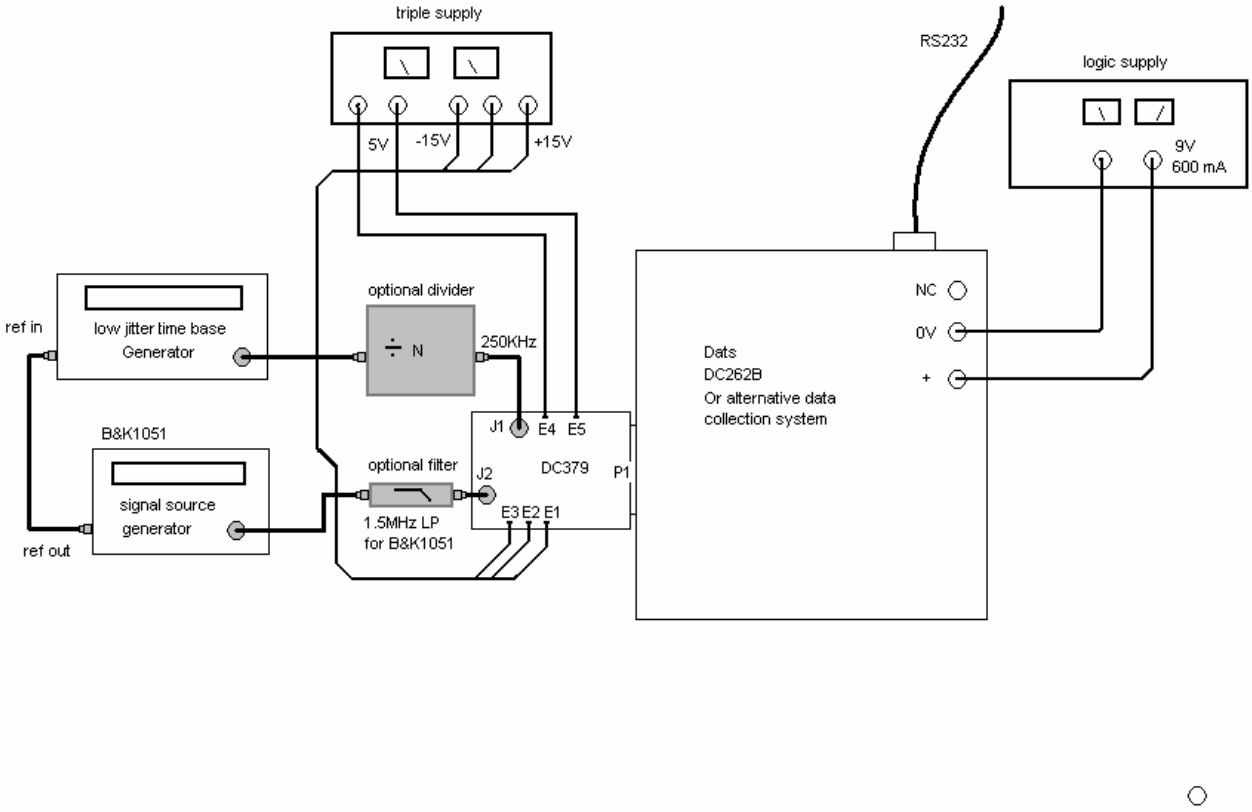
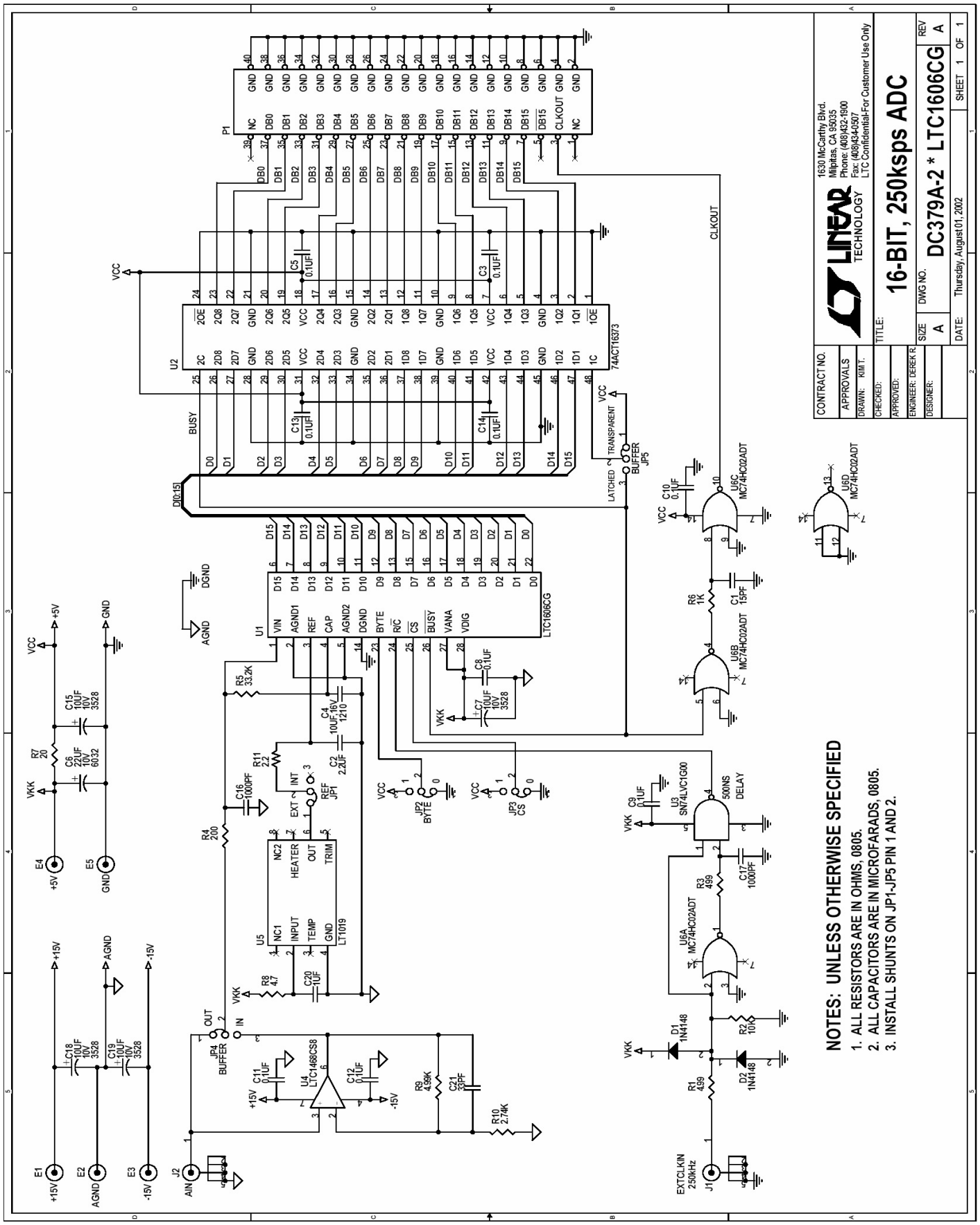


Figure 1. Proper Measurement Equipment Setup


NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE IN OHMS, 0805.
2. ALL CAPACITORS ARE IN MICROFARADS, 0805.
3. INSTALL SHUNTS ON JP1-JP5 PIN 1 AND 2.
LINEAR TECHNOLOGY
1630 McCarthy Blvd.
Milpitas, CA 95035
Phone: (408)432-1900
Fax: (408)434-0507
LTC Confidential-For Customer Use Only
TITLE:
16-BIT, 250ksps ADC
SIZE A
DWG NO. DC379A-2 * LTC1606CG
REV A
DATE: Thursday, August 01, 2002
SHEET 1 OF 1
CONTRACT NO.
APPROVALS
DRAWN: KIM T.
CHECKED:
APPROVED:
ENGINEER: DEREK R.
DESIGNER:
LTC1606CG
74ACT16373
LT1019
LTC1468CS8
SN74LVC1G00
MC74HC02ADT
1N4148
BUSY
CLKOUT
EXTCLKIN 250kHz
AIN
+15V
AGND
-15V
+5V
GND
VCC
VKK
DGND
BUFFER
TRANSPARENT
LATCHED
JP1
JP2
JP3
JP4
JP5
500NS DELAY

Linear Technology Corporation-LTC1606CG

16-BIT, 250ksps ADC

BILL OF MATERIALS
DC379A-2
QTY- 275
6/25/03
9:41 AM

Item	*Qty*	*Reference*	*Part Description*	*Manufacture / Part #*	*Kit Qty*
				NUMBER OF BOARDS =	***275***
1	1	C1	CAP., NPO 15pF 50V 10%	AVX 08055A150KAT1A	275
2	1	C2	CAP., Y5V 2.2uF 10V +80% -20%	AVX 0805ZG225ZAT2A	275
3	9	C3,C5,C8-C14	CAP., X7R 0.1uF 25V 20%	AVX 08053C104MAT1A	2475
4	1	C4	CAP, X5R, 10uF 16V, 20%, 1210	TAIYO YUDEN EMK325BJ106MN	275
5	1	C6	CAP., TANT 22uF 10V 20%,6032	AVX TAJC226M010R	275
6	4	C7,C15,C18,C19	CAP., TANT 10uF 10V 20%,3528	AVX TAJB106M010R	1100
7	2	C16,C17	CAP., NPO 1000pF 50V 10%	AVX 08055A102KAT1A	550
8	1	C20	CAP., X7R 1uF 10V 20%	AVX 0805ZC105MAT1A	275
9	1	C21	CAP., NPO 33pF 50V 10%	AVX 08055A330KAT1A	275
10	2	D1,D2	DIODE, FAST SWITCH DIODE, SOD323	DIODES INC. 1N4148WS-7	550
11	5	E1-E5	TP, TERMINAL TURRET, 1 PIN	MILL-MAX 2308-2	1375
12	5	JP1-JP5	JMP,3 PINS, .100"CC	COMM CON 3801S-03G2	1375
13	5	SHUNTS FOR JP1-JP5	SHUNT, .100cc	COMM CON CCIJ230	1375
14	2	J1,J2	CONN, BNC 50-OHM, BNC5	CONNEX 112404	550
15	1	P1	CONN, HEADER, 2X2O-100", SMT, TB	COMM CON 3201S-40G2	275
16	1	R1	RES., CHIP 4.99-OHM 1/16 1%, 0805	AAC CR10-4R99FM	275
17	1	R2	RES., CHIP 10K 1/16W 5%, 0805	AAC CR10-103JM	275
18	1	R3	RES., CHIP 499-OHM 1/16W 1%, 0805	AAC CR10-4990FM	275
19	1	R4	RES., CHIP 200-OHM 1/16W 5%, 0805	AAC CR10-201JM	275
20	1	R5	RES., CHIP 33.2K 1/16W 1%, 0805	AAC CR10-3322FM	275
21	1	R6	RES., CHIP 1K 1/16W 5%, 0805	AAC CR10-102JM	275
22	1	R7	RES., CHIP 20-OHM 1/16W 5%, 0805	AAC CR10-200JM	275
23	1	R8	RES., CHIP 4.7-OHM 1/16W 5%, 0805	AAC CR10-4R7JM	275
24	1	R9	RES., CHIP 4.99K 1/16W 1%, 0805	AAC CR10-4991FM	275
25	1	R10	RES., CHIP 2.74K 1/16W 1%, 0805	AAC CR10-2741FM	275
26	1	R11	RES., CHIP 2.21K 1/16W 1%, 0805	AAC CR10-2211FM	275
27	1	U1	I.C., LTC1606CG, SSOP28G	LINEAR LTC1606CG	275
28	1	U2	I.C., 74ACT16373DL 48 PINS, SOP48	TEXAS INS. 74ACT16373DL	275
29	1	U3	I.C., 2 INPUT NAND, SOT23-5	TEXAS INS. SN74LVC1G00DBVR	275
30	1	U4	I.C., LTC1468CS8, SO8	LINEAR TECH. LTC1468CS8	275
31	1	U5	I.C., LT1019, SO8	LINEAR TECH. LT1019CS8-2.5	275
32	1	U6	I.C., 2 INPUT NOR, TSSOP14	MOTOROLA MC74HC02ADT	275
33	4	FOR MTG AT 4 CORNERS	SCREW, STEEL, PANHEAD	#4-40 X 1/4"	1100
34	4	FOR MTG AT 4 CORNERS	STAND-OFF NYLON HEX #4-40 X 1/2"	EMOTION HTSP-3	1100
		NOTES: UNLESS OTHERWISE SPECIFIED			
		1. INSTALL SHUNT ON JP1-JP5 PIN 1 AND 2.			
		2. BREAK BOARDS IN THE PANEL WHEN ASSEMBLY IS COMPLETE.			