DEMO MANUAL DC367
LOW DROPOUT REGULATOR

LT1963 1.5A
Low Noise LDO Regulator

DESCRIPTION

Demonstration circuit DC367 is a low noise micropower voltage regulator using the LT®1963 in the 8-lead SO package. Circuits designed with the LT1963 are used primarily in cellular phones, voltage controlled oscillators, RF power supplies and, in larger systems, as local regulators. The ability to tolerate a wide variety of output capacitors makes the LT1963 ideal in space- and cost-sensitive systems.

PERFORMANCE SUMMARY

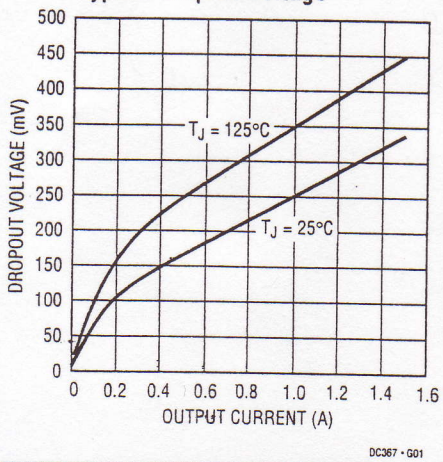
T_A = 25°C, V_{IN} = 2.5V, $V_{\overline{SHDN}}$ = 5V, I_{LOAD} = 1mA, V_{OUT} = 1.21V (JP2 set on Pins 1-2), unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Range		2.5		20	V
Output Voltage		1.192	1.210	1.228	V
Output Voltage (Note 1)	V_{IN} = 2.5V, JP2 on Pins 3-4	1.469	1.500	1.535	V
Output Voltage (Note 1)	V_{IN} = 2.8V, JP2 on Pins 5-6	1.759	1.803	1.856	V
Output Voltage (Note 1)	V_{IN} = 3.5V, JP2 on Pins 7-8	2.417	2.491	2.585	V
Output Voltage (Note 1)	V_{IN} = 4.3V, JP2 on Pins 9-10	3.171	3.280	3.420	V
Line Regulation	ΔV_{IN} = 2.5V to 20V		2	10	mV
Quiescent Current	ΔI_{LOAD} = 0mA		1	1.5	mA
Load Regulation	ΔI_{LOAD} = 1mA to 1.5A		0.2	1	%
$\overline{SHDN}$ Pin Threshold	On-to-Off	0.45	0.65		V
	Off-to-On, I_{LOAD} = 1mA		0.85	1.8	V
Output Voltage Noise	I_{LOAD} = 1.5A, BW = 10Hz to 100kHz		40		μV_{RMS}

Note 1: Output voltage variations include ±1% tolerance of feedback divider network. For tighter voltage range, use lower tolerance resistors or use fixed voltage output devices.

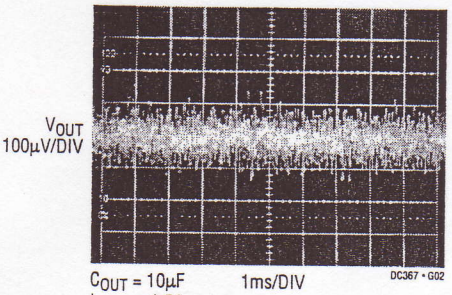
TYPICAL PERFORMANCE CHARACTERISTICS AND BOARD PHOTO

Typical Dropout Voltage

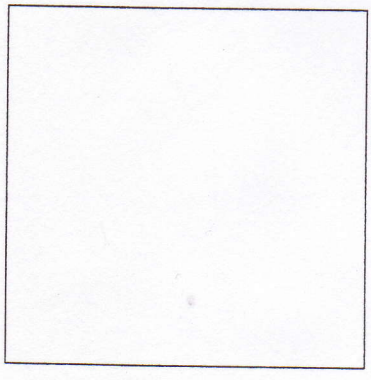


DC367 • G01

LT1963 (3.3V Output)
10Hz to 100kHz Output Noise

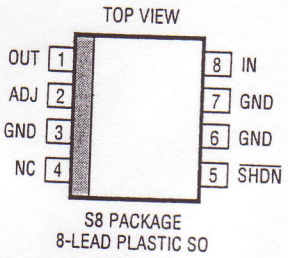


Component Side (Board Photo)



PACKAGE AND SCHEMATIC DIAGRAMS

LT1963ES8



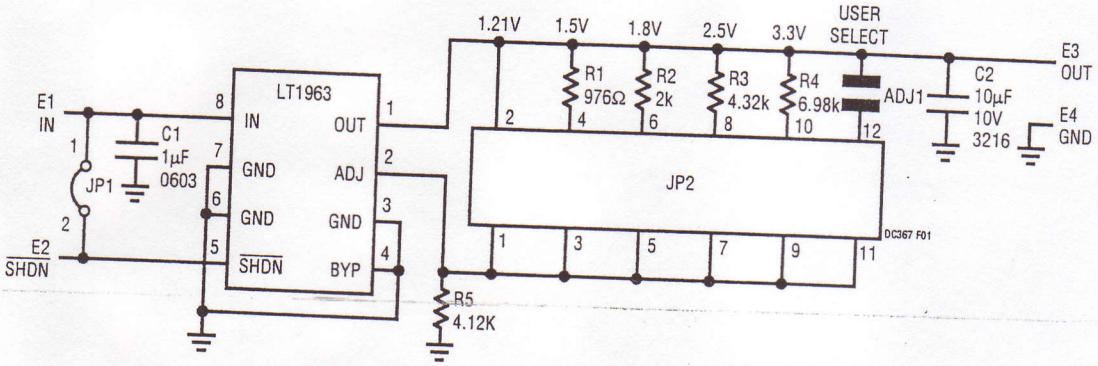


Figure 1. LT1963 1.5A Low Noise Micropower LDO Regulator

PARTS LIST

REFERENCE DESIGNATOR	QUANTITY	PART NUMBER	DESCRIPTION	VENDOR	TELEPHONE
ADJ1	0	0402	Optional		–
C1	1	0603ZG105ZAT1A	1µF 10V Y5V 80% Capacitor	AVX	(843) 946-0362
C2	1	TAJA106M010R	10µF 10V Tantalum Capacitor	AVX	(843) 946-0362
E1 to E4	4	2308-2	1-Pin 0.064" Hole Terminal Turret	Mill-Max	(516) 922-6000
JP1	1	2802S-02-G1	2-Pin 1 Row 0.079 cc Jumper	Comm-Con	(626) 301-4200
JP2	1	6351-12P1	Connector, SMT2X6, 0.39" Gap	Comm-Con	(626) 301-4200
Shunts for JP1	1	CCIJ2MM-138G	Shunt 0.079" Center	Comm-Con	(626) 301-4200
Shunts for JP2	1	CTAIJ1MM-G	Shunts 0.39 cc	Comm-Con	(626) 301-4200
R1	1	CR05-9760FM	976 1/16W 1% Chip Resistor	AAC	(800) 508-1521
R2	1	CR05-2001FM	2k 1/16W 1% Chip Resistor	AAC	(800) 508-1521
R3	1	CR05-4321FM	4.32k 1/16W 1% Chip Resistor	AAC	(800) 508-1521
R4	1	CR05-6981FM	6.98k 1/16W 1% Chip Resistor	AAC	(800) 508-1521
R5	1	CR05-4121FM	4.12k 1/16W 1% Chip Resistor	AAC	(714) 255-9186
U1	1	LT1963ES8	8-Lead SO IC	LTC	(408) 432-1900

OPERATION

HOOK-UP

Solid turret terminals are provided for easy connection to supplies and test equipment. Connect a 0V to 20V, 1.6A power supply across the IN and GND terminals and the load across the OUT and GND terminals. The $\overline{SHDN}$ pin can be disconnected from IN via JP1 to allow for separate shutdown control via a secondary control line. JP2 can be used to select any of a number of common fixed output voltages, or used in conjunction with ADJ1 to create a custom output voltage using the formula:

$$ADJ1 = (V_{OUT} - 1.21V)/297\mu A$$

Thermal Characteristics

Demonstration Circuit DC367 has been laid out to illustrate and achieve maximum power handling capabilities. Although a simple two-layer board might have been sufficient for electrical operation of the LT1963, the four-layer board with vias to internal ground planes offers excellent thermal characteristics. A two-layer board of the same size with no thermal vias will exhibit a thermal resistance of 60°C/W, whereas DC367 exhibits a thermal resistance of 50°C/W.

OUTPUT CAPACITOR SELECTION

The output capacitor C3 is a 10µF tantalum capacitor. Should a different output capacitor be desired, care must be exercised with the selection. Many ceramic capacitor dielectrics exhibit strong temperature and voltage characteristics that reduce their effective capacitance to as low as 10% to 20% of nominal over the full temperature range. For further information, see Linear Technology Application Note 83, "Performance Verification of Low Noise, Low Dropout Regulators," Appendix B, "Capacitor Selection Considerations," reprinted below.

CAPACITOR SELECTION CONSIDERATIONS

Output Capacitance and Transient Response

The regulators are designed to be stable with a wide range of output capacitors. Output capacitor ESR affects stability, most notably with small capacitors. A 10µF minimum output value with ESR of 3Ω or less is recommended to prevent oscillation. Transient response is a function of output capacitance. Larger values of output capacitance decrease peak deviations, providing improved transient response for large load current changes. Bypass capacitors, used to decouple individual components powered by the regulator, increase the effective output capacitor value.

Ceramic Capacitors

Ceramic capacitors require extra consideration. They are manufactured with a variety of dielectrics, each with different behavior across temperature and applied voltage. The most common dielectrics are Z5U, Y5V, X5R and X7R. The Z5U and Y5V dielectrics provide high capacitance in a small package, but exhibit strong voltage and temperature coefficients, as shown in Figures B1 and B2. Used with a 5V regulator, a 10µF Y5V capacitor shows values as low as 1µF to 2µF over the operating temperature range. The X5R and X7R dielectrics have more stable characteristics and are more suitable for output capacitor use. The X7R type has better stability over temperature, while the X5R is less expensive and available in higher values.

Voltage and temperature coefficients are not the only problem sources. Some ceramic capacitors have a piezoelectric response. A piezoelectric device generates voltage across its terminals due to mechanical stress, similar to the way a piezoelectric accelerometer or microphone works. For a ceramic capacitor, the stress can be induced by vibrations in the system or thermal transients. The resulting voltages can cause appreciable amounts of noise, especially when a ceramic capacitor is used for noise bypassing. A ceramic capacitor produced Figure B3's trace in response to light tapping from a pencil. Similar vibration-induced behavior can masquerade as increased output voltage noise.

OPERATION

OUTPUT VOLTAGE NOISE

Measuring output voltage noise can be a tricky process, further complicated by the low levels of noise inherent in a circuit such as this. Consideration must be given to regulator operating conditions, as well as the noise bandwidth of interest. Linear Technology has invested an enormous amount of time to provide accurate, relevant data to customers regarding noise performance. For further information on measuring output voltage noise, see Linear Technology Application Note 83, "Performance Verification of Low Noise, Low Dropout Regulators."

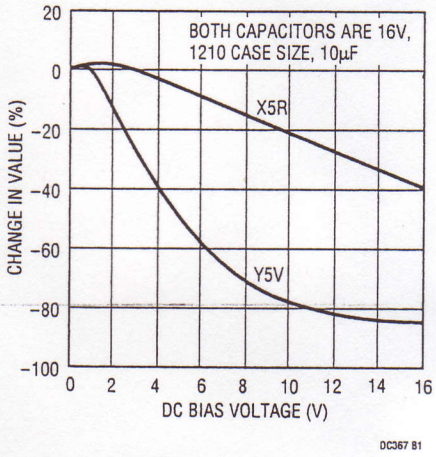


Figure B1. Ceramic Capacitor DC Bias Characteristics Indicate Pronounced Voltage Dependence. Device Must Provide Desired Capacitance Value at Operating Voltage

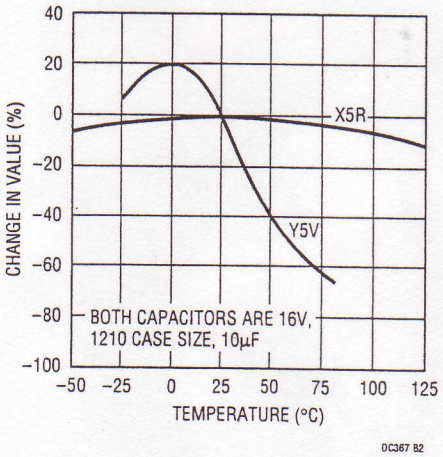


Figure B2. Ceramic Capacitor Temperture Characteristics Show Large Capacitance Shift. Effect Should Be Considered When Determining Circuit Error Budget

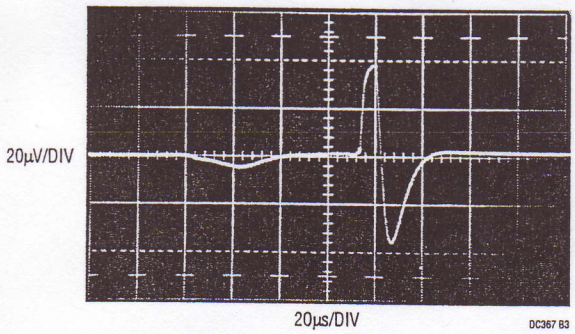


Figure B3. A Ceramic Capacitor Responds to Light Pencil Tapping. Piezoelectric Based Response Approaches 80μV_{P-P}

OPERATION

Noise Testing Considerations

What noise bandwidth is of interest and why is it interesting? In most systems, the range of 10Hz to 100kHz is the information signal processing area of concern. Additionally, linear regulators produce little noise energy outside this region.[1] These considerations suggest a measurement bandpass of 10Hz to 100kHz, with steep slopes at the band limits. Figure 2 shows a conceptual filter for LDO noise testing. The Butterworth sections are the key to steep slopes and flatness in the passband. The small input level requires 60dB of low noise gain to provide adequate signal for the Butterworth filters. Figure 3 details the filter scheme. The regulator under test is at the diagram's center.[2] A1–A3 make up a 60dB gain highpass section. A1 and A2, extremely low noise devices (<1nV$\sqrt{Hz}$), comprise a 60dB gain stage with a 5Hz highpass input. A3 provides a 10Hz, 2nd order Butterworth highpass characteristic. The LTC®1562 filter block is arranged as a 4th order Butterworth lowpass. Its output is delivered via the 330µF-100Ω highpass network. The circuit's output drives a thermally responding RMS voltmeter.[3] Note that all circuit power is furnished by batteries, precluding ground loops from corrupting the measurement.

Note 1: Switching regulators are an entirely different proposition, requiring very broadband noise measurement.

Note 2: Component choice for the regulator, more critical than might be supposed, is discussed in "Capacitor Selection Considerations."

Note 3: The choice of the RMS voltmeter is absolutely crucial to obtaining meaningful measurements. See Appendix C, Application Note 83 "Understanding and Selecting RMS Voltmeters."

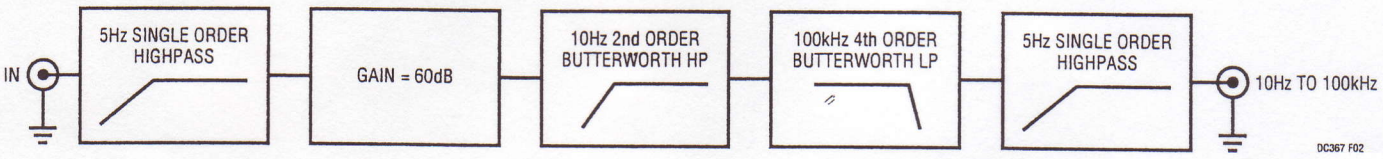


Figure 2. Filter Structure for Noise Testing LDOs. Butterworth Sections Provide Appropriate Response in Desired Frequency Range

OPERATION

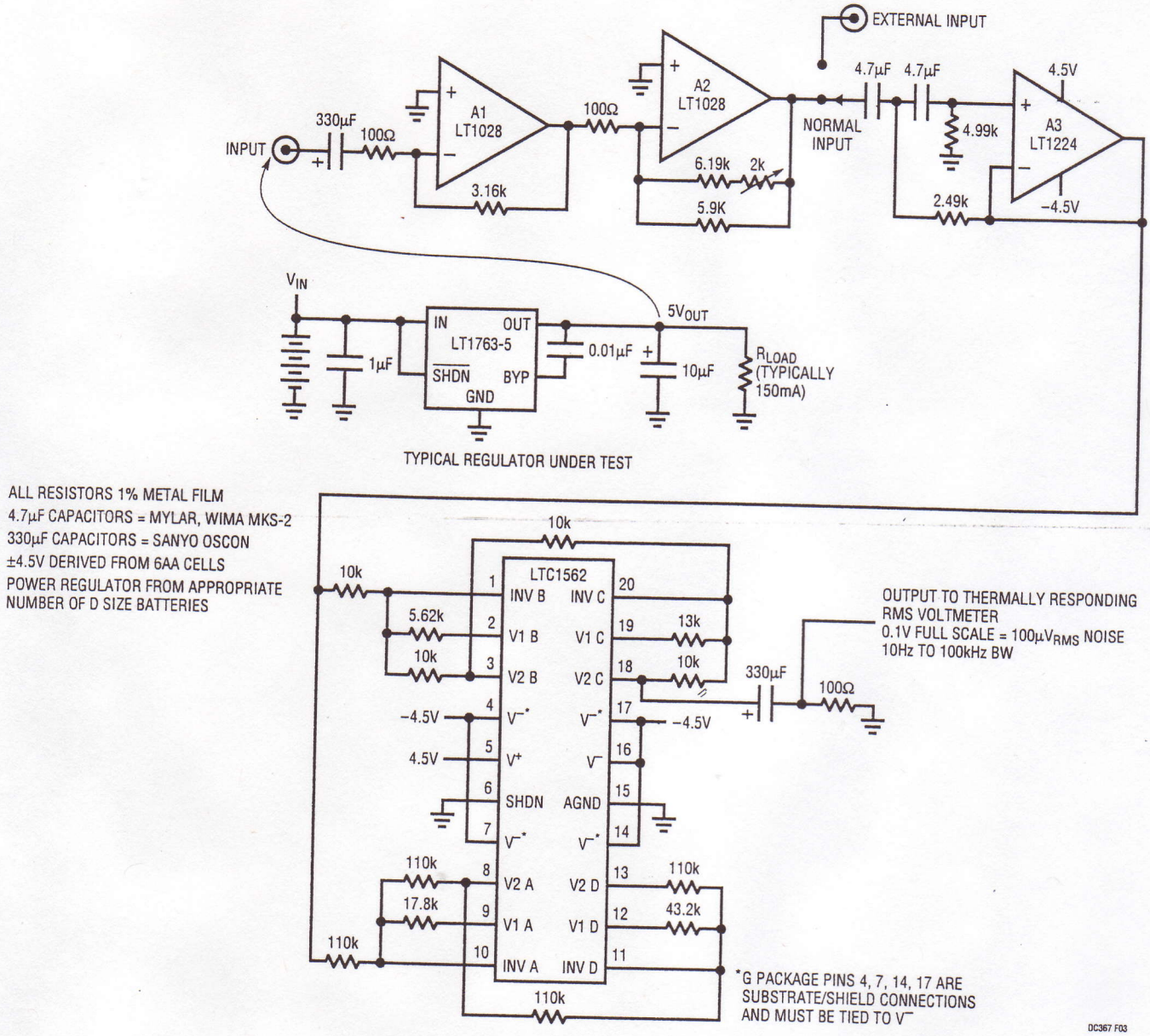
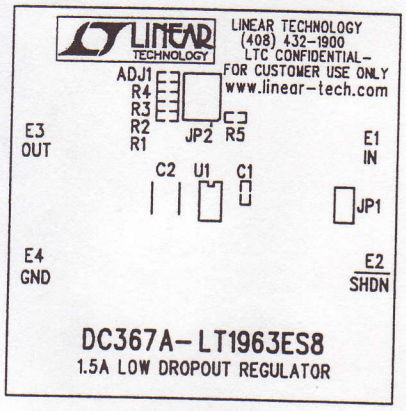
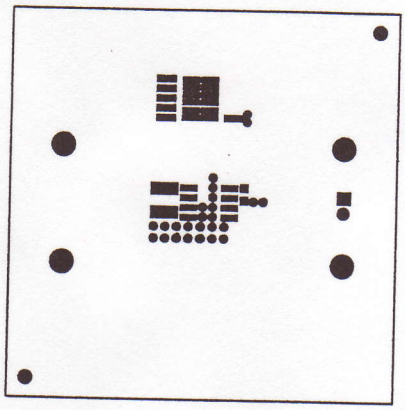


Figure 3. Implementation of Figure 2. Low Noise Amplifiers Provide Gain and Initial Highpass Shaping. LTC1562 Filter Supplies 4th Order Butterworth Lowpass Characteristic

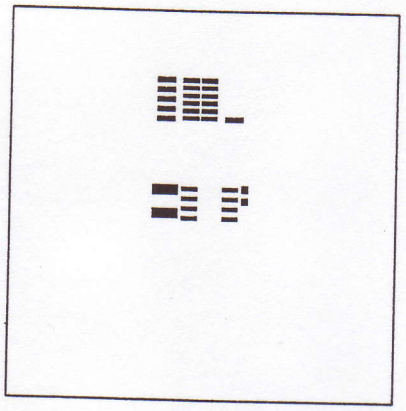
PCB LAYOUT AND FILM



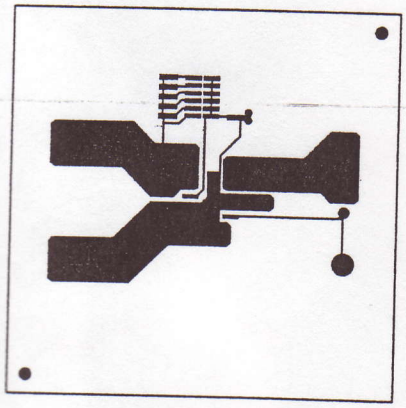
Silkscreen Top



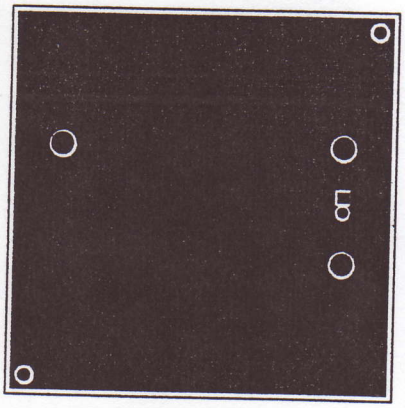
Solder Mask Top



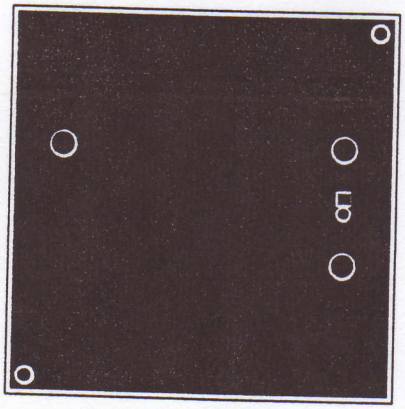
Paste Mask Top



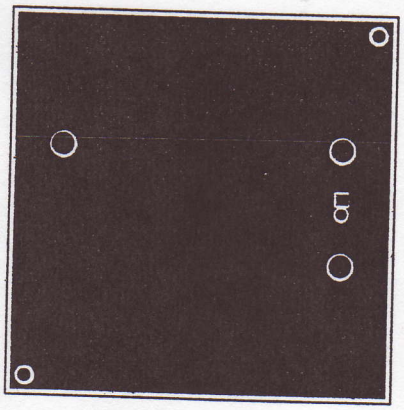
Layer 1, Component Side



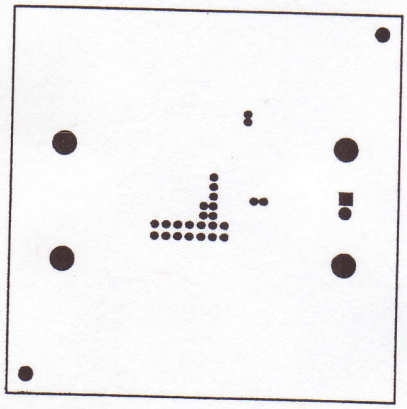
Layer 2, GND Plane*



Layer 3, GND Plane*



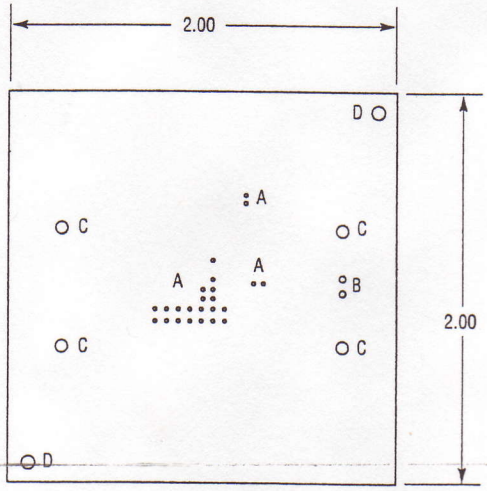
Layer 4, Solder Side*



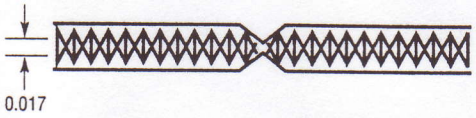
Solder Mask Bottom

* These layers are shorted to L1 with vias and function as heat dispersants.

PC FAB DRAWING



NOTES: UNLESS OTHERWISE SPECIFIED
1. MATERIAL: FR4 OR EQUIVALENT EPOXY, 2 OZ. COPPER CLAD
   THICKNESS 0.062 ± 0.006 TOTAL OF 4 LAYERS.
2. FINISH: ALL PLATED HOLES 0.001 MIN/0.0015MAX COPPER PLATE
   ELECTRODEPOSITED TIME-LEAD COMPOSITION
   BEFORE REFLOW, SOLDER MASK OVER BARE COPPER (SMOBC)
3. SOLDER MASK: BOTH SIDES USING LPI OR EQUIVALENT.
4. SILKSCREEN: USING WHITE NON-CONDUCTIVE EPOXY INK.
5. UNUSED SMD COMPONENTS SHOULD BE FREE OF SOLDER.
6. FILL UP ALL VIAS WITH SOLDER.
7. SCORING:



SYMBOL	DIAMETER	NUMBER OF HOLES	PLATED
A	0.02	25	YES
B	0.035	2	YES
C	0.064	4	YES
D	0.07	2	NO

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