DC3159A and DC3017A LTC9101-1/LTC9102/LTC9103 24-Port, 4-Pair IEEE 802.3bt PSE

DESCRIPTION

Demonstration kit 3160A-KIT is an Ethernet Alliance Gen 2 PoE certified, 24-port IEEE 802.3at/bt-compliant power sourcing equipment (PSE) composed of a DC3159A daughter card (48-channels) and DC3017A motherboard (24, 4-pair ports). The DC3160A-KIT features the LTC®9101-1/LTC9102/LTC9103 PSE platform chipset.

In the DC3160A-KIT, a single LTC9101-1 digital controller interfaces with up to four analog controllers. The DC3159A-A daughter card has four LTC9102, 12-channel, analog controllers for 48 power channels total. The DC3159A-B daughter card has two LTC9102, 12-channel, analog controllers and two LTC9103, 8-channel, analog controllers for 40 power channels total. Up to twenty-four IEEE 802.3af, IEEE 802.3at, or IEEE 802.3bt powered devices (PDs) can be connected to the DC3160A-KIT and powered from this system using a single power supply.

The LTC9101-1, LTC9102, and LTC9103 use a proprietary isolated data interface allowing the LTC9101-1 to directly connect to the host controller I^2C interface and eliminates the need for costly opto-couplers and an additional 3.3V supply. The DC3160A-KIT can operate completely autonomously without a host controller or with a DC590 for I^2C interfacing.

Robust surge protection is provided by design and onboard surge protection devices. Indicator LEDs show channel status for up to 48 power channels. An optional on-board buck regulator provides 3.3V from the VEE supply for the digital circuity. This demonstration manual provides an auto mode quick start procedure and DC3160A-KIT overview.

Design files for this circuit board are available.

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BOARD PHOTO

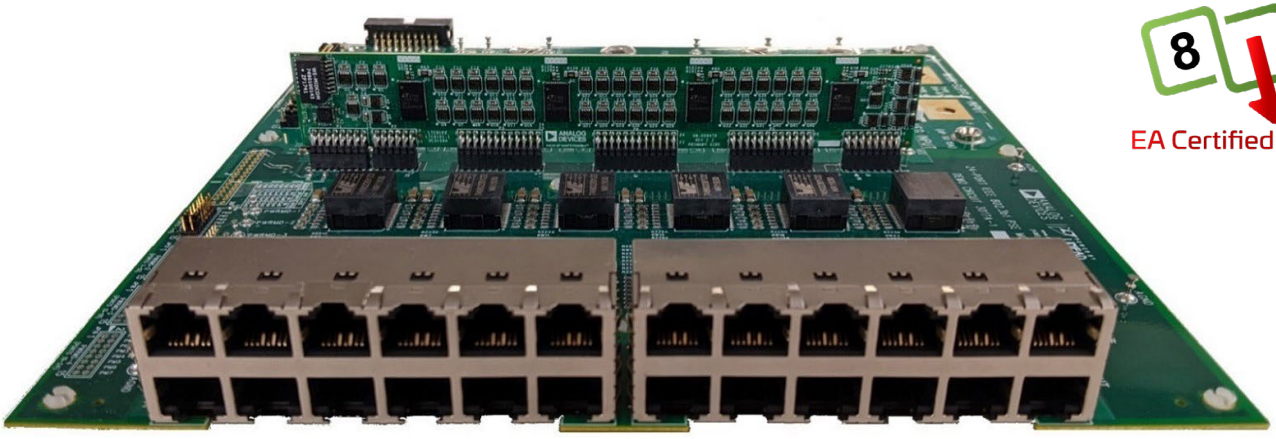

Table 1. DC3160A-KIT Options and PSE Controller Chipsets

DEMO KIT	DAUGHTER CARD	MOTHERBOARD	LTC9101 VERSION	LTC9102 COUNT	LTC9103 COUNT	4-PAIR PORTS
DC3160A-A-KIT	DC3159A-A	DC3017A-A	-1	4	0	24
DC3160A-B-KIT	DC3159A-B	DC3017A-A	-1	2	2	20

QUICK START PROCEDURE

DC3160A-KIT Operation in Auto Mode

DC3160A-KIT includes the DC3159A daughter card and DC3017A motherboard. This kit allows for evaluating the LTC9101-1/LTC9102/LTC9103 chipset configured as a either a 20-port or 24-port, 4-pair PSE Endpoint. Refer to Table 1 for the differences between DC3160A-A-KIT and DC3160A-B-KIT.

Follow the procedure below and refer to Figure 1 through Figure 3, and Table 2 through Table 9 for proper equipment setup and default configuration. This default setup will automatically power all valid PDs at all power classes.

1. On the DC3017A motherboard, set AUTO jumper (JP16) to HI to enable autonomous operation.
2. On the DC3017A motherboard, set $\overline{\text{4PVALID}}$ jumper (JP14) to LO to only power IEEE 802.3 compliant PDs that present a valid detection signature on both Alternative A and Alternative B pairsets. $\overline{\text{4PVALID}}$ is ignored while the system is configured as a 2-pair PSE.
3. On the DC3017A motherboard, set the jumper PWRMD-1 (JP1) for the maximum power level, PM6.
4. On the DC3017A motherboard, set the address switches AD2 and AD3 (SW5) to LO for the default 20h base I^2C address.
5. On the DC3017A motherboard, set the CFG0 (JP20), CFG1 (JP21), and CFG2 (JP22) jumpers to HI to set CFG[2:0] logically to 111b for 4-pair operation at all ports.
6. Align pin 1 of the 16-pin male connector P1 on the DC3159A daughter card with pin 1 of the 16-pin female connector J11 on the DC3017A motherboard as shown in Figure 2. The six male connectors and six female sockets should match. Keyed pins in J16 and J12 assist with the alignment shown in Figure 3. Carefully push the daughter card straight down until the male and female connectors are flush with each other.
7. Connect a supply to the DC3017A motherboard with the positive rail to POS INPUT (+) and negative rail to NEG INPUT (–) as shown in Figure 3. Use a power supply capable of sourcing the maximum sourced power for all ports to be tested. Ramp the supply up to within the recommended voltage range specified in Table 2.

NOTE: Banana jacks J8 and J10 should only be used for up to 15A of supply current. Use the lugnut terminals J7 and J9 with the provided Panduit S4-14R lugs for supply currents of up to 50A; enough for 24 ports at maximum power.

8. Connect up to twenty-four IEEE 802.3af, 802.3at, or 802.3bt PDs to the motherboard's RJ45 connectors J3 and J4, as shown in Figure 3.

NOTE: RJ45 ports 15, 16, 20 and 21 on J3 are blocked on the DC3017A-A motherboard in the DC3160A-B-KIT. See the section on Port Output for more information.

QUICK START PROCEDURE

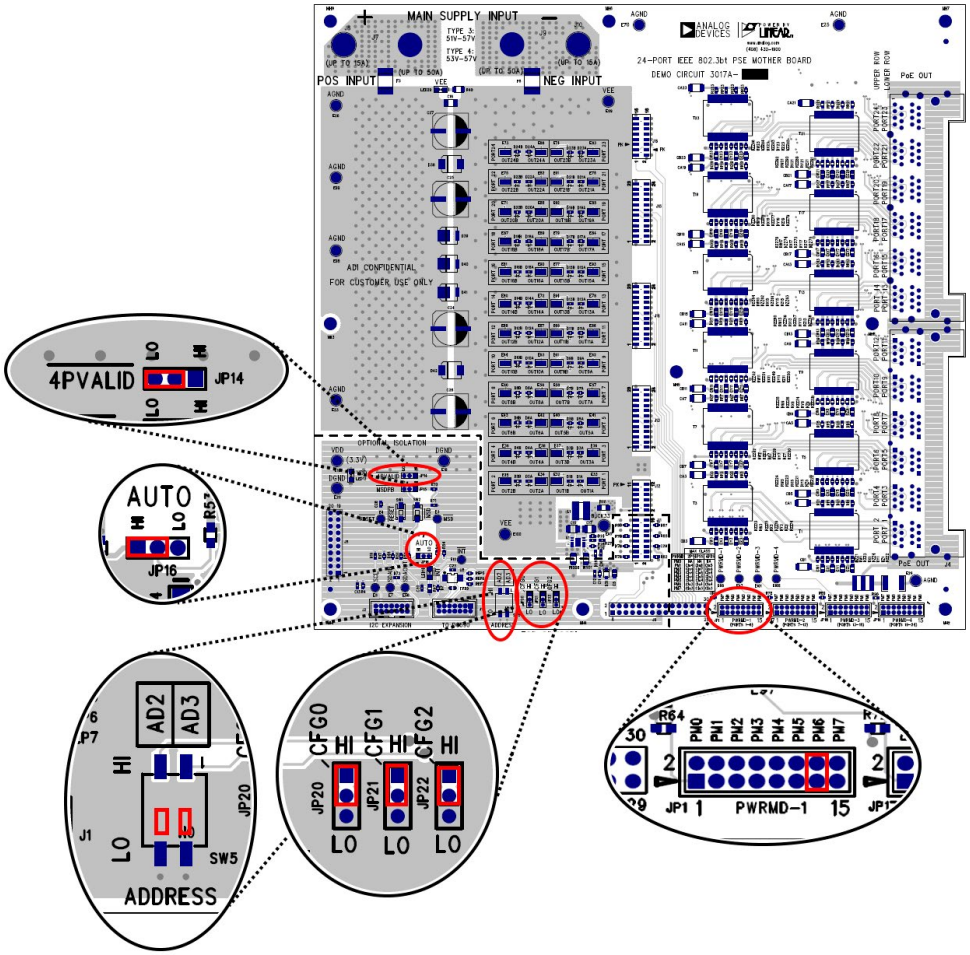

Figure 1. Default Settings for DC3017A Motherboard, Jumpers: $\overline{\text{4PVALID}}$, AUTO, PWRMD0, CFG0, CFG1, and CFG2; Switches: AD2 and AD3

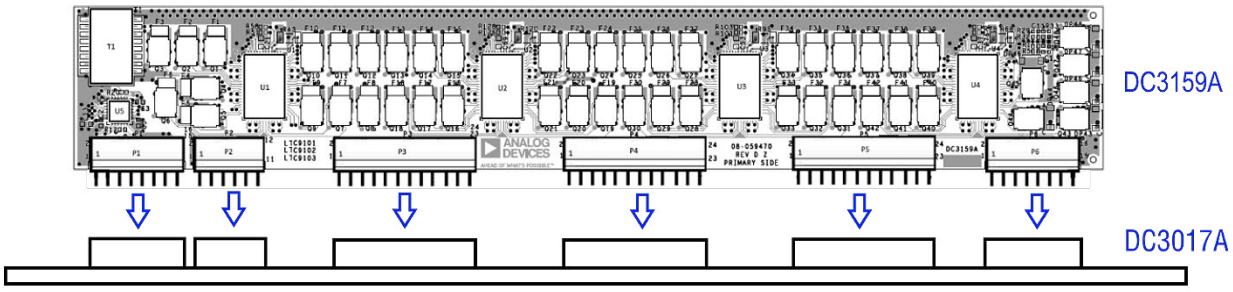

Figure 2. Inserting the DC3159A Daughter Card into J1 through J6 of the DC3017A Motherboard

QUICK START PROCEDURE

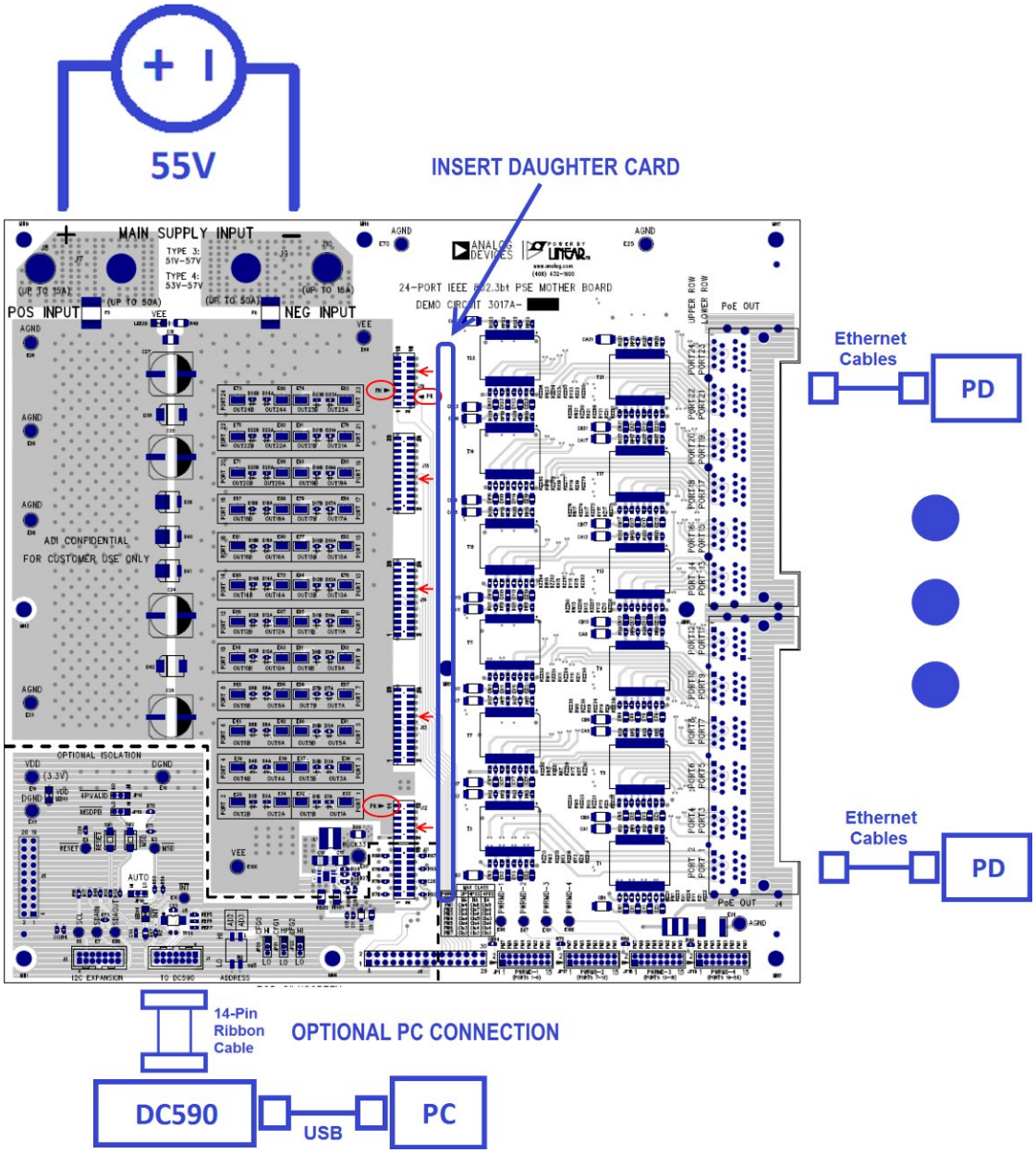

Figure 3. DC3160A-KIT Connections

Table 2. DC3160A-KIT Power Supply Voltage per PSE Type

IEEE 802.3 TYPE, MAX CLASS	SUPPLY VOLTAGE RANGE
Type 2 or 3, Up to Class 6	51V to 57V
Type 4, Up to Class 8	53V to 57V

QUICK START PROCEDURE

Table 3. DC3160A-KIT AUTO and $\overline{\text{4PVALID}}$ Jumper Settings

JUMPER	SETTING	OPERATION
AUTO (JP16)	LO	Host control required.
	HI	Autonomous
$\overline{\text{4PVALID}}$ (JP14)	LO	4-pair port powered only when both pairsets present a valid signature – IEEE Compliant.
	HI	Any pairset presenting a valid signature is powered.

Table 4. DC3160A-KIT I^2C Address Settings

SW5		
AD3	AD2	I^2C BASE ADDRESS
LO	LO	20h
LO	HI	24h
HI	LO	28h
HI	HI	2Ch

Table 5. DC3160A-KIT CFG2 and CFG1 Jumper Settings

JUMPER		NUMBER OF ANALOG CONTROLLERS
CFG2 (JP22)	CFG1 (JP21)	
LO	LO	1
LO	HI	2
HI	LO	3
HI	HI	4

Table 6. DC3160A-KIT CFG0 Jumper Settings

CFG0 (JP20)	PORT TYPE
LO	2-Pair
HI	4-Pair

Table 7. DC3160A-A-KIT Device Configuration Options

JUMPER			NUMBER OF PORTS	
CFG2 (JP22)	CFG1 (JP21)	CFG0 (JP20)	4-PAIR PORTS	2-PAIR PORTS
LO	LO	LO	0	12
LO	LO	HI	RESERVED	
LO	HI	LO	0	24
LO	HI	HI	12	0
HI	LO	LO	0	36
HI	LO	HI	RESERVED	
HI	HI	LO	0	48
HI	HI	HI	24	0

Table 8. DC3160A-B-KIT Device Configuration Options

JUMPER			NUMBER OF PORTS	
CFG2 (JP22)	CFG1 (JP21)	CFG0 (JP20)	4-PAIR PORTS	2-PAIR PORTS
LO	LO	LO	0	12
LO	LO	HI	RESERVED	
LO	HI	LO	0	24
LO	HI	HI	12	0
HI	LO	LO	0	32
HI	LO	HI	16	0
HI	HI	LO	0	40
HI	HI	HI	20	0

Table 9. DC3160A-KIT Auto Mode Maximum Class for PWRMD0 Pin, R_{PWRMD} and the PWRMD-1 Jumper

PWRMD-1 JUMPER SETTING	R_{PWRMD} RESISTOR	2-PAIR MODE	4-PAIR MODE	
		MAX PORT POWER	MAX PORT POWRER SINGLE-SIGNATURE PD	MAX PORT POWRER DUAL-SIGNATURE PD*
PM0	OPEN	Class 3: 13.0W	Class 3: 13.0W	Class 3: 13.0W
PM1	24.3k		Class 4: 25.5W	Class 4: 25.5W
PM2	18.7k	Class 4: 25.5W		
PM3	14.3k		Class 5: 40.0W	Class 3: 13.0W
PM4	11.0k		Class 6: 51.0W	Class 4: 25.5W
PM5	8.45k		Class 7: 62.0W	
PM6	6.49k		Class 8: 71.3W	Class 5: 35.6W
PM7	1.00k	RESERVED		

*In auto mode, total port power allocation is double this value, reflecting the two halves of a dual-signature PD.

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DC3160A-KIT includes the DC3017A, a 24-Port, 4-pair IEEE 802.3bt PoE PSE motherboard for a PSE endpoint. This motherboard accepts a DC3159A daughter card with up to 48 power channels. It contains two, 2 × 6, RJ45 connectors and twenty-four, 1000BASE-T, Ethernet transformers rated for IEEE 802.3bt Type 4, Class 8 power levels. The DC3017A motherboard also has switches, jumpers, and pushbuttons for configuring the PSE, with status LEDs and test points.

Port Output

PDs are connected using an Ethernet cable (Cat5, Cat5e or better cabling as specified by IEEE 802.3) to any of the ports at the two, 2 × 6, RJ45 connectors J3 and J4 on the DC3017A motherboard. The LTC9101-1/LTC9102/LTC9103 delivers power over one or two power channels when configured as a 2-pair or 4-pair port, respectively. Each pairset is driven by a dedicated power channel. The term "channel" refers to the PSE circuitry assigned to a corresponding pairset. Each port is connected as a 4-pair port driven by two power channels; OUTnA and OUTnB connect to port n (n = port #). OUTnA pairset connects to Alternative A (pairs 1,2 and 3,6) and OUTnB pairset connects to Alternative B (pairs 4,5 and 7,8).

A 2-pair PSE uses a single power channel per port, connected to either Alternative A or Alternative B. Refer to the section on Evaluating the DC3160A-KIT as a 2-pair PSE for more information. Test points for each channel output, OUT1A through OUT24B are provided.

The DC3160A-A-KIT supports all 24, 4-pair ports allowed by the PCB layout. Refer to Figure 4 for the port output map of the DC3160A-A-KIT.

The DC3160A-B-KIT supports up to 20, 4-pair ports. Ports 15, 16, 21, and 22 are not connected with the DC3159A-B daughter card, and these ports are blocked on the DC3017A-A motherboard in the DC3160A-B-KIT. Ports 15 through 20 are remapped on J3, the second 2 × 6 RJ45 block. Refer to Figure 5 for the DC3160A-B-KIT port map.

Daughter Card Insertion Precautions

When inserting or removing the daughter card into the DC3017A motherboard, verify all supplies and LEDs are off. Push the card straight down for insertion or pull straight up for removal to avoid bending the connector pins. Follow the instructions in the Quick Start Procedure for alignment and refer to Figure 2.

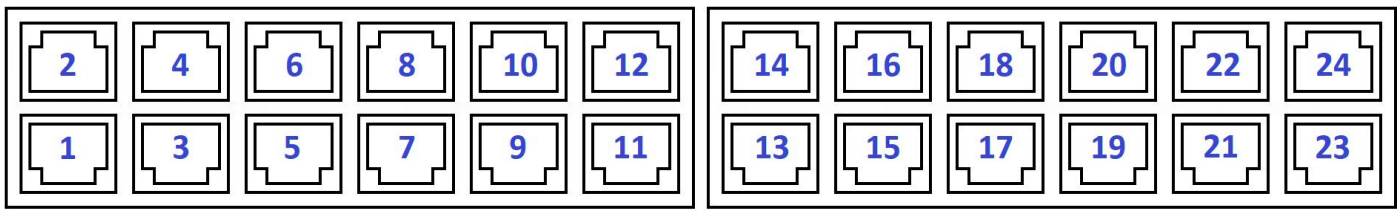

Figure 4. DC3160A-A-KIT Port Output Map

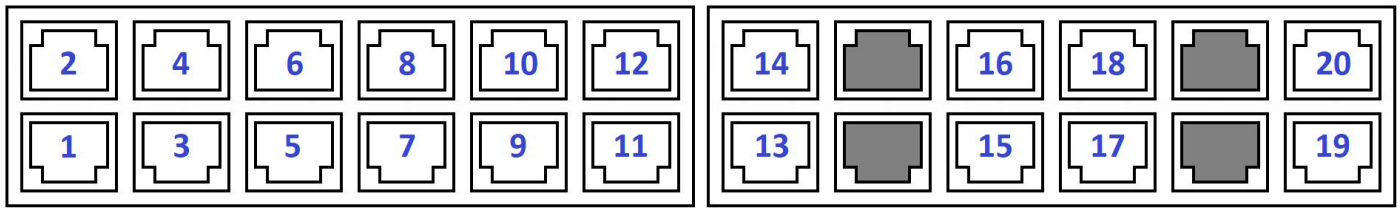

Figure 5. DC3160A-B-KIT Port Output Map

DEMONSTRATION CIRCUIT 3160A KIT

Main VEE PoE Supply

The VEE supply is the main PoE supply connected to the DC3017A motherboard. Refer to the Quick Start Procedure for proper connection and Table 2 for appropriate supply voltage ranges.

Choose a power supply with a current limit set higher than the maximum allowed output power at each port. Use the appropriate input supply connections per the maximum current expected during testing; banana jacks for up to 15A or the provided Panduit S4-14R lugnuts for up to 50A, as seen in Figure 6. The lugs are designed for crimping to 4 AWG welding cable. Use a Thomas & Betts WT115 crimping tool to crimp the S4-14R lugs to 4 AWG welding cable; do not mash or solder the lugs. To avoid damage to the motherboard, do not over tighten the lugs. A torque sufficient to fully compress the split washer (roughly equivalent to 400 in-oz applied to the ¼-28 hex nut) is sufficient to produce good electrical contact.

Isolation

IEEE 802.3 Ethernet specifications require network segments (including the analog PoE circuitry) to be electrically isolated from the chassis ground. The DC3017A motherboard and DC3159A daughter card layouts and high voltage capacitors provide an isolation barrier between analog and digital domains. Transformers and layout provide a galvanic barrier between DGND and AGND on the DC3159A daughter card. By default, this isolation barrier is bridged by resistors on the motherboard to allow for evaluation using a single power supply. Remove RISO1 and RISO2, then provide an external 3.3V supply between VDD and DGND to evaluate this board as an isolated system.

All RJ45 shields and terminations are connected to chassis ground. AGND and VEE each connect to chassis ground with two pairs of 1nF, 2kV capacitors (C6 to C9). AGND and VEE also connect to DGND each with 10nF, 2kV capacitors (C32 to C33). An optional 0Ω resistor can be installed at RISO3 to tie the chassis ground to DGND. Two series 5.1M, 1206 resistors connect between AGND and DGND for high voltage capacitance discharge. See Figure 7 for diagram of connections between Analog and Digital domains, as well as chassis ground on the DC3017A motherboard.

LED Indicators

The VEE LED (D29) and VDD LED (LED13) indicate if a voltage is present at the respective supplies. Verify these LEDs are off before inserting or removing the daughter card.

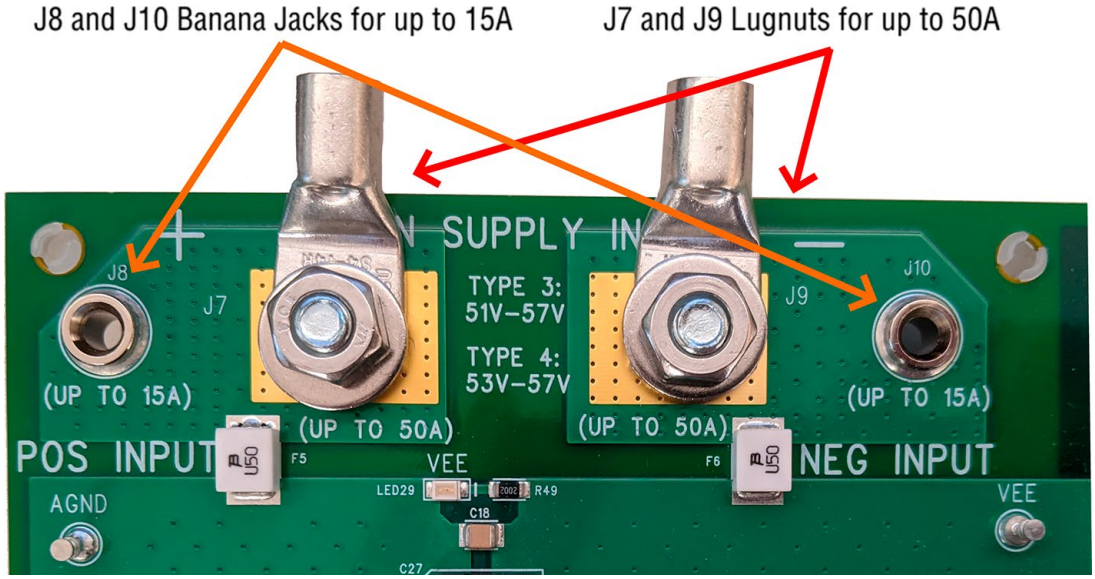

Figure 6. Motherboard Power Supply Connections

DEMONSTRATION CIRCUIT 3160A KIT

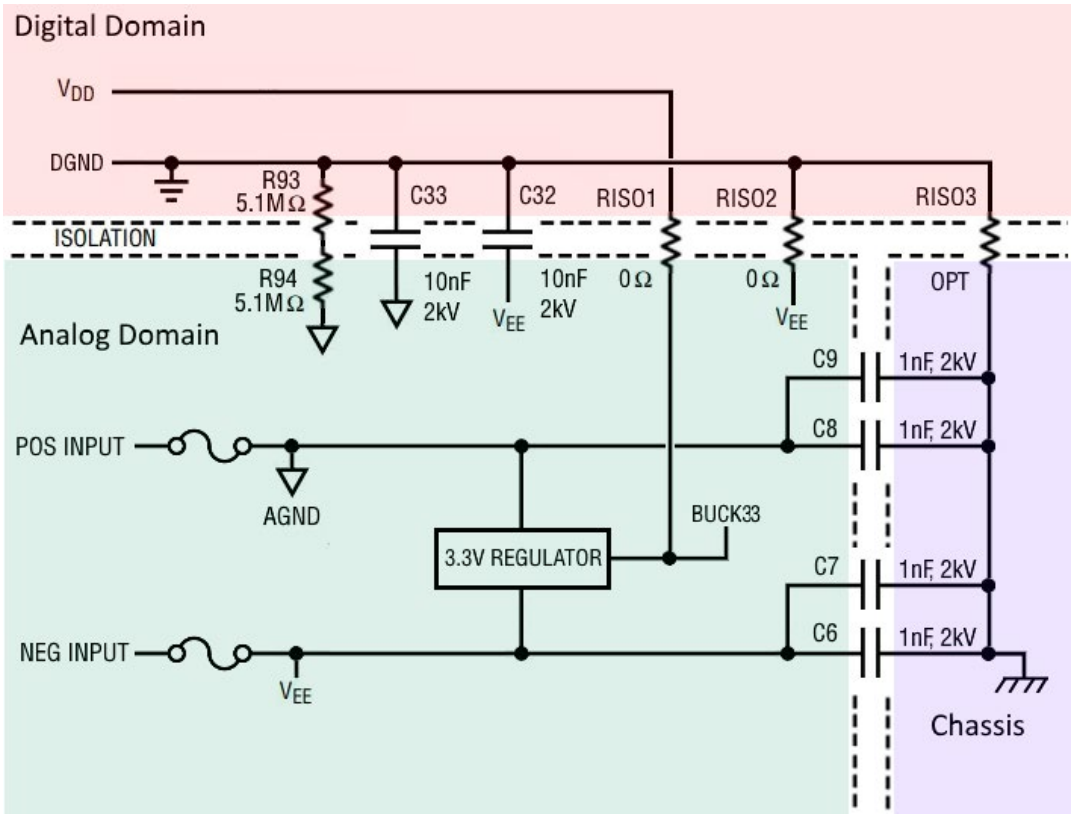

Figure 7. Motherboard Power Supply Connections and Isolation Barriers

Each port pairset power channel has a respective OUTnM (n = port #, M = port powered pairset; with A = Alternative A, and B = Alternative B) LED to indicate if the channel is detecting, classifying, or powered. A blue LED is connected to each OUTnA, while a green LED is connected to each OUTnB. The red $\overline{INT}$ LED (LED14) indicates if the interrupt line is pulled low by the daughter card.

For the DC3160A-B-KIT with the DC3159A-B (40-channel) daughter card, the OUT15A, OUT15B, OUT16A, OUT16B, OUT21A, OUT21B, OUT22A, and OUT22B LEDs do not indicate port status as these power channels are not connected with the populated LTC9103s.

AUTO, $\overline{4PVALID}$, and PWRMD0 Settings

The LTC9101-1/LTC9102/LTC9103 settings depend on the AUTO pin state during reset. Reset occurs on a VDD or VEE power cycle, $\overline{RESET}$ pin is pulled low and released high, or when the global Reset All bit is set. If the AUTO pin is set to HI during reset, then $\overline{4PVALID}$, PWRMD0, and CFG[2:0] pin settings are used to configure auto mode operation. Changing the state of these pins will not change the PSE configuration until a reset occurs. The AUTO pin is set by the AUTO jumper, JP16. When set to HI, this jumper enables autonomous operation. Setting AUTO pin LO requires software configuration of the PSE. The $\overline{4PVALID}$ pin of the LTC9101-1 is controlled by the $\overline{4PVALID}$ jumper, JP14. When $\overline{4PVALID}$ is LO, the port is only powered when both pairsets present a valid signature, per IEEE 802.3 requirements. If $\overline{4PVALID}$ is HI, any pairset presenting a valid signature is powered. $\overline{4PVALID}$ is ignored when configured as a 2-pair PSE. Reference Table 3 for AUTO and $\overline{4PVALID}$ settings.

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The PWRMD0 pin of the LTC9102/LTC9103 at address ID:00b sets the maximum power allocation while operating autonomously. This pin connects to the R_{PWRMD} resistor using the PWRMD-1 jumper (JP1). R_{PWRMD}, along with the AUTO mode reset state are used to automatically determine the power allocation per port. Refer to Table 9 for the PWRMD0 and R_{PWRMD} settings.

Device Configuration

The CFG0, CFG1, and CFG2 pins configure the number of analog controllers and the port type in the system. Each pin connects to a jumper that pulls either HI for a logical 1, or LO for logical 0. CFG2 and CFG1 set the number of analog controllers in the system. Refer to Table 5 for the CFG[2:1] settings. CFG0 sets whether the system is configured as a 2-pair or 4-pair PSE, per Table 6. Refer to Table 7 and Table 8 for specific port type and number of ports for each of the DC3160A-KITs. Refer to the Evaluating the DC3160A-KIT as a 2-pair PSE section for more information on 2-pair PSEs.

Custom Configurations

An LTC9101-1/LTC9102/LTC9103 system may be configured in an arbitrary combination of 2-pair or 4-pair quads by storing a custom configuration package in a dedicated flash partition. If a stored configuration is utilized, the state of the AUTO, CFG0, PWRMD0, and $\overline{\text{4PVALID}}$ pins can be overwritten by the configuration package. CFG[2:1] are still required to inform the LTC9101-1 how many analog controllers are in the system. AD[3:2] are still required to inform the LTC9101-1 of the base I^2C chip address. Refer to the data sheet for more information and contact ADI Applications for assistance with generating custom configuration packages.

Digital Connections

The DC590 USB to I^2C controller board is connected to the DC3017A motherboard at J1 through a 14-pin ribbon cable. I^2C address pin AD3, and AD2 are set with a 2-bit switch, SW3 on the DC3017A. Refer to Table 4 for setting the individual I^2C address for each DC3160A-KIT. SDAOUT and SDAIN can be tied together through a shunt resistor, R73. Turrets on the DC3017A motherboard provide test points for SCL, SDAIN, SDAOUT, VDD, DGND, $\overline{\text{INT}}$, $\overline{\text{MSD}}$, and $\overline{\text{RESET}}$.

$\overline{\text{MSD}}$ and $\overline{\text{RESET}}$ Pushbuttons

Pushbutton switch SW1, when pressed, pulls the $\overline{\text{RESET}}$ pin of the daughter card logic low. The PSE controller is then held inactive with all ports off. When SW1 is released, $\overline{\text{RESET}}$ is pulled high, and the PSE returns to the AUTO mode reset state. Pushbutton switch SW2, when pressed pulls the maskable shutdown input, $\overline{\text{MSD}}$ pin of the daughter card logic low. When pressed, all ports that have their corresponding mask bit set in the mconfig register of the PSE controller will be shutdown. These ports must then be manually re-enabled via I^2C or by resetting the PSE.

Onboard 3.3V Supply

The DC3017A motherboard has an onboard (non-isolated) 3.3V/100mA buck regulator that provides a local 3.3V, with the net named BUCK33. This onboard logic supply is for demonstration purposes only and allows for use of a single supply while evaluating the DC3160A-KIT.

Surge Testing

The DC3160A-KIT can be configured with either the Digital domain connected to reference ground plane, or with the Digital domain floating with the Analog domain for different surge test setups. The default DC3160A-KIT configuration has DGND connected to VEE and floating from chassis ground.

Evaluating the DC3160A-KIT as a 2-pair PSE

The LTC9101-1/LTC9102/LTC9103 PSE chipset supports both 2-pair and 4-pair modes of operation, but the DC3160A-KIT layout is specifically for 4-pair ports. Each 4-pair port may be physically split into two separate 2-pair ports using an Ethernet splitter such as Tripp Lite's N035-001 or a custom Y-Cable. This device or cable splits the pairsets from one RJ45 port at the PSE into two separate

DEMONSTRATION CIRCUIT 3160A KIT

RJ45 ports or plugs that connect to two separate PDs. An Ethernet splitter is required for each RJ45 port in 2-pair mode on the DC3160A-KIT. Figure 8 shows a Y-Cable that connects Alternative A from the 4-pair PSE (pairs 1,2 and 3,6) to the Alternative A of one PD, and connects Alternative B from the 4-pair PSE (pairs 4,5 and 7,8) to Alternative B for the second PD.

Thermal Performance

The DC3159A-A daughter card demonstrates a compact layout solution for 48, IEEE 802.3bt, PSE power channels on a 1.1-inch × 6.95-inch PCB area. In such a tight layout with little thermal relief, the LTC9101-1/LTC9102/LTC9103 platform is able to keep heat low by utilizing a low resistance sense resistor and low $R_{DS(ON)}$ external MOSFET at each power channel. Figure 9 is a thermal image of the DC3159A-A daughter card with each of the 24, 4-pair, PoE ports loaded to 1.73A and a VEE supply of –55V; no fan was used.

For even further heat reduction on the daughter card, the LTC9102 and LTC9103 respective CAP3 pin can be supplied with an external 3.3V and not rely on the internal supply of the IC. The DC3160A-KIT provides component stuffing options to connect BUCK33 to each of the LTC9102 or LTC9103 CAP3 pins and configure the respective EXT3 pins.

EMI Performance

The DC3160A-KIT has exceptionally low radiated emissions. Figure 10 and Figure 11 show CISPR 32 radiated emissions tests performed in a 3-meter semi-anechoic chamber. Both horizontal and vertical tests pass the Class B limits by more than 15dB.

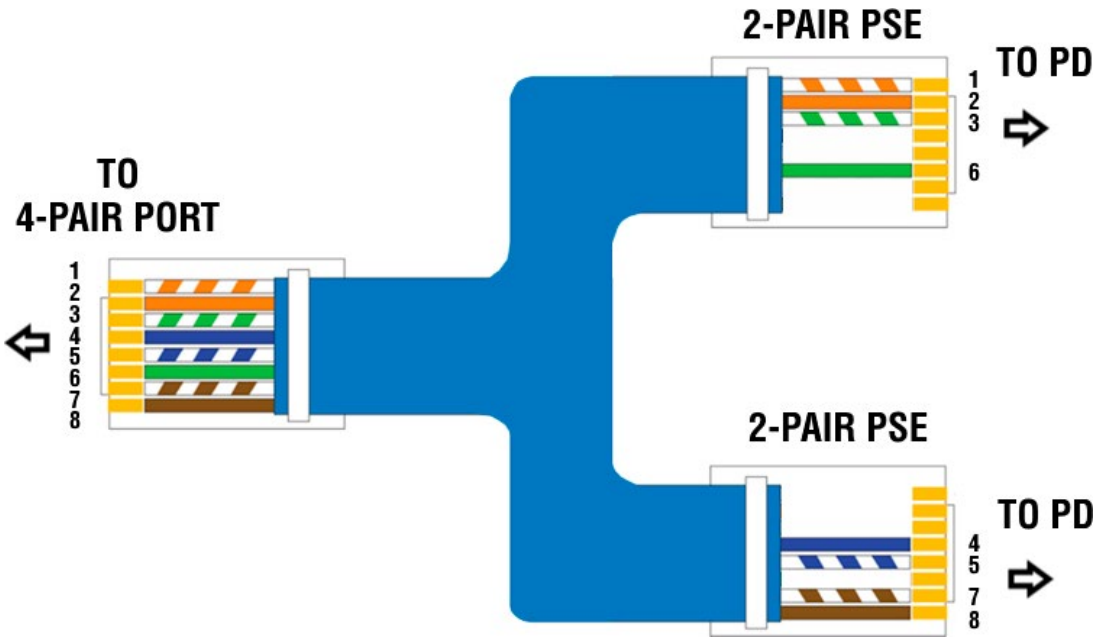

Figure 8. Example Connections and Pinout for Ethernet Splitter or Y-Cable

DEMONSTRATION CIRCUIT 3160A KIT

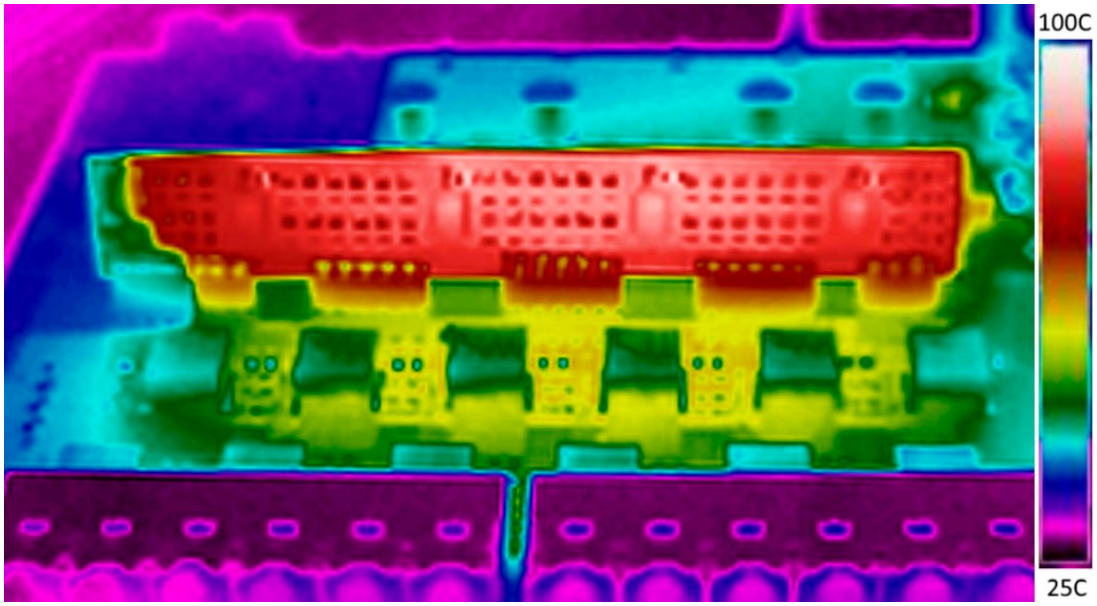

Figure 9. Thermal Image of the DC3159A-A Daughter Card with All 24, 4-pair Ports Loaded with 1.73A Each and VEE at –55V

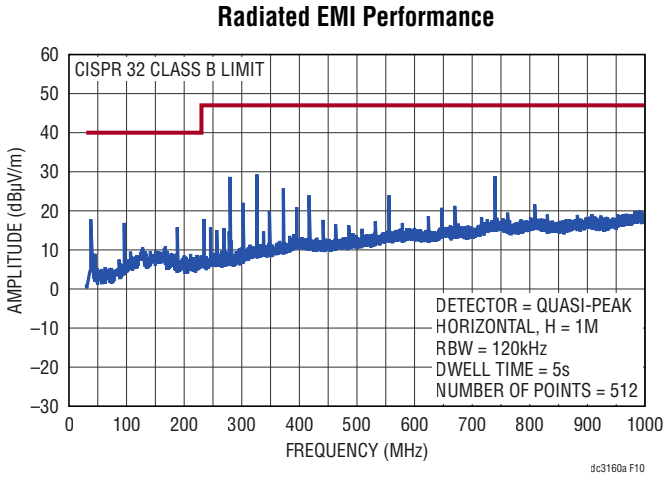

Figure 10. DC3160A-A-KIT Radiated Emissions Performance; CISPR 32 Radiated Emissions Test, Antenna Polarization: Horizontal, 3-Meters

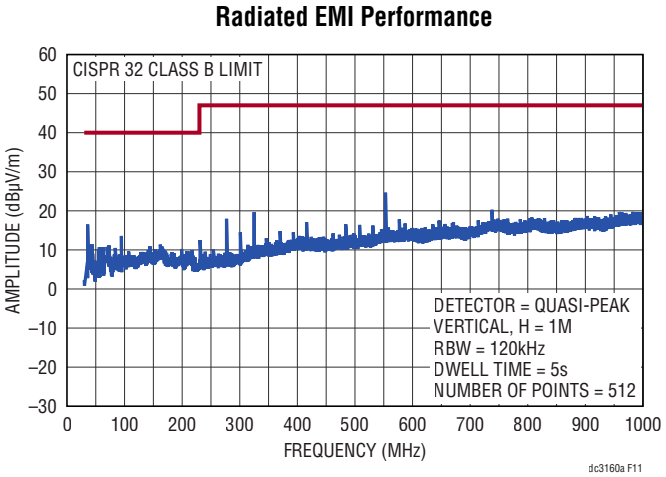

Figure 11. DC3160A-A-KIT Radiated Emissions Performance; CISPR 32 Radiated Emissions Test, Antenna Polarization: Vertical, 3-Meters

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ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Legal Terms and Conditions

By using the evaluation board discussed herein (together with any tools, components documentation or support materials, the "Evaluation Board"), you are agreeing to be bound by the terms and conditions set forth below ("Agreement") unless you have purchased the Evaluation Board, in which case the Analog Devices Standard Terms and Conditions of Sale shall govern. Do not use the Evaluation Board until you have read and agreed to the Agreement. Your use of the Evaluation Board shall signify your acceptance of the Agreement. This Agreement is made by and between you ("Customer") and Analog Devices, Inc. ("ADI"), with its principal place of business at One Technology Way, Norwood, MA 02062, USA. Subject to the terms and conditions of the Agreement, ADI hereby grants to Customer a free, limited, personal, temporary, non-exclusive, non-sublicensable, non-transferable license to use the Evaluation Board FOR EVALUATION PURPOSES ONLY. Customer understands and agrees that the Evaluation Board is provided for the sole and exclusive purpose referenced above, and agrees not to use the Evaluation Board for any other purpose. Furthermore, the license granted is expressly made subject to the following additional limitations: Customer shall not (i) rent, lease, display, sell, transfer, assign, sublicense, or distribute the Evaluation Board; and (ii) permit any Third Party to access the Evaluation Board. As used herein, the term "Third Party" includes any entity other than ADI, Customer, their employees, affiliates and in-house consultants. The Evaluation Board is NOT sold to Customer; all rights not expressly granted herein, including ownership of the Evaluation Board, are reserved by ADI. CONFIDENTIALITY. This Agreement and the Evaluation Board shall all be considered the confidential and proprietary information of ADI. Customer may not disclose or transfer any portion of the Evaluation Board to any other party for any reason. Upon discontinuation of use of the Evaluation Board or termination of this Agreement, Customer agrees to promptly return the Evaluation Board to ADI. ADDITIONAL RESTRICTIONS. Customer may not disassemble, decompile or reverse engineer chips on the Evaluation Board. Customer shall inform ADI of any occurred damages or any modifications or alterations it makes to the Evaluation Board, including but not limited to soldering or any other activity that affects the material content of the Evaluation Board. Modifications to the Evaluation Board must comply with applicable law, including but not limited to the RoHS Directive. TERMINATION. ADI may terminate this Agreement at any time upon giving written notice to Customer. Customer agrees to return to ADI the Evaluation Board at that time. LIMITATION OF LIABILITY. THE EVALUATION BOARD PROVIDED HEREUNDER IS PROVIDED "AS IS" AND ADI MAKES NO WARRANTIES OR REPRESENTATIONS OF ANY KIND WITH RESPECT TO IT. ADI SPECIFICALLY DISCLAIMS ANY REPRESENTATIONS, ENDORSEMENTS, GUARANTEES, OR WARRANTIES, EXPRESS OR IMPLIED, RELATED TO THE EVALUATION BOARD INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTY OF MERCHANTABILITY, TITLE, FITNESS FOR A PARTICULAR PURPOSE OR NONINFRINGEMENT OF INTELLECTUAL PROPERTY RIGHTS. IN NO EVENT WILL ADI AND ITS LICENSORS BE LIABLE FOR ANY INCIDENTAL, SPECIAL, INDIRECT, OR CONSEQUENTIAL DAMAGES RESULTING FROM CUSTOMER'S POSSESSION OR USE OF THE EVALUATION BOARD, INCLUDING BUT NOT LIMITED TO LOST PROFITS, DELAY COSTS, LABOR COSTS OR LOSS OF GOODWILL. ADI'S TOTAL LIABILITY FROM ANY AND ALL CAUSES SHALL BE LIMITED TO THE AMOUNT OF ONE HUNDRED US DOLLARS ($100.00). EXPORT. Customer agrees that it will not directly or indirectly export the Evaluation Board to another country, and that it will comply with all applicable United States federal laws and regulations relating to exports. GOVERNING LAW. This Agreement shall be governed by and construed in accordance with the substantive laws of the Commonwealth of Massachusetts (excluding conflict of law rules). Any legal action regarding this Agreement will be heard in the state or federal courts having jurisdiction in Suffolk County, Massachusetts, and Customer hereby submits to the personal jurisdiction and venue of such courts. The United Nations Convention on Contracts for the International Sale of Goods shall not apply to this Agreement and is expressly disclaimed.

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