DC2683A and DC2684A-B
LTC4291-1/LTC4292
4-Port IEEE 802.3bt PSE

DESCRIPTION

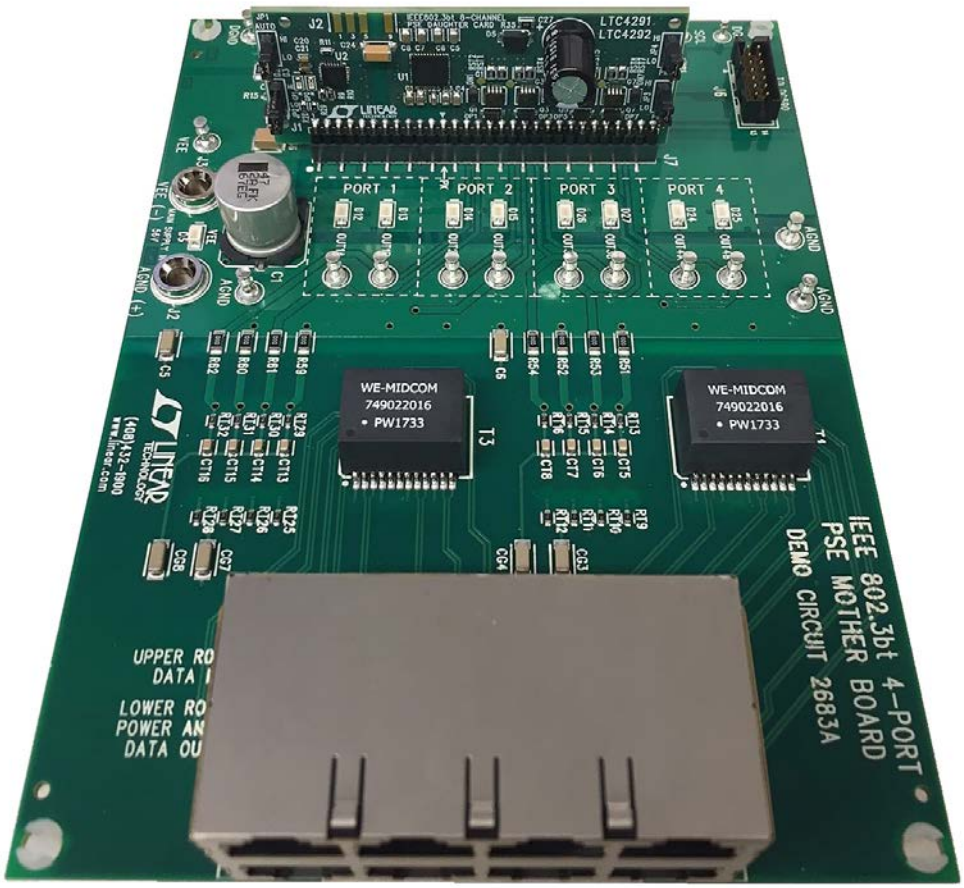
Demonstration circuit 2685B is a 4-port IEEE 802.3bt power sourcing equipment (PSE) composed of a DC2684A-B (daughter card) and DC2683A (mother-board). The DC2685B (kit) is used for evaluation of the LTC®4291-1/LTC4292 PSE chipset. Up to four IEEE 802.3af, IEEE 802.3at, or IEEE 802.3bt powered devices (PDs) can be connected and powered from this system using a single power supply. A DC590 is connected to the DC2685B for I²C interfacing with QuikEval™.

This demonstration manual provides a quick start procedure, a DC2684A-B daughter card overview, a DC2683A mother board overview, schematics, and layout printouts.

Design files for this circuit board are available.

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BOARD PHOTO



QUICK START PROCEDURE

Follow the quick start procedure below for basic operation of the DC2685B kit. Refer to Figure 1 through Figure 3 and Table 1 through Table 4 for proper equipment setup.

1. On the DC2684A-B daughter card set AUTO jumper JP1 (Figure 1) to a selected AUTO mode setting shown in Table 1.
2. On the DC2684A-B daughter card set 4PV# jumper JP2 (Figure 1) to a selected 4-Pair Valid setting as shown in Table 1.
3. On the DC2684A-B daughter card set PM1 jumper JP4 and PM0 jumper JP3 (Figure 1) to the power mode for evaluation specified in Table 2.
4. Align pin 1 of the 30-pin male connector on the DC2684A-B daughter card with pin 1 of the 30-pin female connector on the DC2683A motherboard as shown in Figure 2. Pin 12 is polarized to assist with the alignment. Carefully push the daughter card straight down until the male and female 30-pin connectors are flush with each other.
5. Connect a supply to the motherboard with the positive rail to AGND (+) and negative rail to V_{EE} (–) as shown in Figure 3. Use a power supply capable of sourcing the maximum delivered power for all four ports set by JP3 and JP4 on the daughter card (or I^2C configured power). Ramp the supply up to within the recommended voltage range specified in Table 3.
6. Set the LTC4291-1/LTC4292 I^2C address switch SW1 on the motherboard to the one of the four addresses shown in Table 4.
7. On the DC590, set the VCCIO jumper JP6 to 3.3V. (Refer to Table 5 and the DC590 demo manual for further instructions for the DC590.)
8. Connect the DC590 to the DC2683A at connector J6 with a 14-pin ribbon cable as shown in Figure 3 and open the QuikEval GUI. A GUI for the LTC4291-1/LTC4292 is brought up by QuikEval. (Follow the DC590 demo manual instructions if this has not been previously setup.)
9. Connect up to four PDs to the DC2685B RJ45 connector J1, bottom row ports 1-4 as shown in Figure 3.
10. Optionally a 1000BASE-T data source may be connected to the DC2685B RJ45 connector J1, top row ports 1-4 for data pass through testing.

QUICK START PROCEDURE

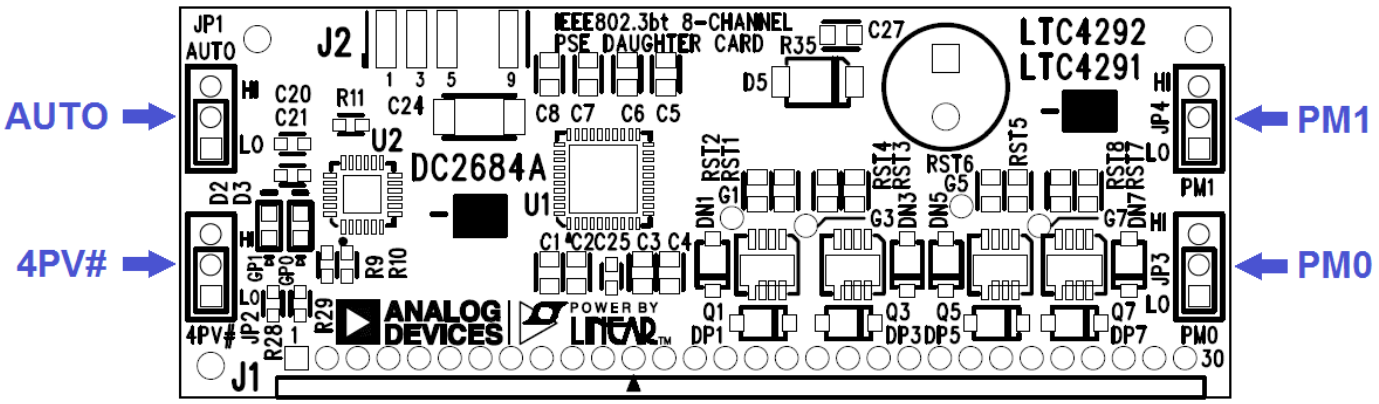


Figure 1. DC2684A-B Jumpers: AUTO, 4PV#, PM0 and PM1

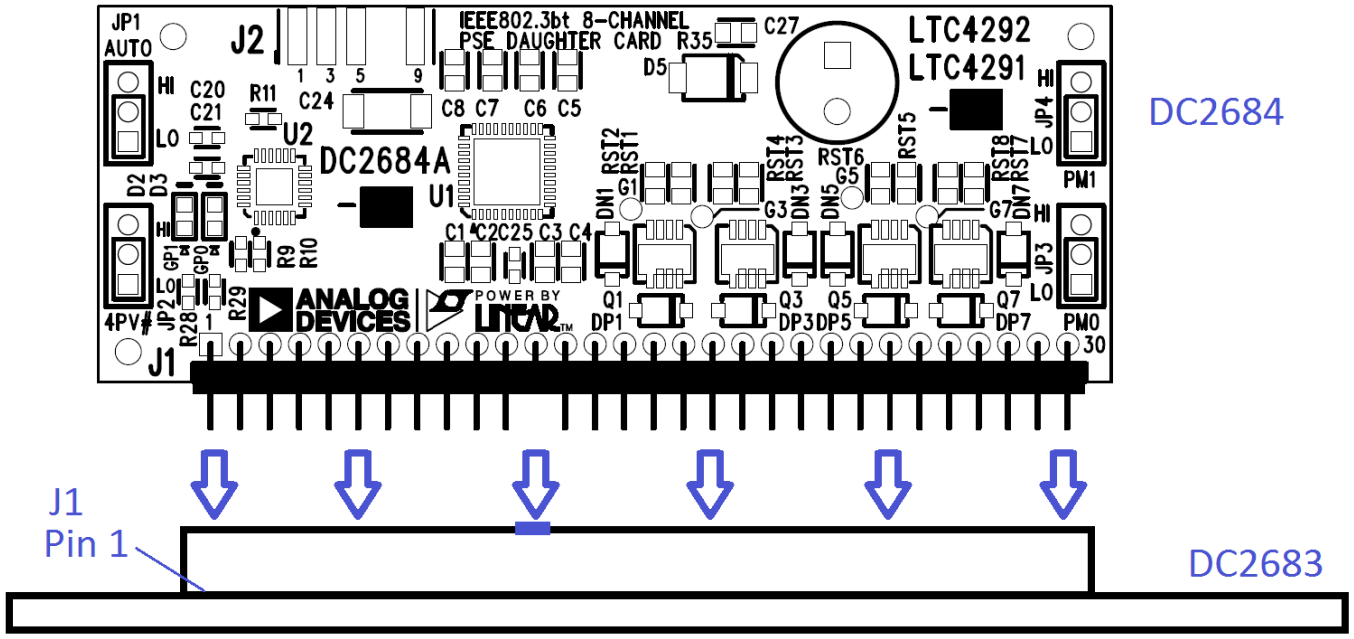


Figure 2. Inserting the DC2684A-B Daughter Card Into J7 of the DC2683A Motherboard

QUICK START PROCEDURE

Table 1. DC2684A-B AUTO and 4PV# Jumper Settings

JUMPER	SETTING	OPERATION
AUTO (JP1)	LO	Host Control Required
	HI	Autonomous
4PV# (JP2)	LO	Port powered only when both pairsets present a valid signature
	HI	Any pairset presenting a valid signature is powered

Table 2. DC2684A-B Auto Mode Maximum Delivered Power Capabilities Jumper Settings

PM1 (JP4)	PM0 (JP3)	Max Port Power (Single-Signature)	Max Pairset Power (Dual-Signature)
LO	LO	40W	13W
LO	HI	51W	25.5W
HI	LO	62W	25.5W
HI	HI	71.3W	35.6W

Table 3. DC2685B Power Supply Voltage Range per PSE Type

IEEE TYPE	Supply Voltage Range
Type 3	51V to 57V
Type 4	53V to 57V

Table 4. DC2685B Address Settings

SW3		ADDRESS
AD3	AD2	
LO	LO	20h
LO	HI	24h
HI	LO	28h
HI	HI	2Ch

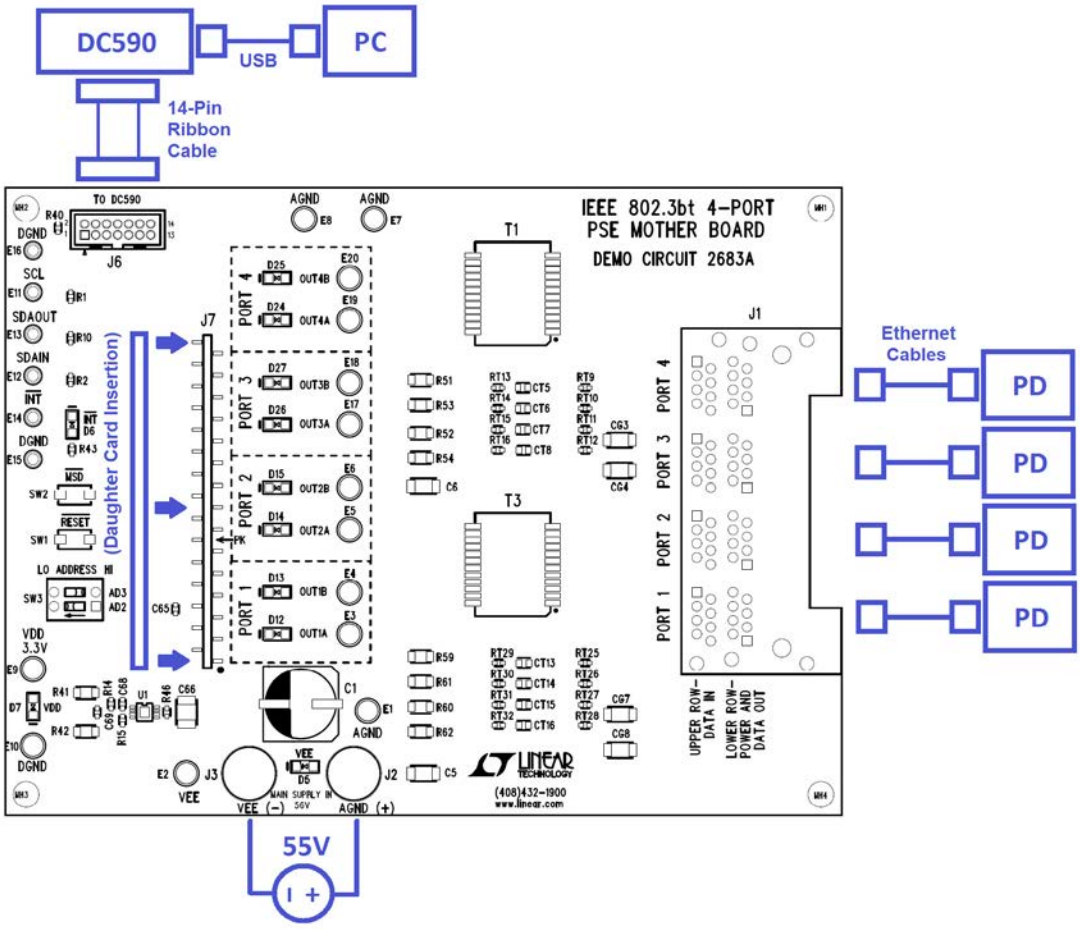


Figure 3. DC2685B Kit Connections

DEMONSTRATION CIRCUIT 2684A-B DAUGHTER CARD

Demonstration circuit 2684A-B is an IEEE 802.3bt 8-channel PSE daughter card that features the LTC4291-1/LTC4292 chipset. This daughter card mates with a 4-Port, 4-Pair PoE motherboard for use in IEEE 802.3bt Type 3 or 4 compliant Power over Ethernet PSE systems.

Board Layout

Parts placement, sense resistor block and Kelvin sensing, copper fill, trace routing, and spacing are crucial for LTC4291-1/LTC4292 chipset operation, robustness, and measurement accuracy. It is imperative to follow the layout requirements specified in the LTC4291-1/LTC4292 data sheet. The DC2684A-B demonstrates proper LTC4291-1/LTC4292 board layout on a compact daughter card approximately the height and width of a 2 × 4 RJ45 connector.

Isolation and Power Supplies

The LTC4291-1/LTC4292 chipset provides communication across an isolation barrier through a data transformer (Figure 4). All digital pins reside on the digital ground reference and are isolated from the analog PoE supply on the daughter card layout. A V_{DD} logic supply and V_{EE} PoE supply is brought in at the 30-pin connector J1.

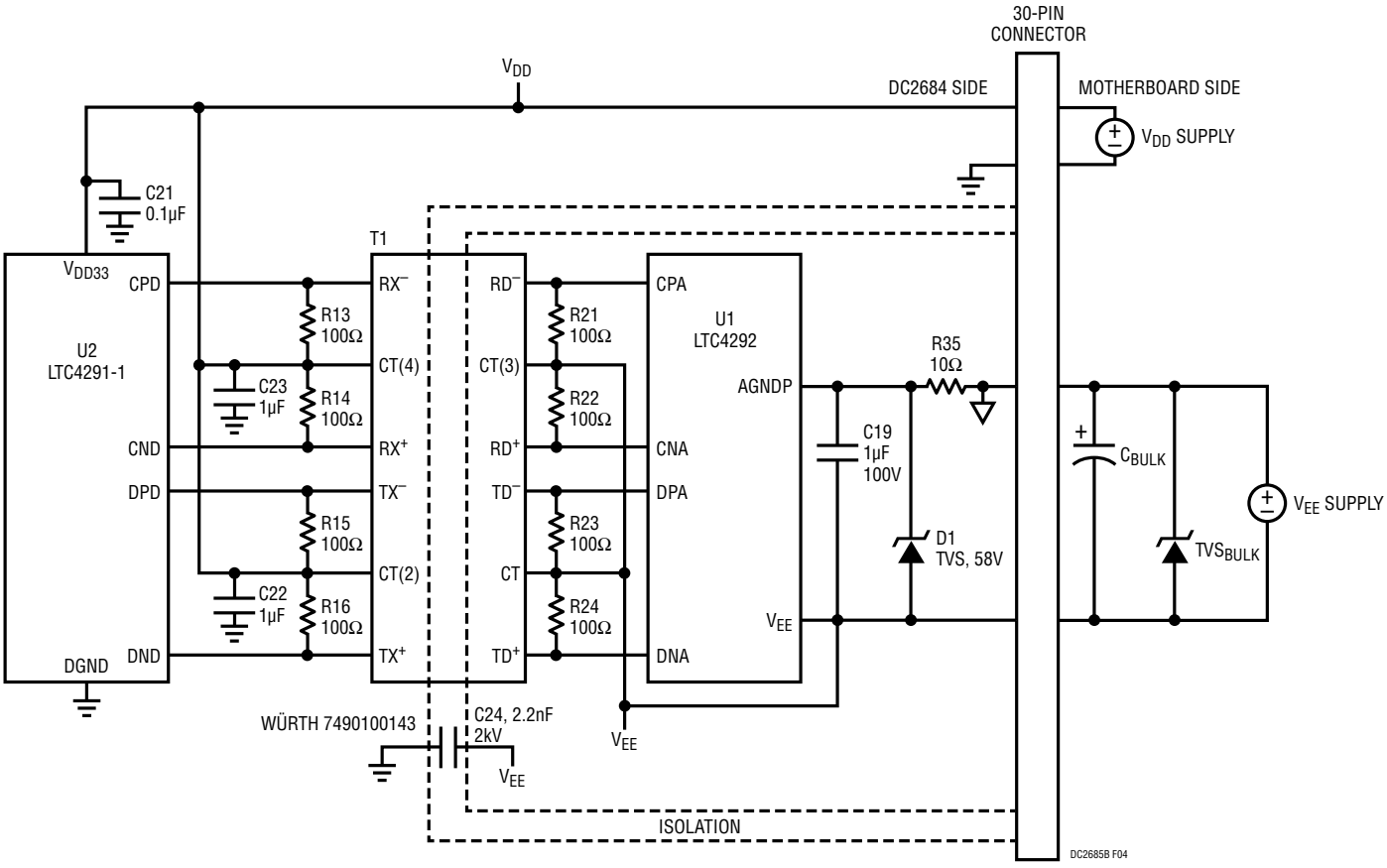


Figure 4. DC2684A-B Digital and Analog Isolation

DEMONSTRATION CIRCUIT 2684A-B DAUGHTER CARD

I/O LED Indicators

The DC2684A-B features two LEDs to indicate the states of the LTC4291-1/LTC4292 general purpose input/output pins GP0 and GP1. These pins are configured as inputs or outputs via I²C. GP1 and GP0 are referenced to DGND and driven by the LTC4291-1 when set as outputs (Figure 5). J2 provides test points for these pins.

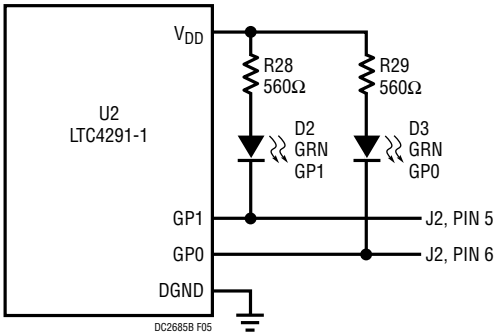


Figure 5. DC2684A-B, LTC4291-1 General Purpose I/O LED Indicators

I²C Communication and Addressing

The LTC4292/LTC4291 internal registers are accessed via I²C to read and/or write configuration, status, events and interrupt registers. The I²C lines SDAOUT, SDAIN and SCL connect to the 30-pin connector (Figure 6). Subsequently, the I²C bus is accessed on the motherboard. SDAOUT and SDAIN are tied together through shunt resistor R11 on the DC2684A-B for a common SDA line.

The LTC4291-1 address pins AD0 and AD1 are tied to DGND through shunt resistors R9 and R10 respectively. This sets these two address bits low. Address pins AD2 and AD3 are brought out to the 30-pin connector for configuration on the motherboard. See Figure 6 and Table 4.

4PV# Jumpers

The $\overline{\text{4PVALID}}$ pin of the LTC4291-1 is set by the 4PV# jumper JP2 on the DC2684A-B. See Table 1 for jumper settings. This jumper configuration along with Auto mode reset state is used to automatically determine the number

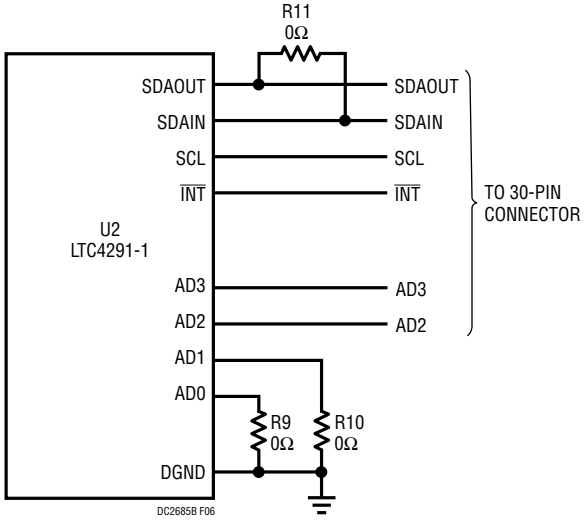


Figure 6. DC2684A-B, LTC4291-1 I²C and Address Connections

of powered pairs. Refer to Table 1 for the configuration description.

Power Mode and Power Path Components

The DC2684A-B power mode jumpers PM1 and PM0 either tie the respective LTC4291-1/LTC4292 PWRMD1 and PWRMD0 pins to V_{EE} or CAP2 through a 100Ω resistor. This configures the maximum port output power in the Auto mode reset state (see Table 2). The power path components (hot swap MOSFETs and resistors) for each channel on the DC2684A-B have been selected to handle all four power levels.

Surge Protection

The DC2684A-B has basic surge protection components across the V_{EE} supply, V_{EE} and AGNDP supply pins, and OUTnM pins. Refer to the LTC4291-1/LTC4292 hardware data sheet for further details on surge protection. D5 and C27 on the DC2684A-B provide example bulk TVS and

DEMONSTRATION CIRCUIT 2683A MOTHER BOARD

capacitance components; these components must be sized to the final system requirements.

Demonstration circuit 2683A is a 4-Port, 2-channels per port IEEE 802.3bt PoE PSE motherboard. This board accepts an IEEE 802.3bt four port PSE daughter card featuring the LTC4291-1/LTC4292 chipset.

Daughter Card Insertion Precautions

When inserting or removing the daughter card into the DC2683A motherboard, verify all supplies and LEDs are off. Push the card straight down for insertion or pull straight up for removal to avoid bending the connector pins. Follow the instructions in the Quick Start Procedure for alignment.

Main V_{EE} PoE Supply

The V_{EE} supply is the main PoE supply and connects to the DC2683A with the positive rail to AGND (+) and the negative rail to V_{EE} (–) as shown in Figure 3 of the Quick Start Procedure. The voltage must be within the range shown in Table 3 depending on the application PSE type. For full load testing at each port, choose a power supply that is set with a current limit higher than the maximum allowed output power at each port.

Onboard 3.3V Supply

The DC2683A motherboard has an onboard (non-isolated) 3.3V LDO for the LTC4291-1/LTC4292 V_{DD} supply which is generated from the V_{EE} supply. This onboard logic supply is for demonstration purpose to allow for a single supply connection to the DC2685B kit. DGND is tied to V_{EE} through shunt resistor R42. To isolate the logic supply from the PoE supply, remove R42 and R41 and apply an external isolated 3.3V supply across V_{DD} and DGND. If the DC2685B kit is connected in parallel for multi-quad port evaluation, verify all ground connections are correct before applying power.

LED Indicators

V_{EE} LED (D5) and V_{DD} LED (D7) indicate if a voltage is present at these supplies. Verify these LEDs are off before inserting or removing the daughter card.

Each pairset channel (2 per port) has a respective OUTnM LED to indicate if the channel is powered on with PoE.

The $\overline{INT}$ LED (D6) indicates if the interrupt line is pulled low by the daughter card. When the interrupt is cleared (high) via I^2C interrupt servicing, the LED is turned off.

Digital Connections

The DC590 (USB to I^2C) controller board is connected to the DC2683A at J6 through a 14-pin ribbon cable. The QuikEval software must be previously installed. When QuikEval is opened, the software will automatically detect the DC2685B kit and open the LTC4291-1 GUI.

I^2C address pins AD3 and AD2 are set with a 2-bit switch SW3 on the DC2683A. Refer to Table 4 for setting the individual I^2C address for each DC2685B kit.

Turret digital test points for SCL, SDA, DGND, $\overline{INT}$, $\overline{MSD}$, and $\overline{RESET}$ are provided on the DC2683A.

RJ45 Connections

PDs are connected using an Ethernet cable to any of the bottom row ports at 2 × 4, RJ45 connector J1 on the DC2683A. Test points for each channel output OUT1A through OUT4B, are provided. Optionally, an Ethernet data source may be connected with an Ethernet cable to any of the top row ports at J1.

$\overline{MSD}$ and $\overline{RESET}$ Pushbuttons

Pushbutton switch SW1, when pressed, pulls the $\overline{RESET}$ pin of the daughter card logic low. The PSE controller is then held inactive with all ports off. When SW1 is released, $\overline{RESET}$ is pulled high, and the PSE returns to the AUTO pin reset state.

Pushbutton switch SW2, when pressed, pulls the maskable shutdown input ($\overline{MSD}$) pin of the daughter card logic low. When pressed, all ports that have their corresponding mask bit set in the mconfig register of the PSE controller will be shutdown. These ports must then be manually re-enabled via I^2C or by resetting the PSE.

SUPPLEMENTARY

Table 5. DC590 Jumper Selection. Refer to the DC590 Demo Manual for Further Details.

JUMPER	SETTING	OPERATION
JP1	PROG	Microcontroller in-circuit programming header. Do NOT install jumper; make no connections.
JP2	MODE	Do NOT install jumper; make no connections.
JP3	Watchdog Enables	Do NOT install jumper; make no connections.
JP4	EE	Jumper MUST be in the EN position.
JP5	SW (Right Hand Side)	MUST be in the ON position. See Connections section.
	ISO (Left Hand Side)	Controls the isolated supply. See Connections section.
JP6	VCCA Control	See Connections section.

DC2684A-B DAUGHTER CARD LAYOUT FILES

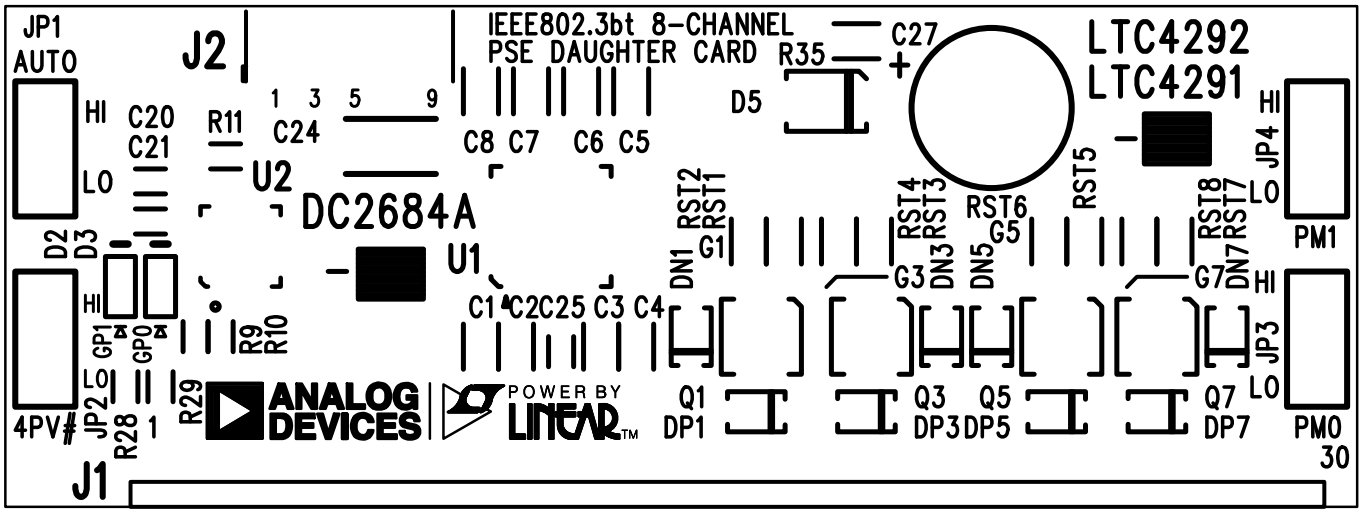


Figure 7. DC2684A-B Top Silkscreen

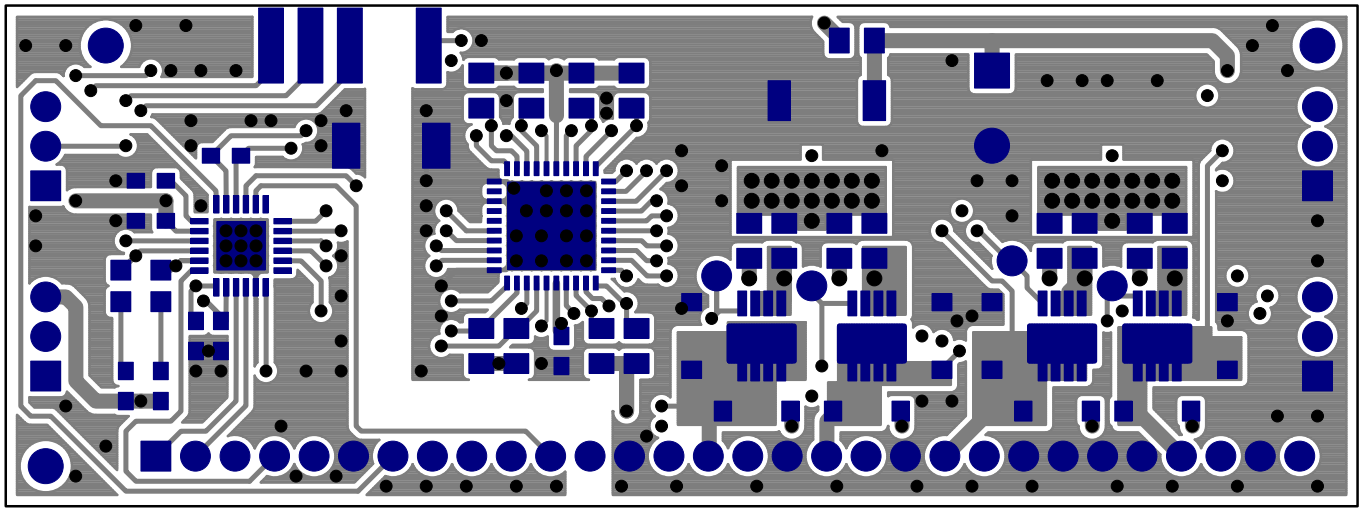


Figure 8. DC2684A-B Top Layer

DC2684A-B DAUGHTER CARD LAYOUT FILES

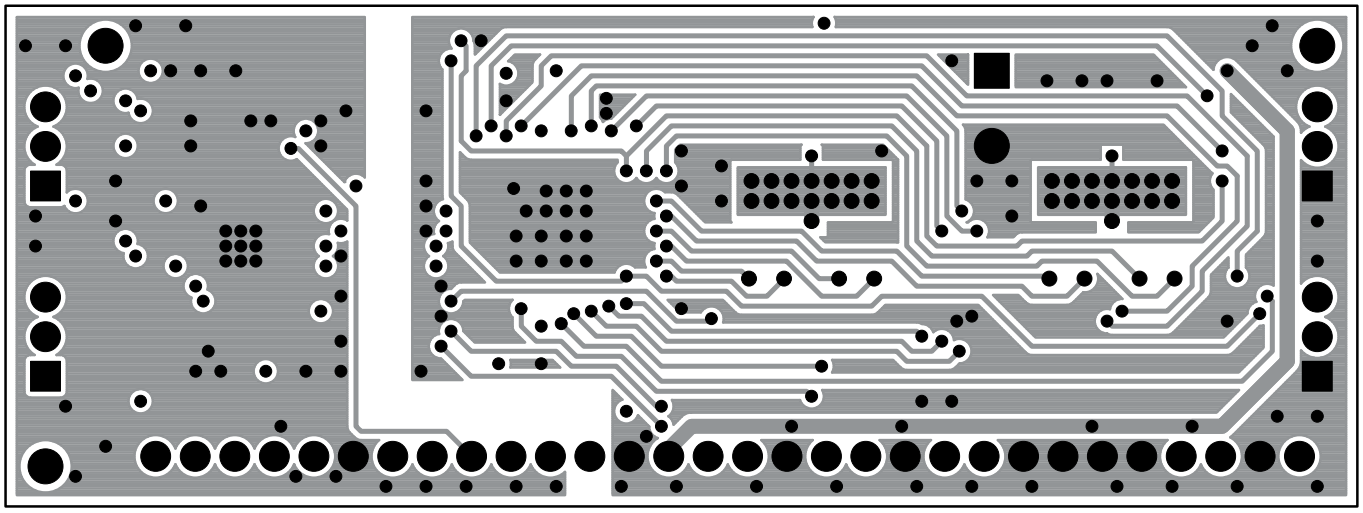


Figure 9. DC2684A-B Inner Layer 2

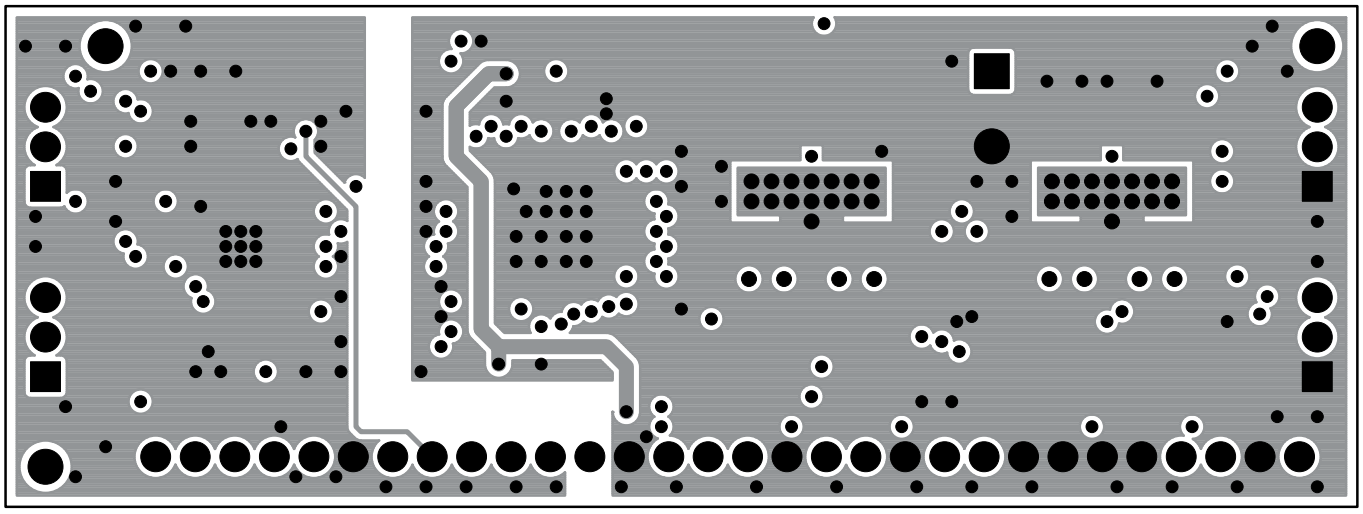


Figure 10. DC2684A-B Inner Layer 3

DC2684A-B DAUGHTER CARD LAYOUT FILES

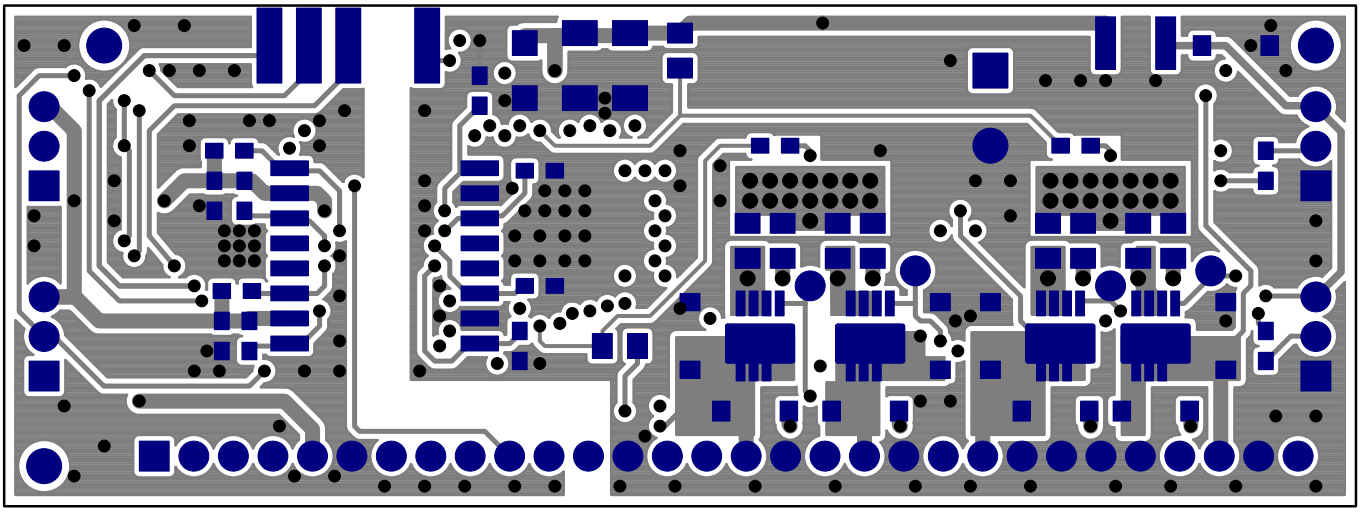


Figure 11. DC2684A-B Bottom Layer

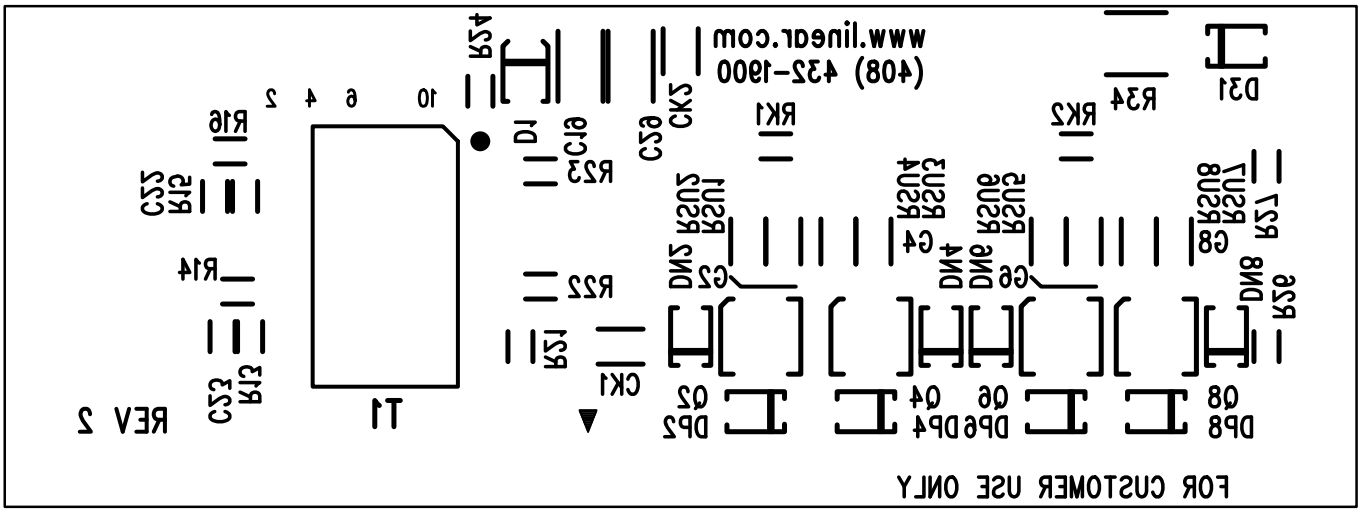


Figure 12. DC2684A-B Bottom Silkscreen

DC2683A MOTHER BOARD LAYOUT FILES

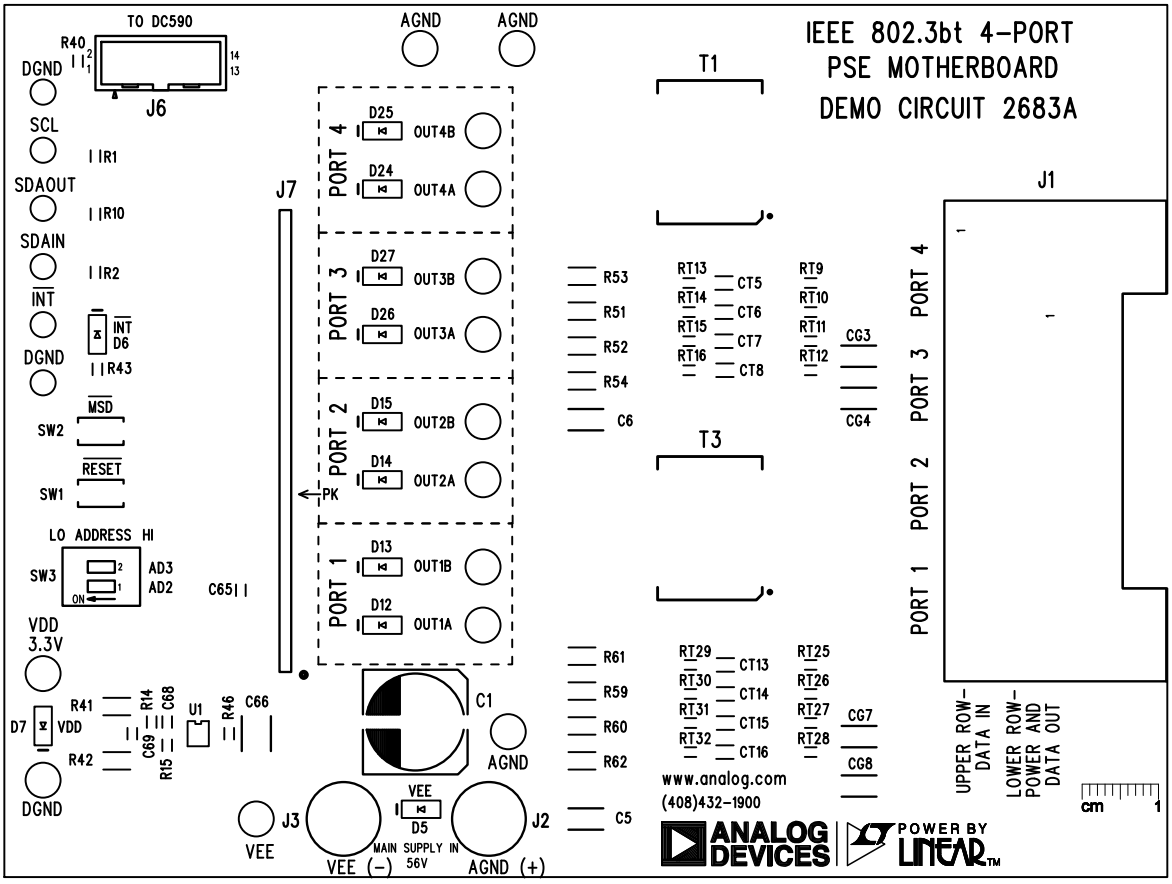


Figure 13. DC2683A Top Silkscreen

DC2683A MOTHER BOARD LAYOUT FILES

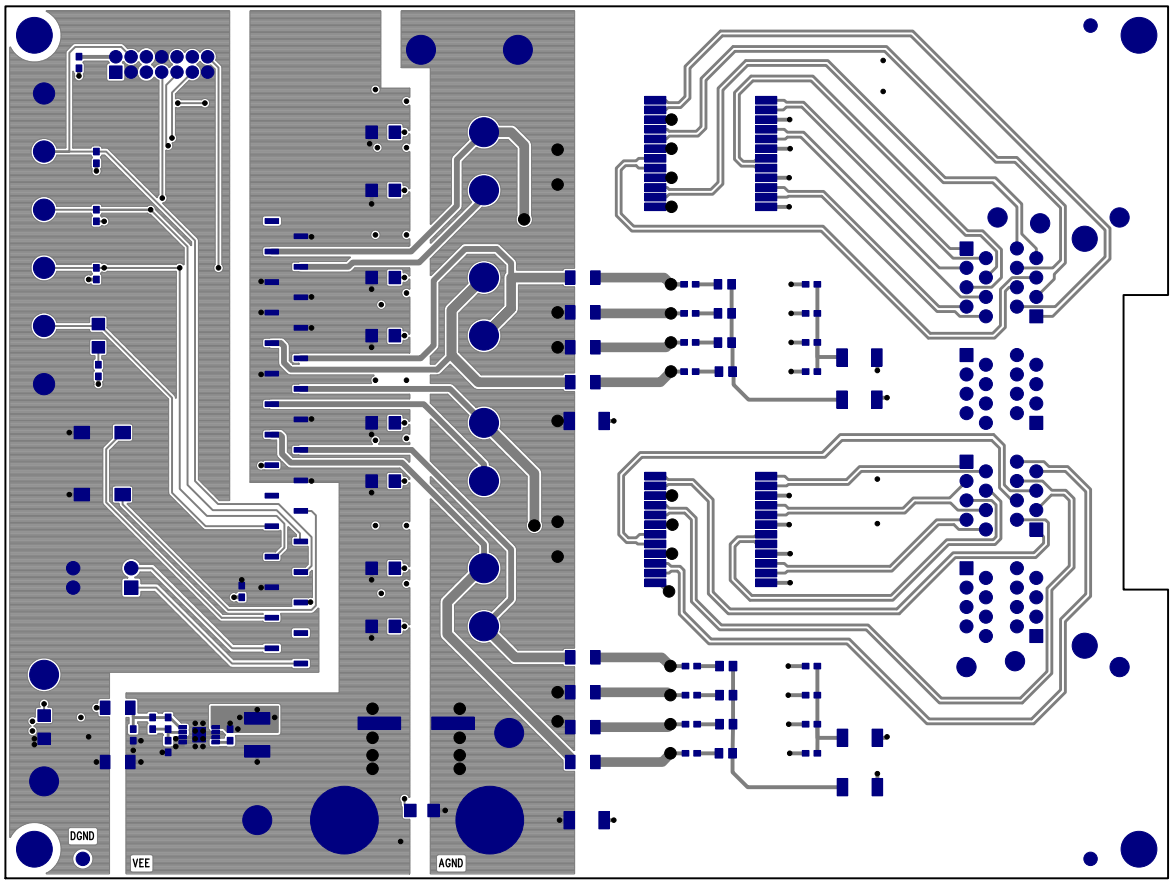


Figure 14. DC2683A Top Layer

DC2683A MOTHER BOARD LAYOUT FILES

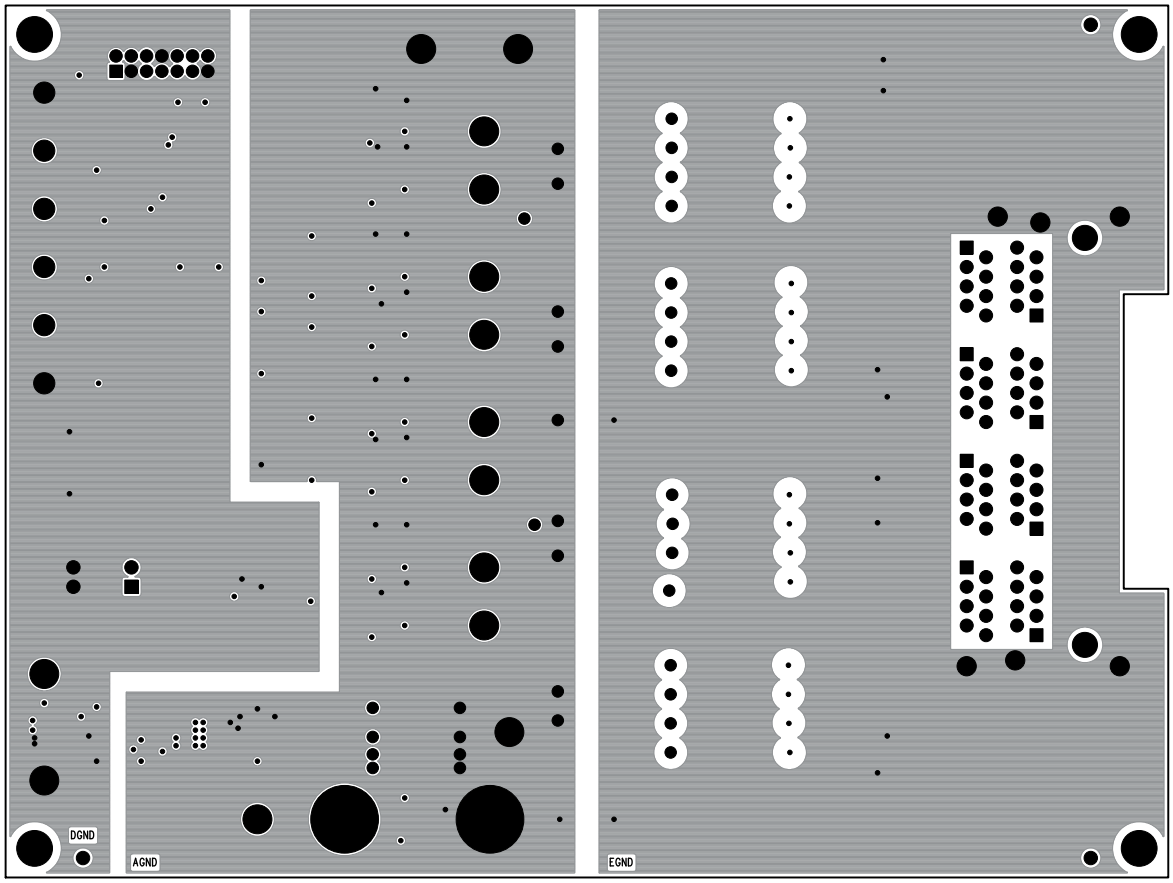


Figure 15. DC2683A Inner Layer 2

DC2683A MOTHER BOARD LAYOUT FILES

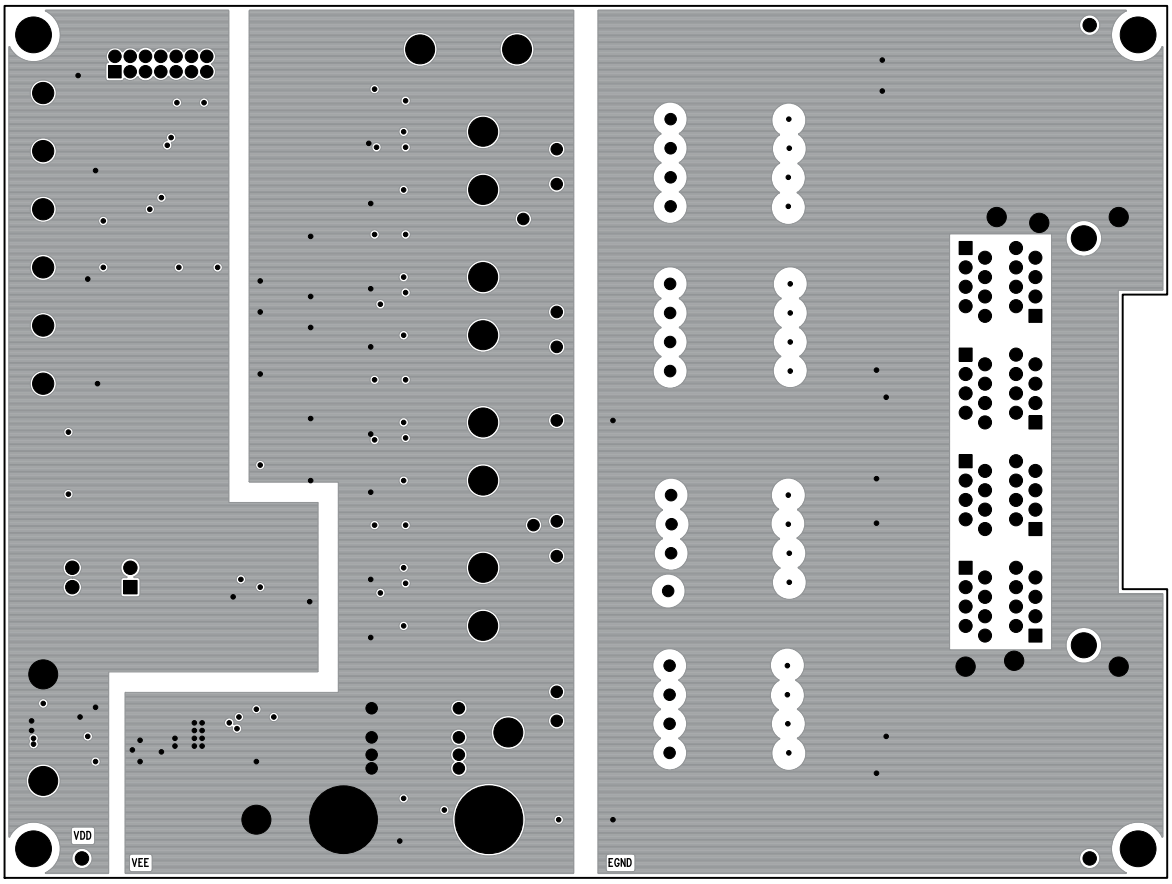


Figure 16. DC2683A Inner Layer 3

DC2683A MOTHER BOARD LAYOUT FILES

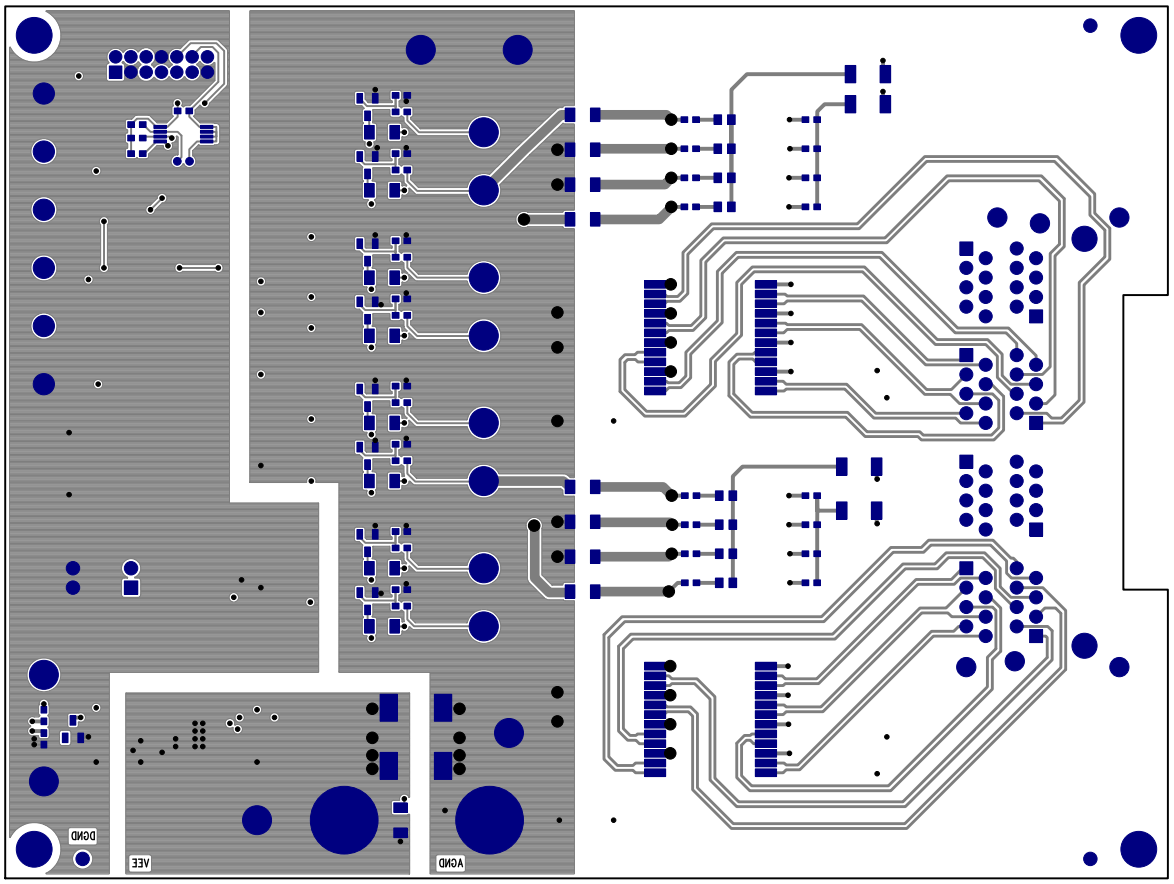


Figure 17. DC2683A Bottom Layer

DC2683A MOTHER BOARD LAYOUT FILES

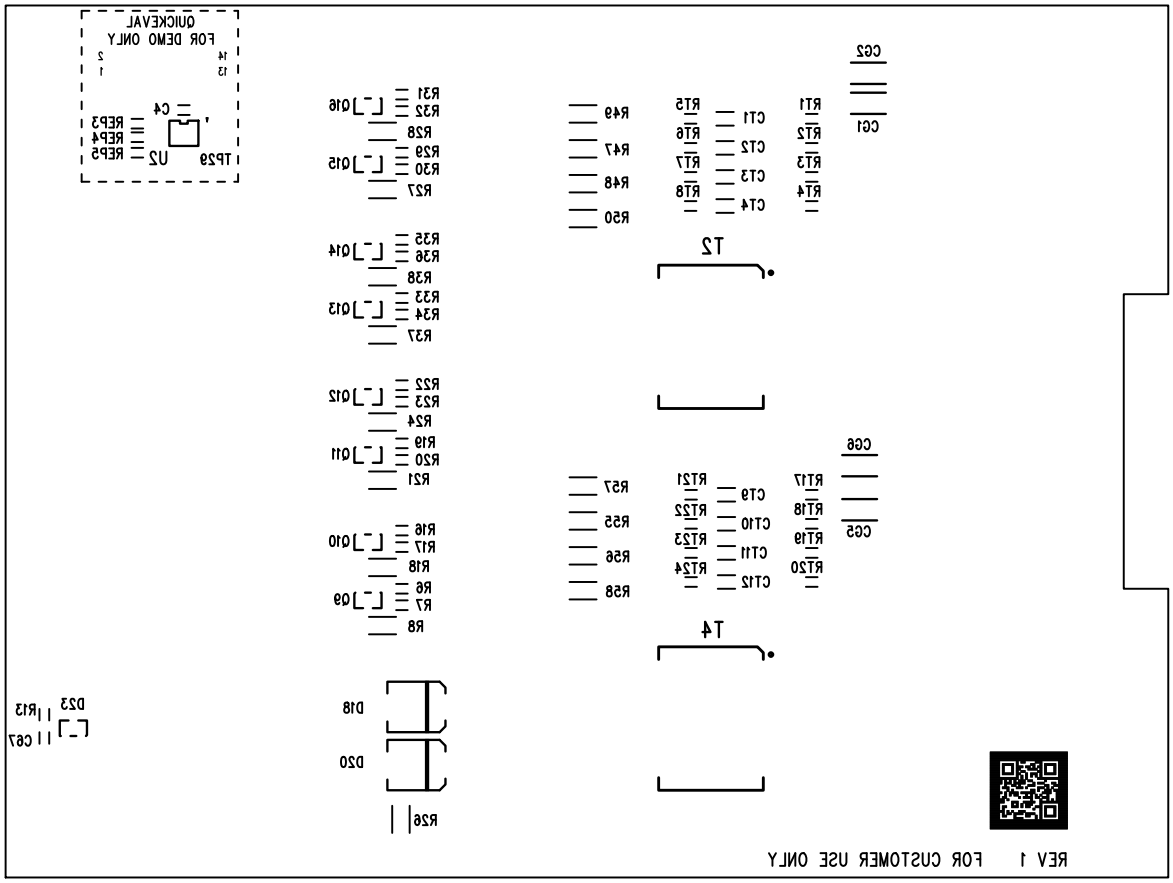
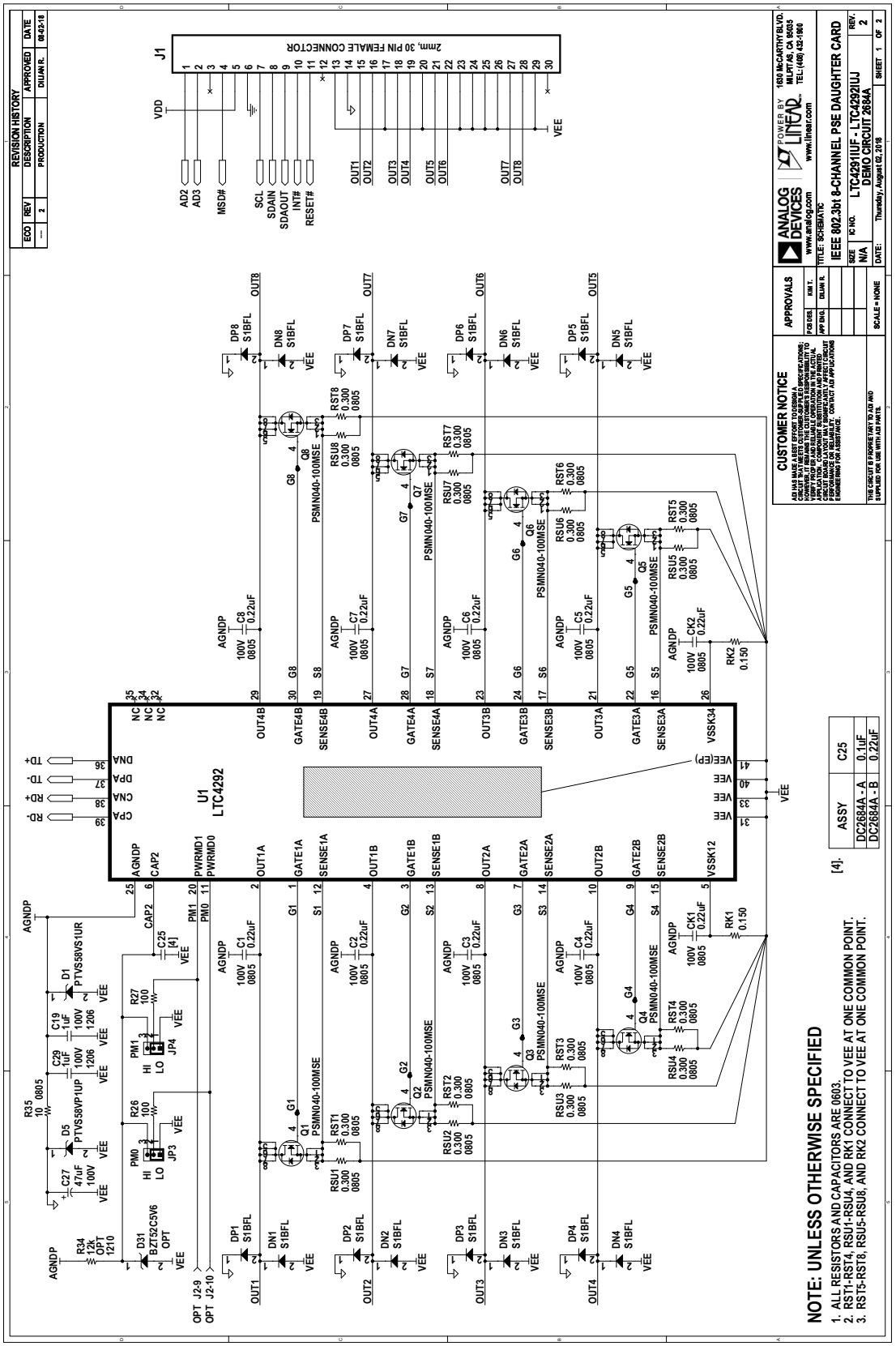
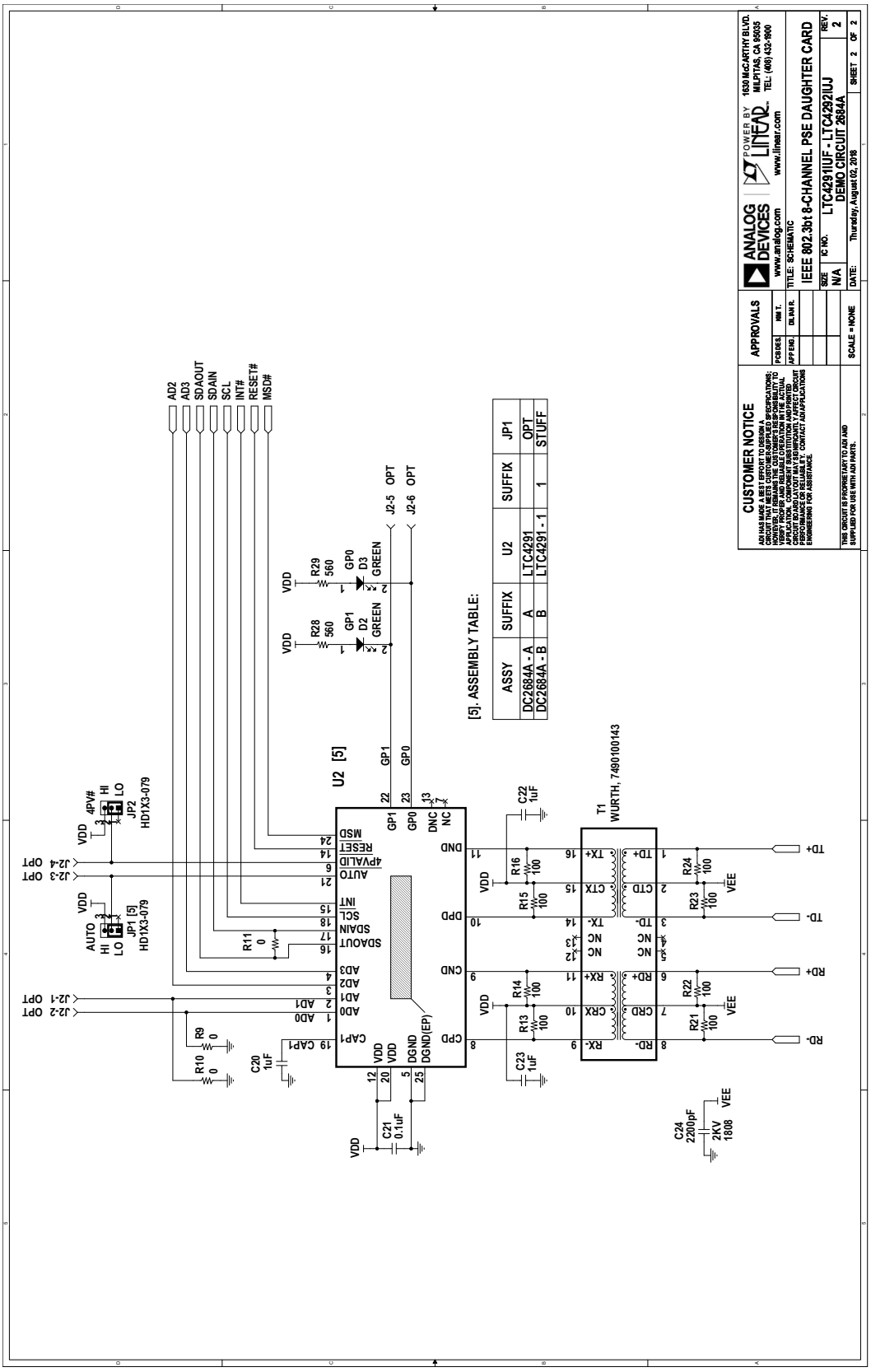


Figure 18. DC2683A Bottom Silkscreen

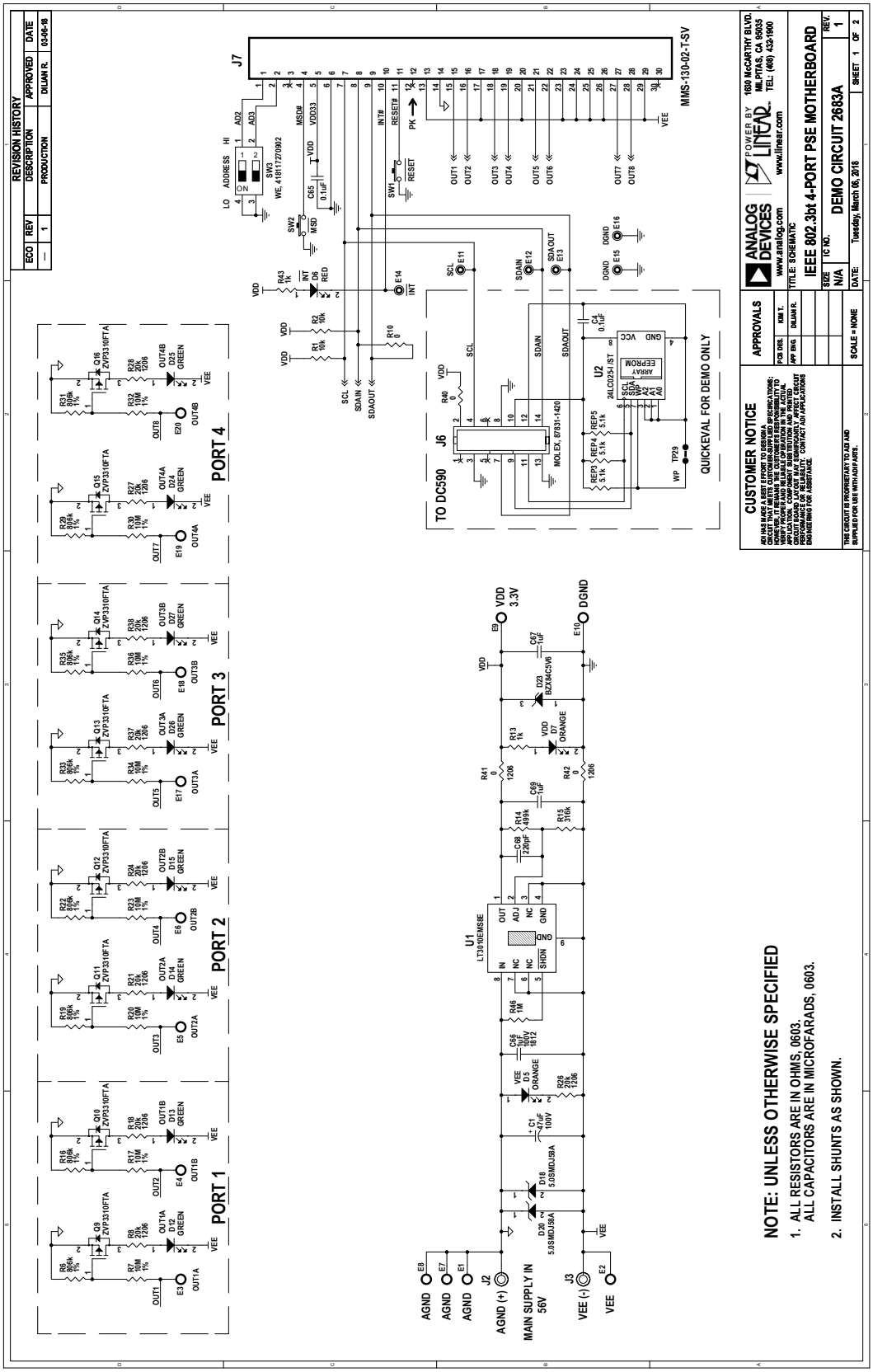
DC2684A-B DAUGHTER CARD SCHEMATIC



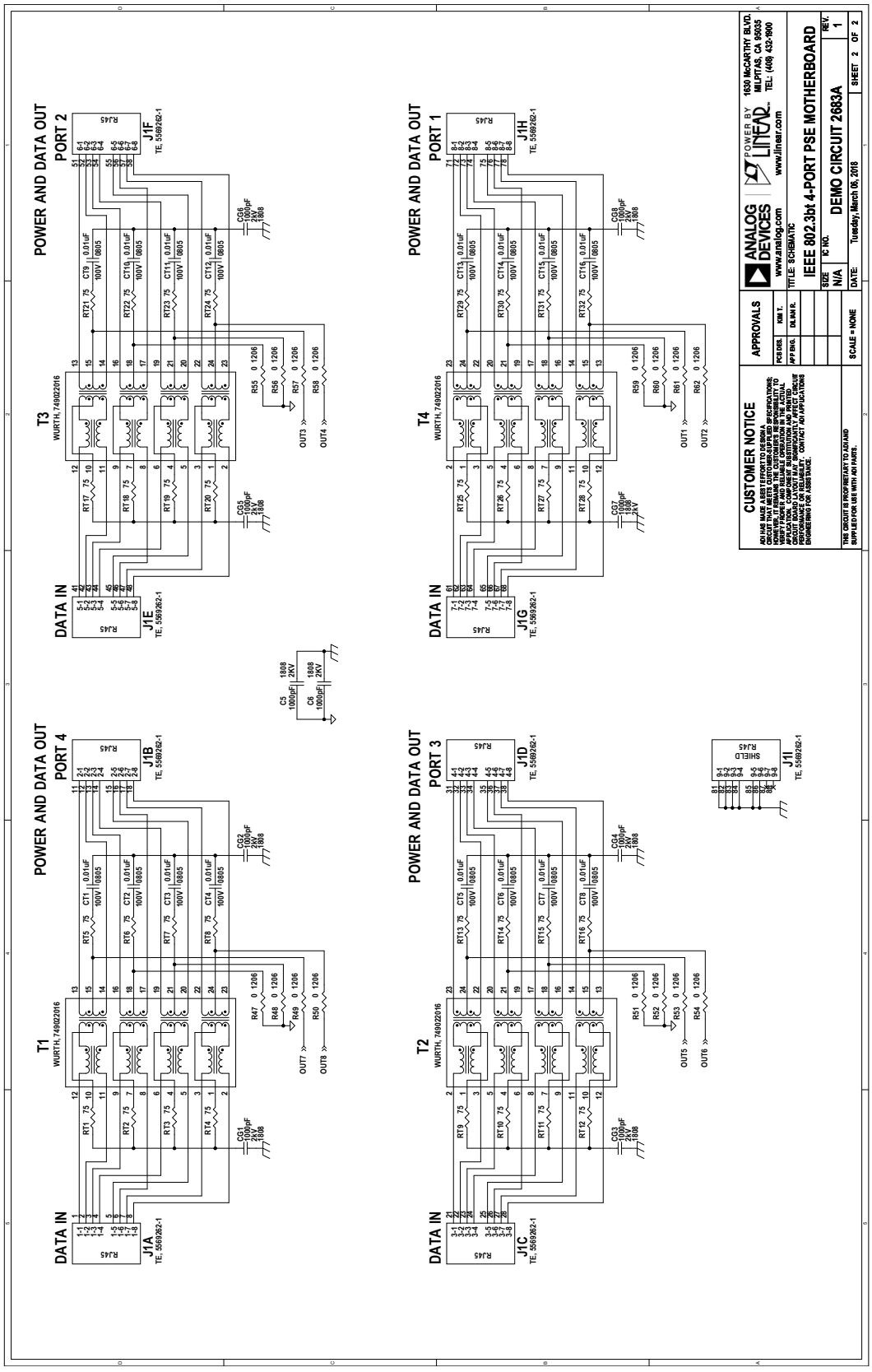
DC2684A-B DAUGHTER CARD SCHEMATIC



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